Design of a Soft-Switching Asymmetrical Half-Bridge Converter as second stage of a LED driver for Street-Lighting Application

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Abstract--**High-Brightness Light Emitting Diodes (HB-LEDs) are considered as a remarkable lighting device due to their high reliability, chromatic variety and increasing efficiency. As a consequence, a high number of solutions for supplying LED strings are coming out. One-stage solutions are cost-effective, but their efficiency is low as they have to fulfill several purposes with only one converter: Power Factor Correction (PFC), galvanic isolation (in some cases) and current regulation. Two-stage and three-stage solutions have higher efficiency as each stage is optimized for only one or two tasks and they are the preferred option when supplying several strings at the same time.**

In this paper, a two stage solution is proposed. The first stage is the well-known PFC Boost converter. The second stage, on which is focused this paper, is the Asymmetrical Half Bridge (AHB). Its design has been optimized taking into account the needs and characteristic of LED-based street lighting applications. The proposed transformer design (with asymmetrical secondary windings) minimizes the conduction losses while the model of the converter during the transitions allows us to optimize the duration of the dead times reducing switching losses in the MOSFETs and diodes.

Experimental results obtained with a 40-W prototype show an efficiency as high as 94.5% for this second stage and validate the proposed design procedure and model.

Index Terms--**Asymmetrical Half-Bridge dc-dc converter, Complementary control Half-Bridge dc-dc converter, LED's driver, street lighting based on LEDs.**

I. INTRODUCTION

High-Brightness Light Emitting Diodes (HB-LED) are gaining importance in lighting applications as their efficiency is increasing [1]. In fact, their theoretical maximum efficiency is higher than the theoretical maximum efficiency of other devices such as gas-discharge lamps or incandescent lamps. Besides, they have other important advantages, such as high reliability, chromatic variety, etc. As a consequence, a high number of different ac-dc and dc-dc topologies have been proposed for supplying LED strings. The key issues of these topologies are high reliability (which involves the absence of electrolytic capacitors), high efficiency, Power Factor Correction (PFC) in ac-dc converters and, in some cases, galvanic isolation. These topologies can be classified attending to the number of stages in cascade: one, two or three.

One-stage solutions [2-5] imply low-cost designs and only one energy conversion. Nevertheless, this also means that all tasks need to be satisfied with only one stage, what normally means a considerably reduction in efficiency. Besides, PFC converters without electrolytic capacitors have a high output voltage ripple. Due to the nature of the load (i.e. LEDs) this means a considerable low-frequency current ripple, which leads to flickering. These one-stage solutions are the most suitable option for LED-based replacement lamps [6], in which the converter size needs to be quite small.

Two-stage topologies [7] usually have a PFC converter as first stage and a second stage in charge of canceling the low-frequency ripple of the PFC converter and regulating the current provided to the LED string [8, 9]. The second stage also provides the galvanic isolation when needed. The two-stage topology provides the highest efficiency but, as there are needed as many second stages as LED strings are supplied, this can raise the cost considerably, especially if the second stages need to provide galvanic isolation.

A possible option for reducing the cost is the integration of the two stages into only one [10, 11]. Although efficiency significantly decreases with this approach, cost and size are highly reduced. It should be taken into account that this approach has the same problem as the conventional two-stage topology when the number of strings increases. A possible solution to this problem is using only one converter and equalizing the current through each string with a quasi-non-dissipative technique [12]. Besides, in many of these topologies the voltage of the energy-storage capacitor may be very high, increasing the voltage stress in the rest of the components.

In the three-stage solutions [13, 14] each converter is optimized for just one task: PFC, galvanic isolation and current regulation in each string. Hence, although three energy conversions are done, efficiency can be still quite high due to the optimization of each stage. Nevertheless, this approach only make sense when galvanic isolation is needed while supplying two or more LED strings. Typically, the first stage is a Boost converter for achieving Power Factor Correction (PFC) [15-17]. The second stage is in charge of providing the galvanic isolation and, in some cases, canceling the voltage ripple of the first stage. The first and the second stages are common to all the LED strings, while there are as many third stages as LED strings are supplied. In this way, the current provided to each

string can be independently regulated. An example of this three-stage topology can be found in [13]. The first stage is a Power Factor Corrector (PFC) Boost converter operating in boundary conduction mode (BCM). The second stage is an LLC resonant converter which cancels the low-frequency ripple and provides galvanic isolation. The regulation of each LED string current is achieved by means of Buck converters. As can be seen, the first and the second stages operate at variable frequency, which may cause EMI problems and increases the difficulty of calculating the input EMI filter.

In this paper, a two-stage solution is proposed for LED-based street lighting application. The main targets of this topology are achieving high efficiency and high reliability while providing galvanic isolation. The second target implies that the whole topology needs to be implemented without electrolytic capacitors. The first one, achieving high efficiency, strongly determines the design of the second stage (on which is focused this paper). As can be seen in Fig. 1, the first stage is a Boost converter common to all the LED strings and its purpose is achieving PFC. This topology has proven to be a perfect option for this kind of application as can be implemented without electrolytic capacitor and with an efficiency as high as 97%. The second stages (one for each LED string) are Asymmetrical Half Bridges (AHBs) and they are in charge of providing the galvanic isolation and regulating the current supplied to the LED string (this topology is also known as Complementary-Control Half-Bridge). They also have to reduce the voltage ripple of the first stage, which is high due to the absence of electrolytic capacitors. It should be taken into account that this reduction is achieved by means of the close-loop regulation, not by its output filter. In other words, its close-loop regulator can be fast enough to reduce the low-frequency ripple. One of the main advantages of this converter is that it can achieve soft-switching in primary switches. Besides, it is not a valid topology when the input voltage range is wide. Nevertheless, in this application the average input voltage of the second stage is constant and the only voltage variation is due to the already-mentioned low-frequency ripple. The key issue in the design of this converter is reducing the losses. On one hand, this topology has a transformer magnetizing current whose average value is not zero. This implies that the conduction losses in the transformer and the MOSFETs are higher than in traditionally-controlled HB. Moreover, it is not possible to use Schottky diodes at the output due to the voltage levels demanded by LED strings (in the case of standard street-lighting in Europe, around 150 V); hence, it is necessary to develop a method for reducing the switching losses of the ultrafast diodes that are going to be used (standard AHB only achieves soft-switching in primary switches). These two points will be deeply analyzed in the paper, as they are the key issues for boosting the efficiency of the topology.

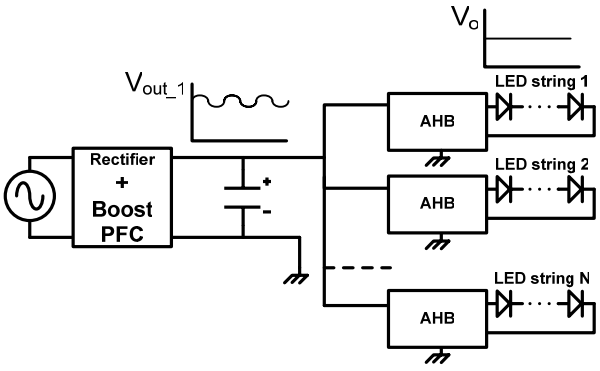


Fig. 1. Proposed topology.

As the final application of this LED driver is street lighting, some additional details should be taken into account. Wavelength (color) quality is less important than other issues such as cost and efficiency (including electricity-to-light conversion efficacy). Besides, the current stress on the LEDs should be the lowest as a way of boosting the reliability and, indirectly, reducing the cost. These points can be achieved by means of, among other things, the use of amplitude-mode driving technique as it has lower current stress on LEDs and semiconductors than the PWM one.

The main advantages and disadvantages of this proposed topology in comparison to other topologies used in LED-based street lighting are:

- High efficiency. Up to 94% in the second stage and 91% taking into account the first and the second ones (PFC Boost + AHBs). Besides, the proposed topology also benefits from a high-efficacy electricity-to-light conversion due to the dimming technique employed [1].
- Color quality. It is lower than the one obtained with digital dimming, but it is not a critical issue due to the final application (i.e. street lighting).
- High reliability. It is high due to the absence of electrolytic capacitor and the use of amplitude-mode driving technique, which reduces the current stress of the LEDs.
- Constant switching frequency. The second stages of the proposed system operate at constant switching frequency. The first stage, the boost converter, can be implemented in two different ways. If it is implemented with SiC diodes, then it can be controlled by a standard controller base on the "multiplier approach" (i.e. UC3854) and it can operate in the Continuous Conduction Mode (CCM). Of course, this means that the converter operates at constant switching frequency. In this case, high efficiency is due to the use of the aforementioned SiC diodes. On the other hand, high efficiency can also be achieved with ultrafast silicon diodes if the converter operates in BCM. In this case, the switching frequency is not constant but the cost is considerably lower.
- Galvanic isolation. It is provided by the proposed second stage. This requirement is sometimes necessary in order to comply with certain regulations or customer demands. Using galvanic

isolated topologies in the second stage increases the size of the whole converter when the number of outputs is high. Nevertheless, in this design, size is not the key point as will be explained at the end of this section. The main issue is achieving high efficiency. If the galvanic isolation is provided by the second stages, the first stage can be a Boost converter in Critical Mode, which has an efficiency as high as 97%. Hence, if the number of independent outputs is low (2, 3 or 4) or even is a single output, the size is not significantly increased by achieving galvanic isolation in the second stage but efficiency is considerably improved.

- Smaller filter. The voltage at the output of the second-stage rectifier is easier to filter (see Fig. 2) and, consequently, the necessary size of the filter is smaller. This is especially important taking into account that no electrolytic capacitors can be used.

It should be taken into account that size is not the key point in the design of the second stages due to the characteristics of the first stage. As electrolytic capacitors cannot be used, the size of the output capacitor of the first stage is going to be high because this converter is a PFC. Besides, the size of this capacitors is not determined by the chosen switching frequency, but by the line frequency (in fact, twice the line frequency). Hence, the bulkiest stage is the first one and any size reduction in the second stages will not considerably affect the overall size of the LED driver.

This paper is organized as follows. Section II is focused on the steady-state analysis of the second stage, the AHB. Section III analyses the minimization of the average value of the magnetizing current by means of the asymmetrical design of the transformer. Section IV describes the model of the converter during the dead time, which is useful for designing an AHB with reduced switching losses. Finally, section V is a design guideline following all the previous explanations, section VI describes the experimental results and section VII gathers the conclusions.

II. Asymmetrical Half Bridge

First of all, it should be taken into account that the first stage of the proposed topology is a boost converter whose purpose is to achieve PFC with high efficiency. The principle of operation of this kind of converter is very well known [18, 19].

For the proposed two-stage topology, the main issue is that implementing this Boost converter without electrolytic capacitors implies a considerable low-frequency ripple at the output. This ripple is then determinant in the design of the second stages. The relative value of this peak to peak ripple will be denoted as r_v in this paper and is referred to the nominal output voltage V_g. Hence, the output voltage as a function of time can be expressed as:

$$V_g = V_{g\_nom}\cdot\left(1+\frac{r_v}{2}\cdot\sin(2\cdot\omega_{in}\cdot t)\right). \quad (1)$$

where $\omega_{in} = 2\cdot\pi\cdot f_{in}$, f_{in} being the line frequency, and V_{g_nom} is the nominal value of the first stage output voltage. It should be taken into account that the ripple of the first stage will not affect the output voltage of the second stage as its close-loop control can be fast enough to cancel this ripple.

The schematic of the AHB can be found in Fig. 2 [20-23]. As can be seen, it consists of a Half-Bridge (HB) converter with their switches controlled with complementary signals (i.e. ideally, one of the two primary switches is always on, different from what happens in standard HBs). The main consequence of this control technique is that, due to the necessity of maintaining the volt·second balance in the transformer magnetizing inductor, the input capacitor voltages will vary according to the following equations:

$$V_{C1} = (1-D)\cdot V_g, \quad (2)$$

$$V_{C2} = D\cdot V_g, \quad (3)$$

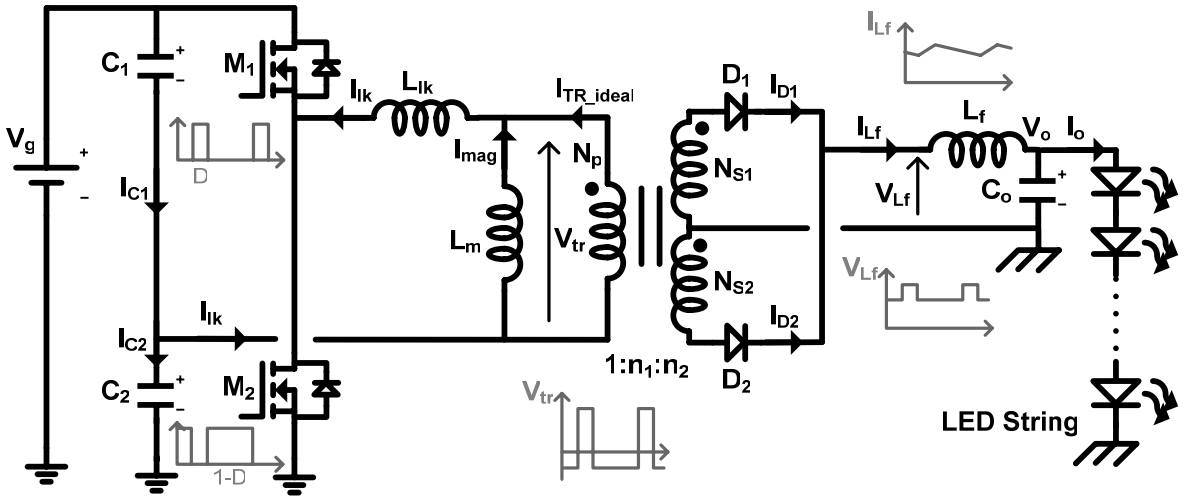


Fig. 2. Schematic of the proposed AHB.

where V_{ci} is the voltage across each input capacitor, D is the duty cycle of S_1 and V_g is the input voltage of the AHB. It should be taken into account that in the AHB, D must be always lower than 0.5.

The output voltage will depend on the input voltage, the duty cycle and the turns ratios of the transformer ($n_1=N_{s1}/N_p$ and $n_2= N_{s2}/N_p$):

$$V_o = n_1 \cdot V_{C1} \cdot D + n_2 \cdot V_{C2} \cdot (1-D) = \\ = V_g \cdot D \cdot (1-D) \cdot (n_1 + n_2) \quad (4)$$

Analyzing the current balance in the primary side, it should be taken into account that the current through the leakage inductance satisfies the following equation:

$$I_{lk} = I_{C1} - I_{C2} = I_{mag} + I_{TR\_ideal}, \quad (5)$$

where I_{TR_ideal} is the current through the ideal transformer, I_{mag} the current through the magnetizing inductor, I_{C1} and I_{C2} are the currents through the input capacitors C_1 and C_2 and I_{lk} is the current of the leakage inductance. The average value of I_{C1} and I_{C2} is zero as they are capacitor currents. Hence, in average value I_{mag} is equal to I_{TR_ideal} with different sign. Besides, during D·T, the current through the ideal transformer is equal to $I_o \cdot n_1$ while, during (1-D)·T is equal to $-I_o \cdot n_2$. Considering this, the average value of the magnetizing current of the transformer is:

$$\overline{I}_{TR\_ideal} = -\overline{I}_{mag} = -I_o \cdot [D \cdot (n_1 + n_2) - n_2], \quad (6)$$

As can be seen from (6), the average value of the magnetizing current is not necessarily zero, which is different from the situation of conventionally-driven HBs. The main consequence of this average value in that the conduction losses of the transformer are going to be higher. This non-zero average value also increases the conduction losses of the MOSFETs. Taking into account the low power level that this converter will be driving (normally, LED strings are rated for 40-50 W), these losses imply a considerable reduction in efficiency. In section III, the method employed for reducing this average value of the magnetizing current will be described. The basic idea is using asymmetrical secondary windings in the transformer. This is different from the current design and results in a minimization of the average value of the magnetizing current.

A second important aspect regarding the AHB is the switching losses in MOSFETs and diodes. The switching losses of the MOSFETs can be easily reduced by employing techniques that allow them to reach Zero Voltage Switching (ZVS). Nevertheless, these techniques usually use the energy stored in the leakage inductance. Due to the low value of the output current in LED-based applications (usually it is around 0.350 A), the value of the current through the leakage inductance is also low and so is the energy stored in it. As a consequence, in this low-current application it is not always possible to reach real ZVS and close-to-ZVS situations become acceptable. A possible solution is reducing the value of the magnetizing inductance. This leads to an increase of the magnetizing current ripple and, consequently, an increase in the amount of energy stored in the leakage inductance at the moment when the MOSFETs are switched. The application of this technique in this kind of converter will be deeply analyzed in section IV, as it is possible to reach ZVS even with low current levels at the output. Regarding the switching process of the diodes, an important issue should be highlighted. Due to the voltage levels at the secondary side of the transformer, it is not possible to use Schottky diodes. Hence, switching losses become relevant as ultrafast diodes are used. As will be explained in section IV, these switching losses are, in fact, the main factor of losses in this converter. In this section, the model of the converter during dead times will be also explained. This model will be used in section V for designing an AHB with reduced switching losses not only in MOSFETs, but also in diodes.

Apart from galvanic isolation, which is an important feature in order to comply with some regulations and/or customer requirements, another important advantage of the proposed topology is the size of the output filter. The voltage at the output of the AHB rectifier is easier to filter (see Fig. 2.). Hence, the size of the output inductor and/or the output capacitor can be smaller. This is especially important taking into account that no electrolytic capacitors can be used.

III. AVERAGE MAGNETIZING CURRENT MINIMIZATION

Normally, the analysis of the steady state of the AHB is done considering an equal number of turns in both secondary windings. Even when this is not considered as a design rule, such as in [24], the aim is different from reducing losses. In this section, the minimization of the average magnetizing current (and therefore of the conduction losses) will be analyzed.

As can be seen from equation (6), the average magnetizing current depends on the output current, the turn ratios of the transformer and the duty cycle. Hence, for a given value of the output current there is a linear relation between the magnetizing current and the duty cycle (n_1 and n_2 are fixed for a given AHB). Therefore, the minimum value of the average magnetizing current corresponds to the situation in which the duty cycle is maximum (D_{max}):

$$\overline{I}_{mag\_min} = -I_o \cdot [D_{max} \cdot (n_1 + n_2) - n_2]. \quad (7)$$

Besides, the maximum average magnetizing current takes place when the duty cycle is minimum (D_{min}):

$$\overline{I}_{mag\_max} = -I_o \cdot [D_{min} \cdot (n_1 + n_2) - n_2]. \quad (8)$$

Therefore, the overall minimization of both values is achieved when they are equal in absolute value. This leads to the following condition:

$$(D_{max} + D_{min}) = 2 \cdot \frac{n_2}{(n_1 + n_2)}. \quad (9)$$

This condition and the aforementioned linear relation imply that there is a duty cycle (D_{lm0}) for which the average value of the magnetizing current is zero:

$$0 = I_o \cdot [D_{lm0} \cdot (n_1 + n_2) - n_2], \quad (10)$$

so,

$$D_{lm0} = \frac{n_2}{(n_1 + n_2)}. \quad (11)$$

Considering equations (9) and (11), D_{lm0} can be expresses as:

$$D_{lm0} = \frac{D_{min} + D_{max}}{2}. \quad (12)$$

which fixes the condition for minimizing the average value of the magnetizing current of the transformer. The required values for D_{min} and D_{max} are explained in section V. The main consequence of this design method is that n_1 and n_2 are going to be different, as can be deduced from equation (11).

A graphical explanation can be found in Fig. 3. As can be seen, the average magnetizing currents of two different AHB are plotted. The red line (proposed design) represents an AHB designed taking into account equation (12). This is achieved by wisely choosing the values of n_1 and n_2 [see equation (11)]. The AHB that corresponds to the blue line followed a standard design in which n_1 and n_2 values are equal and do not satisfy equations (11) and (12). For both converters, the valid range of the duty cycle is [0.24, 0.4]. As can be seen, the maximum value of the average magnetizing current of the converter designed observing equation (12) is equal to the minimum one in absolute value ($I_{mag\_max\_1}$ and $I_{mag\_min\_1}$). Nevertheless, when this equation is not considered (blue line), these minimum and maximum values are unbalanced ($I_{mag\_max\_2}$ and $I_{mag\_min\_2}$).

IV. Zero Voltage Switching

As has been said, due to the low value of the nominal output current, ZVS is quite difficult to achieve in the AHB because the amount of energy stored in the leakage inductance is not high enough. Three options are possible in this situation:

- Increasing the amount of energy stored in the leakage inductance by increasing the value of the magnetizing current.
- Increasing the amount of energy stored in the leakage inductance by increasing the value of the leakage inductance.
- Accepting the closest situation to ZVS that can be achieved for the amount of energy that is stored in the leakage inductance without increasing either the magnetizing current or the leakage inductance.

The last option may be valid if high efficiency is not a primary concern. Nevertheless, in this application the overall efficiency is very important and the switching losses have a great impact on it.

The second option, in a real design, leads to a high-size external inductor in series with the transformer. Besides, ZVS would not be achieved for the whole load range.

Therefore, in this kind of application it is necessary to increase the amount of energy stored in the leakage inductance by increasing the magnetizing current in the moment in which the switching processes take place. Nevertheless, it should be taken into account that this increment cannot be achieved by increasing the average value of the magnetizing current. As can be seen in the upper graph of Fig. 4, the aforementioned increase of the average value of the magnetizing current raises the amount of energy stored in the leakage inductance when one of the MOSFETs is going to be turned on (see M_1-ZVS-proper-sign point in Fig. 4). Hence, for this MOSFET is easier to achieve ZVS. Nevertheless, it is impossible for M_2 to reach ZVS because the leakage current has still positive sign (wrong sign) when this MOSFET is going to be turned on (see Fig. 2 and Fig. 4). Even if the sign were correct, the amount of energy stored in the leakage inductance would not be high enough to achieve ZVS due to the influence of the average value of I_{mag} on the value of I_{lk} at this moment. Hence, reducing the average value of I_{mag} not only reduces the conduction losses of the transformer and the MOSFETs, but it also makes easier to achieve ZVS in both MOSFETs (see lower graph of Fig. 4).

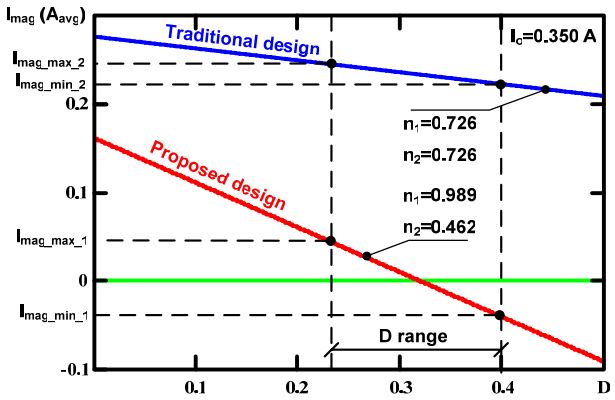


Fig. 3. Average magnetizing current for two different AHB.

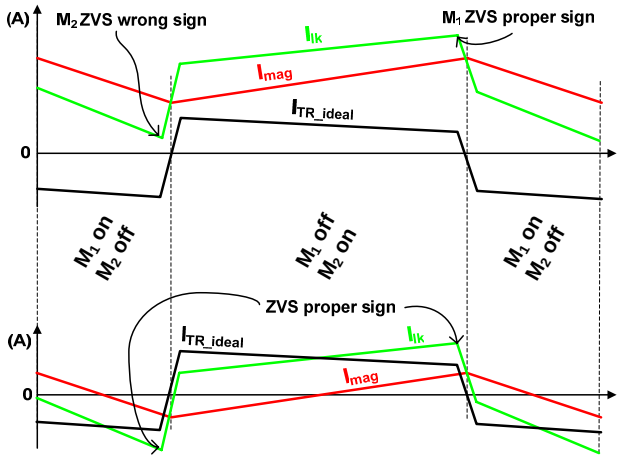


Fig. 4. Leakage inductance current for two different conditions of the average magnetizing current.

The best option for increasing the magnetizing current in the right instants (i.e., switching instants) is reducing the value of the magnetizing inductance. In this way, the ripple of I_{mag} increases and so it does the energy stored in the leakage inductance L_{lk} when the MOSFETs are going to be switched. This also increments the rms value of the current and, consequently, the conduction losses in the transformer and the MOSFETs. Nevertheless, the increment of the conduction losses is less significant than the decrease in the switching losses. The calculation of the necessary transformer magnetizing inductance will be done later in this section.

Although the switching losses in the MOSFETs before the aforementioned reduction were relevant, in this kind of application the most critical issue are the switching losses in the diodes. Due to the value of the output voltage (in the case of standard street-lighting in Europe, around 150 V), it is not possible to use Silicon Schottky diodes and, therefore, ultrafast ones must be used. Hence, it is necessary to wisely analyze their switching process in order to assure that MOSFETs are not switched before the diodes have naturally turned off and on. In this way, switching losses in the four switches (MOSFETs and diodes) are considerably reduced and efficiency is increased. First of all, it should be taken into account that the switching process of the diodes is related to the switching process of the MOSFETs. Hence, in the next sections the behaviour of currents and voltages across diodes and MOSFETs are described during the switching dead time. In this way, the equations that describe this dead time will help in the design of the proposed AHB. Some considerations are done in this analysis:

- The voltages of the input capacitors (C_1 and C_2) are considered constant, so they will be represented as voltage sources V_{C1} and V_{C2} in Fig. 5, Fig. 6 and Fig. 7.
- The current through the output inductor can be considered constant during the switching dead time.
- The value of the leakage inductance L_{lk} is considerably lower than the value of the magnetizing inductance L_m.

The switching dead time can be divided into three different stages. For the sake of simplicity, only the dead time between M_2 is turned off and M_1 is turned on is going to be analyzed. Nevertheless, similar equations can be obtained for the other dead-time transient response (i.e., when M_1 is turned off and M_2 is turned on).

FIRST STAGE

The beginning of this first stage takes place when the MOSFET M_2 is turned off and the equivalent circuit for describing the operation is the one shown in Fig. 5. The primary side of the ideal transformer can be modelled as a current source ($I_{TR\_ideal\ S1}$). This source can be considered constant due to the high value of the output inductor and the short duration of the dead time, but the ripple in the output-inductor current should be taken into account.

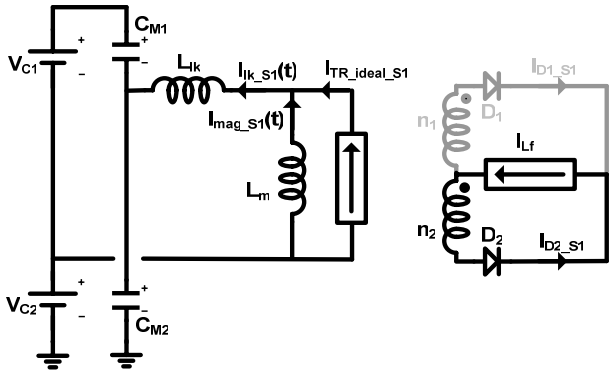


Fig. 5. Equivalent circuit of the AHB during the first stage.

Hence, its constant value referred to the transformer's primary side can be expressed as:

$$I_{TR\_ideal\_S1} = \max\left[0, \left(I_o - \frac{V_g \cdot D \cdot (1-D) \cdot (n_1 + n_2) - V_g \cdot D \cdot n_2}{2 \cdot L_f} \cdot \frac{1-D}{f}\right) \cdot n_2\right] \quad (13)$$

where L_f is the value of the output filter inductor, f is the switching frequency of the AHB and I_0 is the output current. As the Discontinuous Conduction Mode (DCM) may take place, negative values are not possible and the max function is introduced to obtain a general expression for both CCM and DCM.

The output current, considering the characteristic of the load (i.e. LED string) and equation (4), can be expressed as:

$$I_o = \max\left[0, \frac{V_g \cdot D \cdot (1-D) \cdot (n_1 + n_2) - V_{\gamma\_LED} \cdot N}{R_{LED} \cdot N}\right], \quad (14)$$

where V_{γ_LED} is the knee voltage of one LED diode, N the number of LEDs in the string and R_{LED} the dynamic resistance of a single LED. Obviously, negative current is not possible in this kind of load and the max function is again necessary.

Considering the circuit of Fig. 5, the equation that defines the voltage V_{CM2_S1} across the parasitic capacitance of MOSFET M_2 (C_{M2}) during this stage is:

$$V_{CM2\_S1}(t) = V_g \cdot D - V_g \cdot D \cdot \cos(\omega \cdot t) + \left(I_{TR\_ideal} + \frac{1}{2 \cdot L_m} \cdot V_g \cdot D \cdot \frac{1-D}{f} - I_o \cdot [D \cdot (n_1 + n_2) - n_2]\right) \cdot L_T \cdot \omega \cdot \sin(\omega \cdot t), \quad (15)$$

where L_m is the value of the magnetizing inductance, L_T is the value of L_m plus the value of the leakage inductance L_{lk} and ω is:

$$\omega = \frac{1}{\sqrt{L_T \cdot C_T}}, \quad (16)$$

where C_T is the sum of the two MOSFET parasitic capacitances C_{M1} and C_{M2}.

In equation (15), the second addend takes into account the current of the ideal transformer, the ripple of the magnetizing current and its average value. If the average

magnetizing current has been minimized as explained in the previous section, it can be disregarded:

$$V_{CM2\_S1}(t) = V_g \cdot D - V_g \cdot D \cdot \cos(\omega \cdot t) + \\ + \left(I_{TR\_ideal} + \frac{1}{2 \cdot L_m} \cdot V_g \cdot D \cdot \frac{1-D}{f} \right) \cdot L_T \cdot \omega \cdot \sin(\omega \cdot t) \quad (17)$$

The end of this stage takes place when the voltage across the ideal transformer is zero, which means that the voltage across the magnetizing inductor is zero. In that moment, the voltage of the secondary windings is zero and the diodes change their situation: diode D_2 is going to be turned off while D_1 is going to be turned on. Considering that L_T is nearly equal to L_m (due to the low value of L_{lk}), the end of this stage can be obtained by finding the instant in which the input voltage of the real transformer is zero (i.e. V_{CM2_S1} is equal to V_{C2}):

$$V_g \cdot D \cdot \cos(\omega \cdot t_1) - \\ - \left(I_{TR\_ideal} + \frac{1}{2 \cdot L_m} \cdot V_g \cdot D \cdot \frac{1-D}{f} \right) \cdot L_T \cdot \omega \cdot \sin(\omega \cdot t_1) = 0 \quad (18)$$

All the parameters are known in equation (18) except t_1, which is the end of the first stage of the dead time.

For the next step, the current through the leakage inductance at the end of this step [$I_{lk\_S1}(t_1)$] is going to be needed as an initial condition for the differential equation:

$$I_{lk\_S1}(t_1) = V_g \cdot D \cdot \omega \cdot C_T \cdot \sin(\omega \cdot t_1) + \\ + \left(I_{TR\_ideal} + \frac{1}{2 \cdot L_m} \cdot V_g \cdot D \cdot \frac{1-D}{f} \right) \cdot \cos(\omega \cdot t_1) \quad (19)$$

SECOND STAGE

In the second stage (see Fig. 6), the current source is no longer constant and the switching process of the diodes needs to be analyzed.

At the beginning of this second stage, diode D_2 has begun the turning-off while D_1 has begun the turning-on. This means that the current through diode D_2 is going to be negative and equal to its reverse recovery current. Considering that the current through the output inductor is constant, the current through D_1 [$I_{D1}(t')$]can be expressed as:

$$I_{D1\_S2}(t') = \max\left[0, \right. \\ \left., \left(I_0 - \frac{V_g \cdot D \cdot (1-D) \cdot (n_1 + n_2) - V_g \cdot D \cdot n_2}{2 \cdot L_f} \cdot \frac{1-D}{f} \right) \right] - \\ - I_{D2\_S2}(t') \quad (20)$$

where $I_{D2\_S2}(t')$ is the current through D_2 and t' is the time referred to t_1 (i.e. t'=t-t_1).

Hence, the current through the ideal transformer is:

$$I_{TR\_ideal\_S2}(t') = -\left[\max\left[0, \right. \right. \\ \left. \left., \left(I_0 - \frac{V_g \cdot D \cdot (1-D) \cdot (n_1 + n_2) - V_g \cdot D \cdot n_2}{2 \cdot L_f} \cdot \frac{1-D}{f} \right) \right] - \\ \left. - I_{D2\_S2}(t') \right] \cdot n_1 + I_{D2\_S2}(t') \cdot n_2 \quad (21)$$

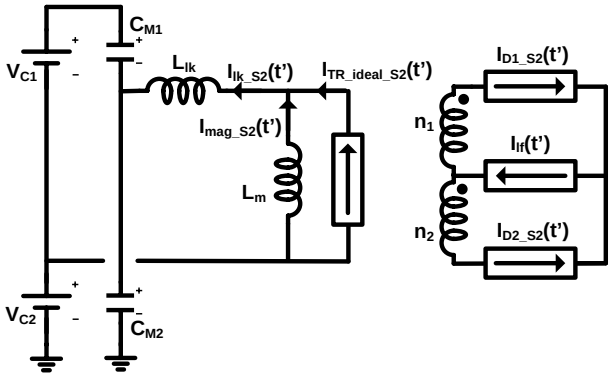


Fig. 6. Equivalent circuit during the second stage.

Although it has an exponential behaviour, the reverse recovery current of a diode can be modelled with a linear equation:

$$I_{D2\_S2}(t') = -I_{pk} + \frac{I_{pk}}{t_{rr}} \cdot t', \quad (22)$$

where I_{pk} is the reverse peak current and t_{rr} is the reverse recovery time of the diode D_2. These two parameters should be obtained from experimental data or from the datasheet, as they will strongly depend on I_o, V_g, D, etc.

L_M and L_f are considerably higher than L_{lk}, and, as a consequence, any sudden variation of the current in the secondary windings (such as the reverse recovery current) will mainly affect the current of the leakage inductance after a very short transitory which is disregarded in this analysis. Hence, considering this and equations (14), (21) and (22), the initial current through the leakage inductance in this second stage (t'=0) is:

$$I_{lk\_S2}(0) = I_{lk\_S1}(t_1) - \left[\max\left[0, \right. \right. \\ \left. \left., \left(I_0 - \frac{V_g \cdot D \cdot (1-D) \cdot (n_1 + n_2) - V_g \cdot D \cdot n_2}{2 \cdot L_f} \cdot \frac{1-D}{f} \right) \right] + \\ \left. + I_{pk} \right] \cdot (n_1 + n_2) \quad (23)$$

As can be seen from this equation, the initial value (after a very short transitory) of the leakage inductance at the beginning of the second stage is equal to the value of its current at the end of the first stage minus a factor which depends on the reverse peak current of D_2 and the current of the output inductor.

The equations that define this second stage are:

$$V_{CM2\_S2}(t') = V_g \cdot D - \frac{L_m \cdot (n_1 + n_2) \cdot I_{pk}}{t_{rr}} \cdot \cos(\omega \cdot t) + \\ + L_T \cdot \omega \cdot I_{lk\_S2}(0) \cdot \sin(\omega \cdot t') + L_m \cdot (n_1 + n_2) \cdot \frac{I_{pk}}{t_{rr}} \quad (24)$$

$$I_{lk\_S2}(t') = \frac{L_m \cdot (n_1 + n_2) \cdot I_{pk}}{L_T \cdot t_{rr} \cdot \omega} \cdot \sin(\omega \cdot t) + I_{lk\_S2}(0) \cdot \sin(\omega \cdot t') \quad (25)$$

The time needed by the parasitic capacitor of M_2 to be completely charged can be calculated with equation (24):

$$0 = V_g \cdot (D-1) - \frac{L_m \cdot (n_1 + n_2) \cdot I_{pk}}{t_{rr}} \cdot \cos(\omega \cdot t'_{2\_aux}) + \\ + L_T \cdot \omega \cdot I_{lk\_S2}(0) \cdot \sin(\omega \cdot t'_{2\_aux}) + L_m \cdot (n_1 + n_2) \cdot \frac{I_{pk}}{t_{rr}} \quad (26)$$

The duration of this second stage is not always equal to t'_{2_aux}. It is necessary to compare this time with t_{rr}. If it is shorter, the parasitic capacitor M_2 will be fully charged and ZVS will be achieved if MOSFET M_1 is turned on. Nevertheless, if t'_{2_aux} is longer than t_{rr}, ZVS has not been achieved and a third stage needs to be analyzed:

$$t'_2 = \min(t'_{2\_aux}, t_{rr}) . \quad (27)$$

A very important issue of this stage is that the variation of the voltage applied by the secondary windings to the diodes is slow in comparison to the situation in which M_1 is turned on and $(n_1+n_2)\cdot(1\text{-}D)\cdot V_g$ is directly applied to the reverse biased diode. Hence, the reverse peak current is going to be small and, therefore, the di/dt of the current is going to be small also. As a consequence, the reverse recovery time (t_{rr}) is going to be longer as can be deduced from [25, 26] or the datasheet of any diode. Although it is longer, the reduction in the reverse recovery current is considerable and, as a consequence, losses in diodes are reduced. The precise variation of t_{rr}, I_{pk} and di/dt for different operating conditions of this converter is quite difficult to predict. Datasheets only provide part of the information and not for so low values of the diode voltage. Hence, two options are possible:

- Developing a mathematical expression as a result of experimental data.
- Considering the same values of these variables for any valid operating condition of the converter. These values should reflect the worst possible situation (i.e.: highest I_{pk}, etc.)

THIRD STAGE

In this final stage, the conditions are similar to the first stage (see Fig. 7). Only one diode is turned on (D_1) while the other is turned off (D_2). The only difference, apart from the initial conditions, is that the current of the output inductor referred to the primary side of the transformer has different sign in this third stage.

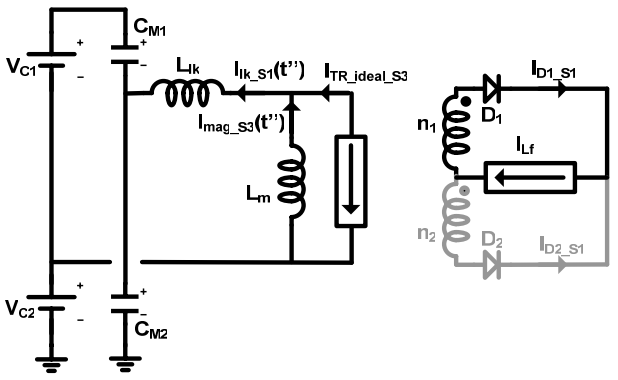


Fig. 7. Equivalent circuit during the third stage.

The equation of the parasitic capacitor voltage for this stage is:

$$V_{CM2\_S3}(t'') = V_g \cdot D - \left[V_g \cdot D - V_{CM2\_S2}(t_2') \right] \cdot \\ \cdot \cos(\omega \cdot t'') + L_T \cdot \omega \cdot I_{lk\_S2}(t_2') \cdot \sin(\omega \cdot t'') \quad (28)$$

This stage ends when the voltage of this capacitor is equal to V_g or when it reaches a maximum lower than V_g (in this case, ZVS would be impossible to achieve). It should be taken into account that, under certain circumstances, this voltage is reached in the second stage. The time (t_3'') for this to happen can be calculated from equation (28) as follows:

$$0 = V_g \cdot (D-1) - \left[V_g \cdot D - V_{CM2\_S2}(t_2') \right] \cdot \\ \cdot \cos(\omega \cdot t_3'') + L_T \cdot \omega \cdot I_{lk\_S2}(t_2') \cdot \sin(\omega \cdot t_3'') \quad (29)$$

OVERALL ANALYSIS

Considering the three stages, equations (18), (26) and (29) allow us to calculate the minimum time needed by a certain AHB to reach ZVS in MOSFETs, taking into account how the rectifier diodes affect this process and assuring that the MOSFETs switch when the diodes has naturally turned on and off:

$$t_T = t_1 + t_2' + t_3'' . \quad (30)$$

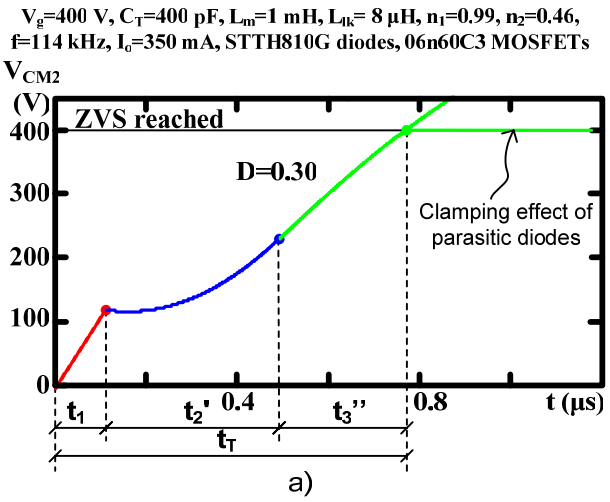
Besides, with equations (17), (24) and (28) and the time needed for each stage to finish (t_1, t_2' and t_3'') it is possible to predict the behaviour of V_{CM2} during the transition time (i.e., dead time) as shown in Fig. 8. As the input voltage (V_g) is 400 V, ZVS is achieved when the voltage across C_{M2} reaches this value (solid black line). Besides, the end of each stage (t_1, t'_2 and t''_3) is represented with a dot of the corresponding colour. As can be seen in Fig. 8a, each stage shows a different behaviour ruled by the previously defined equations. The fist stage ends when the voltage is close to 120 V (which is the voltage across C_2 when D=0.30). The second one depends on the reverse recovery time t_{rr} of D_2. The third stage lasts until the voltage across the parasitic capacitor C_{M2} is equal to the input voltage V_g. In that moment, V_{CM2} is clamped to V_g due to the parasitic diodes of the MOSFETs. In Fig. 8a and Fig. 8b, the evolution of V_{CM2} during the third stage has been represented both with the clamping effect of the diodes and without it. In Fig. 8b, the voltage of C_{M2} is represented for specific conditions and two possible duty cycles. As can be seen, for lower duty cycles the relevant time is t_3'' while for higher ones is t_2'.

It is important to highlight that t_T represents the minimum required time for the AHB to achieve ZVS. Hence, any dead time (t_{dead}) longer than t_T will assure ZVS:

$$t_{dead} \geq t_T . \quad (31)$$

This condition will be taken into account in the design guideline for a valid AHB (section V).

In Fig. 9, the minimum needed dead time t_T is represented for specific conditions as a function of D. As



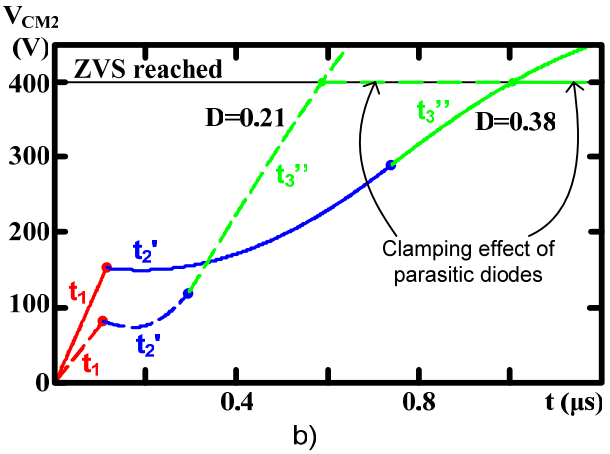


Fig. 8. Voltage of C_{M2} for different duty cycles.

can be seen, t_1 is quite short if compared with t_2' or t_3''. It should be taken into account that during the first stage, the current of the ideal transformer is added to the current of the magnetizing inductance. Hence, the amount of energy stored in the leakage inductance is high and, consequently, the parasitic capacitors are easily charged/discharged. As can be seen, t_2' increases with the duty cycle. It should be taken into account that, for this representation, the value of t_{rr} and I_{pk} for different conditions of current and voltage (i.e. for different duty cycles) has been obtained by experimental analysis of the diodes. For low values of the duty cycle, the current demanded by the LED string is zero. Hence, the time of this second stage is nearly zero because diodes are nearly not-biased. For higher values, the output current increases. As a consequence, the amount of energy stored in the leakage inductance decreases [see equation (23)] and slows down the charge/discharge process of the parasitic capacitors of the MOSFETs. Finally, the duration of the third stage (t_3'') decreases as the duty cycle increases. Although it should behave like t_2' (i.e. the higher the output current, the lower the leakage current), the starting voltage of this third stage increases with D, so the voltage swing of each capacitor is lower.

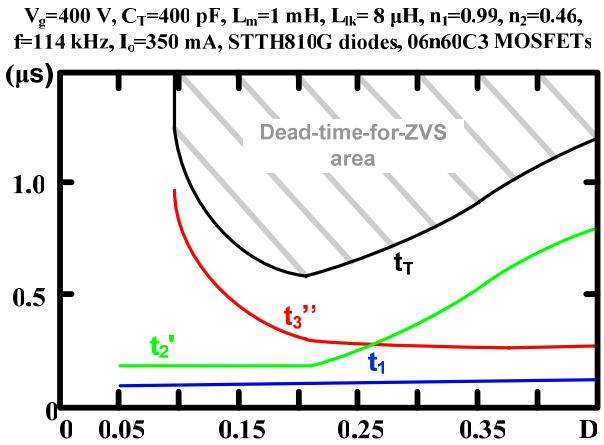


Fig. 9. Minimum dead time needed for achieving ZVS.

In Fig. 10, the minimum needed dead time for ZVS t_T is represented for different input voltages (solid lines). It should be highlighted that, in this figure, the reverse peak current I_{pk} and the reverse recovery time t_{rr} of the diodes are considered constant and equal to the worst possible value for any input voltage and for any duty cycle (in Fig. 8 and Fig. 9, the mathematical expressions of t_{rr} and i_{pk} for V_g=400 V were used). As can be seen, there are certain values of D for which the leakage inductance energy is so low (or V_g so high) that it is not possible to reach ZVS for the given conditions (for example, V_g=450 V, L_m=1mH and D<0.1 or D>0.35). This should be taken into account in the design process as ZVS should be reached, preferably, in nominal conditions.

Finally, the equations obtained during the previous sections not only allow us to predict the behaviour of the voltage across the parasitic capacitors and the time needed for reaching ZVS, they also allow us to determine the maximum magnetizing inductance L_m that ensures ZVS. For doing so, the first step is calculating when the voltage of the parasitic capacitance V_{CM2} reaches its maximum during the third stage by differentiating equation (28) and making it equal to zero:

$$0 = \left[V_g \cdot D - V_{CM2\_S2}(t_2')\right] \cdot \omega \cdot \sin(\omega \cdot t_{max}'') + \\ + L_T \cdot \omega^2 \cdot I_{lk\_S2}(t_2') \cdot \cos(\omega \cdot t_{max}'') \quad , \qquad (32)$$

where t_{max}'' is the instant when the voltage of C_{M2} reaches a maximum due to the under-damped behaviour of the equivalent circuit of stage three (Fig. 7).

Using (28) and the value of t_{max}'' obtained from (32), it is possible to obtained the maximum value of the magnetizing inductance (L_{m_max}) for any duty cycle D and for any input voltage V_g. For doing so, the condition to analyze is that when the magnetizing inductance is equal to L_{m_max}, the voltage across the parasitic capacitance C_{M2} when it reaches its maximum (t_{max}'') is equal to the input voltage V_g:

$$V_{CM2\_S3}(t_{max}'') = V_g \cdot D - \left[V_g \cdot D - V_{CM2\_S2}(t_2')\right] \cdot \\ \cdot \cos(\omega \cdot t_{max}'') + (L_{m\_max} + L_{lk}) \cdot \omega \cdot I_{lk\_S2}(t_2') \cdot \qquad . \qquad (33) \\ \cdot \sin(\omega \cdot t_{max}'') = V_g$$

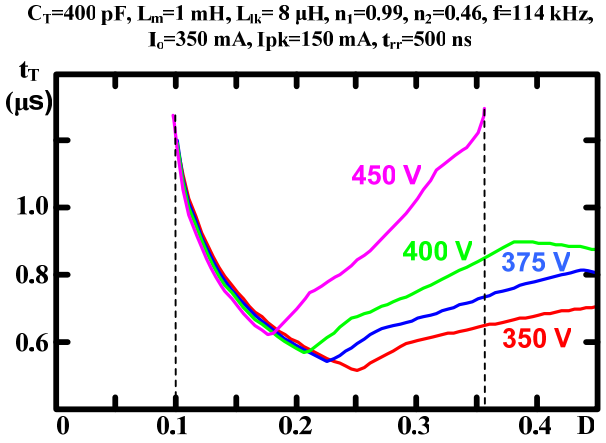


Fig. 10. t_T for different input voltages (V_g).

It should be taken into account that $V_{CM2\_s2}(t_2')$ and $I_{lk\_s2}(t_2')$ are obtained from equations that also depends on the magnetizing inductance. Hence, there is no analytical solution and a calculation software, such as MathCad®, needs to be used. In Fig. 11, the value of L_{m_max} is given for specific conditions as an example. As can be seen, the maximum value of the magnetizing inductance varies as D is modified. Assuring ZVS for the whole range involves analyzing the worst situation and selecting a magnetizing inductance lower than the corresponding value of L_{m_max}. In Fig. 11, the worst situation takes place when D=0.45 and, consequently, L_m should be lower than 2 mH in order to ensure ZVS in any situation.

V. Design Guideline

The design of this AHB for street lighting needs to consider the equations defined in the previous two sections in order to obtain a high efficiency converter. The design of this two-stage topology should begin with the second stages (i.e. the AHB) but fixing the value of the first-stage output voltage and its ripple, which cannot be neglected due to the absence of electrolytic capacitors. Typical values, taking into account that no electrolytic capacitors are going to be used, are around 10%. The other values that should be known are given by the LED strings:

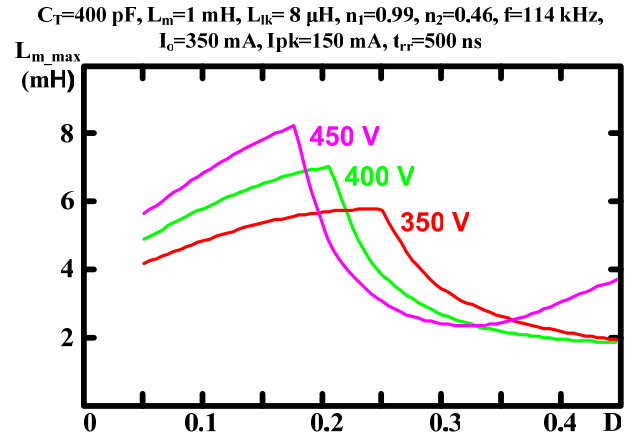


Fig. 11. $L_{m\ max}$ for different values of Vg and D.

number of LEDs per string (N), knee voltage of each LED (V_{γ_LED}), its dynamic resistance (R_{LED}) and its nominal current (I_{nom}) or its nominal power (P_{nom}).

The maximum and minimum values of the output voltages of the AHB for total dimming can be calculated as:

$$V_{out\_max} = N \cdot V_{\gamma\_LED} + N \cdot R_{LED} \cdot I_{nom} = \frac{P_{nom}}{I_{nom}} . \quad (34)$$

$$V_{out\_min} = N \cdot V_{\gamma\_LED} . \quad (35)$$

To achieve ZVS, a suitable value for the total dead time (considering both transitions) may be around 15%-20%. This leads to a maximum duty cycle (D_{max}) of 43%-40%. Using equations (1), (4) and (34):

$$n_1 + n_2 = \frac{N \cdot \frac{P_{nom}}{I_{nom}}}{V_{g\_nom} \cdot \left(1 - \frac{r_v}{2}\right)} \cdot \frac{1}{D_{max} \cdot (1 - D_{max})} . \quad (36)$$

The value of D_{min} can be obtained from (36) and (4), considering the minimum output voltage (35) and the maximum input voltage (1). Once D_{min} and D_{max} are known, it is possible to obtain D_{Im0} from (12) and, finally, n_1 and n_2 from (11) and (36).

With these parameters, it is possible to design the output inductor and the transformer by standard methods. Once they are designed, and taking into account the resulting leakage inductance of the transformer, it is possible to use the equations of section IV for fixing the necessary magnetizing inductance of the transformer. With equation (33), it is possible to determine the value of L_{m_max}. As has been said, this equation cannot be solved analytically. The chosen magnetizing inductance needs to assure ZVS for any condition (input voltage V_g and duty cycle D) and it can be easily obtained by wisely choosing the gap in the core. Nevertheless, this equation does not provide any kind of information about the time needed for reaching ZVS. With the selected value of L_m, it is possible to use equation (30) in order to obtain the value of the minimum dead time t_T required for reaching ZVS. If this time represents an excessive percentage of the total switching time, the maximum duty cycle may be compromised and it is necessary to reduce t_T. For doing so, the value of L_m needs to be reduced. That increases the amount of energy stored in the resonant circuit during the third stage of the transition and it also increases its resonant frequency. As a consequence, the parasitic capacitances are charged/discharged quicker and t_T is shorter (i.e., ZVS is reached earlier).

VI. Experimental Results

A prototype of the AHB (second stage) has been built and tested (see Fig. 12). It is designed for supplying a 40-W LED string with a $N \cdot V_{\gamma\_LED}$=95 V and a $N \cdot R_{LED}$=140 Ω. The nominal input voltage is (400 ± 7%) V. The MOSFETs are 06N60C3 and they have a parasitic capacitance of 200 pF each at V_{DS}=25 V. The transformer is built in an E30 core and the output inductor in an E20 one. The rectifier diodes are STTH810G. C_{pos} and C_{neg} are 300-nF capacitors (three 100-nF capacitors in parallel each) and C_f is a 1-µF MKP capacitor. The switching frequency is 114 kHz in order to obtain a switching period considerably longer than the dead times.

Using equations of sections III and V, and fixing the maximum duty cycle (in this case, D_{max}=0.4), it is possible to obtain D_{Im0}, D_{min}, n_1 and n_2 (equal to 0.327, 0.253, 1.075 and 0.521, respectively, in the built prototype). With these values, the design of the output inductor and the transformer and the selection of the semiconductors can be carried out achieving the minimization of the average value of the magnetizing current. The optimum design for this prototype leads to an 8-µH transformer leakage inductance and a 2.5 mH filter inductor. Once this point of the design process is completed, it is possible to use equation (33) in order to determine the maximum value of L_m (see L_{m_max} in Fig. 11). In this case, a magnetizing inductance of 2 mH assures ZVS for any condition. Nevertheless, the resulting t_T for this value (around 4 µs for each transition) is excessively long for the 114-kHz switching frequency. Hence, the transformer gap is increased so that the resulting magnetizing inductance of the transformer is reduced to 1 mH and t_T for the worst possible situation is reduced to 1 µs (i.e. each transition lasts 10% of the total period).

In Fig. 13a, the V_{DS} and the V_{GS} of MOSFET M_2 is shown when the prototype is providing the nominal current. As can be seen, ZVS is achieved. This means that the amount of energy stored in the leakage inductance is enough. In Fig. 13b, a detail of the transition is shown.

In Fig. 14, the voltage V_{DS} across one of the MOSFETs and the leakage inductance current are shown at full load (a) and at no-load (b) condition. In both situations, ZVS is achieved. As can be seen in Fig. 14a, at the beginning of t_2' (i.e. second stage of the dead time), the leakage current is strongly reduced as a consequence of the reverse recovery current of the diode that is being turned off and the current of the diode that is being turned on (which is driving a current equal to the output current plus the other diode current). Nevertheless, the remaining amount of energy stored in the leakage inductance is high enough in order to finally reach ZVS. As can be seen in the highlighted area in Fig. 14a, ZVS is not fully reached when turning on the other MOSFET. Its corresponding dead time was slightly reduced so that the effect of non-ZVS could be seen. In Fig. 14b, the ZVS at no-load is shown. Considering that the energy stored in the leakage inductance not only depends on the load current, but also on the magnetizing current, it is possible to achieve ZVS even at no load. Besides, the reduction in the leakage inductance current in the second stage of the dead time is considerably lower because the reflected current in the primary winding of the transformer is lower (i.e. the load current is zero and the reverse recovery current is quite low). Hence, with this design, it is possible to reach ZVS at any load.

In Fig. 15 the current through diode D_1 is shown. As can be seen, when the diode is turned off, its current is

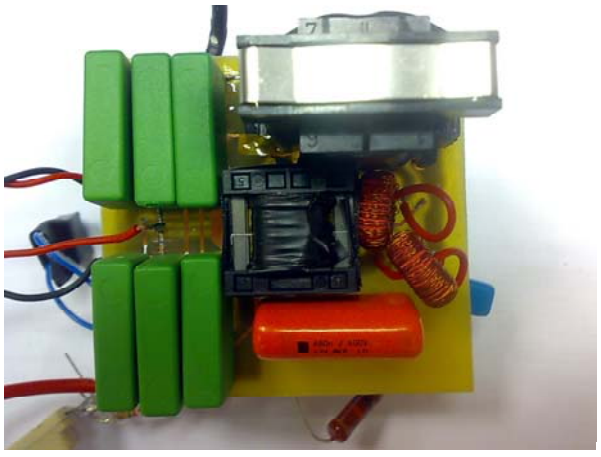
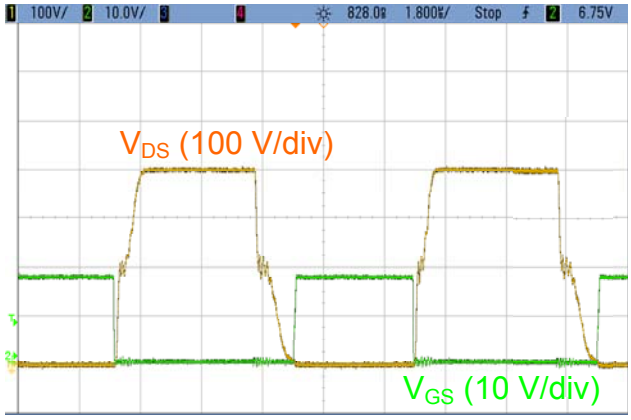
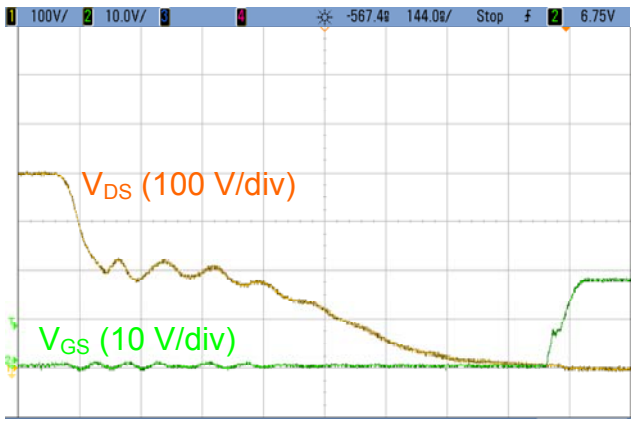


Fig. 12. Photograph of the prototype.



a)



b)

Fig. 13. a) V_{GS} and V_{DS} of M_2; b) detail of both voltages during the dead time.

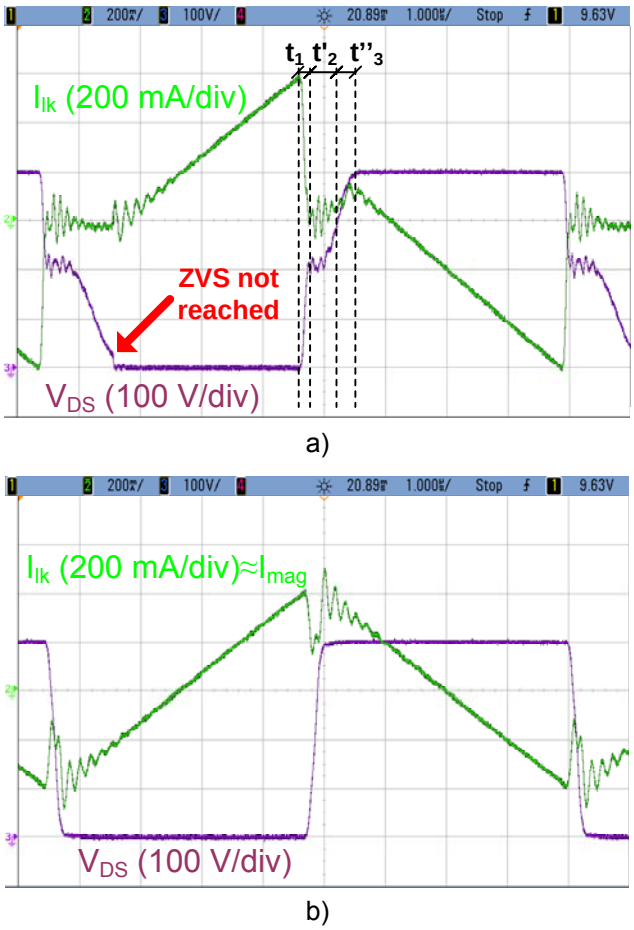


Fig. 14. Magnetizing current and V_{DS} (a) at full load, (b) at no-load condition.

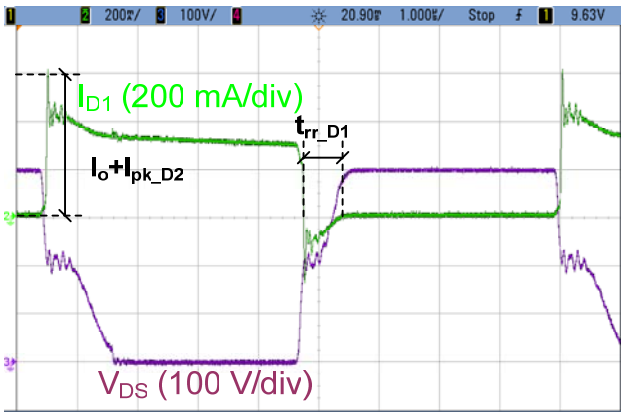


Fig. 15. D_1 current and V_{DS} of M_2.

equal to the reverse recovery current with a considerably long t_{rr}. Besides, when it is turned on, its current is equal to the output current plus the reverse recovery current of the other diode (D_2). This leads to the aforementioned considerable reduction in the leakage inductance current during t_2' and t_3'' (see Fig. 14).

A comparison between the model of the transitory and the experimental results is shown in Fig. 16 for different duty cycles at nominal input voltage. The only different between the model and the experimental results is that the former does not include the resonance at the beginning of the second stage of the transitory caused by the forced variation of the leakage inductance current due to the reversed bias of the diode that was turned on.

In Fig. 17, the input voltage, output voltage and output current of the AHB are shown when the input voltage (output voltage of the first stage) is affected by a 100-Hz ripple. It should be taken into account that due to the fact that the load is a LED string, the relative ripple of the output current is always considerably higher than the relative ripple of the output voltage. In this case, the control of the AHB is not optimized and it has been designed in order to have a 10% peak-to-peak current ripple, which means a 1.6% peak-to-peak ripple in the output voltage. Without the control (i.e. in open loop), the relative peak-to-peak ripple in the input voltage would be totally transferred to the output voltage and the current peak-to-peak ripple would be as high as 50%.

Finally, in Fig. 18a, the efficiency at different loads for different design considerations is shown. The "traditional design" implies that the secondary windings of the transformer are symmetrical and that Silicon diodes are used. As has been said, this implies that ZVS is not easy to obtain in both MOSFETs due to the non-zero average value of the magnetizing current of the transformer. In this design, the dead times has been independently optimized in order to be as close as possible to ZVS, although it was not possible to reach it in certain conditions. The "standard design" implies that the average magnetizing current is minimized as explained in this paper, but the transient during the dead time is not analyzed in order to determine the optimum value of the magnetizing inductance. On the other hand, the "proposed design" involves that both considerations are made (average magnetizing current reduction and calculation of the optimum magnetizing inductance). In this way, the "proposed" and the "standard" designs can be directly compared as the only hardware difference between them is the gap of the transformer (i.e., the turns ratios are the same in both cases). Besides, two "standard designs" are proposed: one with Si ultra-fast diodes (the same used in the "proposed design") and the other with SiC Schottky diodes. As can be seen, the "standard design" with Si diodes has the worst efficiency. Using SiC Schottky diodes improves the efficiency in 2% as the switching losses in secondary switches are the most critical point in this topology. Nevertheless, the "proposed design" using the same Si diodes as those used in the "standard design" presents the best efficiency results. This means that the AHB can be implemented using low-cost components (i.e., Si technology) but maintaining high efficiency if the design rules proposed in this paper are considered. If the "standard" and the "proposed" designs are compared with the "traditional" one, it should be taken into account that the main difference is the transformer secondary windings (the size of the core is the same in all the designs for proper comparison). As can be seen, the efficiency obtained with the "traditional design" is lower. Conduction losses in the transformer were higher and switching losses

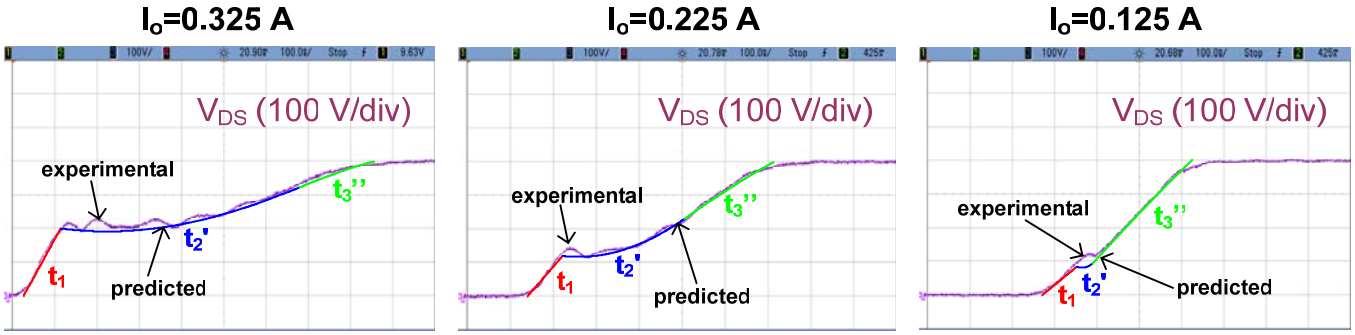


Fig. 16. Comparison between experimental results and the proposed model. Red line - the first stage of the transitory, blue line - second stage of the transitory and green line - third stage of the transitory.

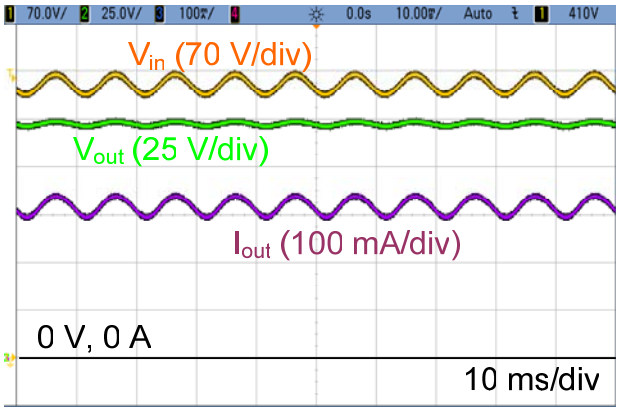


Fig. 17. Input voltage, output voltage and output current

in the MOSFETs were also increased as it was harder to reach ZVS.

In Fig. 18b, the efficiency achieved with the design proposed in this paper and for different input voltages is shown. As can be seen, at nominal load the efficiency is as high as 94.5%. Considering that the first stage may reach an efficiency as high as 97%, the overall efficiency of the whole topology is around 91.5%. This high efficiency leads to a reduced temperature in components, which allows the prototype to be built without any kind of heatsink. Besides, the efficiency at 425 V is lower than the efficiency at 375 V or 400 V. At this input voltage, ZVS is partially lost (L_{m_mag} and t_T were calculated for a 400-V input voltage) and, consequently, this increases the switching losses in the diodes and the MOSFETs.

VII. Conclusions

The use of HB-LEDs has boosted the development of new topologies for favouring the inherent advantages of LED-based lighting. Hence, high-efficiency high-reliability converters have been proposed in the recent years and dimming techniques have been also developed.

In this paper, a two-stage solution for LED-based street lighting applications is proposed. As the first stage is the well-known Boost converter, this paper is focused on the second stage, the Asymmetrical Half Bridge. Modifying the traditional design usually proposed for this converter, it is possible to optimize it for such a particular load as the

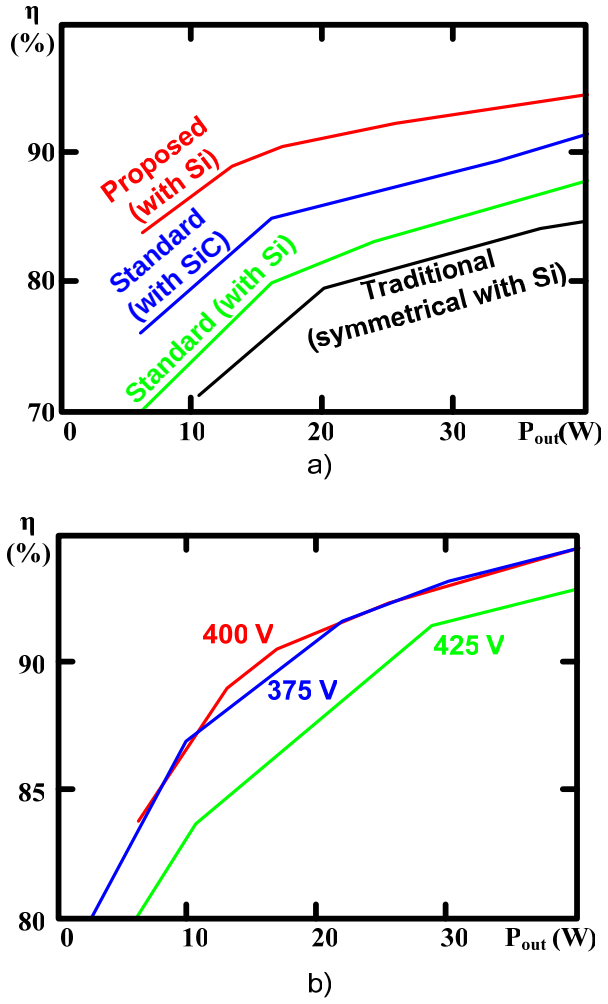


Fig. 18. Efficiency of the prototype a) for different design methods; b) for different input voltages (using the design proposed in this paper).

LED string. As a result, its efficiency and reliability are boosted. This new design has two advantages. First, the average value of the magnetizing current is reduced by the asymmetrical design of its transformer, what implies a reduction in conduction losses. Second, a model for describing transitions is developed. It can be used in the design process for reducing switching losses in MOSFETs and diodes.

An efficiency of 94.5% has been obtained for a 40-W prototype. Experimental results also indicate that the proposed model is accurate and helpful for designing AHB optimized for LED-based applications.

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