ELIMINATION OF THE TRANSFER TIME EFFECTS IN LINE-INTERACTIVE AND PASSIVE STANDBY UPSs BY MEANS OF A SMALL-SIZE INVERTER

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Abstract--**The main drawback of line-interactive and passive standby uninterruptible power supplies (UPS) is the transfer time when changing from normal-mode of operation to battery-mode of operation. During this time, the critical loads protected by the UPS are under the influence of the grid disturbance which forced the mode change. On the other hand, equipment protected by a double conversion UPS is never affected by any disturbance in the mains. Nevertheless, the efficiency of this topology is lower and its size and cost are considerably higher. Hence, the elimination of the transfer process between modes in line-interactive and passive standby UPSs would make them more competitive than double conversion ones in many situations. In this paper, a method for eliminating the transfer time is proposed. It is based on a half-bridge inverter with a hysteretic controller whose output voltage is only applied to the load during the transfer time. Considering the random nature of the grid failures and the short duration of the transfer time, the design and selection of the components is nothing but standard. This also leads to a non-standard hysteretic controller that needs to be fully analyzed. Experimental results are provided for a 750-W line-interactive UPS whose transfer time of 4 ms was eliminated by the proposed system.**

Index Terms—**Line-Interactive UPSs, Hysteretic controller, Transfer time in UPSs.**

I. INTRODUCTION

IEC 62040-3 [1] regulation analyses the performance of any uninterruptible power supply (UPS), detailing all the information that should be gathered and all the tests that should be done in order to obtain a complete classification sheet [2]. These sheets can be used for comparing several UPSs and determining which is the most suitable for a certain application [3-6]. In the third section of this classification sheet, the dynamic of the output voltage under several conditions is analyzed and compared with one of the three possible behaviors considered in the regulations (see Fig. 1 for behaviors type 1 and 2). These behaviors establish the output voltage tolerance as a function of time (measured from the starting point of the transient). During the change of operation mode, the double conversion UPS (Fig. 2a) [7-9] can always be allocated in type-1 behavior (Fig. 1a), whereas line-interactive (Fig. 2b) and passive standby UPSs (Fig. 2c) [10-13], due to their 'off-line' topology, can only reach type 2 (Fig. 1b) or 3 (which is more permissive than type 2), but never type 1. As a consequence, even when their efficiency is higher and their cost and size are considerably lower, 'off-line' topologies are usually pushed into background because grid failures reach the critical loads during the short duration of the transfer time.

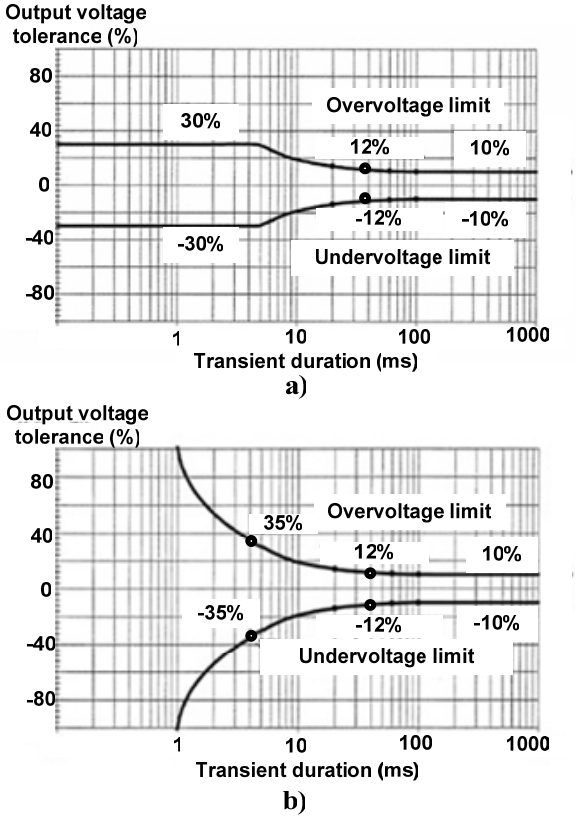

Fig. 1. a) Behavior type 1 and b) behavior type 2 of IEC 62040-3 for output voltage dynamic.

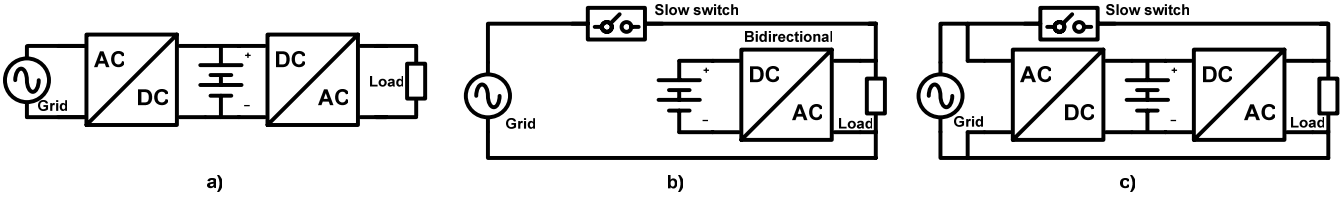

Fig. 2. Schematic of: a) double conversion ('on-line') UPS; b) line-interactive ('off-line') UPS; c) passive standby ('off-line') UPS.

In this paper, a solution that allows 'off-line' UPSs to be classified as type 1 according to IEC62040-3 regulation is presented. In this way, their field of application would be widened and their competitiveness would be increased. This solution is based on adding a small-size dc-ac converter connected in parallel with the UPS output and whose purpose is supplying power to the critical loads only during the transfer time (see Fig. 3a). It should be taken into account that the size of this additional converter must be considerably small and its cost must be considerably low, so that an 'off-line' UPS equipped with this new additional converter maintains the inherent competitive advantages of this kind of UPSs (i.e., small size and low cost) but eliminating one of its main inherent drawback (i.e., the transfer time). Moreover, it should be noted that the high efficiency of 'off-line' topologies should not be appreciably affected either by this new additional converter.

Hence, the proposed system and its principle of operation need to be as simple as possible (as explained in section II and section III of this paper). Also, the short duration of the transfer time in standard 'off-line' UPSs (a few milliseconds) and its sporadic nature make the design and selection of the components of the new solution nothing but standard, so they will be deeply explained in section IV. The experimental results for a 750-W system are shown in section V and conclusions are presented in section VI.

II. Principle of Operation

In this section, a simplified explanation of the principle of operation of the proposed system is given. A more detailed explanation, including all the equations that define its output voltage, can be found in section III.

The basic schematic of the proposed system is presented in Fig. 3a. As can be seen in Fig. 3b, it is based on a half-bridge inverter with a hysteretic controller. During normal-mode or battery-mode of operation of the UPS, the proposed converter switches S_{pos} and S_{neg} are off whereas the isolating switch (S_{iso}) is on, so that the critical load can be fed by the mains or the UPS. On the other hand, during the transfer time S_{iso} is turned off and the half-bridge switches (S_{pos} and S_{neg}) are switching in such a way that the inverter supplies a sinusoidal voltage to the critical loads. The control of these switches is carried out by the hysteretic controller. The energy supplied to the critical loads during this time is extracted from the input capacitor C_{pos} during the positive half-period and from C_{neg}

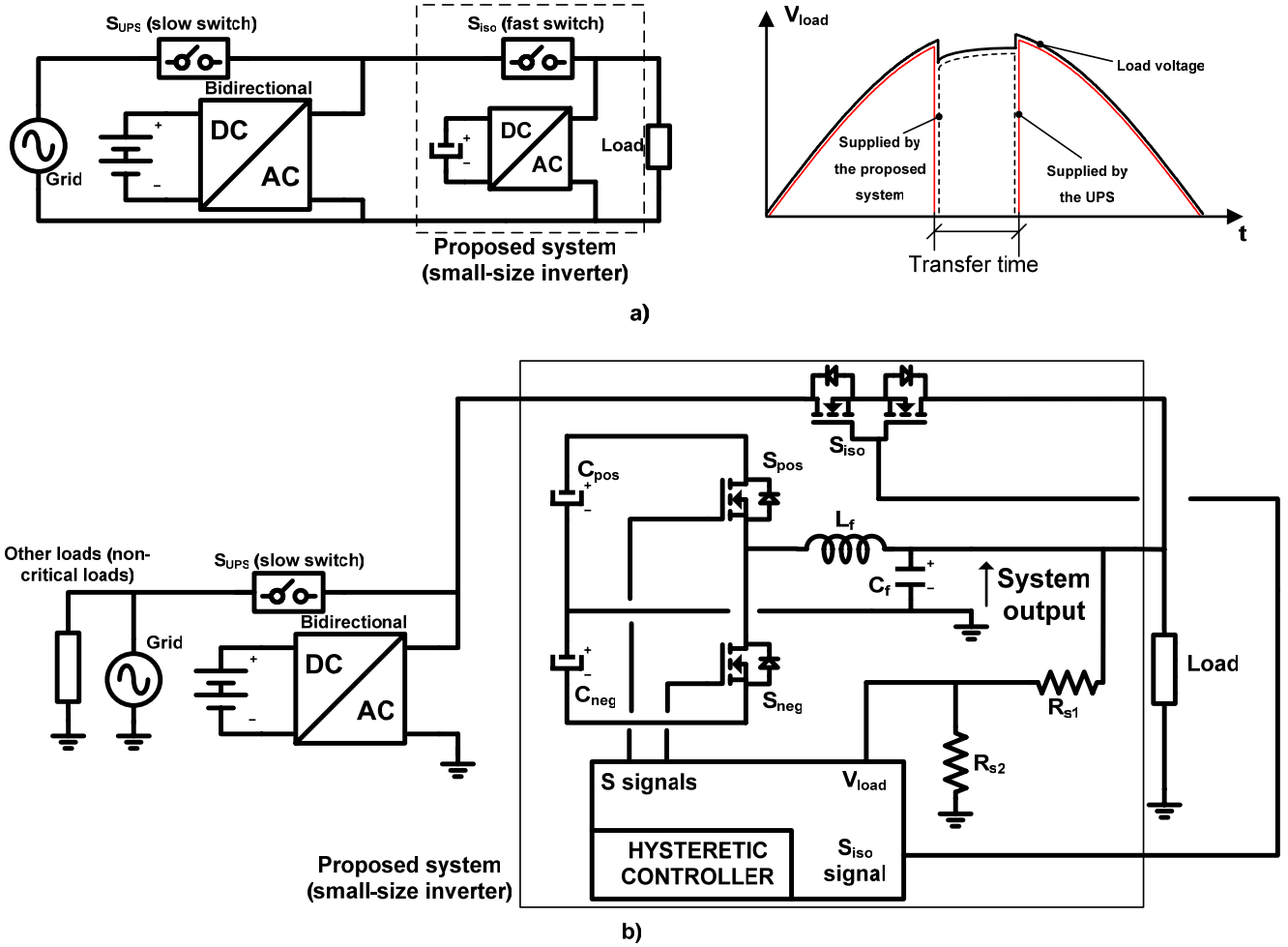

Fig. 3. a) Simplified schematic of the proposed system (including the UPS schematic); b) Complete schematic.

during the negative one. These capacitors are charged in a very simple way by means of the parasitic diodes of S_{pos} and S_{neg} during normal-mode and/or battery-mode operation. Hence, no additional stage in needed for the charging process and, consequently, the capacitors have to be rated for a voltage equal to the peak value of the grid voltage (taking into account the tolerance).

The first point that should be highlighted is that the load voltage needs to be sensed in order to control the small-size half-bridge inverter of the proposed system during the transfer time. Moreover, sensing the load voltage also allows us to detect the beginning of this transfer time (i.e., the beginning of a grid failure). The reason why it is possible to detect a grid failure by sensing the load voltage is that, during normal-mode operation and during transfer time, critical loads are directly connected to the grid in a passive standby or line-interactive UPS (i.e., S_{UPS} shown in Fig. 3 is on). Besides, this detection should be achieved by means of a fast and simple method in order not to increase the cost of the proposed system. With that purpose, the sensed load voltage is constantly compared with two sinusoidal voltage references synchronized with it (V_{upper} and V_{lower} in Fig. 4) and set to 110% and 90% of the nominal value of the sensed load voltage. Taking into account these values, if the UPS output voltage is inside the limits established by type-1 behavior for the steady state (±10%, see Fig. 1a), then it will be also between the sinusoidal voltage references (V_{upper} and V_{lower}) shown in Fig. 4. If a grid failure takes place, the sensed load voltage will exceed one of the sinusoidal voltage limits (i.e., V_{lower} in the case of a voltage sag or V_{upper} in the case of a voltage surge). In this way, the beginning of the transfer time (grid failure) is quickly detected and, as a consequence, S_{iso} can be quickly turned off (see Fig. 4). This allows the inverter to supply power to the critical loads without supplying it to the grid failure (see Fig. 3b). This detection process can be easily carried out by a couple of standard analog comparators.

As has been mentioned, once the switch S_{iso} is off, the half-bridge inverter starts its activity controlled by the hysteretic controller. The voltage reference used by this controller is the sinusoidal upper limit (V_{upper}). Also, it should be taken into account that the grid failure detection and the inverter control can be achieved by means of the same circuit. In this way, the proposed system is simplified

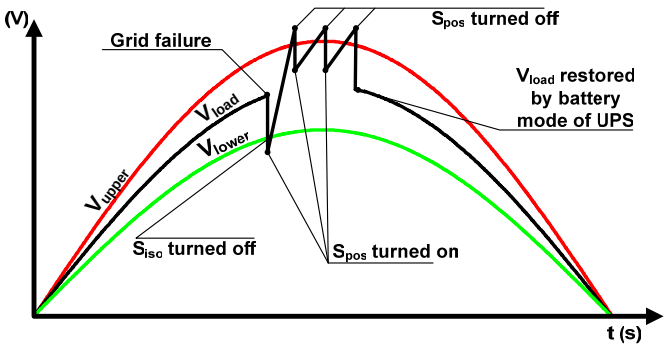

Fig. 4. Detection of the voltage disturbance and modulation of system output voltage.

and its size and cost can be reduced.

Finally, when the transfer time has expired, the output voltage of the UPS is restored by its own dc-ac converter. Hence, it is possible to stop the activity of the proposed system (half bridge inverter) and to switch on S_{iso} again.

As can be seen, the control and principle of operation have been considerably simplified in order to reduce the cost and size of the system. Nevertheless, this simplification and the small size of the output capacitor of the half bridge (explained in the next section) lead to a considerable ripple in the output voltage. This ripple needs to be analyzed in order to assure that the voltage supplied by the proposed system complies with the limits of type-1 behavior.

III. Output Capacitor and Ripple Calculation

Electrolytic capacitors cannot be used for implementing the output filter of the half-bridge inverter (the output voltage is ac). This fact, added to the strong restrictions in cost and size, leads to a limited capacitance at the inverter output. This restriction has two important consequences. One of them is related to the output-voltage ripple caused by the hysteretic control and it will be explained later.

The other consequence is that when a grid failure takes place, and until S_{iso} is turned off by the system (hundred of nanoseconds later), all the energy demanded by the grid failure, the critical loads and the non-critical ones is extracted from the filter capacitor (C_f in Fig. 3b). This period of time is caused by the turning off of S_{iso} and is considerably shorter than the transfer time, which is mainly caused by the slow switch S_{UPS} (or the start-up time of the UPS inverter). As a consequence, capacitor C_f must be designed for maintaining the load voltage inside the limits of type-1 behavior only until S_{iso} is completely turned off. It should be taken into account that it is not possible to use a capacitor for maintaining the load voltage inside type-1 limits during the whole transfer time, as this would mean an excessively-high capacitance for a non-electrolytic capacitor. Also, the resulting voltage would not be sinusoidal, exceeding the limits of type-1 behavior.

Analyzing the amount of energy extracted from the filter capacitor C_f until S_{iso} is turned off, it is possible to obtain the necessary value of C_f. The minimum amount of energy stored in the output capacitor C_f at the beginning of a transfer time, $e_{Cf\_ini}(t_{ini})$, is (see Fig. 5):

$$e_{Cf\_ini}(t_{ini}) = \frac{1}{2}\cdot C_f \cdot \left[Tol_{begin\_iso} \cdot \sqrt{2} \cdot V_{nom\_rms} \cdot \sin(\omega \cdot t_{ini}) \right]^2, \quad (1)$$

where V_{nom_rms} is the nominal rms value of the grid voltage, t_{ini} is the instant in which the transfer time begins and Tol_{begin_iso} is the voltage tolerance allowed at the beginning of the transfer time (the level of the load voltage when the failure is detected by the proposed system).

The minimum amount of energy, $e_{Cf\_end}(t_{ini}+t_{iso})$, that the output capacitor C_f may have at the end of the

transfer time in order to assure that the allowed tolerance is not exceeded is (see Fig. 5):

$$e_{Cf\_end}(t_{ini}+t_{iso}) = \frac{1}{2}\cdot C_f \cdot \left[Tol_{end\_iso}\cdot\sqrt{2}\cdot V_{nom\_rms}\cdot\sin(\omega\cdot(t_{ini}+t_{iso}))\right]^2, \quad 2)$$

where Tol_{end_iso} is the voltage tolerance allowed when S_{iso} is switched off by the control circuit and t_{iso} is the time needed for turning off this switch. Due to the short duration of t_{iso} (some hundreds of nanoseconds), the value of $\sin(\omega\cdot(t_{ini}+t_{iso}))$ can be considered equal to the value of $\sin(\omega\cdot(t_{ini}))$.

The amount of energy demanded by the load and by the grid failure during t_{iso}, $e_{demand}(t_{ini})$, can be expressed as:

$$e_{demand}(t_{ini}) = \frac{\left[Tol_{begin\_iso}\cdot\sqrt{2}\cdot V_{nom\_rms}\cdot\sin(\omega\cdot t_{ini})\right]^2}{R_{load}}\cdot t_{iso} + \frac{\left[Tol_{begin\_iso}\cdot\sqrt{2}\cdot V_{nom\_rms}\cdot\sin(\omega\cdot t_{ini})\right]^2}{R_{iso}+R_{nc}}\cdot t_{iso} \quad (3)$$

where R_{iso} is the resistance of S_{iso}, R_{nc} is the resistance of the non-critical loads and R_{load} is the resistance of the critical load. It should be taken into account that a resistive load is considered because any piece of electronic equipment connected to the output of a UPS is actually designed to be connected to the grid. Hence, those pieces of electronic equipment have to comply with standard regulations regarding Power Factor (IEC 61000-3-2 or ENERGYSTAR). As a consequence, they can be considered as close-to-resistive-behavior systems. Besides, IEC 62040-3 regulation does not include tests with inductive loads. Hence, the proposed system is not designed for working with such loads and the output voltage during transfer times would probably exceed the upper limit (depending on the beginning of the transfer time and its duration). Nevertheless, this is the only consequence as none of its components would be damaged if the system is connected to an inductive load.

The difference between equations (1) and (2) allows us to obtain the amount of energy that can be extracted from the output capacitor C_f during t_{iso} without exceeding the allowed limits. This amount of energy has to be equal to the one demanded by the load and the grid failure during t_{iso} (i.e., equation (3)). As a consequence, it is possible to obtain the following equation:

$$C_f = \frac{2\cdot(1-Tol_{begin\_iso})^2\cdot t_{iso}}{[(1-Tol_{begin\_iso})^2-(1-Tol_{end\_iso})^2]}\cdot\left(\frac{1}{R_{iso}+R_{nc}}+\frac{1}{R_{load}}\right), \quad (4)$$

Considering that t_{iso} is shorter than some hundreds of nanoseconds, Tol_{end_iso} can be fixed in 0.3 (see Fig. 5). Also, the value of Tol_{begin_iso} is 0.1 as the beginning of the transfer time is detected when the load voltage exceeds one of the limits of the detection circuit (V_{upper} and V_{lower} Fig. 4 and Fig. 5). Finally, the worst case situation for the calculation of C_f implies that a short-circuit failure is taking place in the grid, which means that R_{nc} can be considered equal to zero as the non-critical loads are in parallel with the grid failure. In this way, equation (4) can be rewritten as:

$$C_f = \frac{2\cdot 0.9^2\cdot t_{iso}}{(0.9^2-0.7^2)}\cdot\left(\frac{1}{R_{iso}}+\frac{1}{R_{load}}\right). \quad (5)$$

As can be seen, this equation is not affected by L_f or any other parameter of the proposed inverter (C_{pos}, C_{neg}, etc.). The reason is that during t_{iso}, none of the MOSFETs of the half bridge (S_{pos} and S_{neg}) has been turned on for the first time and, consequently, none of those parameters affects the initial discharge of C_f. Equation (5) also shows that the higher R_{iso}, the lower C_f. However, this switch is in series with the load during normal-mode and battery-mode operation. Due to this, its value must be selected as low as possible in order not to degrade UPS efficiency. Defining K_R as the quotient between the R_{iso} and (R_{load} + R_{iso}), it is possible to represent (see Fig. 6) the needed capacitance depending on t_{iso} for suitable values of K_R. This parameter represents the efficiency lost (referred to the initial efficiency of the UPS) due to the addition of the isolating switch (S_{iso}) in series with the load. As can be seen, with a small reduction in efficiency it is possible to keep the capacitance C_f under suitable values for non-electrolytic capacitors. Hence, it is possible to calculate C_f with the nominal power of the UPS and the characteristics of the MOSFET used in the isolating switch S_{iso}. The nominal power defines R_{load}, the R_{DSON} of the MOSFETs defines R_{iso} and their turn-off delay time plus their turn-off

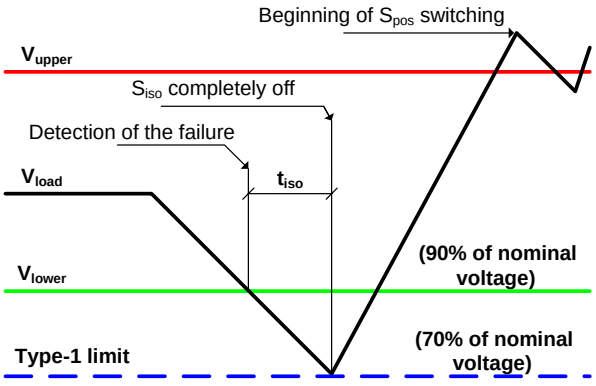

Fig. 5. Beginning of the transfer time when the UPS is equipped with the proposed system.

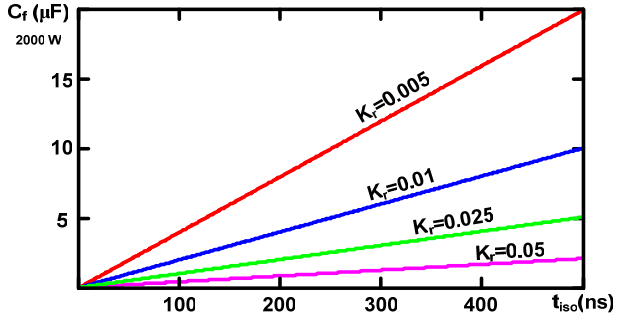

Fig. 6. Needed output capacitor for a 2000-W UPS (R_{load} = 26.5 Ω).

fall time defines t_{iso}. The rest are constants in equation (5).

The other consequence of a small-size output capacitor is that the hysteretic controller implies a considerable ripple in the output voltage. This kind of control is typically used in dc-dc converters, in which electrolytic capacitor can be implemented at the output. As a consequence, in the analysis of the voltage ripple only the equivalent series inductor (ESL) and the equivalent series resistor (ESR) of the output capacitor are taken into account, disregarding the effect of its capacitance [14-21]. In the proposed system, the capacitor cannot be electrolytic and, hence, the effect of its small capacitance needs to be analyzed. In fact, the effects of its ESR and its ESL can be neglected.

For simplicity, the analysis of the voltage ripple will be presented for the positive half-period (i.e., the grid failure takes place in the positive half-period and the transfer time is completely included in it). Nevertheless, it is perfectly suitable for the negative one as well. With this simplification, the circuit presented in Fig. 3b can be represented as shown in Fig. 7. Besides, before beginning with the analysis, some points need to be highlighted:

- The circuit of Fig. 7 is similar to the one of a Buck converter. The only difference is C_{neg}, which affects the demagnetization of the filter inductor.
- The inverter control is done by means of unipolar modulation. Hence, during the failures in the positive half-period S_{neg} remains off all the time. This implies that it is possible to achieve Discontinuous Conduction Mode (DCM) in the operation of this converter.
- The voltage across the output inductor when the MOSFET S_{pos} is turned on is smaller than the voltage across the inductor when S_{pos} is off and the parasitic diode of S_{neg} in on (it would be equal during the zero-crossing of the load voltage). Hence, the magnetization of the output inductor takes more time than its demagnetization and, as a consequence, the part of the ripple when S_{pos} is on is always larger than the part of the ripple during the time in which S_{pos} is off.
- The circuit of Fig. 7 shows an under-damped response due to the values of output inductor and capacitor necessary for the proposed system and different from a conventional design (see appendix A).

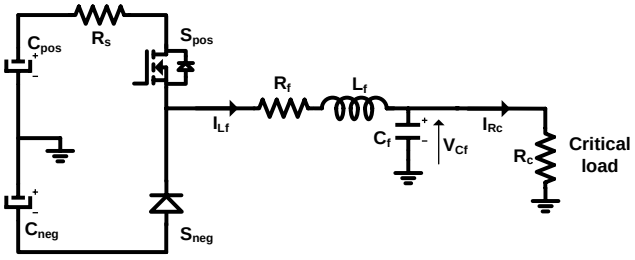

Fig. 7. Equivalent circuit of the small-size inverter schematic shown in Fig. 3b for the positive period.

Considering the last two points, the output voltage during a whole positive half-period is shown in Fig. 8. In this figure, two different behaviors can be seen depending on the voltage value across C_{pos}:

- When the voltage across C_{pos} is higher than the output voltage that must be achieved (V_{upper} in Fig. 4 and Fig. 8), then S_{pos} will be turned off and on by the hysteretic controller (see points P_A in Fig. 8).
- When the voltage across C_{pos} is lower than the desired output voltage (V_{upper}), then S_{pos} will remain continuously on (see point P_B in Fig. 8) until the voltage reference (V_{upper}) can be reached again (see point P_c in Fig. 8).

For the first case, the equation that defines the output voltage when S_{pos} is turned on is (see Appendix A):

$$V_{Cf}(t) = e^{-m\cdot t'}\cdot\left[\left(\frac{k_1(t)}{C_f} - \frac{k_2(t)}{C_f}\cdot F\cdot\frac{m}{\omega}\right)\cdot\sin(\omega\cdot t') + \left(\frac{k_1(t)}{C_f}\cdot\frac{m}{\omega} - \frac{k_2(t)}{C_f}\right)\cdot F\cdot\cos(\omega\cdot t')\right] + V'_{Cpos}(t), \quad (6)$$

$$\omega = \frac{\sqrt{\frac{4}{L_f\cdot C_f} - \left(\frac{1}{R_{load}\cdot C_f} + \frac{R_p}{L_f}\right)^2}}{2}, \quad (7)$$

$$m = \frac{1}{2\cdot R_{load}\cdot C_f} + \frac{R_p}{2\cdot L_f}, \quad (8)$$

$$F = \frac{\omega}{m^2 + \omega^2}, \quad (9)$$

where L_f is the inductance of the output filter inductor, R_p is the R_{DSON} of S_{pos} plus the filter inductor resistance, t' represents the time evolution referred to the beginning of each switching cycle and t is the time since the last zero-crossing of the load voltage (see Fig. 8 for more details about time references).

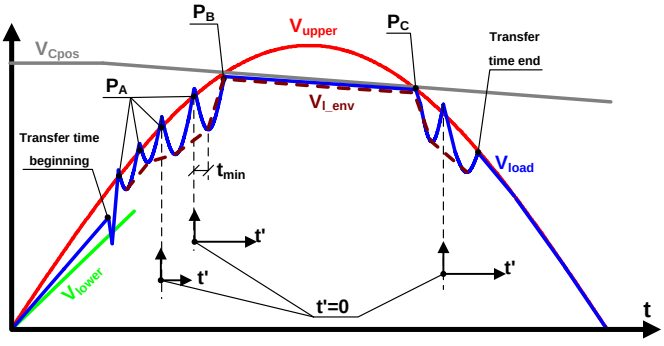

Fig. 8. Complete evolution of the output voltage provided by the proposed system.

Equation (6) determines the behavior of the output voltage since S_{pos} is on until it is turned off again by the control circuit. This means that, for each switching cycle, it will be necessary to define the value of the constants $k_1(t)$, $k_2(t)$ and $V'_{Cpos}(t)$. The first two constants can be calculated analyzing the current and the voltage of the output capacitor at the beginning of the magnetizing process of the filter inductor (i.e., at the beginning of each switching cycle). This leads to these two equations:

$$k_1(t) = \frac{-V_{upper}(t)\cdot\frac{R_{s1}+R_{s2}}{R_{s2}}\cdot e^{\frac{-t_{on}}{R_{load}\cdot C_f}}}{R_{load}}, \qquad (10)$$

$$k_2(t) = \frac{-C_f}{F}\cdot\left(-K_1(t)\cdot R_{load} - V'_{Cpos}(t)\right) - \frac{m}{\omega}\cdot K_1(t), \qquad (11)$$

where R_{s1} and R_{s2} are used for sensing the load voltage (see Fig. 3b) and t_{on} is the turning on delay time of S_{pos}.

Moreover, $V'_{Cpos}(t)$ is the steady state value of the voltage across the output capacitor C_f shown in Fig. 7 when S_{pos} is on:

$$V'_{Cpos}(t) = \frac{R_{load}}{R_{load}+R_p}\cdot V_{Cpos}(t), \qquad (12)$$

where $V_{Cpos}(t)$ is the voltage of the bulk capacitor C_{pos}, which depends, not only on the instant analyzed (t), but also on the moment in which the transfer process began.

To properly determine the lower envelope (V_{l_env} in Fig. 8) of the load voltage, the value of t'_{min} in Fig. 8 must be determined. t'_{min} is the time in which V_{load} reaches its minimum value in each switching cycle (so t'_{min} will be a function of t). This value can be easily determined by differentiating equation (6) and making it equal to zero. The resulting equation, without analytical solution, is:

$$e^{-m\cdot t'_{min}(t)}\cdot\left[k_1(t)\cdot\cos\left(\omega t'_{min}(t)\right) + k_2(t)\cdot\sin\left(\omega t'_{min}(t)\right)\right] = 0 \qquad (13)$$

Replacing t' in (6) with the value of t'_{min} calculated in (13) it is possible to obtain the expression of V_{l_env} (see Fig. 8), the lower envelope of the load voltage, during the transfer time and for any value of t. In section V, the validation of these equations will be done by comparing their results with the experimental ones. This lower envelope allows us to determine if a certain design of the proposed system will satisfy the type-1 behavior of IEC62040-3 regulations (which is its final objective). As has been mentioned, the part of the ripple above the voltage reference (V_{upper}) is smaller than the part of the ripple which is below the reference. Hence, as the limits fixed by the type-1 behavior are symmetrical (see Fig. 1), if the lower envelope (V_{l_env}) does not exceed the minimum limit, it is sure that the maximum limit will not be exceeded by the output voltage of the proposed system either. The lower envelope will therefore help in selecting and designing the components (especially the filter inductor) in order to obtain a suitable transfer-time suppressor system for a certain UPS (this will be explained in the next section).

As has been said, the energy supplied to the load during the transfer time is extracted from bulk capacitors (C_{pos} and C_{neg}). Although this is possible due to the short duration of the transfer time, it means a noticeable decrement in the capacitor voltage (input voltage of the proposed system). When V_{Cpos} is lower than the reference (V_{upper}), then the switch S_{pos} will remain turned on. Therefore, after a transitory defined by equation (6), the output voltage will be equal to $V'_{Cpos}(t)$, whose value depends on the input capacitor voltage. Hence, the last two equations necessary for defining the output voltage are the equations that define the input capacitor voltage depending on whether it is higher or lower than the voltage reference (V_{upper}). These equations can be easily calculated by analyzing the energy demand pattern of the load when S_{pos} is switching (sinusoidal output current with a progressive decrement in amplitude due to the input capacitor discharge) and when it is constantly on (decreasing current due to the input capacitor discharge). The first pattern corresponds to the periods of time from 'transfer time beginning' to 'P_B' and from 'P_C' to 'transfer time end' in Fig. 8. The second pattern correspond to the period of time from 'P_B' to 'Pc' in Fig. 8. With these patterns, an energy balance between input and output leads to:

$$V_{Cpos}(t) = \sqrt{\left(V_{upper\_rms}\cdot\frac{R_{s1}+R_{s2}}{R_{s2}}\right)^2\cdot\left(\frac{2\cdot\omega\cdot\left(t-t_{ini}\right)+\left(\sin(2\cdot\omega\cdot t_{ini})-\sin(2\cdot\omega\cdot t)\right)}{\omega\cdot C_{pos}\cdot\left(R_{load}+R_p\right)}\right)+V_{Cpos}(t_{ini})^2}, \quad \text{when } V_{Cpos}(t) > V_{upper}(t) \qquad (14)$$

$$V_{Cpos}(t) = \left(V_{upper}(t_{lmt})\right)\cdot e^{-\frac{t-t_{lmt}}{\left(R_p+R_{load}\right)\cdot C_{pos}}}, \quad \text{when } V_{Cpos}(t) < V_{upper}(t) \qquad (15)$$

where V_{upper_rms} is the rms value of the upper limit (V_{upper}).

The boundary is defined by the instant t_{lmt}, which is also a variable necessary for solving equation (15) and its value is the instant in which V_{Cpos} [equation (14)] is equal to the reference $V_{upper}(t)$ (P_B in Fig. 8).

To sum up, by means of equations (6), (13) and (14) when V_{Cpos} is higher than the desired output voltage or by means of equations (6) and (15) when it is lower, it is possible to know the minimum output voltage (V_{l_env}) for a specific transfer time and for every possible beginning of it.

Finally, it is important to highlight again that the part of the voltage ripple generated when S_{pos} is off (i.e. the part of the voltage ripple which is above the voltage reference V_{upper}) is smaller than the part of the voltage ripple that corresponds to the on-state of S_{pos} (i.e., which is

below the voltage reference). Hence, if the type-1 behavior is not exceeded by the lower part of the ripple, it will not be exceeded by the upper part either (see type 1 behavior in Fig. 1a).

IV. Electrical Design

Once the equations that define the output voltage behavior are defined, it is possible to explain the rules about component design and selection.

Regarding the MOSFETs, S_{pos} and S_{neg} have to withstand two times the peak value of the output voltage. Besides, considering the random nature of grid failures and the short duration of the transfer time, it is not necessary to analyze I_D (continuous drain current) as the MOSFETs are not going to drive the nominal current during long periods of time. Instead, the current parameter that should be observed is I_{DM} (pulsed drain current). Another important aspect is determining their R_{DSON}, as it will have an important influence in the output voltage and in the IEC 62040-3 compliance [see R_p in equation (8)]. For this R_{DSON} determination, it should be considered that although the duration of the transfer time is quite short, the high value of the driven current compared with I_D implies a considerable increase of the junction temperature. Due to the short duration of the transfer time, the thermal steady state in the MOSFETs is not reached and, therefore, this means that the R_{DSON} of the MOSFETs S_{pos} and S_{neg} will be higher than the value that can be estimated from the case temperature. Nevertheless, the switching frequency and the duty cycle applied to the MOSFETs during the transfer time are not constant and, as a consequence, it is not possible to use the transient thermal response curves provided in the datasheets either. Hence, it is necessary to use complex thermal models, Foster or Cauer models (see Fig. 9a), for making a deep analysis of the junction temperature during the transfer time in the worst possible situation [22-28]. In Fig. 9a, the current sources represents the switching and conduction losses and the RC-pairs the

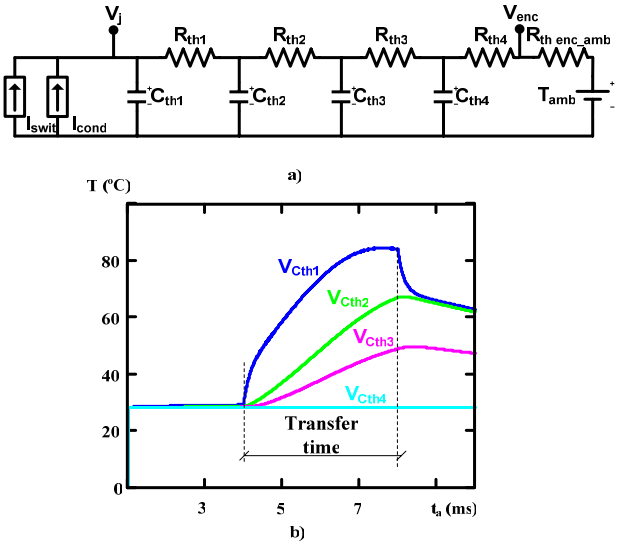

Fig. 9. a) Cauer transitory thermal model for a MOSFET; b) Thermal response of a MOSFET during a given transfer time.

thermal resistance and capacitance of different sections of the die. The construction of this thermal model (i.e., determination of the parameters R_{thi} and C_{thi}) is quite complex and is beyond the scope of this paper. In Fig. 9b, an example of the temperature obtained with a Cauer model for a MOSFET during a transfer time is shown. As can be seen, it is possible to obtain all the internal temperatures in the case and in the junction. This model shows that the temperature of the case surface is nearly not affected but the temperature of the junction is considerably higher at the end of the transfer time. The temperature obtained in this analysis can be then used to determine the MOSFET R_{DSON}, which affects R_p in equation (8), by means of the 'T_j- R_{DSON}' curve.

Another important result of this thermal analysis can also be seen in Fig. 9b. As has been already mentioned, during the transfer time the temperature of the case surface is not affected by the current flow through the MOSFET. This means that using heat sinks in S_{pos} and S_{neg} would not improve the thermal response of the switches and would not reduce their R_{DSON} during the transfer time. As heat sinks are not necessary for S_{pos} and S_{neg}, the cost and size are considerably reduced, which is something mandatory for the proposed system.

C_{pos} (and C_{neg}) needs to be designed with an iterative process in which the worst situation (longest transfer time and highest critical load power) is analyzed for different beginnings of the transfer time. The resulting highest capacitance value of this iterative process will be the one that should be selected for the capacitors. Typically, the worst case for type-1 compliance implies that the end of the transfer time is close to the instant in which the sinusoidal voltage reference reaches its peak value, as the maximum output voltage is demanded when the input voltage (voltage of the input capacitor) is minimum. The rated voltage of these capacitors, due to the charging process described at the beginning of section II, should be equal to the peak value of the grid voltage (including tolerance).

Finally, it should be taken into account that equation (5) defines the output capacitance needed and equations (6), (13), (14) and (15) allow the calculation of the minimum value of the filter inductor as the lower envelope of the output voltage (V_{l_env}) must comply with the limits of type 1 behavior. It could be possible to increase the value of the inductor and/or the capacitor with the objective of reducing the output voltage ripple. Nevertheless, this would mean increasing the cost and size of the converter, which need to be low for maintaining the competitive advantages of the 'off-line' UPS to which is connected.

The thermal design of the inductor is similar to the MOSFETs one. The current through the inductor will increase its internal temperature (due to the copper losses). Nevertheless, this is something transitory and, hence, steady-state equations cannot be used. A transitory thermal model of the inductor is not as easy to obtain as the thermal model of MOSFETs. Hence, a simplification

needs to be made. Due to the short duration of the transfer time, it is possible to suppose that no thermal energy is transferred to the ambient. This means that all the energy is used for increasing the copper temperature. Hence, the resulting equation is quite simple:

$$\Delta T_{inductor} = \frac{1}{Q_{cu}} \cdot \frac{E_{max}}{V_{cu} \cdot \rho_{cu}}, \quad (16)$$

in which Q_{cu} is the copper specific heat capacity, V_{cu} is the volume of copper used in the inductor, ρ_{cu} is its resistivity and E_{max} is the maximum energy lost in the inductor due to conduction losses in the inductor. This last parameter can be easily calculated considering the series resistor of the inductor, the maximum current through it and the maximum duration of the transfer time. The worst situation for this calculation takes place when the middle point of the transfer time coincides with the moment in which the load current reaches its peak value.

V. Experimental results

A prototype has been built and tested (Fig. 10). It is designed for a 750-W UPS with a 110-V output voltage. S_{pos} and S_{neg} are implemented with MOSFETs IRF840 whereas S_{iso} is implemented with two MOSFETs FB11N50 and a small heat-sink (S_{iso} has to be designed following the usual guidelines). The output filter is implemented with a 4.4-µF capacitor and a 55-µH air-core inductor (E30 size). C_{pos} and C_{neg} are 670-µF electrolytic capacitors. V_{upper} and V_{lower} (the two signals which are constantly compared to the sensed load voltage) are obtained by means of a small-size microcontroller and some additional circuitry. The PWM module of the microcontroller generates a signal which is filtered, obtaining a sinusoidal signal. Two different offset are added to this signal in order to obtain V_{upper} and V_{lower}. As their amplitude is determined by the nominal value of the voltage (American or European range) and not by its instant value, it is not necessary to constantly analyze the peak value of the grid voltage. Nevertheless, both signals need to be synchronized with the grid. Hence, the microcontroller detects the zero crossings of the grid voltage with a very simple circuit and adjusts the signal generated by the PWM module so that V_{upper} and V_{lower} are always synchronized with the grid.

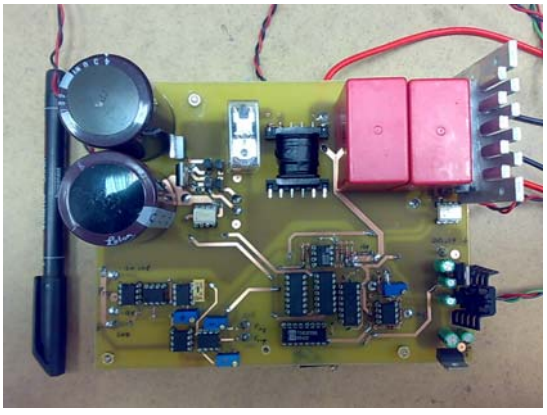

Fig. 10. Photograph of the prototype.

Due to the simplicity of the control circuitry, no hysteretic band is used (the turning on and off of the MOSFETs is determined by the same voltage level). Adding a hysteretic band (and keeping V_{upper} as reference) would lead to a lower envelope of the output voltage closer to the limit established by the normative (i.e., type-1 behavior limit). Nevertheless, if a hysteretic band ($\pm V_{band}$) is added and V_{upper} is kept as the reference, $V_{upper}(t)$ should be replaced with $V_{upper}(t)-V_{band}$ in (10), as it defines the starting voltage of the output capacitor each time the MOSFET is turned on. Besides, $V_{upper}(t)$ in (14) and (15) should be replaced with $V_{upper}(t)+V_{band}$ as it defines the moment when the switching process stops (i.e., the MOSFET remains turned on because the load voltage cannot reach the reference).

Considering that no hysteretic band is used, the maximum switching frequency of the output voltage is determined by the turn-on and turn-off time of the MOSFETs, the delay of the control circuitry (a standard LM393 comparator plus some logical gates have been used) and the resonance that affects the output voltage. In this prototype, the maximum switching frequency is around 400 kHz and takes place during the zero crossing of the output voltage. The minimum switching frequency is zero during the time between P_B and P_C in Fig. 8. Right before P_B, the switching frequency is as low as 10 kHz. As can be seen, due to the resonance of the output voltage, the maximum switching frequency is not too high even when no hysteretic band is used.

The capacitance of the output capacitor and the maximum R_{DSON} of S_{iso} MOSFETs have been calculated with equation (5). The inductor value is the highest that can be obtained with an E30 core taking into account R_p. If the number of turns is large, the maximum diameter of the wire will be small and the series resistance of the inductor will be high. Hence, the number of turns and the R_{DSON} of S_{pos} and S_{neg} MOSFETs should be selected taking into account that R_p has a maximum value given by IEC62040-3 compliance [see equation (6)].

Fig. 11a shows the results obtained when connecting the proposed system to the 110-V_{rms} UPS. As can be seen, although the output voltage of the UPS is zero during the first 4 milliseconds of the grid failure, the load voltage is restored by the proposed system until the inverter of the UPS provides a sinusoidal output voltage. The voltage provided by the proposed system is always higher than the lower limit established by the type-1 behavior of the regulations (70% of the nominal voltage). The output current (Fig. 11b), which is the most critical parameter for the proposed system, is 5.5 A_{rms}.

As can be seen in Fig. 11c and Fig. 11d, the ripple is considerable due to the low capacitance of the output capacitor, but it does not exceed the limits imposed by the type-1 behavior of the regulations, which establishes a 30% tolerance for the initial 8 milliseconds of the transfer time. The equations developed in section III are valid considering that the estimation of the lower envelope

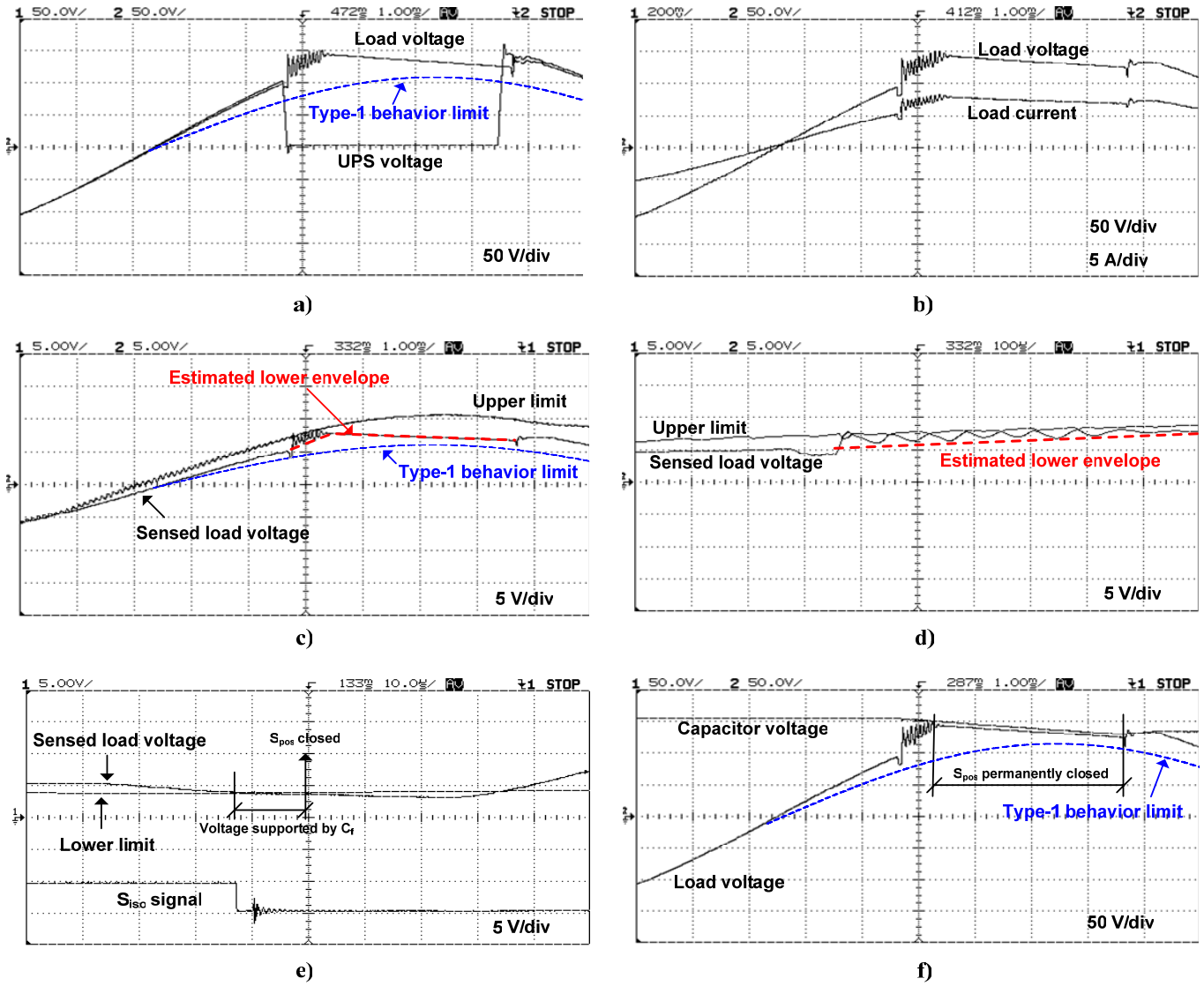

Fig. 11. a) Load and UPS output voltage during a transfer time due to a voltage sag; b) load voltage and load current during the transfer time; c) estimation of the ripple (red line) based on the previously explained equations; d) detail of the upper limit used as reference and the ripple of the output system; e) voltage supporting effect of the system output capacitor during the turning off of S_{iso} f) effect of input capacitor discharge in the system output voltage behavior.

(V_{l_env}) is very accurate (see dotted red line in Fig. 11c and Fig. 11d).

Fig. 11e shows how the load voltage is supported by the output capacitor of the proposed system until S_{iso} is turned off and S_{pos} is on; hence, equation (5) is validated. Finally, Fig. 11f not only shows the C_{pos} discharge effect mentioned at the end of section III, but also that its iterative calculation (mentioned in section IV) is valid.

Besides, as the ripple below the reference is greater then the ripple above (Fig. 11c), the upper limit is used as reference for the hysteretic controller, instead of the lower limit, in order to be farther from exceeding the limits of type-1 behavior (this is valid not only during the positive half-period, but during the negative as well).

VI. Conclusions

Transfer time is the main disadvantage of line-interactive and passive standby UPSs. During this time, the grid disturbance that forces the UPS mode change reaches, and may affect, the critical loads. As a consequence, these two UPS topologies are limited to low-power applications. In this paper, a system that eliminates the transfer time is presented. Due to the short duration and sporadic behavior of the transfer time, the standard design and selection criteria of components must be modify. In this way, it is possible to obtain a low-cost low-size system that can supply power to the critical loads during the transfer time. Hence, adding this system to line-interactive or passive standby UPS will not increase its size or cost and will not affect their efficiency either (the most important advantage of these topologies).

The design of this proposed system implies also a non-standard analysis of the hysteretic control: as a non-electrolytic capacitor is implemented at the output, the voltage ripple due to its capacitance cannot be neglected. Furthermore, the ripple due to the ESR and the ESL of the capacitor can be disregarded, which is something not standard in hysteretic control analysis. The model of the lower envelope of the output voltage resulting from this analysis can be used for determining if the restored output voltage during the transfer time is going to be inside the limits established by type-1 behavior of the IEC 62040-3 regulations. In other words, if the proposed system fulfills its objective or if it is necessary to modify its design in order to assure that the output voltage of the small-size inverter does not exceed the limits. This modification can be achieved in several ways: incrementing the input capacitors capacitance in order to decrease the voltage reduction during the transfer time, reducing the output impedance of the proposed system, incrementing the inductance value of the output inductor or incrementing the capacitance value of the output capacitor. All this modifications help to maintain the lower envelope of the output voltage higher than the lower limit established by the IEC62040-3 regulations.

VII. Appendix A

The second order linear ordinary differential equation that needs to be solved in order to obtain equation (6) is:

$$\frac{1}{L_f \cdot C_f}\cdot\left(1+\frac{R_p}{R_{load}}\right)\cdot i_{Cf}(t')+ \\ +\left(\frac{R_p}{L_f}+\frac{1}{R_{load}\cdot C_f}\right)\cdot\frac{di_{Cf}(t')}{dt'}+\frac{d^2 i_{Cf}(t')}{dt'^2}=0 \quad (17)$$

where $i_{Cf}(t')$ is the current of the output capacitor and the rest of variables have been previously defined.

The analysis of its discriminant (considering that $R_p \ll R_{load}$) allows us to know if the capacitor current has an over-damped or under-damped behavior. This discriminant, taking into account equation (5), is:

$$\left(\frac{R_p}{L_f}+\frac{1}{\frac{2\cdot 0.9^2\cdot t_{iso}}{(0.9^2-0.7^2)}\cdot\left(\frac{1}{K_R}\right)}\right)^2 - \\ -\frac{4}{\frac{L_f}{R_{load}}\cdot\frac{2\cdot 0.9^2\cdot t_{iso}}{(0.9^2-0.7^2)}\cdot\left(\frac{1}{K_R}\right)}=0 \quad (18)$$

As the influence of the proposed system on the UPS efficiency should be quite low, the value of K_R should not exceed 0.01, as it has been previously explained. Nevertheless, it should be taken into account that the lower the R_{DSON} of S_{iso}, the higher the value of the output capacitance [see equation (5)]. Hence, this should be considered when designing the system for a specific UPS.

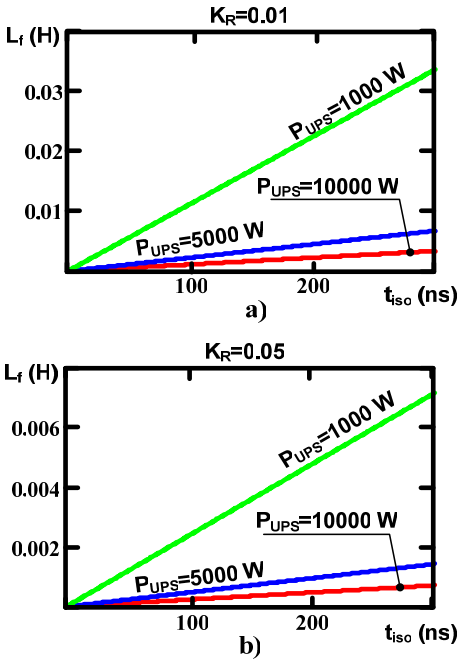

Fig. 12. Limit between over-damped and under-damped behavior as a function of t_{iso}, K_R and P_{UPS}.

Fig. 12 is the solution to this last equation for different nominal powers and for two possible values of K_R. All the L_f values above the curves imply over-damped behaviors of the capacitor current for a given nominal power, whereas values below the curves imply under-damped behaviors. As can be seen, the necessary inductance for over-damped behavior is quite high in the case in which K_R is equal to 0.01. When it is equal to 0.05, the needed inductance is considerably lower, but the efficiency loss is excessive. Hence, although over-damped behavior is preferred as it implies lower ripple in the output of the proposed system, it is impractical due to the necessary size of the inductor or the efficiency loss. As a consequence, the output of the proposed system is going to have an under-damped behavior and a precise analysis of the ripple has to be done in order to assure compliance with type-1 limits.

Acknowledgements

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