Steady-State Analysis and Modeling of Power Factor Correctors with Appreciable Voltage Ripple in the Output-Voltage Feedback Loop to Achieve Fast Transient Response

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Abstract- The classical design of an active Power Factor Corrector (PFC) leads to slow transient response in this type of converter. This is due to the fact that the compensator placed in the output-voltage feedback loop is usually designed to have narrow bandwidth to filter the voltage ripple of twice the line frequency coming from the PFC output. This feedback loop is designed with this filtering effect because a relatively high ripple would cause considerable distortion in the reference of the line current feedback loop and hence in the line current. However, the transient response of the PFC can be substantially improved if the bandwidth of this compensator is relatively wide, thus permitting certain distortion in the line current which leads to a trade-off between transient response (and hence voltage ripple at the output of the compensator) and harmonic content in the line current. As a consequence of the voltage ripple at the output of the compensator (which is considered the control signal), both the static and the dynamic behaviour of the PFC changes in comparison with the standard case; i.e., with no voltage ripple on the control signal. The static behaviour of a PFC with appreciable voltage ripple in the output-voltage feedback loop is studied in this paper using two parameters: the amplitude of the relative voltage ripple on the control signal and its phase lag angle. The total power processed by the PFC depends on these parameters, which do not vary with the load and which determine the Total Harmonic Distortion (THD) and the Power Factor (PF) at the input of the PFC. Furthermore, these parameters also determine the maximum power that can be processed by the converter while still complying with EN 61000-3-2 regulations for Class A and Class B equipment. When the converter must comply with the aforementioned regulations for Class C or Class D equipment, however, the compliance does not depend on the power processed by the PFC. In the case of Class C equipment, not all the possible combinations of the relative ripple of the control signal and of its phase lag angle manage to comply with these regulations. Finally, the study was verified by simulation and in a real prototype.

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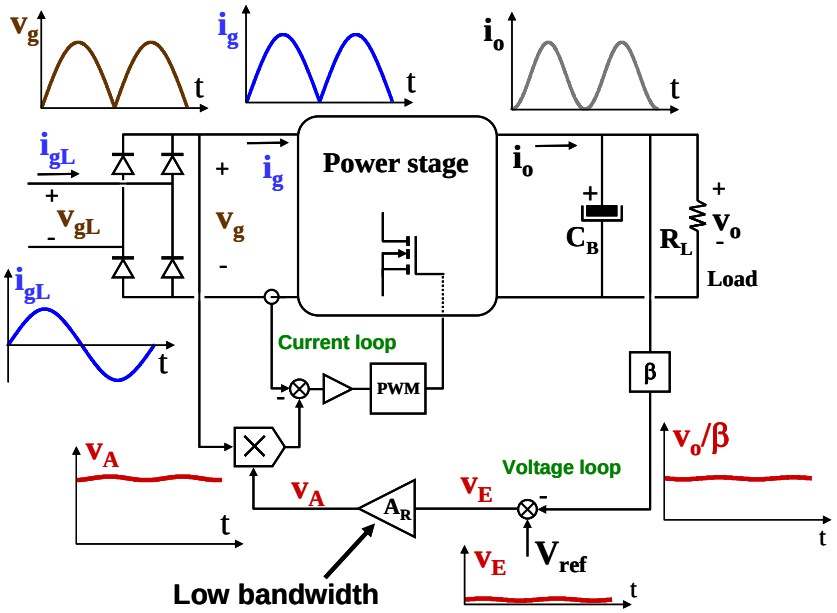
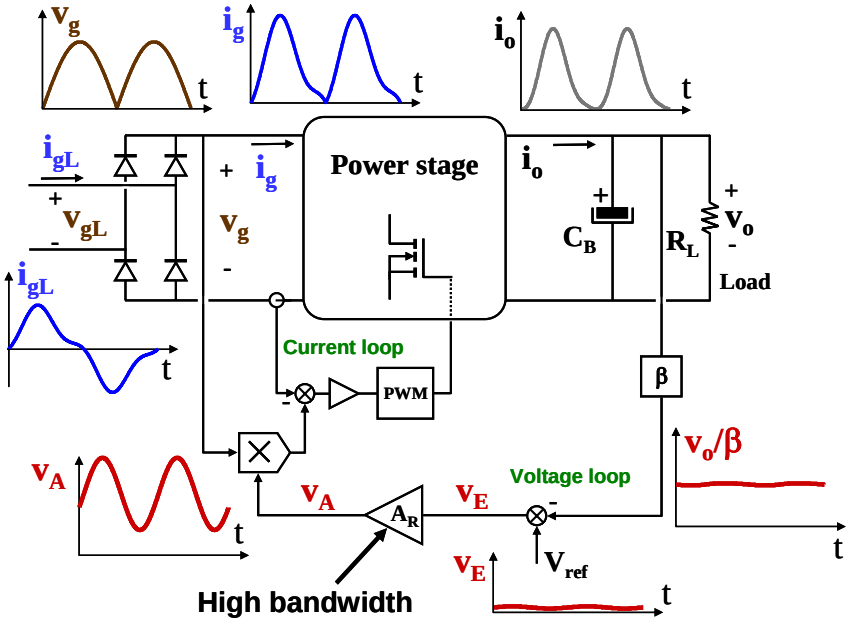
I. INTRODUCTION

In order to limit the harmonic content on the line current of mains-connected equipment, the use of an active Power Factor Corrector (PFC) [1, 2] is virtually mandatory. Figure 1a shows a general scheme of an active PFC controlled by two feedback loops, which is the most popular circuitry to control power converters of this type. In this figure, the inner feedback loop is an input-current feedback loop, while the outer one is an output-voltage feedback loop. The current loop makes the line current follow a reference signal which is obtained by multiplying a rectified sinusoidal waveform (obtained from the line voltage) by the control signal v_A. Thus, the line current i_{gL} is a sinusoid whose amplitude is determined by the value of v_A. The standard design of the voltage feedback loop implies low ripple in v_A [2] (see Fig. 1a). This is because a relatively high ripple would



(a)



(b)

Fig. 1: a) PFC with no appreciable voltage ripple on the control signal v_A. b) PFC with appreciable voltage ripple on v_A.

cause considerable distortion in the reference of the line current feedback loop and hence in the line current. To have low ripple on the control signal v_A, the bandwidth of the compensator A_R must be relatively low, which leads to a low bandwidth in the entire output-voltage feedback loop. This fact limits the transient response of the PFC. Unfortunately, the transient response of a PFC under these conditions is not fast enough to satisfy the requirements of some loads [2, 3]. Accordingly, a second stage must be connected in cascade with the PFC to provide fast response as well as the required galvanic isolation between line and load. Although the two-stage arrangement is the best solution for many applications above 600 W, it is relatively expensive due to requiring two converters.

In some specific applications, the use of only one PFC with galvanic isolation as the complete power supply may be an attractive option, especially if the output voltage is relatively high (above approximately 40 V). In this case, the poor transient response obtained with the standard low-bandwidth compensator becomes inadequate and a faster output-voltage feedback loop must be implemented. To achieve this, the bandwidth of the compensator A_R must be relatively high [3, 4], thus leading to considerable voltage ripple in the control signal v_A (see Fig. 1b). A number of solutions have been proposed to cancel this voltage ripple [4-13], but they are not easily implemented in low cost PFCs.

Therefore, the easiest method to obtain a relatively fast transient response in a PFC is to design the compensator A_R with relatively wide bandwidth, thus leading to appreciable voltage ripple on the control signal v_A. As given in [14], the line current distortion due to this voltage ripple has a limited effect on the compliance with EN 61000-3-2 regulations. It should be noted that these regulations only impose the condition that the harmonic content of the line current must be lower than the limits they impose. Consequently, many authors have introduced PFC topologies with non-sinusoidal line current waveforms (but with limited harmonics) [15-25].

The voltage ripple on the control signal v_A modifies both the static and dynamic model of the power stage and has a strong effect on the line current waveform obtained at the input of the PFC. The study of the influence of this voltage ripple on the static characteristics of a PFC is in fact the goal of this paper.

II. Static Modelling of a Power Factor Corrector with Appreciable Voltage Ripple in the Output-Voltage Feedback Loop

The voltage and the current at the input of the power stage shown in Fig. 1b can be written as follows:

$$v_g(\omega_L t) = v_{gp}\left|\sin(\omega_L t)\right|, \qquad (1)$$

$$i_g(\omega_L t) = \frac{v_{gp}\left|\sin(\omega_L t)\right| v_A(t)}{K_M}, \qquad (2)$$

where v_{gp} is the peak value of $v_g(\omega_L t)$, ω_L is the angular frequency of the line, $v_A(t)$ is the output voltage of the compensator and K_M is a constant determined by the controller. The voltage $v_A(t)$ can be rewritten as follows (see Fig. 2):

$$v_A(t) = v_{Adc} + v_{Aac}(t), \qquad (3)$$

$$v_{Aac}(t) = v_{Aacp}\sin(2\omega_L t - \phi_L), \qquad (4)$$

where v_{Adc} is the dc component of $v_A(t)$, $v_{Aac}(t)$ is its ac component, v_{Aacp} is the amplitude of $v_{Aac}(t)$ and ϕ_L is its phase lag angle, as given in Fig. 2 (i.e., the delay time between the zero crossing of the line voltage and the zero crossing of the ripple on v_A is $\phi_L/2\omega_L$). Note that only a component of twice the line frequency has been considered as the ac component of $v_A(t)$. This is because the only significant harmonic in the voltage ripple across the bulk capacitor C_B is that of twice the line frequency, the remaining harmonics having been considerably filtered by this capacitor. Moreover, the voltage gain of the

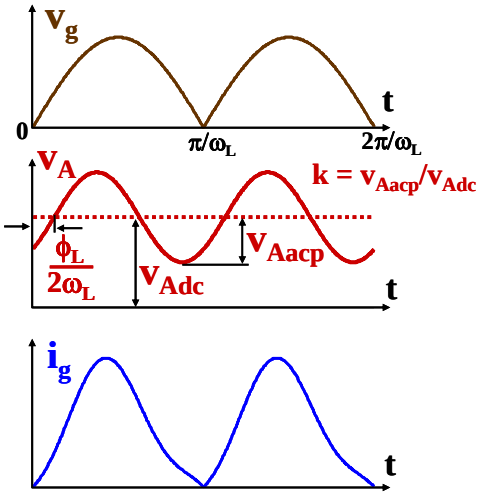


Fig. 2: Main waveforms in a PFC with appreciable voltage ripple on the control signal v_A.

compensator A_R at frequencies greater than twice the line frequency will be lower than at twice the line frequency, thus contributing to filtering the harmonics of frequencies higher than twice the line frequency.

The pulsating input power $p_g(\omega_L t)$ can be obtained by multiplying the values of $v_g(\omega_L t)$ and $i_g(\omega_L t)$ obtained from (1) and (2):

$$p_g(\omega_L t) = v_g(\omega_L t) i_g(\omega_L t) = \frac{V_{gp}^2 V_{Adc}}{K_M} \sin^2(\omega_L t) \cdot (1 + k \sin(2\omega_L t - \phi_L)), \qquad (5)$$

where:

$$k = \frac{V_{Aacp}}{V_{Adc}}. \qquad (6)$$

Note that k is the value of the relative ripple on v_A. The pulsating output power (the power delivered by the power stage in Fig. 1b) can be obtained by multiplying the output voltage v_o by the current i_o injected by the power stage into the output cell made up of the bulk capacitor C_B and the load R_L:

$$p_{oi}(\omega_L t) = v_o i_o(\omega_L t). \qquad (7)$$

After establishing the balance between $p_g(\omega_L t)$ and $p_{oi}(\omega_L t)$, we obtain:

$$i_o(t) = \frac{V_{gp}^2 V_{Adc}}{v_o K_M} \sin^2(\omega_L t) \cdot (1 + k \sin(2\omega_L t - \phi_L)). \qquad (8)$$

The average value of $p_g(\omega_L t)$ in half a line cycle will thus be:

$$p_{gav} = \frac{\omega_L}{\pi} \int_0^{\frac{\pi}{\omega_L}} p_g(\omega_L t) dt = \frac{V_{gp}^2 V_{Adc}}{4K_M} (2 + k \sin \phi_L). \qquad (9)$$

This equation shows that for a given dc value of v_A, the power processed by the power stage depends strongly on the voltage ripple on v_A (through k and ϕ_L), as shown in Fig. 3. In this figure, the power has been normalized to the no-ripple case (i.e., k=0).

The dc output power over the load will be:

$$p_o = \frac{v_o^2}{R_L}, \qquad (10)$$

and after establishing the balance between p_{gav} and p_o, we obtain:

$$p_{gav} = p_o = \frac{v_o^2}{R_L} = \frac{v_{gp}^2 v_{Adc}}{4K_M}(2 + k\sin\phi_L). \qquad (11)$$

From (2-4) and (11), the value of $i_g(\omega_L t)$ can be rewritten as follows:

$$i_g(\omega_L t) = \frac{4v_o^2}{v_{gp}R_L} \cdot \frac{[1 + k\sin(2\omega_L t - \phi_L)]}{(2 + k\sin\phi_L)} |\sin\omega_L t|. \qquad (12)$$

Taking into account (12), the line current i_{gL} will be:

$$i_{gL}(\omega_L t) = \frac{4v_o^2}{v_{gp}R_L} \cdot \frac{[1 + k\sin(2\omega_L t - \phi_L)]}{(2 + k\sin\phi_L)} \sin\omega_L t. \qquad (13)$$

Figure 4 shows the line current waveforms corresponding to different values of k and ϕ_L, which have been obtained from (13). As can be seen, k and ϕ_L has a strong influence on the line current waveforms, especially for the highest values of k.

Also taking into account (11), (8) can be rewritten as follows:

$$i_o(\omega_L t) = \frac{4v_o}{R_L} \cdot \frac{[1 + k\sin(2\omega_L t - \phi_L)]}{(2 + k\sin\phi_L)} \sin^2\omega_L t. \qquad (14)$$

The harmonic content of both $i_g(\omega_L t)$ and $i_o(\omega_L t)$ is easily obtained from (13) and (14) by applying basic trigonometric relationships:

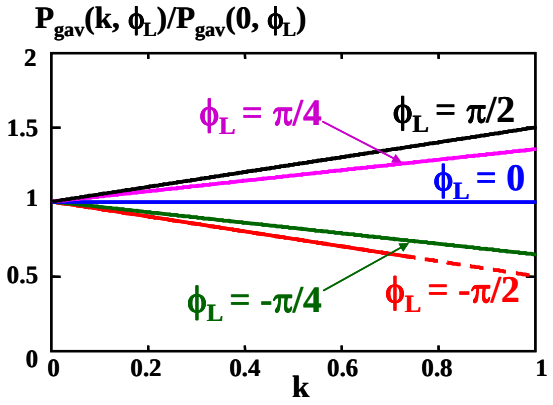


Fig. 3: Normalized power processed by the PFC versus k and ϕ_L.

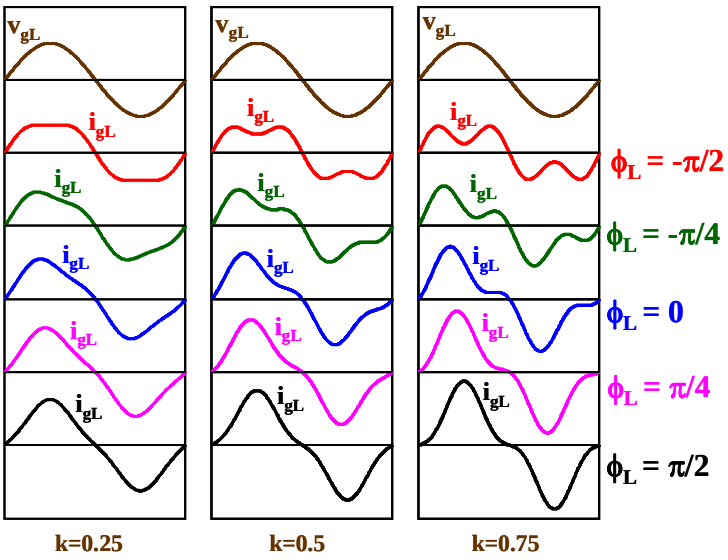


Fig. 4: Line current for different values of k and ϕ_L.

$$i_{gL}(\omega_L t) = i_{gL1}(\omega_L t) + i_{gL3}(\omega_L t)\,, \tag{15}$$

$$i_o(\omega_L t) = i_{odc} + i_{o2}(\omega_L t) + i_{o4}(\omega_L t)\,, \tag{16}$$

where:

$$i_{gL1}(\omega_L t) = \frac{4v_o^2}{v_{gp} R_L (2 + k\sin\phi_L)}\left[\sin\omega_L t + \frac{k}{2}\cos(\omega_L t - \phi_L)\right], \tag{17}$$

$$i_{gL3}(\omega_L t) = \frac{2v_o^2 k}{v_{gp} R_L (2 + k\sin\phi_L)}\cos(3\omega_L t - \phi_L)\,, \tag{18}$$

$$i_{odc} = \frac{v_o}{R_L}\,, \tag{19}$$

$$i_{o2}(\omega_L t) = \frac{2v_o}{R_L (2 + k\sin\phi_L)}\left[k\sin(2\omega_L t - \phi_L) - \cos(2\omega_L t)\right], \tag{20}$$

$$i_{o4}(\omega_L t) = \frac{-v_o k}{R_L (2 + k\sin\phi_L)}\sin(4\omega_L t - \phi_L)\,. \tag{21}$$

The static model of the PFC can be directly derived from (17) through (21). Figure 5 shows the equivalent circuit that allows us to predict the output voltage ripple, the relationship between this ripple and the ripple on the control signal and, finally, the line harmonic content.

III. Output Voltage Ripple

An important design parameter of any PFC is the output voltage ripple. This ripple is assumed to be much lower than the dc component of the output voltage. This means that the value of this ripple can be neglected when the output voltage is analysed. However, the small value of this ripple cannot be neglected when the output-voltage feedback loop is analysed, due to the fact that this ripple is amplified by the compensator A_R, which has not been designed to have low gain at twice the line

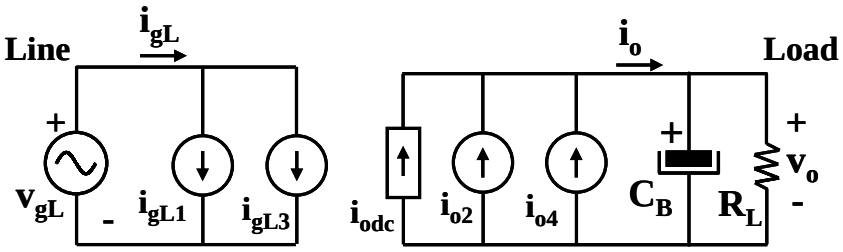


Fig. 5: Static model of a PFC with appreciable ripple on the control signal.

frequency. In this case (as in the case of any PFC), this ripple is mainly generated by the current source $i_{o2}(\omega_L)$. Its amplitude (i_{o2p}) and its phase lag angle (ϕ_{io2}) can be easily obtained from (20) after applying basic trigonometric relationships:

$$i_{o2p} = \frac{2v_o}{R_L} \cdot \frac{\sqrt{1+k^2+2k\sin\phi_L}}{2+k\sin\phi_L}, \tag{22}$$

$$\phi_{io2} = \arctan\frac{1+k\sin\phi_L}{k\cos\phi_L}. \tag{23}$$

The value of the output voltage ripple $v_{o2}(\omega_L t)$ can be calculated by multiplying the value of $i_{o2}(\omega_L t)$ by the impedance constituted by C_B and R_L connected in parallel. Thus, the amplitude of the output voltage ripple will be:

$$v_{o2p} = i_{o2p} Z_{CBRL}, \tag{24}$$

where Z_{CBRL} is the magnitude of that impedance at twice the line frequency, given by:

$$Z_{CBRL} = \frac{R_L}{\sqrt{1+(2\omega_L C_B R_L)^2}}. \tag{25}$$

From (22), (24) and (25), we obtain:

$$v_{o2p} = \frac{2v_o}{\sqrt{1+(2\omega_L C_B R_L)^2}} \cdot \frac{\sqrt{1+k^2+2k\sin\phi_L}}{2+k\sin\phi_L}. \tag{26}$$

As regards the impedance phase lag angle, its value is:

$$\phi_{CBRL} = \arctan(2\omega_L C_B R_L), \tag{27}$$

and hence the phase lag angle of the output voltage ripple will be:

$$\phi_{vo2} = \phi_{io2} + \phi_{CBRL} = \arctan\frac{1+k\sin\phi_L}{k\cos\phi_L} + \arctan(2\omega_L C_B R_L) \tag{28}$$

However, the impedance of C_B at twice the line frequency must be much lower than R_L in order to maintain the output voltage ripple at a reasonable value. Hence, the parallel impedance of C_B and R_L can be approximated by the impedance of C_B in many cases. We thus obtain from (26) and (28):

$$v_{o2p} \cong \frac{v_o}{R_L C_B \omega_L} \cdot \frac{\sqrt{1+k^2+2k\sin\phi_L}}{2+k\sin\phi_L}. \tag{29}$$

$$\phi_{vo2} \cong \arctan\frac{1+k\sin\phi_L}{k\cos\phi_L}+\frac{\pi}{2}. \qquad (30)$$

The value of the relative output voltage ripple at twice the line frequency, r_{V2}, can be easily obtained from (26):

$$r_{V2}=\frac{v_{o2p}}{v_o}=\frac{2}{\sqrt{1+(2\omega_L C_B R_L)^2}}\cdot\frac{\sqrt{1+k^2+2k\sin\phi_L}}{2+k\sin\phi_L}. \qquad (31)$$

In the case of neglecting the influence of R_L on the impedance of the C_BR_L cell (i.e., $2\omega_L C_B R_L>>1$), we obtain from (29):

$$r_{V2}\cong\frac{1}{R_L C_B\omega_L}\cdot\frac{\sqrt{1+k^2+2k\sin\phi_L}}{(2+k\sin\phi_L)}. \qquad (32)$$

Similarly, the amplitude of the output voltage ripple at four times the line frequency, v_{o4p}, and its relative value, r_{V4}, can be easily obtained. In this case, the influence of R_L on the impedance of the C_BR_L cell is always negligible. Therefore, we obtain from (21):

$$v_{o4p}=\frac{i_{o4p}}{C_B 4\omega_L}=\frac{v_o k}{4C_B\omega_L R_L(2+k\sin\phi_L)}, \qquad (33)$$

$$r_{V4}=\frac{v_{o4p}}{v_o}=\frac{1}{R_L C_B\omega_L}\cdot\frac{k}{4(2+k\sin\phi_L)}. \qquad (34)$$

The quotient between both output ripples (v_{o2p} and v_{o4p}) has been plotted in Fig. 6. For the sake of simplicity, Equation (32), has been used in this plot instead of Equation (31). As the figure shows, the value of v_{o4p} is negligible in comparison with v_{o2p} for values of ϕ_L in the range between -45º and +90º, which are the values of ϕ_L obtained when a standard compensator is implemented. Only for the case in which the value of k is near 1 and the value of ϕ_L is near -90º does the value of v_{o4p} become significant in comparison with v_{o2p} (and even exceeds it). Moreover, it should be noted that the influence of $v_{or4}(\omega_L t)$ on the voltage ripple on the control signal v_A is also attenuated by the gain of the compensator A_R (see Fig. 1b) at four times the line

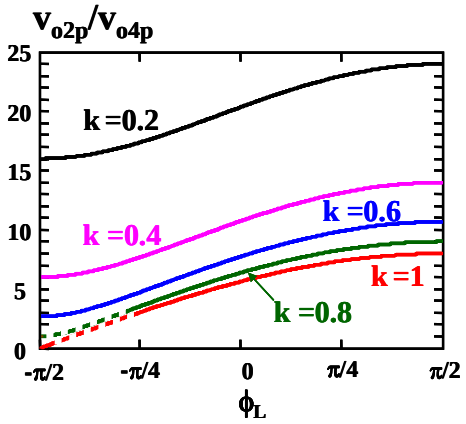


Fig. 6: Value of the quotient between the output-voltage ripple of twice and four times the line frequency for different values of k and ϕ_L,

frequency, which is always lower than its gain at twice the line frequency. This fact reinforces the initial assumption of having ripple of only twice the line frequency on the control signal v_A, at least for ϕ_L values in the range between -45º and +90º, which is the range with practical interest, as we shall see in the following sections.

IV. Deriving the Relationship Between the Output Voltage Ripple and the Voltage Ripple on the Control Signal

So far, we have shown that the values of the amplitude and phase lag angle of the output voltage ripple (v_{o2p} and ϕ_{vo2}) are functions of the relative voltage ripple on the control signal v_A and its phase lag angle (k and ϕ_L) through (26) and (28). However, the values of v_{o2p} and ϕ_{vo2} will determine the values of k and ϕ_L through the output-voltage feedback loop. According to Fig. 1b, the amplitudes of the output voltage ripple and the voltage ripple on the control signal are related as follows:

$$v_{Aacp} = \beta A_{R2\omega L} v_{o2p}, \qquad (35)$$

where $A_{R2\omega L}$ is the gain of the compensator at twice the line frequency and β is the gain of the voltage sensor (see Fig. 1b). Similarly, the phase lag angles of both ripples are related as follows:

$$\phi_L = \phi_{vo2} - \pi + \phi_{R2\omega L} = \arctan\frac{1 + k\sin\phi_L}{k\cos\phi_L} + \arctan(2\omega_L C_B R_L) - \pi + \phi_{R2\omega L}, \qquad (36)$$

where $\phi_{R2\omega L}$ is the phase lag angle of the compensator at twice the line frequency and the phase lag of $-\pi$ radians is due to the inversion of the sign in the feedback loop. Moreover, the value of ϕ_L can be obtained from (36) after using some trigonometric relationships:

$$\phi_L = \arccos\left(k\cos\phi_{R2\omega L}\right) + \phi_{R2\omega L} + \arctan(2\omega_L C_B R_L) - \pi. \qquad (38)$$

In the case of neglecting the influence of R_L on the impedance of the $C_B R_L$ cell ($\arctan(2\omega_L C_B R_L) \cong \pi/2$), we obtain from (38):

$$\phi_L \cong \arccos\left(k\cos\phi_{R2\omega L}\right) + \phi_{R2\omega L} - \pi/2. \qquad (39)$$

Equation (39) has been plotted in Fig. 7. In practice, the values of $\phi_{R2\omega L}$ must be in the range between 0º and +90º due to the real compensator used. It should be noted that in the case of a design with no appreciable ripple on the control signal v_A (i.e., slow transient response), this phase lag angle will be near +90º due to the low-pass filtering behaviour of the compensator used. On the other hand, this phase lag angle will be clearly lower than +90º in the case of appreciable ripple on v_A. However, this phase lag angle will never reach negative phase lag angles, because that would mean high-pass filtering behaviour in the compensator, which is not desired at all.

As Fig. 7 shows, the majority of the possible values of $\phi_{R2\omega L}$ correspond to values of ϕ_L in the range from -45º to +90º, which once more reinforces the initial assumption of only having ripple of twice the line frequency on v_A.

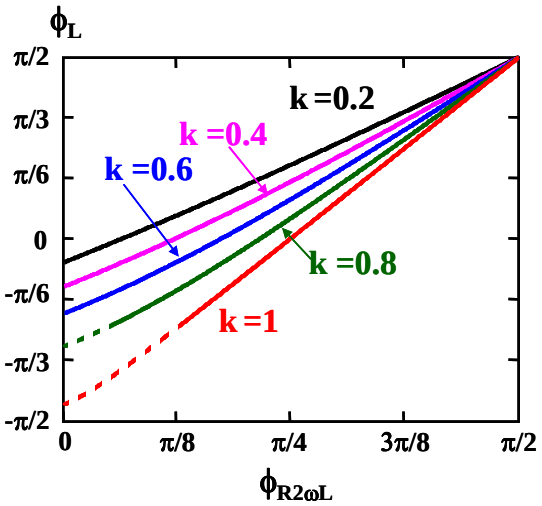


Fig. 7: Values of ϕ_L as a function of $\phi_{R2\omega L}$ for different values of k.

From (35) and (36) and taking into account (6) and (31), the values of $A_{R2\omega L}$ and $\phi_{R2\omega L}$ needed for a set of desired values of k and ϕ_L are directly obtained as follows:

$$A_{R2\omega L} = \frac{v_{Aacp}}{v_{o2p}\beta} = \frac{v_{Adc}k}{v_o r_{v2}\beta}, \tag{40}$$

$$\phi_{R2\omega L} = \phi_L - \arctan\frac{1+k\sin\phi_L}{k\cos\phi_L} - \arctan(2\omega_L C_B R_L) + \pi . \tag{41}$$

Taking into account (11) and (26), (40) can be rewritten as follows:

$$A_{R2\omega L} = \frac{2v_o K_M}{v_{gp}^2\beta}\cdot\frac{\sqrt{1+(2\omega_L C_B R_L)^2}}{R_L}\cdot\frac{k}{\sqrt{1+k^2+2k\sin\phi_L}} . \tag{42}$$

To study the steady-state variation of k and ϕ_L with the load variations, the quantities at full load will be denoted by subscript "0". Thus, (31), (41) and (42) become:

$$r_{V20} = \frac{2}{\sqrt{1+(2\omega_L C_B R_{L0})^2}}\cdot\frac{\sqrt{1+k_0^2+2k_0\sin\phi_{L0}}}{2+k_0\sin\phi_{L0}}, \tag{43}$$

$$\phi_{R2\omega L} = \phi_{L0} - \arctan\frac{1+k_0\sin\phi_{L0}}{k_0\cos\phi_{L0}} - \arctan(2\omega_L C_B R_{L0}) + \pi , \tag{44}$$

$$A_{R2\omega L} = \frac{2v_o K_M}{v_{gp}^2\beta}\cdot\frac{\sqrt{1+(2\omega_L C_B R_{L0})^2}}{R_{L0}}\cdot\frac{k_0}{\sqrt{1+k_0^2+2k_0\sin\phi_{L0}}} . \tag{45}$$

Taking into account (41), (42), (43), (44) and (45), we obtain:

$$k = \frac{1}{\cos\phi_L \tan\left(\phi_L - \phi_{L0} + \arctan\frac{1+k_0\sin\phi_{L0}}{k_0\cos\phi_{L0}} + \arctan\sqrt{\lambda_0} - \arctan\left(\sqrt{\lambda_0}\frac{R_L}{R_{L0}}\right)\right) - \sin\phi_L}, \tag{46}$$

$$\phi_L = \arcsin\left(\frac{k\left(1+k_0^2+2k_0\sin\phi_{L0}\right)\left(1+\lambda_0\left(\frac{R_L}{R_{L0}}\right)^2\right)}{2k_0^2\left(1+\lambda_0\right)\left(\frac{R_L}{R_{L0}}\right)^2}-\frac{1+k^2}{2k}\right), \qquad (47)$$

where:

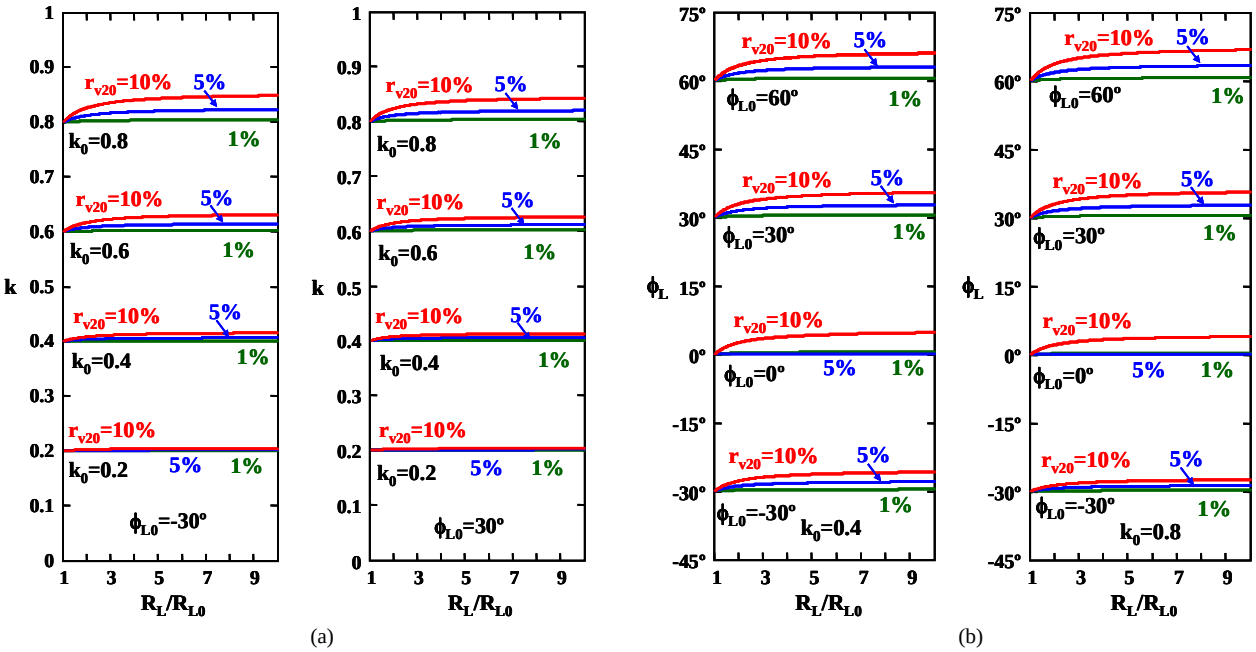
$$\lambda_0 = \frac{4\left(1+k_0^2+2k_0\sin\phi_{L0}\right)}{r_{v20}^2\left(2+k_0\sin\phi_{L0}\right)^2}-1. \qquad (48)$$

The simultaneous equations (46) and (47) can be solved using a Mathcad spreadsheet. The results obtained are summarized in Fig. 8. As this figure shows, the values of k and ϕ_L are practically independent of the variations of R_L when the relative output voltage ripple at full load is small. We can obtain the same conclusion by neglecting the influence of R_L on the impedance of the C_BR_L cell in (41) and (42), thus obtaining:

$$\phi_{R2\omega L} = \phi_L - \arctan\frac{1+k\sin\phi_L}{k\cos\phi_L}+\frac{\pi}{2}. \qquad (49)$$

$$A_{R2\omega L} = \frac{4v_o K_M C_B \omega_L}{v_{gp}^2\beta}\cdot\frac{k}{\sqrt{1+k^2+2k\sin\phi_L}}. \qquad (50)$$

From the simultaneous equations (49) and (50), we can deduce that the values of k and ϕ_L do not change with the load R_L, as they can be solved independently of the R_L value. This important conclusion means that if the relative output voltage ripple is small (which is the most common case), then the line current waveform (and hence the relative line current distortion) is



(a) (b)

Fig. 8: a) Variation of k for different values of r_{v20}, k_0 and ϕ_{L0} when the load changes. b) Variation of ϕ_L for different values of r_{v20}, k_0 and ϕ_{L0} when the load changes.

independent of the load.

As stated previously, (41) and (42) allow us to calculate the magnitude and phase lag angle of the compensator at twice the line frequency ($A_{R2\omega L}$ and $\phi_{R2\omega L}$) as a function of the desired values of k and ϕ_L and from some parameters of the converter (namely v_o, v_{Adc}, β and r_{v2}). However, the choice of $A_{R2\omega L}$ and $\phi_{R2\omega L}$ also affects the value of the compensator gain at other frequencies and must therefore be compatible with the stability of the output voltage feedback loop. This means that not all the possible values of k and ϕ_L can be used in a practical design. The harmonic content and compliance with the regulations regarding the line harmonic content establish a first constraint that will be presented in the following sections of this paper, but this constraint is not the only one. The choice of k and ϕ_L (and therefore of $A_{R2\omega L}$ and $\phi_{R2\omega L}$) must be compatible with the closed-loop stability and with the desired transient response. However, a complete analysis of the stability of the output-voltage feedback loop requires having an ac small-signal model of the power stage, which is beyond the scope of this paper (though it is approached in [26] and in [27]). However, the starting point to obtain the small-signal model of a PFC with appreciable voltage ripple on the control signal is in fact the static analysis carried out here.

V. Line Harmonic Content

As mentioned in the previous sections, the voltage ripple on the control signal v_A causes line current distortion at the input of the PFC. Assuming that the ripple on v_A is mainly twice the line frequency, then the line current is expressed by (15). As (15) shows, the only significant harmonics in the line current are the first and the third. The amplitude of the third harmonic can be easily deduced from (18):

$$i_{gL3p} = \frac{2v_o^2}{v_{gp}R_L} \cdot \frac{k}{(2 + k\sin\phi_L)} . \qquad (51)$$

Moreover, after taking into account (11) and some trigonometric relationships, (17) can be rewritten as follows:

$$i_{gL1}(\omega_L t) = \frac{4v_o^2}{v_{gp}R_L(2+k\sin\phi_L)}\left[(1+\frac{k}{2}\sin\phi_L)\sin\omega_L t + \frac{k}{2}\cos\phi_L \cos\omega_L t\right]. \qquad (52)$$

The amplitude of the first harmonic can be easily calculated from the following equation:

$$i_{gL1p} = \frac{4v_o^2}{v_{gp}R_L} \cdot \frac{\sqrt{1 + 0.25k^2 + k\sin\phi_L}}{(2 + k\sin\phi_L)} . \qquad (53)$$

As the only harmonics are the first and the third, the Total Harmonic Distortion (THD) will thus be:

$$THD = \frac{i_{gL3p}}{i_{gL1p}} = \frac{k}{\sqrt{4 + k^2 + 4k\sin\phi_L}} . \qquad (54)$$

The values of the THD for different values of k and ϕ_L have been plotted in Fig. 9. As this figure shows, the PFC generates moderate values of the THD when ϕ_L is positive, even if the value of k is relatively high. However, the THD obtained is always very low for low values of k, no matter the value of ϕ_L.

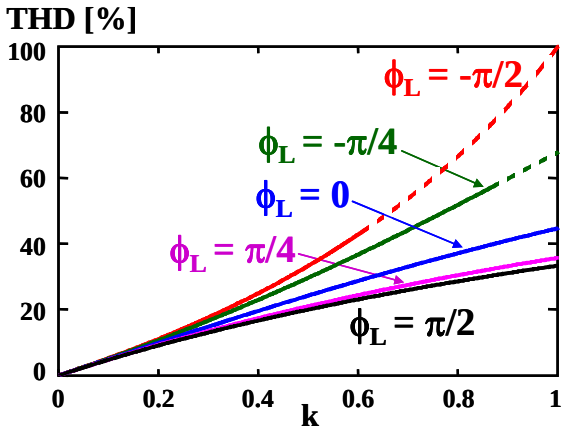


Fig. 9: Line THD as a function of k and ϕ_L.

The rms value of the line current can be calculated from (13) as follows:

$$i_{gLrms} = \sqrt{\frac{1}{T}\int_0^T i_{gL}(\omega_L t)^2 dt} = \frac{4v_o^2\sqrt{0.5 + 0.25k^2 + 0.5k\sin\phi_L}}{v_{gp}R_L(2 + k\sin\phi_L)} = \frac{p_{gav}\sqrt{2 + k^2 + 2k\sin\phi_L}}{v_{gp}(1 + 0.5k\sin\phi_L)}. \qquad (55)$$

Bearing in mind (55), the Power Factor (PF) can be easily calculated:

$$PF = \frac{p_{gav}}{i_{gLrms}\, v_{gp}/\sqrt{2}} = \frac{\sqrt{2}(1 + 0.5k\sin\phi_L)}{\sqrt{2 + k^2 + 2k\sin\phi_L}}. \qquad (56)$$

The values of the PF for different values of k and ϕ_L are shown in Fig. 10. High values of the PF can be obtained when ϕ_L is positive, even if the value of k is relatively high. However, the PF becomes quite poor when ϕ_L is negative and k is relatively high.

VI. Compliance with EN 61000-3-2 Regulations

To comply with EN 61000-3-2 regulations, the rms value of each harmonic must be lower than the limit imposed by the regulations. In the case of a PFC with appreciable voltage ripple on the control signal, the only significant harmonics in the line current are the first and the third. Hence, only the third harmonic must be compared with the limits specified by the

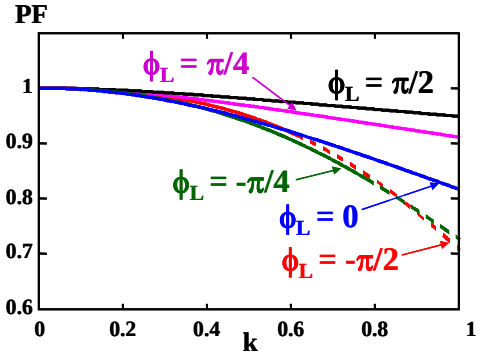


Fig. 10: PF as a function of k and ϕ_L.

aforementioned regulations to test whether the converter complies with them. Moreover, any piece of equipment can be classified in four classes according to these regulations [28, 29]:

Class A

For equipment classified in Class A, the limit for the third harmonic is 2.3 A rms when the line voltage is 230 V rms. Note that this limit is an absolute value and does not depend on the power handled by the piece of equipment.

The rms value of the third harmonic is given by (51). Taking into account (11), this equation can be rewritten as follows:

$$i_{gL3p} = \frac{2p_{gav}}{v_{gp}} \cdot \frac{k}{(2 + k\sin\phi_L)} . \qquad (57)$$

The maximum power compatible with the regulations in Class A can be easily calculated by substituting the aforementioned current and voltage values in (57):

$$P_{gmax\_A} = 529\frac{(2 + k\sin\phi_L)}{k} . \qquad (58)$$

Equation (58) is plotted in Fig. 11. This figure shows that the PFC will comply with the regulations for Class A equipment up to the highest possible power specified in the regulations (16 A at 230 V; i.e., 3680 W) if k is lower than 0.25. For higher values of k, the maximum power compatible with the regulations strongly depends on ϕ_L. As in the case of the THD and of the PF, the best results will be obtained with values of ϕ_L as close to +90º as possible.

Class B

In this case, the limits for each harmonic are also absolute values, which means that they do not depend on the power processed by the PFC. The only difference in relation to Class A is that these limits are slightly higher. Thus, the limit for the third harmonic is 3.45 A rms when the line voltage is 230 V rms. The maximum power compatible with EN 61000-3-2 in Class B equipment can be easily calculated by following the same procedure as that for Class A:

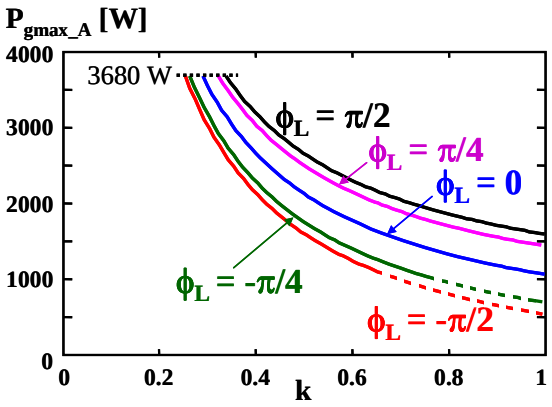


Fig. 11: Maximum power compatible with the regulation in Class A as a function of k and ϕ_L.

$$P_{g\max\_B} = 793.5\frac{(2 + k\sin\phi_L)}{k}. \qquad (59)$$

This equation is plotted in Fig. 12. As this figure shows, the PFC will comply with the regulations for Class B equipment up to 3680 W if k is lower than 0.35.

Class C

In this class, the limit imposed on the third harmonic depends on the PF and on the rms value of the first harmonic as follows:

$$i_{gL3p}/\sqrt{2} \le 0.3 \cdot PF \cdot i_{gL1p}/\sqrt{2}. \qquad (60)$$

After substituting (51), (53) and (56) in (60), we obtain:

$$\frac{0.3}{\sqrt{2}} = 0.212 \ge \frac{k\sqrt{2 + k^2 + 2k\sin\phi_L}}{(2 + k\sin\phi_L)\sqrt{4 + k^2 + 4k\sin\phi_L}}. \qquad (61)$$

This inequality defines the area of compliance shown in Fig. 13a. As can be appreciated in this figure, the PFC always complies with the regulations for Class C equipment if k is lower than 0.45, whereas it never complies with them if k is higher than 0.82. For values of k between 0.45 and 0.82, the compliance depends on the value of ϕ_L. As in the other classes, the best results are obtained with values of ϕ_L as close as possible to +90º.

Class D

In this class of equipment, the limit imposed on each harmonic by the regulations is proportional to the power handled by the PFC. In other words, the quotient between the rms value of any harmonic divided by the input power must be below the limit specified by the regulations. For the third harmonic, this limit is 3.4 mA/W (rms value). Thus, applying this condition to (57), we obtain:

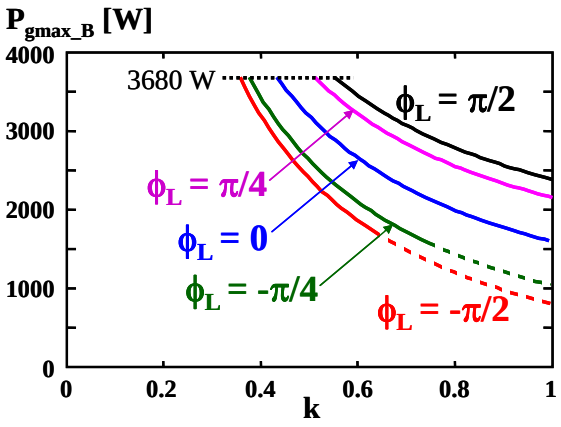


Fig. 12: Maximum power compatible with the regulation in Class B as a function of k and ϕ_L.

$$\frac{i_{gL3p}}{p_{gav}\sqrt{2}} = \frac{\sqrt{2}}{v_{gp}} \cdot \frac{k}{(2 + k\sin\phi_L)} \leq 3.4 \cdot 10^{-3} . \qquad (62)$$

This inequality defines the area of compliance plotted in Fig. 13b. As this figure shows, the relative value of the third harmonic is below the limit imposed by EN 61000-3-2 for almost any design condition. According to (62), the converter fails to comply with the regulations only if ϕ_L is between -90º and -45º and, at the same time, k is higher than 0.878. This design condition is of no real interest and could not be easily implemented. Moreover, the assumption of having negligible value of v_{o4p} is not true for such as values of k and ϕ_L.

VII. Simulated and Experimental Results

The analysis carried out was first confirmed by simulating the operation of an idealized PFC using PSPICE. Figure 14 shows the circuit used for this purpose. The power stage was simulated as two controlled current sources. The one connected to the input is directly controlled by the analog multiplier (which means an ideal input-current feedback loop in the PFC), while the one connected to the output is in charge of transferring all the input power to the output (the converter efficiency is assumed to be 1). The values of the compensator components were adapted to obtain the desired values of $A_{R2\omega L}$ and $\phi_{R2\omega L}$ and hence of k and ϕ_L according to (49) and (50). In all simulations, the line voltage was 230 Vrms and the output voltage, 400 Vdc. Moreover, different values of the bulk capacitor were chosen for each simulation in order to always have the same relative output voltage ripple (1 %). With the simple compensator chosen to close the feedback loop (see Fig. 14), not all the possible values of k (from 0 to 1) and ϕ_L (from -90º to +90º) can be achieved, due to the fact that $\phi_{R2\omega L}$ must be in the range from 0º to +90º (see Fig. 7).

Nonetheless, the line current waveforms for a wide range of k and ϕ_L values are shown in Fig. 15 and compared with the model developed here. As this figure shows, the line waveforms obtained by simulation and using the model agree very well. Only small discrepancies appear when the value of k is near 1 and the value of ϕ_L is negative, due to the influence of v_{o4p} on the control signal v_A, an influence that has been assumed in this study to be negligible in comparison to the influence of v_{o2p}.

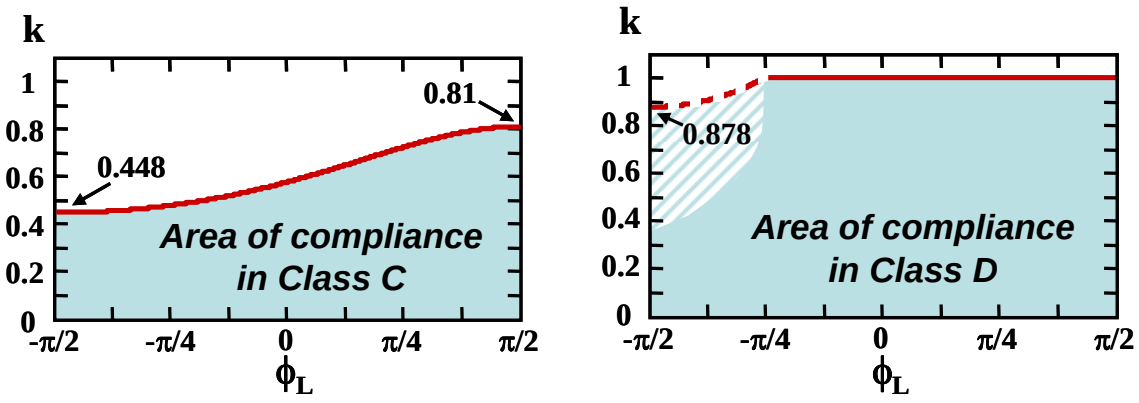


Fig. 13: Area of compliance in Class C (a) and in Class D (b).

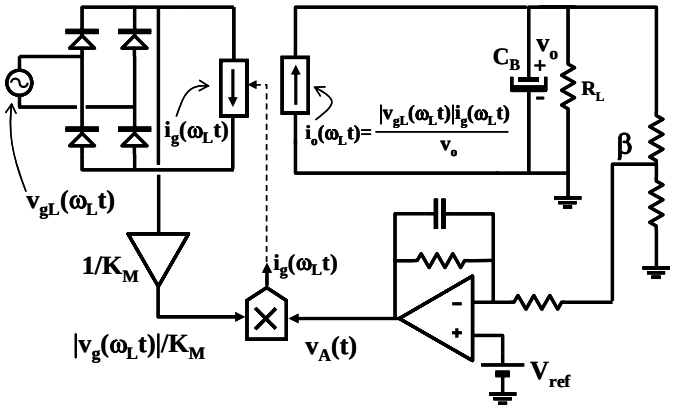


Fig. 14: Circuit used to simulate any PFC with analog multiplier control and appreciable voltage ripple on the control signal v_A.

As stated previously, this is an excellent approach for positive values of ϕ_L, but the assumption becomes false when ϕ_L is near -90º and k is relatively high, as Fig. 6 shows. Nevertheless, this is not a problem, as designs with ϕ_L near -90º are physically difficult (really impossible with the simple compensator shown in Fig.14) and they are not desirable from the harmonic content point of view (see Fig. 9-13).

The influence of both the load variations and the output voltage ripple on the line current waveform has also been studied by simulating the circuit shown in Fig. 14. The results given in Fig. 16 confirm that the line waveform is almost independent of the load variations and of the value of the relative output voltage ripple, especially if this is ripple is moderate (up to 10%).

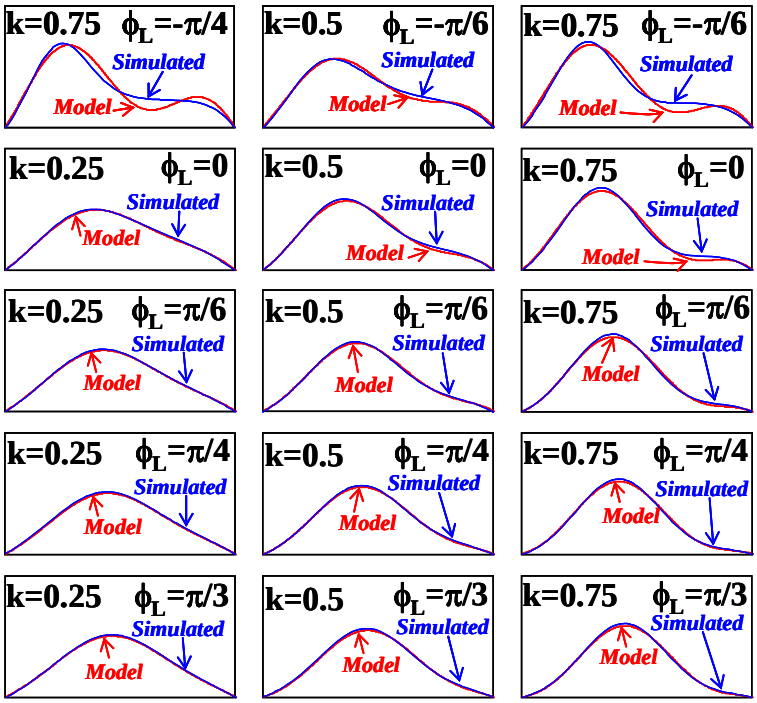


Fig. 15: Simulated and modelled line current waveforms obtained for different values of k and ϕ_L. In all cases, the values of C_B have been chosen to have an output voltage ripple of 1 %.

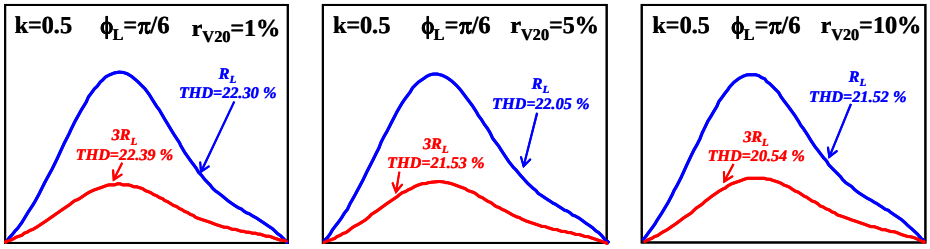


Fig. 16: Simulated current waveforms for different load and output voltage ripple, in all cases with k=0.5 and ϕ_L=30º.

To compare the line waveforms predicted by the model developed here with those obtained in a real prototype, a 500 W boost PFC was designed and built. The main characteristics of this converter are the following:

- Input voltage: 85-265 V.
- Output voltage: 400 V.
- Relative ripple: 1% (approximately).
- Switching frequency: 100 kHz.
- Power MOSFET: SPW47N60C3 (Infineon)
- Power diode: STTA2006 (ST).
- Controller: UC3854B (Texas Instruments)
- Main inductor: 329 μH, 35 turns, Molybdenum Permalloy Powder core (Arnold, μ_r=125, OD=1.84 in).

The results obtained when testing this prototype for different operating conditions are given in Figs. 17-20 and Table 1. The left-hand column of Fig. 17 shows the measured voltage ripple on the control signal, v_{Aac}, and the input voltage, v_g, whereas the line current waveforms obtained in the prototype are compared with those obtained from the model in the right-hand column of the same figure. As in the case of the results obtained by simulation, many different operating points were tested with very good agreement between the measured waveforms and those obtained using the model. The discrepancies between the results measured in the prototype and the model have been quantified in Table 1 by comparing the values of the PF and of the THD in both cases. Only small discrepancies appear when the value of k is relatively high and the value of ϕ_L is negative and near to -45º. Nevertheless, this is not a problem because this type of design is physically difficult and is not desirable from the harmonic content point of view.

Figure 18 shows the measured output-voltage-ripple waveforms corresponding to the values of k and ϕ_L given in Fig. 17. In all these cases, the value of the bulk capacitor C_B has been changed to always have an output voltage ripple of approximately 1 %. This figure shows that this ripple is quite sinusoidal for all the tested values of k and ϕ_L. As the model predicts, the less sinusoidal case corresponds to the negative value of ϕ_L tested in the prototype (ϕ_L = -25º).

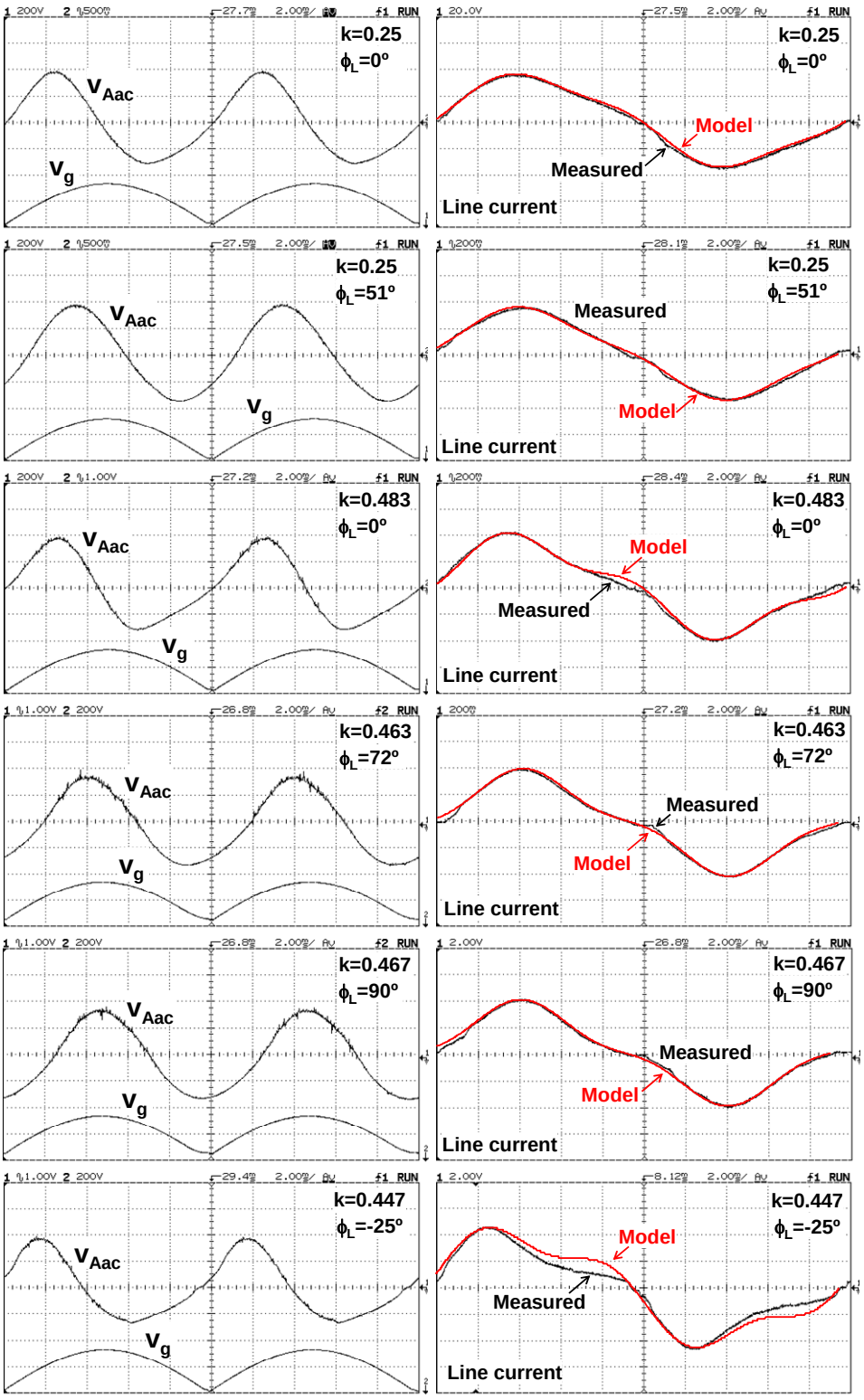


Fig. 17: Left: measured voltage ripple on the control signal (v_{Aac}) and input voltage (v_g) for different values of k and ϕ_L. Right: line current waveforms for different values of k and ϕ_L. In all cases, the values of C_B have been chosen to have an output voltage ripple of 1 %. Similarly, the values of some controller parameters have been changed to always have v_{Adc}=3.5V.

The line current waveforms and the harmonic content in the line when the prototype was designed with k = 0.259 and ϕ_L = -9.2º are given in Fig. 19. As this figure shows, the third harmonic is the only significant one (besides the first harmonic), as was assumed in the theoretical study. Moreover, the influence of both the load variations and the output voltage ripple on the line current

k	ϕ_L	Measured		Model	
		PF	THD [%]	PF	THD [%]
0.25	0º	0.97	11.8	0.985	12.4
0.25	51º	0.974	11.4	0.991	11.4
0.483	0º	0.937	20	0.946	23.5
0.463	72º	0.945	21.3	0.981	18.9
0.467	90º	0.955	21.6	0.983	18.9
0.447	-25º	0.876	33.3	0.949	24.1

Table 1: PF and THD values for the line current waveforms given in Fig. 15.

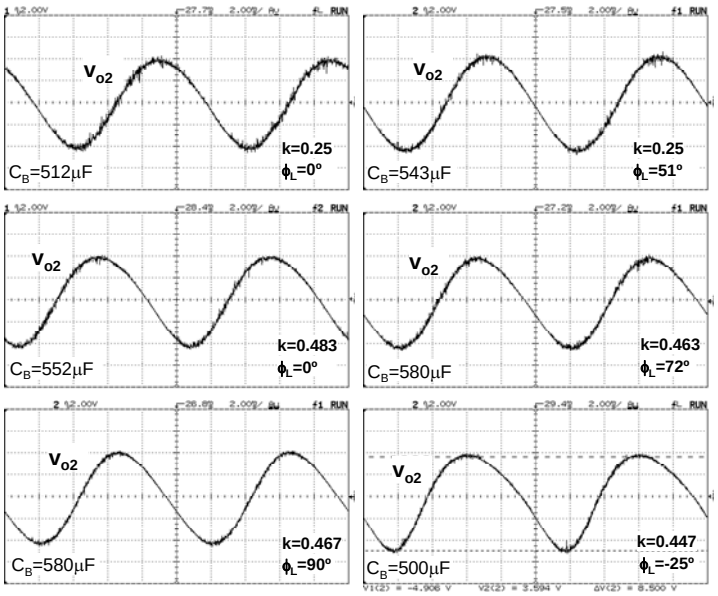


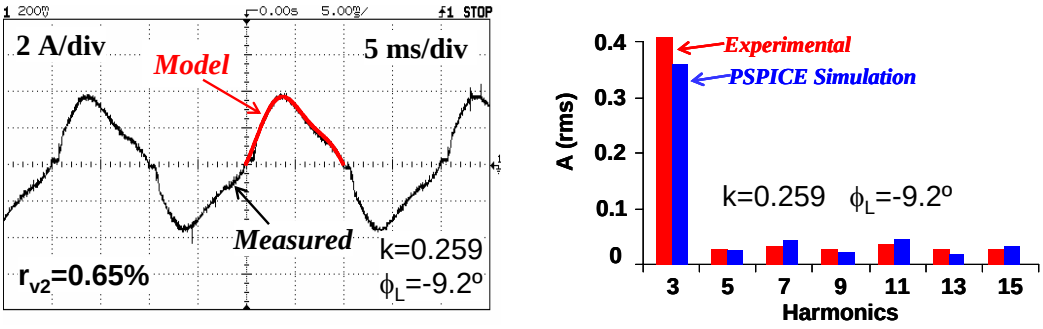
Fig. 18: Measured output voltage ripple for the values of k and ϕ_L given in Fig. 17. In all cases, the values of C_B have been changed to have an output voltage ripple of approximately 1 %.

waveform is given in Fig. 20, where the value of the bulk capacitor and of the feedback-loop compensator have been modified in order to obtain different values of the full-load output voltage ripple r_{v20} (5% and 10%) with the same values of k and ϕ_L (k = 0.259 and ϕ_L = -9.2º). In both cases, the value of the load has also been changed from 500 W to 166 W.

Finally, Fig. 21 shows the experimental results corresponding to a load step in the aforementioned prototype when it was designed with appreciable ripple on v_A in order to achieve fast transient response (k=0.259, ϕ_L = -9.2º) and when it was re-designed with negligible ripple on v_A (k=0.026, ϕ_L = 84.14º). As this figure shows, the settling time in the first case is about 10 ms, whereas it is 70 ms in the second case.

VIII. Conclusions

The static behaviour of a PFC with appreciable voltage ripple in the feedback loop has been studied in this paper using two parameters: the amplitude of the relative voltage ripple of the control signal, k, and its phase lag angle, ϕ_L. All the



(a) (b)

Fig.19: Line waveform (a) and harmonic content (b) when k = 0.259 and ϕ_L = -9.2º.

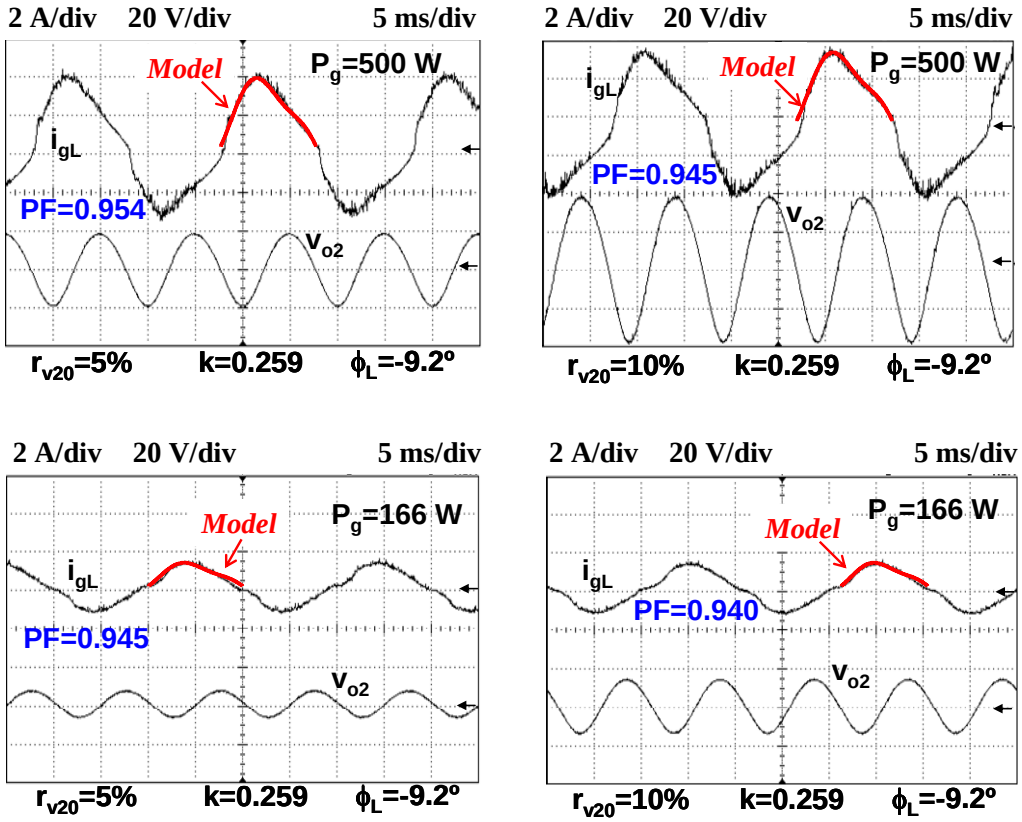


Fig.20: Line waveforms for different output power levels and values of r_{v20} (output voltage ripple at full load). In all cases k = 0.259 and ϕ_L = -9.2º.

characteristics of a PFC are affected by the values of these parameters. Thus, the power processed by the PFC not only depends on the dc value of the control signal, but also on its ripple. High values of the PF and low values of the THD are obtained when ϕ_L is positive, even if the value of k is not very low. However, these quantities become quite poor when ϕ_L is negative and k is relatively high at the same time. Compliance with EN 61000-3-2 regulations for Class A and Class B equipment can be achieved at high power if negative values of ϕ_L are avoided, even when k is situated in the mid-range (for example, 0.4). As regards Class C equipment, the line waveforms comply with the regulations for any value of ϕ_L if k < 0.45

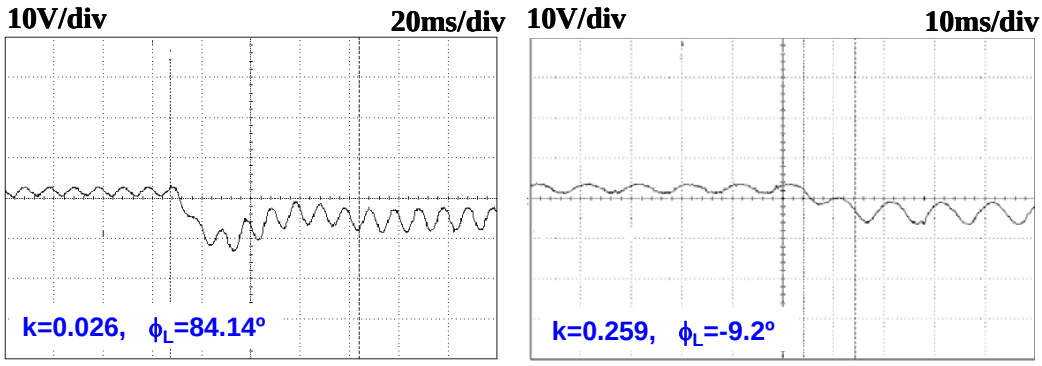


Fig.21: Experimental verification of the transient response of two different designs after a load step from 166 W to 500 W.

(whatever ϕ_L might be), whereas it never complies with them if k > 0.82 (once again, whatever ϕ_L might be). As regards Class D equipment, the line waveforms comply with the regulations for almost any value of k and ϕ_L.

Another important conclusion is that the shape of the line current waveforms does not depend on the load due to the fact that k and ϕ_L do not depend on it.

Finally, the theoretical study was verified both by simulation and in a prototype.

ACKNOWLEDGMENT

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