Dynamic Behavior of Current Controllers for Selective Harmonic Compensation in Three-phase Active Power Filters

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Abstract – Current regulators are a critical part of active power filters (APF's). Design of current regulators capable of compensating high frequency harmonics created by non-linear loads is a challenging task. Selective harmonic current compensation using harmonic regulators is a viable method to achieve this goal. However, their design and tuning is not an easy task. The performance –and even the stability– of harmonic current regulators strongly depends on implementation issues, with the tuning of the controller gains being critical. Furthermore, the presence of multiple current regulators working in parallel can create unwanted couplings with the fundamental current regulator, which can result in a deterioration of APF current control, i.e., oscillations and settling times larger than expected. This paper addresses the design and tuning of selective harmonic compensators, with a focus on their stability analysis and transient behavior.

Index terms – Active filters, current control, selective harmonic compensation, digital control, resonant controllers

I. INTRODUCTION

Shunt active power filters (APF) are power electronic devices designed for the compensation of harmonic current from non-linear loads, which also have the capability of compensating reactive power and unbalanced loads, see Fig. 1 [1–12,14–17]. The current controller is a critical component of these APF's with the choice available of regulating either the line currents [1], Fig. 1 and the block diagram shown in Fig. 2a, or the active filter currents, the block diagram shown in Fig. 2b [1,5,8]. The first option has the advantage that only the line current needs to be measured. The second option requires measurement of both the APF currents and the line currents, which are needed for determining the harmonics that need to be decoupled, but has the advantage of providing over-current protection for the APF. From a dynamic point of view both solutions are similar and the first one will be used in this paper [1].

A number of current control strategies for APF have been proposed, including hysteresis, linear (PI), sliding and deadbeat controllers [6,7]. These methods normally have significant limitations eliminating harmonics injected by non-linear loads. Selective harmonic compensation was developed to address these concerns and is a control strategy in which several (normally linear) harmonic current regulators work in parallel, each canceling a specific harmonic injected by the load [6–12,14–17]. An appealing property of these methods is that they can totally cancel the harmonics included in their design, including the ability to dynamically select the harmonics to compensate when the magnitude of the harmonic currents surpass the APF's capability.

Concerns for the implementation of harmonic current regulators include their computational requirements, tuning, and circuit configuration. While the first one is becoming less important thanks to fast and relatively cheap digital signal processors, selection of the gains for the controllers, as well as circuit configuration options, to guarantee stable operation and adequate dynamic performance is a challenge.
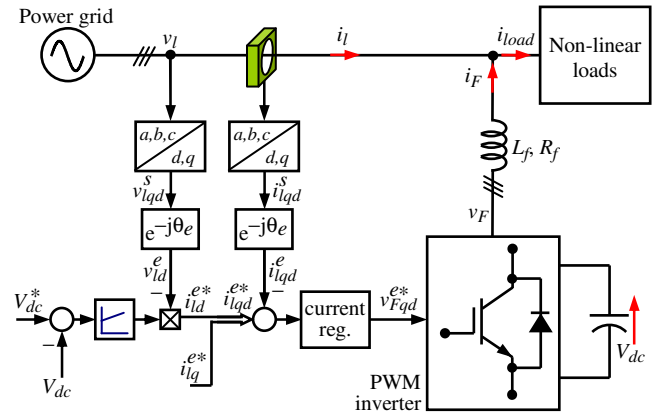

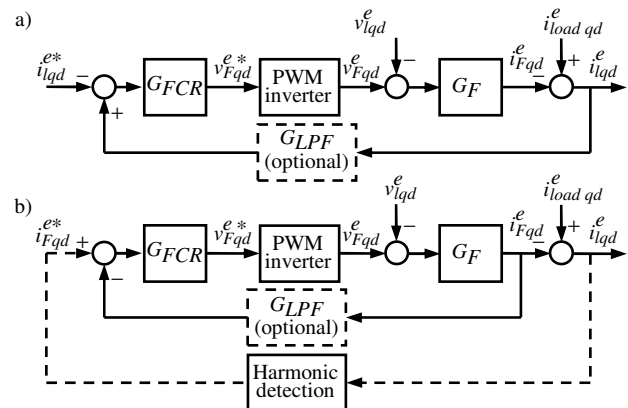Fig. 1.- Block diagram of a parallel APF, including line current and DC bus voltage control.

Fig. 2.- Schematic representation of the APF *qd* current control shown in a synchronous reference frame (outer dc-link voltage control not shown). a) line current is regulated, b) active filter current is regulated. G_{FCR} stands for fundamental current regulator transfer function, G_F for the inductive filter transfer function and G_{LPF} for the (optional) low-pass filter in the current feedback.
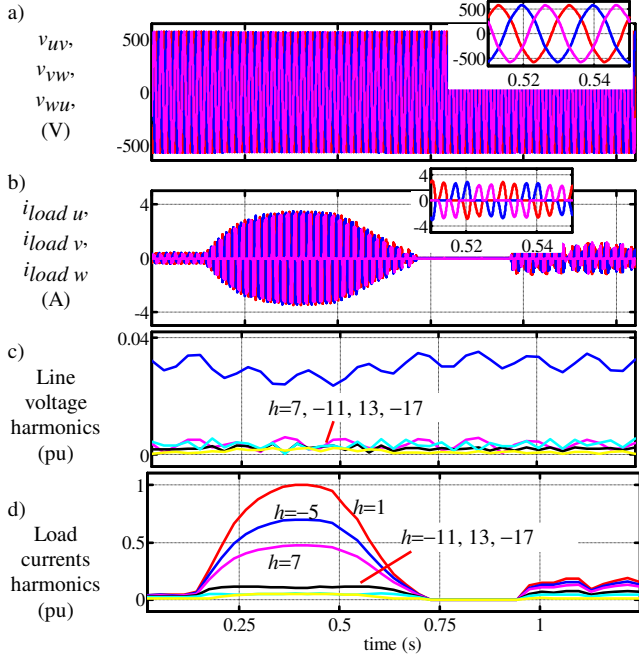
Fig. 3.- Current drawn by an electric drive during an acceleration transient. The drive was connected to the line through a diode rectifier. a) line voltages, b) diode rectifier (load) phase currents, c) harmonic content of the line voltage, in pu of the fundamental component (h=1), d) harmonic content of the load current, in pu of the maximum value of the fundamental component: h=1

This paper analyzes the design, tuning and implementation of harmonic current regulators. Continuous models will be developed first for this analysis, since they make it easier to present the concepts involved. The effects due to a digital implementation of the harmonic current regulators will then be presented, with the goal of maintaining the stability and performance of the resulting discrete current regulators.

II. PARALLEL ACTIVE POWER FILTER CONTROL

An example block diagram of an APF is shown in Fig. 1. The line current references are generated from an outer dc-link voltage control loop and the supply line voltages. These current references are the *ideal line currents*, free of any high frequency harmonics demanded by the load and with the ability to provide any desired power factor, up to the limits of the APF. Fig. 2a shows the schematic representation of the APF current control in a reference frame synchronous with the line voltage vector. It can be noticed from Fig. 2a that the plant dynamics included in this model represent the dynamic characteristics of the APF output filter. An inductive filter, modeled as an *RL* load, is used for these purposes in Fig. 1 [3,5,7-11, 15], with the corresponding transfer function being (1). It should be noted, however, that other options, like an *LCL* filter, can also be used with the appropriate changes in the plant model (1).

$$G_F = \frac{i_{Fqd}^e}{v_{Fqd}^e - v_{lqd}^e} = \frac{1}{L_f(s+j\omega_e)+R_f} \qquad (1)$$

A.- Current harmonics due to non-linear loads

The line voltages and load currents are disturbances to the system. In a synchronous reference frame, the fundamental line voltage becomes a dc quantity and is, therefore, easily compensated by a synchronous frame current regulator. On the other hand, some loads, e.g., diode rectifiers, create currents with a large content of high frequency harmonics. Compensation of the load currents is therefore a much more challenging task.

The current harmonics created by non-linear loads typically have orders of h=−5, 7, −11, 13, … in the stationary reference frame, with h=1 corresponding to the fundamental frequency, ω_e. These harmonics become h=±6, ±12, ±18 … , when transformed to the synchronous reference frame [7,8]. Fig. 3 shows the experimentally measured currents drawn by an electric drive from the line during an acceleration transient, as well as the line voltage. Fig. 3c shows the variation over the time of the harmonics in the line voltage, while Fig. 3d shows the harmonics created by the load, both calculated using the Short-time Fourier Transform. It can be observed from the figure that the harmonics in the currents can change relatively quickly, reaching noticeably large values (relative to the fundamental current). The line voltage harmonics, on the other hand, show minimal change due to the transient currents created by the electric drive during its acceleration. The APF current regulator, therefore, needs to be able to cancel current harmonics that can be at frequencies relatively large compared to the fundamental frequency and has to provide good dynamic response, since these harmonics can change relatively fast.

B.- Synchronous frame PI current regulators

Synchronous frame PI current regulators have been widely used for the control of three-phase power converters [13]. The transfer function of a synchronous reference frame PI current regulator implemented in the synchronous reference frame is shown in (2). A pole-zero notation will be used throughout the paper, with the notation using the proportional K_p and integral K_i gain being indicated in (2).

$$G_{FCR} = \frac{v_{qd}^{e*}}{e_{qd}^e} = K_p \frac{(s + 1/T_i)}{s} = K_p + \frac{K_i}{s} \quad ; \quad K_i = \frac{K_p}{T_i} \quad (2)$$

To evaluate and compare the performance of different current regulators designs, it is useful to use the command tracking, i.e., output−to−reference, (3), and the disturbance rejection, i.e. output−to−disturbance, (4), transfer functions, shown in a synchronous reference frame, with G_{FCR} standing for the

$$\frac{i_{L\_qd}^e}{i_{L\_qd}^{e*}} = \frac{G_{FCR}\,G_F}{1+G_{FCR}\,G_F\,G_{LPF}} \qquad (3)$$

$$\frac{i_{L\_qd}^e}{i_{load\_qd}^e} = \frac{1}{1 + G_{FCR}\,G_F\,G_{LPF}} \qquad (4)$$
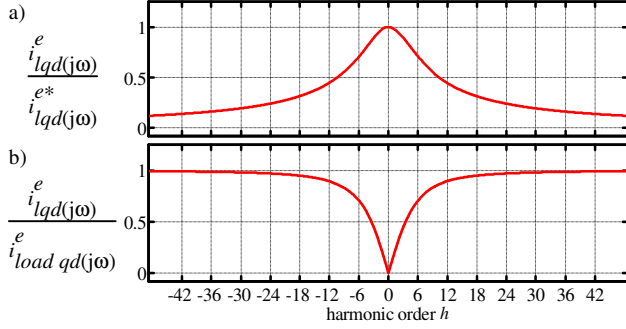
Fig. 4.- Frequency response function (FRF) magnitude, shown in a synchronous reference frame, of the synchronous reference frame PI current regulator. The line frequency is $\omega_e = 50$ Hz, the harmonic order h being used for the frequency axis. The current regulator was tuned for a 400 Hz bandwidth ($8 \cdot \omega_e$) with no low-pass filter. a) Command tracking FRF (eq. (3)), and b) Disturbance rejection FRF (eq. (4)).
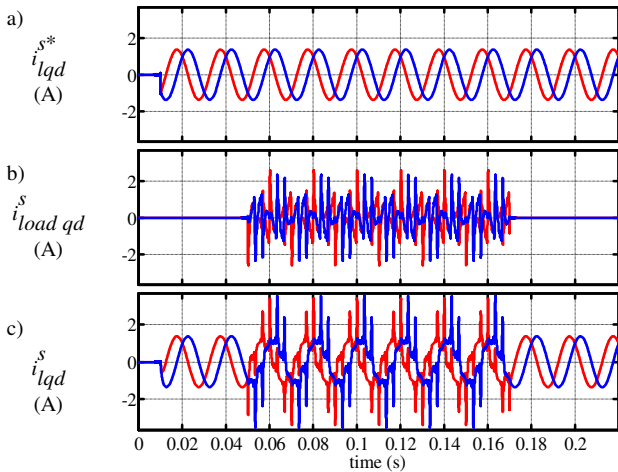

Fig. 5.- Time response of an APF with a synchronous reference frame PI current regulator (simulated): a) line-current command, b) load current, consisting of harmonics $h=\pm6$, ±12, ±18, ±24 and ±30, c) actual line current. All the currents are shown in the stationary reference frame.

fundamental current regulator transfer function in a synchronous reference frame (2), G_F (1) being the APF inductive filter transfer function and G_{LPF} being the transfer function of the low-pass filter in the current feed-back, which can be optional depending on the current measurement strategy.

A convenient way to analyze the performance of APF is through the use of frequency response function (FRF) analysis. Since the APF variables are modeled using complex vector quantities, which can rotate both forward and backwards, both positive as well as negative frequencies need to be considered for the transformation $s=j\omega$. Fig. 4-a and 4-b show the magnitude of the resulting FRF for (3) and (4), respectively. The current regulator was tuned to achieve pole/zero cancellation with a bandwidth of 400 Hz. The gains of the controller being $T_i = L_f / R_f$ and $K_p = 400 \, 2 \, \pi \, L_f$.

It can be observed from Fig. 4-a that the FRF has a gain equal to one at 0 frequency, i.e., dc, which means they APF will have zero error in the steady-state. As for the disturbance rejection capability, current harmonics injected by non-linear
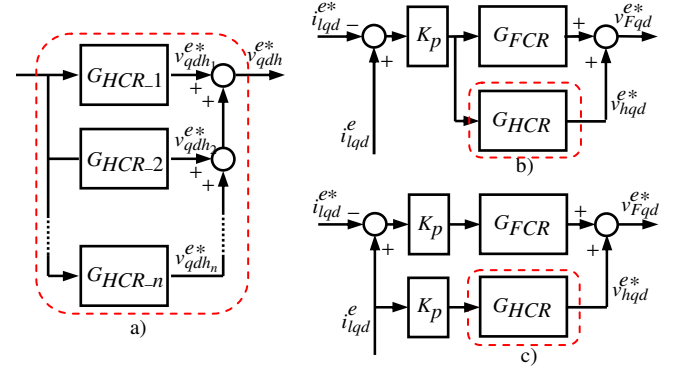

Fig. 6.- a) Harmonic current regulator consisting of n parallel-connected regulators, b) current regulator consisting of a fundamental current regulator G_{FCR} and a harmonic current regulator G_{HCR} with the input to both current regulators being the current error, c) current regulator consisting of a fundamental current regulator and a harmonic current regulator with the input to the harmonic current regulator being the measured current.

loads will have typically orders of $h=\pm6$, ±12, ±18, ... , in the synchronous reference frame [7,8]. Complete elimination of the harmonics injected by the load would require a gain equal to zero in (4) at the frequencies corresponding to those harmonics. It can be observed from Fig. 4-b that synchronous reference frame PI current regulator provides perfect disturbance rejection at 0 frequency, i.e., the fundamental frequency but the disturbance rejection capability decreases rapidly as the frequency (harmonic order) increases. Fig. 5 shows an example of the simulated time response of this current regulator. For this simulation, a constant line current reference consisting of a single component at a frequency ω_e was commanded at t=0.01 s, Fig. 5-a, and a non-linear load is connected between t=0.05 s and t=0.15 s, Fig. 5-b. From this figure, both its capability to follow without significant error the current command, (when the load does not create harmonics the line current in Fig. 5-c perfectly matches the reference of Fig. 5-a), as well as the impact of the current harmonics created by the load (when harmonics created by the load are present there is a noticeable difference between the commanded and the actual line current).

III. HARMONICS CURRENT REGULATOR FOR ACTIVE POWER FILTERS

The principles of synchronous reference frame current regulators can be extended for the cancellation of harmonics created by non-linear loads through the use of *harmonic current regulators*. In this concept, several current regulators, each designed to cancel a specific harmonic, are connected in parallel, Fig. 6a. Several different design approaches for the selective harmonic current regulators have been proposed [6-15] and will be discussed in the following sub-sections.

A.- Harmonic synchronous current regulators design

While all harmonic synchronous current regulators designs place a pole on the imaginary axis at the frequency to be cancelled, different options have been proposed for the selection of the regulator's zero placement. The zero can be

tuned to have the same imaginary component as the pole at a distance $1/T_{ih}$ from the imaginary axis, with (5) being obtained (see Fig .7a-top). A pure integrator can also be used (6), (Fig. 7b top) [8, 15]. Finally, if the zero is placed on the real axis in the fundamental frequency reference frame, (7) is obtained (Fig. 7c top) [8, 15]. It should be noted that the gain K_{ph} in (5)-(7) is normalized by dividing by the gain of the fundamental current controller K_p. This was done for convenience in the root locus analysis presented later in the paper.

$$G_{HCR\_h+} = \frac{v^{e*}_{qd\_h+}}{e^e_{qd}} = \frac{K_{ph}}{K_p} \frac{(s + 1/T_{ih} - j\, h\, \omega_e)}{s - j\, h\, \omega_e} \quad (5)$$

$$G_{HCR\_h+} = \frac{v^{e*}_{qd\_h+}}{e^e_{qd}} = \frac{K_{ph}}{K_p} \frac{1/T_{ih}}{s - j\, h\, \omega_e} \quad (6)$$

$$G_{HCR\_h+} = \frac{v^{e*}_{qd\_h+}}{e^e_{qd}} = \frac{K_{ph}}{K_p} \frac{(s + 1/T_{ih})}{s - j\, h\, \omega_e} \quad (7)$$

As already mentioned, non-linear loads typically create harmonics of order $h=\pm6$, ±12, ±18, ... in a synchronous reference frame, [7,8]. Implementing the current regulators in a fundamental synchronous reference frame has the advantage of allowing simultaneous cancellation of positive and negative sequence harmonics, i.e., $\pm h$, with a single regulator (Fig. 6-a). Eq. (8)-(10) show the regulators that result from (5)-(7) when simultaneous cancellation of the positive and negative sequence components is implemented, with the corresponding pole-zero mapping being shown in the subplots at the bottom of Fig. 7.

$$G_{HCR\_h} = \frac{v^{e*}_{qd\_h}}{e^e_{qd}} = 2 \frac{K_{ph}}{K_p} \frac{(s^2 + 1/T_{ih}\, s + (h\, \omega_e)^2)}{s^2 + (h\, \omega_e)^2} \quad (8)$$

$$G_{HCR\_h} = \frac{v^{e*}_{qd\_h}}{e^e_{qd}} = 2 \frac{K_{ph}}{K_p} \frac{(1/T_{ih}\, s)}{s^2 + (h\, \omega_e)^2} \quad (9)$$

$$G_{HCR\_h} = \frac{v^{e*}_{qd\_h}}{e^e_{qd}} = 2 \frac{K_{ph}}{K_p} \frac{(s^2 + 1/T_{ih}\, s)}{s^2 + (h\, \omega_e)^2} \quad (10)$$

While all the three designs shown in Fig. 7 have the same harmonic rejection capability in the steady-state, differences exist in their transient response due to the different zero placement [8, 15]. Due to space restrictions, the analysis presented in this paper will be limited to the design in Fig. 7a but the following results were found as part of this research. The design in Fig. 7-c was found to have similar dynamics response to the design in Fig. 7-a, while the design in Fig. 7b showed slower dynamic response.

Positive sequence harmonic regulators

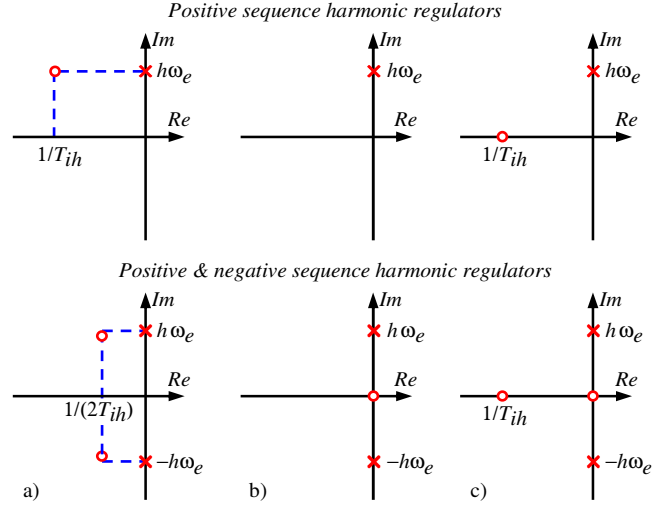*Positive & negative sequence harmonic regulators*

Fig. 7.- Pole-zero configurations for the harmonic current regulators, shown in a fundamental frequency synchronous reference frame
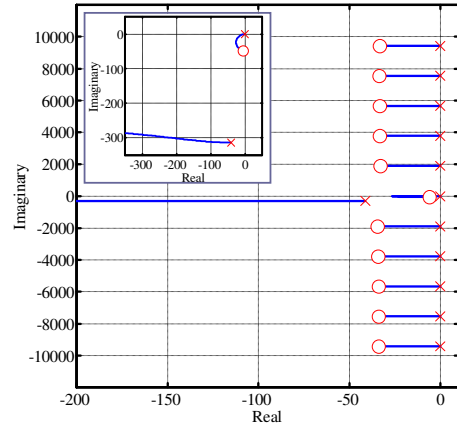

Fig. 8.- Root locus, shown in a synchronous reference frame, when the harmonic current regulator G_{HCR} is fed by the current error (Fig. 6b). G_{HCR} consisting of five regulators to compensate harmonics ±6 to ±30 ($\pm300\ 2\pi$ rad·s^{-1} to $\pm1800\ 2\pi$ rad·s^{-1}). It should be noted that the real and imaginary axis are scaled differently.
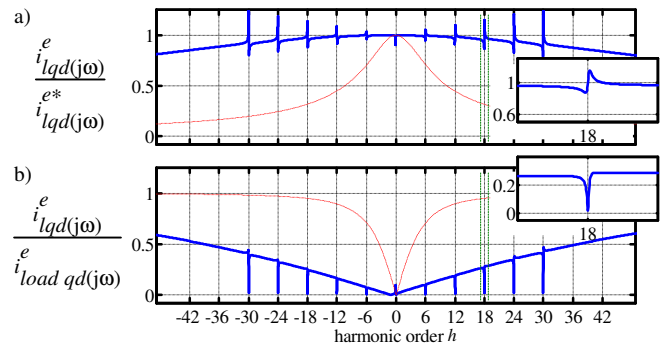

Fig. 9.- FRF shown in a synchronous reference frame, when the harmonic current regulator G_{HCR} is fed by the current error, Fig. 6-b. The rest of conditions are as described in Fig. 8. The dashed line corresponds to the FRF for thee case of only a PI current regulator being used shown in Fig. 4.
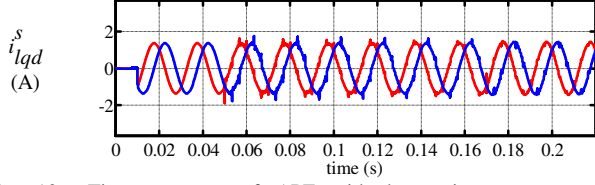
Fig. 10.- Time response of APF with harmonic current regulators (simulated): line current response to the current command and load current shown in Fig. 5 a and b. respectively, when the harmonic current regulator G_{HCR} is fed by the current error (Fig. 6b). The rest of conditions are as described in Fig. 9.

The command tracking and disturbance rejection transfer functions when the fundamental current regulator and the harmonic current regulator are combined (Fig. 6b) are (11) and (12), respectively.

$$\frac{i^e_{l\_qd}}{i^{e*}_{l\_qd}} = \frac{(G_{FCR}+G_{HCR})\,G_F}{1+(G_{FCR}+G_{HCR})\,G_F\,G_{LPF}} \tag{11}$$

$$\frac{i^e_{l\_qd}}{i^e_{load\_qd}} = \frac{1}{1+(G_{FCR}+G_{HCR})\,G_F\,G_{LPF}} \tag{12}$$

Fig. 8 shows the root locus of (11) as a function of K_p, with the pole-zero pairs due to the harmonic current regulators being readily observable. The root locus will be used later for the analysis of the discrete form of the harmonic current regulators. Fig. 9-a and 9-b show the command tracking and disturbance rejection FRF's for this controller. It can be observed from Fig. 9-b that it fully rejects each of the harmonics included in its design (gain equal to zero). It can also be observed from Fig. 9-a that including the harmonic current regulator results in a modification of the command tracking FRF compared to the PI current regulator case (3), with a significant increase of the magnitude at frequencies different from dc. Fig. 10 shows the simulated time response of this current regulator. It can be observed that a dramatic improvement in the cancellation of the distortion introduced by the load current is achieved when compared to the case of no harmonic current regulator shown in Fig. 5.

B.- Harmonic current regulator using synchronous PI current controllers placed in the feedback path

Since the harmonic current regulators are mainly intended for disturbance rejection, they could be placed in the feedback path, Fig. 6-c. The resulting command tracking transfer function for this controller is (13), with the corresponding FRF being shown in Fig. 11-a.

$$\frac{i^e_{l\_qd}}{i^{e*}_{l\_qd}} = \frac{G_{FCR}\,G_F}{1+(G_{FCR}+G_{HCR})\,G_F\,G_{LPF}} \tag{13}$$

It can be observed from this figure that this controller has a dc gain equal to one, and therefore no error regulating the fundamental current. However, a noticeable decrease of the
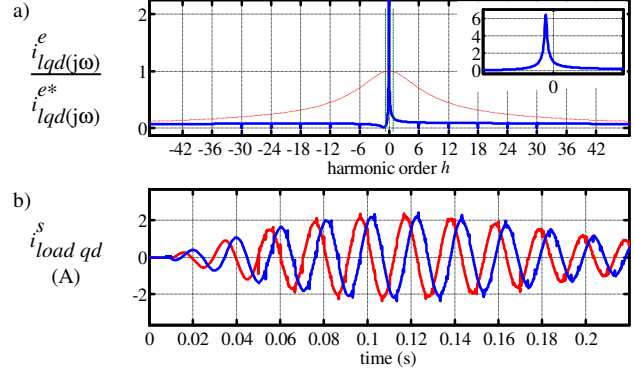

Fig. 11.- a) Command tracking FRF shown in a synchronous reference frame, when the harmonic current regulator G_{HCR} is fed by the measured line current (Fig. 6c). b) Time response of APF with harmonic current regulators (simulated): line current response to the current command and load current shown in Fig. 5-a and -b respectively (Fig. 6c). The rest of conditions are as described in Fig. 9.
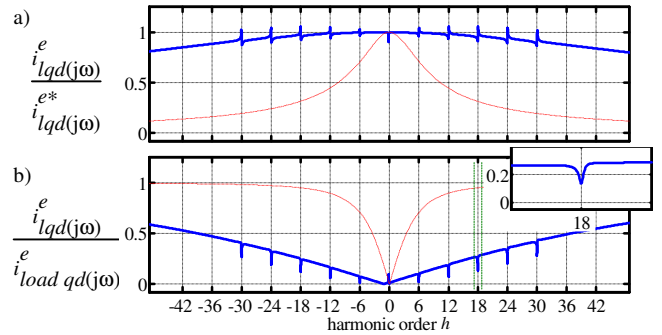

Fig. 12.- Frequency response function (FRF) shown in a synchronous reference frame, when the controllers forming the harmonic current regulator G_{HCR} include damping. The rest of conditions are as described in Fig. 9.

FRF gain at frequencies near dc can be observed, resulting a serious deterioration of its command-tracking characteristics due to the poles of G_{HCR} being placed in the feedback path. The disturbance rejection is the same as for the design in Fig. 6b, i.e., (12), Fig. 9-b. Fig. 11-b shows the time response for this controller. As expected, this configuration rejects the harmonics injected by the load but has poor command tracking properties, which would severely limits it use.

C.- Harmonic current regulator using synchronous reference frame PI current regulators with damping

To alleviate stability concerns seen during the digital implementation of harmonic current regulators, harmonic current regulators with damping were developed [10-12]. The transfer function in the continuous domain is shown in (14), where a new term has been added to the denominator that is tuned through the selection of the quality factor, Q.

$$G_{HCR\_h} = 2\cdot K_{ph}\,\frac{(s^2 + 1/T_{ih}\,s + (h\,\omega_e)^2)}{s^2 + (h\,\omega_e/Q)\,s + (h\,\omega_e)^2} \tag{14}$$

The corresponding FRF's are obtained substituting (14) in (11) and (12) and are shown in Fig. 12. The new term added in the denominator of the current regulator transfer function moves the poles from the imaginary axis towards the left (stable) half of the "*s*" plane, Fig. 8. This results in a more

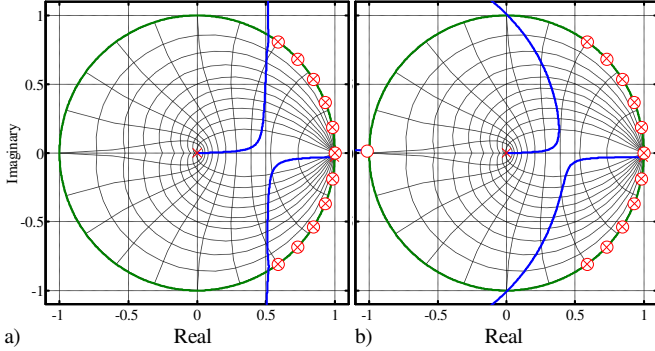well damped system, but at the price of not fully cancelling harmonics created by the load, Fig. 12-b.

a)   Real   b)   Real

Fig. 13.- Root locus current control using harmonic current regulator. Sampling period T=0.1ms. a) sampling delay of T and b) sampling delay T/2 (synchronous sampling), no LPF in the current feedback, harmonics decoupled h=±6, ±12, ±18, ±24 and ±30. (zooms in next figure).

IV. DISCRETE IMPLEMENTATION OF THE HARMONIC CURRENT REGULATOR

All the discussion and analysis presented in the previous section was for the continuous time domain, this section analyzes the issues that are relevant to the digital implementation of harmonic current regulators, and provides a criteria for the selection of the harmonic current regulator gains in the discrete domain.

A.- Discretization methods

Harmonic current regulators are designed to accurately control specific, well defined frequencies. It is therefore mandatory to use discretization methods that exactly match the frequencies interest from the continuous to the discrete domain. Detailed discussion on the principles and performance of discretization methods can be found in [14], the Tustin transform with pre-warping, will be used in this paper.

B.- Current measurement and sampling

Current measurement and sampling is critical for the implementation of harmonic current controllers due to the relatively high frequency of the harmonics being compensated. The current feedback path in a digital current regulator consists of a sensor, an optional low-pass filter, Fig. 2, and a sampling & A/D conversion device that introduces a delay in the control [10]. The current sensors normally have bandwidths greater than tens of kHz and, therefore, have reduced impact. Different configurations for the LPF and sampling are discussed in the next subsection.

C.- Analysis of discretized harmonic current regulators

This section analyzes the discrete harmonic regulators that result from the discretization of the continuous designs from Section III. The Tustin transform with pre-warping was used in all the cases, with a sampling period of T=0.1 ms (except when stated otherwise), which coincides with the switching period of the experimental setup. In the analysis presented in this section only the gains K_p and K_{ph} are initially changed, with $K_p = K_{ph}$. The rest of gains of the fundamental and harmonic current regulators are kept constant, with $T_i = L_f / R_f$ implemented for pole-zero

cancellation, $T_{ih} = T_i/5$ and K_{ph}/K_p=1, (8). The effects of changes in these gains are studied by the end of this section.
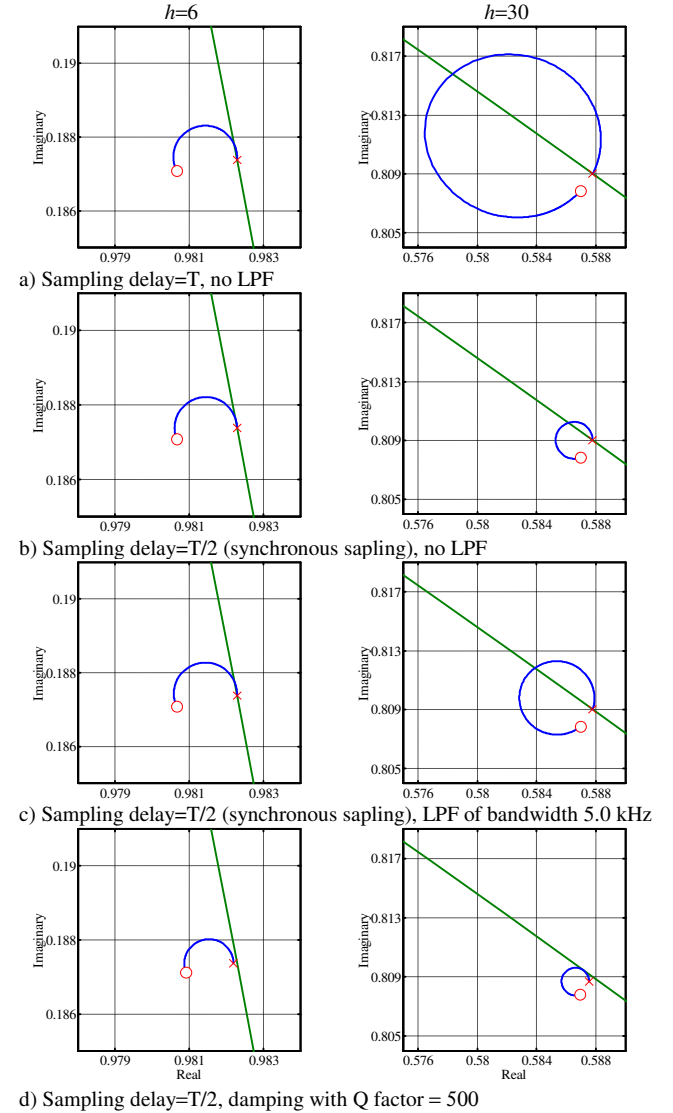

a) Sampling delay=T, no LPF

b) Sampling delay=T/2 (synchronous sapling), no LPF

c) Sampling delay=T/2 (synchronous sapling), LPF of bandwidth 5.0 kHz

d) Sampling delay=T/2, damping with Q factor = 500

Fig. 14.- Zoom of the branches of the root locus corresponding to harmonics h=6 (left) and h=30 (right), for three different configurations of the harmonics current regulator.

Fig. 13-a shows the root locus of the resulting digital implementation of the controller presented in Sub-Section III-A, with the corresponding continuous root locus shown in Fig. 8. The currents were sampled at the beginning of the switching period, resulting in a delay of one switching period T before the voltage command is updated. The pole-zero pairs lying on the imaginary axis in the Fig. 8 are seen to lie on the unit circle in Fig. 13-a. Fig. 14-a shows a zoom of the branches in Fig. 13-a corresponding to the harmonics h=6 and h=30, respectively.

Some facts can be observed form Fig. 13-a and 14-a. A significant portion of the branch corresponding to h=30 lies outside the unit circle, meaning that the system will be unstable for small values of K_p. On the other hand, it can be observed from Fig. 13-a that, for large values of K_p, there are
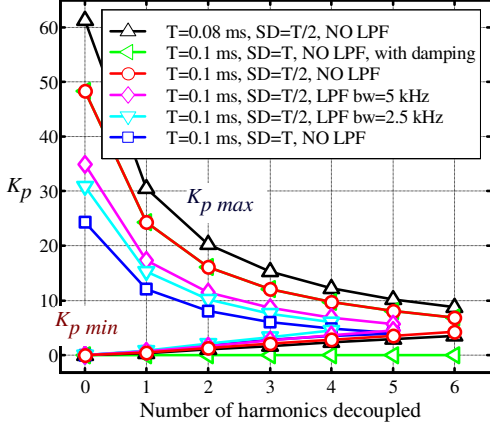
Fig. 15.- Stability limits for gain K_p vs. the number of harmonics pairs being decoupled (1→h=±6; 2→h=±6, ±12; …; 2→ h=±6 to ±36;) for different configurations of the harmonic current regulator: T stands for sampling period, which is equal to the switching period, SD stands for sampling delay (T/2 corresponds to synchronous sampling, T for a complete sampling period delay), and LPF for the low-pass filter in the current measurement. In all the cases, the harmonics current regulators were discretized using Tustin with prewarping, and $K_{ph}=K_p$.

two branches that lie outside of the unit circle. It can be concluded, therefore, that there is a limited range of gains $K_{pmin}<K_p<K_{pmax}$ for which the harmonic current regulator is stable. Fig. 15 (■) shows the values of K_{pmin} and K_{pmax} that provide stable operation as a function of the number of harmonics being compensated. It can be observed from the figure the range of gains for K_p that provide stable operation reduces as the number of harmonics being compensated increases, with this reducing practically to zero, i.e., $K_{pmin} ≈K_{pmax}$, for the case when 5 harmonics are included in the current regulator design. This limits the number of harmonics that can be compensated to 4.

Fig. 13-b and 14-b show the root locus when the sampling delay is reduced from T to T/2 by sampling the currents in the middle of the switching period. Although only slight differences are observed between the root locus in Fig. 13-b and Fig. 13-a, noticeable differences exist when the trajectory of the branch corresponding to h=30 is zoomed in Fig. 14b, which shows a significantly increased range of values of K_p that provide stable operation. The benefits of reducing the sampling delay can also be seen in Fig. 15 (●) through the increased range of K_p values that allow stable operation, including compensation up to the 6th harmonic.

In the two cases discussed so far, there was no low-pass filter in the current feedback. The effects of a low-pass filter can be observed from the root locus in Fig. 14-c. The filter can be seen to have an effect similar to the delay analyzed in Fig. 14-a, due to the filter's lag characteristic. Fig. 15 shows the range of gains that provide stable operation for the case of two different bandwidths for the low-pass filter, 2.5 kHz (▼) and 5 kHz (◆). It can be noticed from this figure that a low-pass filter with a bandwidth as high as 5 kHz (half of the switching frequency) has a visible impact on the stability limits of the harmonic current regulator.
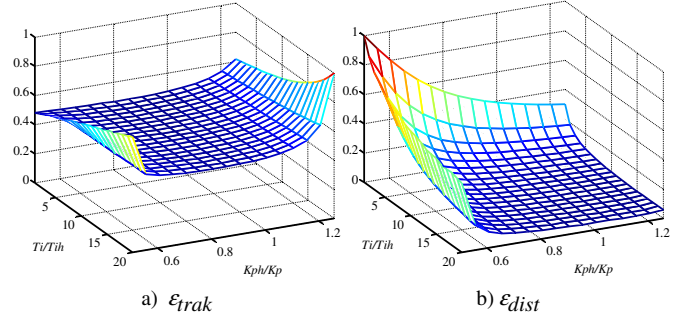

Fig. 16.- Simulation results. a) command tracking and b) disturbance rejection errors as a function of T_{ih}.and K_{ph}.gains, for the case of a harmonic current regulator using resonant controllers (8) to compensate for harmonics h=±6 up to h=±30, with a sampling delay of T/2 and no low-pass filter. The fundamental current regulator gains K_p and T_i were tuned for pole-zero cancellation and a bandwidth of 400 Hz.

Fig. 14-d shows the branches corresponding to the harmonics h=6 and h=30 for the case of the harmonic regulator with damping described in Section III-C. The effects of using damping are evident in the branch for the case of h=30, which always lies within the unit circle, meaning that there is no risk of instability due to the gains being too small. The range of values of K_p that allow stable operation being shown in Fig. 15 (◄).

Finally, the range of gains that allow stable operation, and consequently, the number of harmonics that can be compensated, can be increased by decreasing the sampling period T. Fig. 15 (▲) shows an example of the improvement that is obtained when T is reduced from 1 to 0.08 ms (the switching frequency increases from 10 to 12.5 kHz). It should be noted, however, that increasing the switching frequency can have important implications on the inverter losses, as well as on the inductive filter design, that need to be carefully considered.

E.- Delay compensation

It has already been shown in the previous sections that the delay intrinsic to the digital implementation of the current controllers has an adverse impact on their performance. The importance of this effect becomes more relevant as the regulator harmonic order increases, and also depends on the current regulator design [8] and discretization method [14], which eventually depends of the placement of the zeros of the discrete current regulator.

Delay compensation has been widely analyzed in the literature, and is not addressed in this paper. Proposed methods include advancing the angle of the current regulator output voltage [17], as well as, modifications to the discrete current regulator [14,16]. Selection of the exact delay amount to compensate is often made *ad hoc,* e.g., two sampling periods compensation is recommended in [16] and [17], however, no clear criteria for this selection is given. It should finally be noted that compensation methods normally assume steady-state operation, where it is possible to calculate the phase shift that the delay will produce for each harmonic. However, effectiveness of the compensation will be reduced

during transients [16].

F.-Harmonic current regulator gain selection

In the previous analysis, the controller's gains T_{ih}, T_i and K_{ph} were either kept constant or had a fixed relationship to K_p, which was varied for the controller tuning. The influence of changes in these parameters on the performance of the harmonic current regulators is discussed in this subsection.

The integral time constant of the fundamental current regulator, T_i, is often selected to cancel the inductive filter dynamics (or near that value), with the proportional gain, K_p, selected to obtain the desired closed-loop bandwidth. Using these criteria, the gains, K_{ph} and T_{ih}, of the harmonic current regulators still need to be selected. Given the high order of the resulting transfers functions involved, it is not possible to obtain metrics for the dynamic response (settling time, overshoot, …) from analytical solutions. Numerical evaluations were used instead. Two metrics were defined to evaluate the dynamic performance of the command tracking and disturbance rejection, (15) and (16). In these equations, it was assumed that the system was excited at $t=0$, with Δt being a time large enough so that the line current has reached steady-state in all the cases.

The metric ε_{track} integrates over a time Δt the difference between the response to changes in the fundamental current of the harmonic current regulator (11) minus the ideal response (3), i.e., the line current for the case that no harmonic current regulator is present. This metric measures the impact that the harmonics current regulator has on the command tracking properties of the APF. The metric ε_{dist} integrates the line current over a time Δt, after the load starts creating harmonics at $t=0$.

$$\varepsilon_{trak} = \frac{1}{\Delta t} \int_0^{\Delta t} \sqrt{(i_{lqds} - i_{lqds\ ideal})^2}\ \mathrm{d}t \quad (15)$$

$$\varepsilon_{dist} = \frac{1}{\Delta t} \int_0^{\Delta t} \sqrt{i_{lqds}^2}\ \mathrm{d}t \quad (16)$$

Fig. 16 shows ε_{trak} and ε_{dist} as a function of gains K_{ph} and T_{ih}. Both metrics were normalized by dividing by the largest value. The following conclusions can be reached form the figure.

- The gain T_{ih} has a small impact on the command tracking error (Fig. 16a and 17), but has a noticeable impact on the disturbance rejection capability. This suggests using smaller values of T_{ih}. (increase of T_i/T_{ih}). Values too small of T_{ih} can make the harmonic current regulator too sensitive to noise, values of $T_{ih} \approx T_h/5$ were found adequate.
- Values of K_{ph} close to K_p provide a good trade-off between command tracking and disturbance rejection errors. Increasing the value of K_{ph} improves the disturbance rejection capability, but at the price of an increased command tracking error and making the current regulator more sensitive to noise.

In all the previous analysis, the same gains, K_{ph} and T_{ih}, were used for each individual harmonic current regulator (8)–(10). It is also possible to use different gains for each harmonic being compensated. If this option is chosen, K_{ph} should increase proportionally to harmonic compensated, as higher harmonics require higher gains to get into the stable region of the z-plane. However, from the analysis carrier out, no relevant differences were observed using different K_{ph} and T_{ih} gains with respect to the case of using the same gains for all controllers.

V. EXPERIMENTAL RESULTS

This section presents experimental results for the analysis from this paper. The test bench uses 75 A IGBT's with a switching frequency of 10 kHz (T=0.1 ms) and a DC bus voltage of V_{dc}=700 V. An RL inductive filter was used, with L_f = 2.5 mH, R_f = 100 mΩ, and a maximum current of 30 A (rms). The APF is connected to a line voltage of 50 Hz, 400 V (rms line-line). The APF control was implemented on a TMS320F28335 DSP. Synchronous sampling was used, with a sampling delay of T/2. Due to noise problems, a first-order, low-pass filter, with a cut-off frequency of 2.5 kHz, was used. According to the analysis presented in this paper, harmonics $h=\pm6$, ±12, ±18 and ±24 could be compensated, Fig. 15.
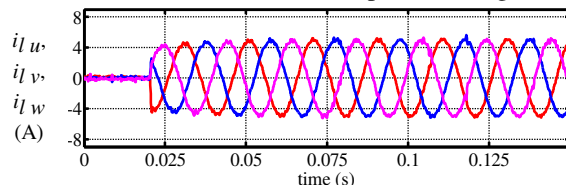

Fig. 17.- Command tracking response to a step un the q-axis line current commend. Harmonic current regulator consisting of $h=\pm6$, ±12, ±18 harmonics.
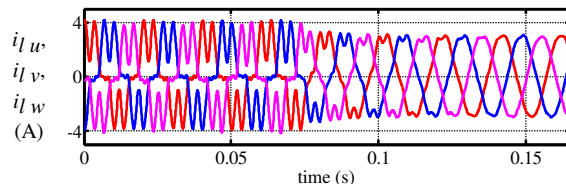

Fig. 18.- Line currents when the load is an uncontrolled rectifier, the harmonic current regulator being connected at $t=0.75$ s. Harmonic current regulator compensates for $h=\pm6$, ±12, ±18 and ±24 harmonics.
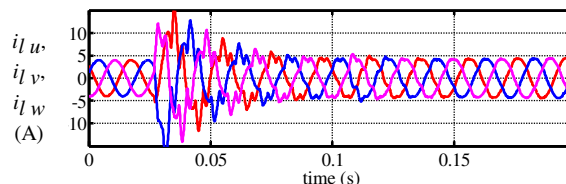

Fig. 19.- Line currents when the APF was active when an uncontrolled rectifier is connected at $t=0.3$. The harmonic current regulator is configured as described in Fig. 18.

The fundamental current was tuned for a 400 Hz bandwidth. The gains used for the harmonic current regulator were K_{ph}=0.7K_p and T_{ih}=T_i/5 (see Fig. 16).

Fig. 16 shows the command tracking response to step of 5 A in the q-axis (reactive current) line current command, with the harmonic current regulator consisting of four harmonic controllers at $h=\pm6$, ±12, ±18 and ±24. It can be observed

from the figure that the APF shows fast response with the system being perfectly stable.

Fig. 18 shows the disturbance rejection capability of the HCR when the load is an uncontrolled rectifier and the APF is connected. Stable operation and good dynamic behavior are observed, confirming the correctness of the gains tuning.

Finally, Fig. 19 shows the disturbance rejection capability of the HCR when it is active and an uncontrolled rectifier is connected to the line, the APF is seen to react the to the distortion restoring nearly sinusoidal line currents.

V. CONCLUSIONS

The design and tuning of harmonic current regulators for APF has been discussed in this paper. Harmonic current regulators are a good solution to perfectly cancel selected harmonics injected by non-linear loads. However, selection of the gains for the controllers, to guarantee stable operation and adequate dynamic performance is a challenge, being often made *ad hoc*. Furthermore, it can strongly depend on circuit configuration options.

Stability analysis of harmonic current regulators has been presented in this paper. From this analysis, the impact that different implementation issues like the sampling strategy, switching period and use of filters, has on the maximum number of harmonics that can be cancelled by the harmonic current regulator, as well as the range of gains that can be used to guarantee the stability of the system, have been established. Experimental results have been provided to support the analysis.

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