UNIVERSITY OF OVIEDO

DEPARTMENT OF ELECTRICAL, ELECTRONIC, COMPUTERS AND SYSTEMS ENGINEERING

PHD THESIS

OFF-LINE SUPPLY OF SOLID-STATE LAMPS. LAMP MODELLING, APPLICATION OF THE INTEGRATED BUCK-FLYBACK CONVERTER, AND PROPOSAL OF A NEW OPTIMISED DIMMING SCHEME

BY

DAVID GACIO VAQUERO

GIJÓN, APRIL 2013

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ALIMENTACIÓN DE LÁMPARAS DE ESTADO SÓLIDO DESDE LA RED ELÉCTRICA. MODELADO DE LÁMPARAS, ESTUDIO DEL CONVERTIDOR REDUCTOR/RETROCESO INTEGRADO Y OPTIMIZACIÓN DEL SISTEMA DE REGULACIÓN DE FLUJO LUMINOSO

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Abstract

This PhD Thesis entitled "Off-Line Supply of Solid-State Lamps. Lamp Modelling, Application of the Integrated Buck-Flyback Converter, and Proposal of a New Optimised Dimming Scheme" is developed as a part of the research activities of the Efficient Energy Conversion, Industrial Electronics and Lighting (EECIEL) group of the University of Oviedo.

Nowadays, LEDs are rising as the most promising light source due to their several advantages on efficiency and versatility. An example of flexibility is the dimming capability of LEDs, a highly interesting feature nowadays in order to reduce the luminous output of an LED lamp to meet the actual luminance requirements, leading to further energy savings. Unfortunately, LED lighting is not exempt of challenges. Some of these challenges are a proper supply of a non-linear load with a high-efficient, low-cost LED driver, or the implementation of a highly dimmable scheme, among others.

This work is focused on the three main areas of research in LED lighting. First, the LED lamp itself is studied regarding its behaviour as a power load, as well as the different lamp configurations that the use of LEDs allows; the LED driver is also a topic of research, where the feasibility and suitability of the Integrated Buck-Flyback Converter, which has already been successfully developed for other applications, is analysed, and the improvement in performance for LED applications is evaluated; and finally, the dimming operation is also covered, exploring the possibilities for dimming integrated single-stage converters such as the Integrated Buck-Flyback Converter proposed in this work.

The main objectives of this PhD work are listed below:

- Study of the static and dynamic characteristics of commercially-available LED diodes as a function of the junction temperature. For this purpose, both single LEDs and LED lamps with power consumption greater than 25 W, entirely built with single devices, will be considered provided that these lamps are valid for general indoor/outdoor lighting, commercial lighting, street lighting, architectural lighting, etc.
- Study on the optimisation of the LED as a power load regarding the different connection strategies possible: single string of series-devices or paralleled strings.
- Study on the possibilities that the Integrated Buck-Flyback converter provides for the aforementioned LED lamps supply from the AC mains. Thus, Power Factor Correction will be mandatory in order to comply with IEC 61000-3-2 Class C requirements.
- Study of the Integrated Buck-Flyback Converter operation considering two solutions: i) either both inductors in Discontinuous Conduction Mode, or ii) with the flyback converter in Continuous Conduction Mode. The advantages of one solution over the other will be evaluated.
- Study of the feasibility of the Integrated Buck-Flyback converter life-span enhancement by the substitution of the electrolytic-based bus capacitor with an MKP-based device.
- Study and review of the different dimming schemes, either analogue (AM) dimming, Pulse-Width Modulation (PWM) dimming, or other techniques present in scientific literature.
- Research and implementation of the PWM dimming technique best suited to the dynamic characteristics of Integrated Single-Stage Converter supplied from the AC mains and featuring Power Factor Correction.

This PhD work is structured as detailed below:

In **Chapter 1**, a brief introduction to lighting is given. Afterwards, the most common light sources are listed and briefly explained. Light-Emitting Diodes are introduced and thoroughly described. Then, the most important issues about LED lighting will be discussed, paying special attention to their characteristics as a power load, which greatly differs from that of incandescent or gas-discharge lamps. The dimming methods will also be covered prior to introducing the commercially-available LEDs and the selected devices.

In **Chapter 2**, the thermal characterisation of LEDs is dealt with, both 1 W single emitters and 60 – 70 W LED lamps. First, a statistical study on the forward voltage of LEDs is conducted in order to determine the typical values and standard deviation for a generic design. Then, the parasitic effects of LEDs are discussed prior to addressing the *I-V* curve thermal characterisation that allows the junction temperature to be estimated. Afterwards, the dynamic-resistance thermal dependence is studied and determined in order to obtain a complete large- and small-signal model of LED lamps as a function of junction temperature. Finally, the implications of the *I-V* curve thermal dependence on the performance of LED drivers are studied, including an illustrative example.

In **Chapter 3**, the performance of Discontinuous Conduction Mode Power Factor Pre-regulators is deeply studied regarding IEC 61000-3-2 Class C regulations compliance. Thus, Power Factor Correction is firstly introduced with the Class C harmonic-content requirements, and then, passive and active techniques for harmonic content reduction and/or Power Factor Correction are listed and described. Afterwards, two types of active Power Factor Pre-regulators are considered: i) those featuring sinusoidal input current – *Ideal PFC stages*, and ii) those featuring non-sinusoidal input current – *Quasi-PFC stages*. Finally a review on the most common structures according to the number of cascaded stages is included prior to comparing the performance of Ideal PFC and Quasi-PFC stages.

In **Chapter 4**, the operation of the Integrated Buck-Flyback converter is discussed. This study considers the operation of both converters cascaded, and the advantages over other topologies are highlighted. Afterwards, the derivation of the Integrated Buck-Flyback Converter is explained from the integration technique present in the literature. The operation of both inductors in DCM or the buck-inductor in DCM and the flyback inductor in CCM is also studied, discussing and comparing the benefits of each operation mode through the ripple-gain factor. Finally, the operation of the Integrated Buck-Flyback converter as an LED driver is covered prior to presenting the design example of a universal input-voltage range LED driver supplying a 70 W LED lamp for street lighting applications.

In **Chapter 5**, the large- and small-signal models are derived. Regarding the large-signal model, both the Loss-Free Resistor and current-source-based approximations are obtained. Simulations are run in order to confirm the accuracy of both models. Afterwards, the small-signal model for several transfer functions is calculated from the current-source-based large-signal model and experimentally verified.

In **Chapter 6**, the most common dimming techniques, namely analogue (AM) dimming and Pulse-Width Modulation (PWM) dimming are introduced. Then, the PWM dimming is deeply discussed attending to the different schemes available in the literature: enable, series, and parallel dimming. The feasibility of each scheme applied to the Integrated Buck-Flyback Converter is analysed. Experimental tests are conducted in the laboratory prior to the proposal of a new PWM dimming technique derived from the series scheme. This new PWM scheme overcomes all the issues observed with conventional PWM dimming techniques. Experimental evidences are also provided.

In **Chapter 7**, the optimisation of a cost-efficient, highly-reliable, fully functional IBFC-based LED driver is described. A study on electrical stresses is addressed in order to enhance the efficiency. Thus, the need for evaluating different lamp configurations rises. After that, two series configurations are considered together with a parallel configuration. The most common equalisation techniques are introduced, and passive, self-equalisation is studied through the statistical study of the LEDs in order to achieve a proper current equalisation between strings. Afterwards, the low-frequency flicker index is considered in order to set the maximum output-current ripple that in turn sets the maximum bus-voltage ripple by means of the ripple-gain factor. Provided that the bus-voltage ripple affects the input current, the optimal dead angle and bus capacitor are studied for reducing the required bus capacitance down to values available in MKP technology while complying with Class C limits. In addition, a controller is designed for reducing the output-current ripple with limited effect on the input-current distortion. The experimental results show that an efficient, low-cost, fully dimmable LED driver is finally achieved.

In **Chapter 8,** the conclusions of this PhD Thesis work are discussed together with the main contributions and the most relevant papers published. In addition, future research developments are mentioned.

Key words: *electronic lighting, Light-Emitting Diode, LED modelling, Power Factor Correction, DCM converters, LED driver, integrated converters, electrolytic-capacitor-less converter, long-life driver, converter modelling, converter optimisation, LED equalisation, dimming, PWM dimming.*

Resumen

Este trabajo de Tesis Doctoral titulado "Alimentación de lámparas de estado sólido desde la red eléctrica, modelado de lámparas, estudio del convertidor reductor-retroceso integrado y optimización del sistema de regulación de flujo luminoso" está desarrollado dentro del grupo de investigación Conversión eficiente de energía, electrónica industrial e iluminación (CEEEII) de la Universidad de Oviedo.

Actualmente, los diodos LED se están mostrando la más prometedora fuente de luz debido a sus numerosas ventajas en términos de eficiencia y versatilidad. Un ejemplo de ésta última es su capacidad de regulación de luz, o *dimming*, que resulta altamente interesante para adecuar los niveles de iluminación a las necesidades precisas, con el consiguiente ahorro energético. Desafortunadamente, la iluminación LED no está exenta de retos. Entre ellos se encuentra la adecuada alimentación de una carga no lineal mediante un convertidor que reúna eficiencia y bajo coste junto con una alta capacidad de regulación de flujo luminoso, entre otros aspectos.

Esta Tesis Doctoral considera las tres principales áreas de interés en iluminación LED. En primer lugar, se estudiará el comportamiento de la lámpara LED como carga de potencia, así como la posibilidad de emplear diferentes configuraciones. En segundo lugar se estudiará la viabilidad e idoneidad del convertidor reductor-retroceso integrado, que ya se desarrolló previamente en otras aplicaciones, para alimentación de lámparas LED. Asimismo, se estudiará la optimización de este convertidor atendiendo a requisitos de rendimiento y vida útil. Finalmente, se explorarán las posibilidades de regulación de flujo luminoso en convertidores integrados, tales como el convertidor reductor-retroceso integrado propuesto.

Los principales objetivos de este trabajo de Tesis Doctoral se muestran a continuación:

- Estudio de las características estáticas y dinámicas de diodos LED comerciales en función de la temperatura de la unión. Para ello, se ensayarán tanto diodos LED individuales como lámparas completas con una potencia eléctrica superior a 25 W, puesto que estas lámparas son válidas para iluminación general de exterior e interior, iluminación arquitectónica, alumbrado público, etc.
- Estudio de la optimización de la lámpara LED como carga de potencia atendiendo a las diferentes configuraciones de los diodos individuales: conexión serie o paralelo.
- Estudio de las posibilidades que aporta el convertidor reductor-retroceso integrado para alimentación de lámparas LED desde la red eléctrica. Por ello, el convertidor deberá corregir el factor de potencia (FP) para cumplir la norma IEC61000 3-2 de Clase C.
- Estudio del convertidor reductor-retroceso integrado evaluando dos alternativas: operación de ambos convertidores en modo de conducción discontinuo (MCD), u operación del convertidor de retroceso en modo de conducción continuo (MCC).
- Estudio de la mejora de vida útil del convertidor reductor-retroceso integrado mediante la sustitución del condensador electrolítico de bus con un condensador MKP.
- Estudio y revisión de las diferentes técnicas de regulación de flujo luminoso, ya sea analógico (*dimming* AM), mediante modulación de ancho de pulso (*dimming* PWM), u otras técnicas presentes en la literatura científica.
- Análisis y desarrollo de la técnica de *dimming* PWM mejor adaptada a las características del convertidor reductor-retroceso integrado con alimentación desde red eléctrica con corrección de factor de potencia.

Este trabajo de Tesis Doctoral está estructurado como se detalla a continuación:

En el **Capítulo 1** se presenta una breve introducción a la iluminación. A continuación, se enumeran las fuentes de luz más comunes. Posteriormente se describen los diodos fotoemisores, o diodos LED, para detallar sus características como carga de potencia, puesto que ésta difiere sustancialmente de aquélla de las lámparas incandescentes o de descarga. También se incluyen los diferentes métodos de regulación de flujo luminoso. Finalmente, se presentan los diodos LED seleccionados para este trabajo.

En el **Capítulo 2** se desarrolla la caracterización térmica de los diodos LED. En primer lugar, se realiza un estudio estadístico de la tensión directa para obtener los valores típicos y desviación estándar para un diseño genérico. Posteriormente, se lleva a cabo un estudio de los efectos parásitos en los diodos LED para obtener una curva de ajuste *V-I* adecuada que se aplicará en la caracterización térmica de los diodos LED y que permitirá estimar la temperatura de la unión con precisión. A continuación, se caracteriza la resistencia dinámica del diodo LED en función de la temperatura de la unión para obtener un modelo completo de gran y pequeña señal para poder predecir el comportamiento de la lámpara LED en función de la temperatura. Finalmente, se estudia teóricamente cuáles serán las implicaciones que la dependencia térmica de la curva característica de los diodos LED conlleva para el buen funcionamiento del convertidor de potencia, incluyendo un ejemplo ilustrativo.

En el **Capítulo 3** se estudia el funcionamiento de convertidores CA/CC funcionando en modo de conducción discontinuo para el cumplimiento de la norma IEC61000-3-2 de Clase C. Así, se introducen el concepto de factor de potencia y los requisitos de contenido armónico de la norma. Se realiza un listado de soluciones activas y pasivas para la corrección del factor de potencia. A continuación, se consideran dos tipos de correctores de factor de potencia: aquéllos con corriente de entrada senoidal (etapas ideales de CFP), o aquéllos con una corriente no senoidal pero contenido armónico limitado (etapas cuasi-CFP). Finalmente, se incluye una revisión de las estructuras más comunes atendiendo al número de etapas en cascada para finalmente comparar el funcionamiento de las etapas ideales de CFP o las etapas cuasi-CFP.

En el **Capítulo 4** se estudia el convertidor reductor-retroceso integrado. De esta forma, se inicia con el estudio de ambos convertidores encascada, enumerando las ventajas frente a otras topologías. A continuación, se aplica el proceso de integración incluido en la literatura científica al convertidor reductor-retroceso. Se analiza también el funcionamiento de ambos convertidores en MCD, o en el convertidor de retroceso en MCC, lo cual permitirá comparar los beneficios de una alternativa frente a la otra mediante el factor de ganancia de rizado. Por último, se muestra un ejemplo de diseño del convertidor reductor-retroceso integrado para alimentar una lámpara LED de alumbrado público de 70 W de potencia y funcionamiento con tensión de entrada de rango universal.

En el **Capítulo 5** se derivan los modelos de gran y pequeña señal. Con respecto al modelo de gran señal, se considera tanto el modelo *Loss-Free Resistor* (LFR), como la aproximación basada en fuentes de corriente, incluyendo simulaciones para comprobar la exactitud de ambos modelos. Posteriormente, se derivan numerosas funciones de transferencia de pequeña señal a partir del modelo de gran señal basado en fuentes de corriente, que serán verificadas experimentalmente.

En el **Capítulo 6** se presentan las técnicas de *dimming* más comunes: analógico (AM) y por modulación de ancho de pulso (PWM). A continuación, se analiza el *dimming* PWM atendiendo a las diferentes estrategias disponibles en la literatura científica: *dimming* por *Enable*, *dimming* en serie, o *dimming* en paralelo. Se analiza la viabilidad de cada estrategia para la regulación de flujo luminoso en el convertidor reductor-retroceso integrado mediante justificación teórica y ensayos de laboratorio para a continuación desarrollar una nueva estrategia basada en el *dimming* PWM en serie. Esta nueva técnica permite resolver los inconvenientes encontrados con las otras técnicas PWM convencionales, a la vista de los resultados experimentales.

En el **Capítulo 7** se presenta la optimización del convertidor reductor-retroceso para obtener un convertidor AC/CC de bajo coste, alto rendimiento y con plena funcionalidad. Se comienza con el estudio de los esfuerzos eléctricos en el convertidor para aumentar el rendimiento. De esta forma, se introducirá la necesidad de estudiar una configuración óptima de la carga LED, por lo que se consideran dos configuraciones en serie junto con una configuración en paralelo. A continuación, se enumeran las técnicas de ecualización de diodos LED más comunes, tanto activas como pasivas, para posteriormente considerar la auto-ecualización de diodos LED mediante su resistencia serie. Para ello, se utilizarán el estudio estadístico incluido en el Capítulo 2 y el índice de parpadeo, *flicker* de baja frecuencia, que permitirá establecer un límite máximo de rizado de corriente que a su vez limitará la componente senoidal de la tensión de bus mediante el factor de ganancia de rizado. Puesto que el rizado de la tensión de bus afecta a la corriente de entrada, se estudia tanto el valor óptimo de ángulo muerto como el valor de capacidad de bus para reducir ésta última a valores fácilmente disponibles en tecnología MKP que permita cumplir con los límites de la Clase C. Por otra parte, se diseña un regulador digital con ancho de banda optimizado para reducir el rizado de corriente de salida con un efecto limitado en la distorsión de la corriente de entrada. Los resultados experimentales obtenidos muestran que finalmente se ha desarrollado un convertidor con alto rendimiento, bajo coste y con plena capacidad de regulación de flujo luminoso.

En el **Capítulo 8** se resumen las principales conclusiones obtenidas en este trabajo de Tesis Doctoral, así como las principales contribuciones realizadas y los artículos científicos publicados más relevantes. Por otra parte, se incluyen las futuras líneas de investigación propuestas.

Palabras clave: *iluminación electrónica, diodo LED, diodo fotoemisor, modelado de diodos LED, Corrección de Factor de Potencia, Modo de Conducción Discontinuo, driver LED, convertidor integrado, convertidor sin condensador electrolítico, convertidor de larga vida útil, modelado de convertidores, optimización de convertidores, ecualización de diodos LED, regulación de flujo luminoso, dimming, dimming PWM.*

Table of Contents

3. High Power Factor Off-line Power Supplies for LED Lighting

4. Study of the High-Power-Factor Off-line Integrated Buck-Flyback Converter for LED Lighting Applications.

List of Figures

List of Tables

List of Acronyms

AC	Alternating current
BCM	Boundary conduction mode
BoM	Bill of materials
CCD	Charge-coupled device
CCM	Continuous conduction mode
CCT	Correlated colour temperature
CFFF	Critical flicker fusion frequency
CFL	Compact fluorescent lamp
CLT	Central limit theorem
CM	Common mode
CMP	Current-mode programming
CPD	Cumulative probability distribution
CR	Contrast ratio
CRI	Colour rendering index
CT	Colour temperature
DC	Direct current
DCM	Discontinuous conduction mode
DF	Distortion factor
DFT	Discrete Fourier transform
DH	Double heterojunction
DUT	Device under test
EMI	Electromagnetic interferences
EN	European norm
ESR	Equivalent series resistance
FFT	Fast Fourier transform
FT	Fourier transform
HB-LED	High-brightness light-emitting diode
HFS	High-frequency series
HID	High-intensity discharge (lamp)
HPF	High power factor
HPM-HME	High-pressure mercury vapour (lamp)
HPS-SON	High-pressure sodium (lamp)
IBF	Integrated buck-flyback
IBFC	Integrated buck-flyback converter
IC	Integrated circuit
IEC	International Electrotechnical Commission
IES	Illuminating Engineering Society
ICS	Input-current shaper
IDBBC	Integrated double-buck-boost converter
IPC	Integrated power converter
IR	Infrared
ISS	Integrated single stage
ISSC	Integrated single-stage converter
JIS	Japanese Industrial Standards
KCL	Kirchhoff's current law
LCI	Lower confidence interval limit

LD	Laser diode
LED	Light-emitting diode
LFFI	Low-frequency flicker index
LFPF	Low-frequency percent flicker
LFR	Loss-free resistor
LPS	Low-pressure sodium (lamp)
MCPCB	Metal-core printed-circuit board
MH	Metal halide (lamp)
MIP	Mega instruction per second
MQW	Multiple quantum well
OA	Operational amplifier
OV	Over voltage
OTA	Operational transconductance amplifier
PCB	Printed-circuit board
PDF	Probability distribution function
PF	Power factor
PFC	Power factor correction
PFP	Power factor pre-regulator
PI	Proportional-integral
PM	Phase margin
PSRR	Power-supply rejection ratio
PWM	Pulse width modulation
RGB	Red, green, blue colours used for white light generation
RHP	Right half-plane
SEPIC	Single-ended primary inductance converter
SM	Switched-mode
SMPS	Switched-mode power supply
SNR	Signal-to-noise ratio
SPD	Spectral power distribution
SR	Synchronous rectifier
SSC	Single-stage converter
SSE	Sum of square errors
TIB	Twin-input buck converter
TFFC	Thin-film flip chip
THD	Total harmonic-distortion
UCI	Upper confidence interval limit
UPS	Uninterrupted power supply
US	United States
UV	Ultraviolet (radiant emission)
ZCS	Zero-current switching
ZVS	Zero-voltage switching

Glossary

- **Active layer:** region of a semiconductor where the recombination is most likely to happen, and as a result, where most of the photons are emitted from.
- **Band gap:** energy levels between the conduction and the valence bands where there are no feasible energy states, and therefore, the probability of an electron occupying one of those states is zero.
- **Boundary conduction mode:** operation mode of a power converter where the energy stored in the inductor reaches zero, with no idle time before a new switching cycle starts.
- **Built-in voltage:** internal electric field in the depletion region of a *p*-*n* junction that features a potential barrier to be overcome by the carriers in order to reach the opposite region.
- **Cladding layer:** in double heterojunction (DH) or multiple quantum wells (MQW) LEDs, each of the layers that delimit the active layers. The cladding layers feature a higher band-gap than the active layer.
- **Conduction angle:** in a Quasi-PFC, the conduction angle refers to the angle for which the converter is drawing current from the AC line.
- **Continuous conduction mode:** operation mode of a power converter where the energy stored in the inductor never reaches zero before a new switching cycle starts. Thus, the inductor current neither does.
- **Correlation coefficient:** in statistics, a parameter that tells how well a least-squares fitting predicts the real data.
- **Critical flicker fusion frequency (CFFF):** frequency of a light stimulation at which it becomes perceived as a stable and continuous sensation.
- **Cross-over (or zero-crossing) distortion:** is the distortion introduced by a dead angle in a voltage/current time-defined waveform.
- **Cumulative probability function:** function that describes the probability of a random variable X being equal to or lower than a given value.
- **Current-spreading layer:** layer underneath the *p*-region of a semiconductor electrode that spreads the current flow to regions not covered by the opaque electrode, enhancing the light extraction.
- **Dead angle:** in a Quasi-PFC, the dead angle refers to the angle for which the converter is not drawing current from the AC line.
- **Discontinuous conduction mode:** operation mode where the energy stored in the inductor reaches zero before a new switching cycle starts, with an idle time, and so the inductor current does.
- **Doping:** introduction of impurities in an intrinsic semiconductor in order to create the *p*-*n* junction and to vary the concentration of carriers.
- **Double heterojunction (DH):** *p*-*n* or *p*-*i*-*n* junction in a semiconductor where the active layer is built with a material featuring a lower bandgap than the cladding layers so that the absorption of the emitted photons in non-active layers becomes unfeasible.
- **Duty cycle:** in a time-defined square waveform, it is the ratio between the time for which the wave is in its high value and the signal period.
- **Dynamic resistance:** the inverse of the *I*-*V* curve slope at a given operation point.
- **Electron-blocking layer:** in a semiconductor device, layer that prevents the electrons from reaching the *p*-region and recombining outside the active layer. This layer features a higher band-gap than that of the active layer and other barriers in the semiconductor structure.
- **Ensemble:** referred to the LEDs composing an LED lamp assembly.

- **Flicker:** lighting variations that can be detected by the human eye.
- **Garnet:** group of silicate minerals with the general formula $A_3B_2(CO_4)_3$. The most usual in optoelectronics is the Cerium-doped Yttrium-Aluminium (YAG) garnet: $Y_3Al_2(AlO_4)_3$.
- **Heterojunction:** *p*-*n* junction where the *p* and *n* regions are made of materials with different band-gap energy.
- **Homojunction:** *p*-*n* junction where the *p* and *n* regions are made of the same material.
- **Ideality factor:** parameter in the Shockley equation that depends on the physical region where recombinations occur.
- **Large-signal model:** set of differential equations used for representing the behaviour of a non-linear system, also accounting for changes in the operation point.
- **Leakage flux:** in a transformer, magnetic flux that crosses one winding but not the other, leading to the presence of an inductance –the leakage inductance, connected in series to the mutually-coupled windings.
- **LED (Light-Emitting Diode):** semiconductor device that emits light because of the radiative recombination of a hole-electron pair.
- **Loss-free resistor:** lossless two-port network used to model the input port of a converter that effectively behaves as a resistor. The power processed by the LFR is transferred to the output. See also the POPI concept.
- **MKP capacitor:** polypropylene-based metallised film capacitor.
- **Multiple quantum wells:** semiconductor structure made with several active layers interspersed with electron-blocking layers featuring higher band-gap energy. These layers are characterised by a reduced thickness that allows quantum confinement effects to appear.
- ***p*-superlattice layer:** sandwich-like structure composed by several *p*-layers.
- ***p*-waveguide layer:** *p*-region placed just behind the electron-blocking layer that allows the photons to be extracted from the active layer. This layer features a higher refraction index, i.e. higher band-gap.
- **Phonon:** vibration of the semiconductor lattice due to the recombination of an electron with the release of both energy and kinetic momentum.
- **Photopic vision:** human retina sensitivity under strong lighting conditions, such as the day.
- **Planck Locus:** colour trajectory in the chromaticity diagram, such as *x*-*y* by CIE1931, of an ideal black-body as its temperature is increased within the visible range.
- **Plasma:** a fundamental state of matter that results from the ionisation of a gas, containing charged particles that make it electrically conductive.
- **POPI concept:** in converter modelling, assumption that the input power is transferred to the output in its entirety. POPI stands for $P_o=P_i$, where P_o and P_i are the output and input power, respectively.
- **Probability density function:** function defined as the derivative of the cumulative probability function of a random variable.
- **Scotopic vision:** human retina sensitivity under weak lighting conditions, such as the night.
- **Skewness:** measure of a probability density function asymmetry.

List of Symbols

$C(s)$	Controller transfer function
C_B, C_o	Bus and output capacitors
C_{min}	Minimum capacitor for a given ripple
C_n, $\overline{C_n}$	Bus specific capacitor
d	Duty cycle
$d(s)$	Duty cycle signal in the Laplace domain
d_D	Dimming duty cycle
D_1, D_2, D_3, D_4	IBFC diodes
D, S	Transistor drain and source (respectively)
$e(s)$	Error signal in the Laplace domain
ESR	Equivalent series resistance
f_L	Line frequency
f_o	Gain-crossover frequency
f_s, f	Switching frequency
$G(s)$	Plant (converter) transfer function
$h(s)$	Sensor signal in the Laplace domain
$H(s)$	Feedback sensor transfer function
$i(t)$, $i_g(t)$	Line current (time varying)
i_B, i_F	Instantaneous buck- and flyback-inductor currents
$i_B(t)$, $i_F(t)$	Buck- and flyback-inductor currents (time varying)
i_g	Instantaneous line current
$i_o(s)$, $I_o(s)$	Output current in the Laplace domain
$i_o(t)$	Output current (through the LED load)
I_1	Line current fundamental harmonic
I_D	LED forward (output) current (forward current across a $_{p\text{-}n}$ junction)
I_n	Line current n^{th} harmonic
I_o	Output current
I_S	Reverse saturation current of a *p-n* junction
I_v	Luminous intensity of a light source
K_{dc}	Controller static gain
$L(s)$	Loop-gain transfer function
L_B, L_F	Buck and flyback inductors
m	Buck-converter conversion ratio
M_1, M_2, M_S, M_D	Transistor
n	Turns ratio
$p(s)$	Output perturbation in the Laplace domain
$p(t)$	Power (time varying)
P_{avg}, P_g	Average power
PF	Power factor
PM	Phase margin
P_n	Specific power
P_o	Output power
q	Electron charge
$r(s)$	Output current reference in the Laplace domain
R_B, R_F	Buck- and flyback-converters equivalent resistors
R_D	LED dynamic resistance

R_L	Load resistance
R_s, R_S	Parasitic series-resistance effect of a semiconductor, series resistance
R_p	Parasitic parallel-resistance effect of a semiconductor
s	Laplace domain variable
$S_u(s)$	Control sensitivity transfer function
t	Time
t_{ON}	Lamp lit-on time
T_{DIM}	PWM dimming period
THD	Total harmonic distortion
THD_I	Input-current THD
T_j	LED junction temperature
T_{jmin}	Minimum LED junction temperature
T_{jmax}	Maximum LED junction temperature
$u(s)$	Controller action in the Laplace domain
u_B	Instantaneous bus voltage
$u_B(t)$	Bus voltage (time varying)
u_g, v_g	Instantaneous line voltage
$u_g(t)$	Line voltage (time varying)
u_o	Instantaneous output voltage
$u_o(t)$, $v_o(t)$	Output voltage (time varying)
U_B, V_B	Bus voltage
U_{D1}, U_{D2}, U_{D3}, U_{D4}	Voltage across the IBFC diodes
U_g	Line voltage
V_D	LED forward voltage (forward voltage across a *p-n* junction)
V_{Dtyp}	Typical LED forward voltage
V_{Dmin}	Minimum LED forward voltage
V_{Dmax}	Maximum LED forward voltage
V_g	Line voltage peak value
$V_g(t)$, $v(t)$,	Line voltage (time varying)
V_o, U_o	Output voltage
V_γ	LED threshold voltage
$y(s)$	Plant output in the Laplace domain
$y'(s)$	Perturbed plant output in the Laplace domain
z, z_o	Zero
α	Converter dead angle
α_L	IBFC inductors ratio
δ	Output-current ripple
Δ	Difference operator
ε	Forward voltage tolerance
η	Ideality factor in semiconductor *p-n* junctions
θ	Converter conduction angle
μ	Average value (random variable average value of a population)
ν	Ripple-gain factor
σ	Standard deviation (random variable standard deviation of a population)
ϕ, φ	Angle between line current and line voltage
ω_L	Line angular frequency
ω_o	Cross-gain angular frequency
$\langle \quad \rangle$	Averaged variable
^	Perturbed variable

Chapter 1

Al	Aluminium
As	Arsenic
c	Speed (of light in vacuum)
E, E_a	Energy (associated to an electromagnetic radiation)
E_c	Minimum energy level of the conduction band
E_g	Semiconductor band-gap. Difference between E_c and E_v
E_v	Maximum energy level of the valence band
$f(E)$	Fermi-Dirac function
$F_r(\lambda)$	Radiant flux emitted by a light source inside the visible spectrum
$g(E)$	States-density function
Ga	Gallium
h	Planck constant
In	Indium
k	Boltzmann constant
k'	Kinetic momentum of an electron
L	Luminance of a light source
N	Nitrogen
P	Phosphorus
R_{EQ}	LED equivalent resistor at a given operation point
v	Speed (of a particle)
$V(\lambda)$	Spectral response curve of the human eye
λ	Wavelength
Φ	Luminous flux emitted by a light source

Chapter 2

a, b ,c, d	Fitting parameters
C	Capacitor
D	Diode
$E(T)$	Expected value of a probability distribution
$E(X)$	Expected value of a random variable
i_{ac}, I_{ac}	AC amplitude of the LED forward current
$i_{ac}(t)$	Output current AC component (time varying)
$i_c(t)$	Capacitor current (time varying)
$i_D(t)$	Diode current (time varying)
I_C	Capacitor current
I_{DC}	DC component of the LED forward current
I_{Di}	LED forward current for a given operation point
$I_{g\_AVG}(t)$	Line average current (time varying)
I_o	Output current DC component
I_p	Current across the parallel parasitic resistance in a *p*-*n* junction
k, $\partial V_D/\partial T_j$	Temperature coefficient of LED forward voltage
k_B	Boltzmann constant
k'	Temperature coefficient of LED forward voltage (measured)
L	Inductor
n	Sample size
$N(\mu, \sigma)$	Gaussian distribution
P	Probability

P_D	Power dissipated in an LED
r^2	Fitting curve correlation coefficient
r_D	Small-signal LED dynamic resistance
R_{Di}	LED dynamic resistance for a given operation point
$R_{\theta j\text{-}b}$	LED junction-to-board thermal resistance
$R_{\theta jc}$	LED junction-to-case thermal resistance
S_V	Sample standard deviation of LED forward voltage
S_T	Sample standard deviation of LED junction temperature
T_A	Ambient temperature
T_B	Board temperature
T_{jAVG}	Average LED junction temperature
v_{ac}	AC component of the LED forward voltage
$Var(T)$	Variance of a probability distribution
V_{Davg}	Average LED forward voltage
V_{Di}	LED forward voltage for a given operation point
V_g	Line voltage rms value
$V_{\gamma i}$	LED threshold voltage for a given operation point
X, T	Random variable
Z	Standard normal random variable
Z_o	Output impedance
ξ	Sample average value
σ^2	Random variable variance of a given population
ϕ_{ac}	Output-current AC-component phasor phase
ϕ_o	Output-current (through the LED load) phasor phase
$\bar{}$	Phasor operator
$\|\bar{}\|$	Phasor modulus operator

Chapter 3

C_1, C_2, C_o	Capacitors
D_1, D_2, D_3	Diodes
$DispF$	Displacement factor
DF	Distortion factor
i_B	Converter output-current
I_B	Converter output-current DC component
$\hat{I}_B$	Converter output-current AC component
i_n	Specific input current
$\overline{I_n}$	Converter output specific current
I_{rms}	Line rms current
LC	Inductor-capacitor filter
p_g	Instantaneous input power
P	Real power
S	Apparent power
RC	Resistor-capacitor filter
R_g	Converter equivalent input-resistance
$\hat{v}_B$	Normalised bus-voltage ripple
V_B	Converter output-voltage
$\hat{V}_B$	Converter output-voltage AC component
V_n	Normalised line voltage
V_{rms}	Line rms voltage

X_B	Bus-capacitor equivalent reactance
Q	Charge injected to the bus capacitor
λ	Power factor

Chapter 4

C_1, C_2	Controller capacitors
C_R	Controller gain
C_{xi}, C_{xo}	EMI filter capacitors
d_B, d_F	IBFC buck and flyback inductors discharging time, respectively
d_{Buck_max}	Buck-converter maximum duty cycle
$d_{Flyback\_max}$	Flyback-converter maximum duty cycle
D_{F1}, D_{F1}	Diodes in an integrated switch
D_{B1}, D_{B2}	Blocking diodes in an integrated switch
G_{d0}	G(s) DC gain
i_{BUS}	IBFC bus output instantaneous current
i_{CB}	Instantaneous current through the bus capacitor
i_{Co}	Instantaneous current through the output capacitor
i_{D1}, i_{D2}, i_{D3}, i_{D4}	Instantaneous currents through the IBFC diodes
i_o	Instantaneous output current
i_S	Instantaneous current through the IBFC transistor
L_1, L_2	EMI filter inductors
n_{opt}	Optimal turns ratio
P_I	Input power
R	Controller resistor
s_p	Controller pole
s_z	Controller zero
T	Switching period
$\hat{u}_B(t)$	IBFC bus-voltage AC component
U_{LB}, U_{LF}	Voltage across the IBFC inductors
U_S	IBFC transistor voltage
η_F	Flyback efficiency
v_{DCM}, v_{CCM}	Ripple-gain factor in DCM and CCM, respectively
ω_{dp}	G(s) pole angular frequency

Chapter 5

d	Instantaneous duty cycle
CS	Current sensor
D	Linearised duty cycle
ESR_C	Capacitor equivalent series resistance
ESR_{LB}, ESR_{LF}	Buck- and flyback-inductor ESR
ESR_{CB}, ESR_{CF}	Buck- and flyback-capacitor ESR
$G_{Bd}(s)$	Duty-cycle to bus-voltage transfer function
$G_{Bg}(s)$	Input-voltage to bus voltage transfer function
$G_{id}(s)$	Duty-cycle to input-current transfer function
$G_o(s)$	Duty-cycle to output current IBFC transfer function
$G_{oB}(s)$	Bus-voltage to output-current transfer function
$G_{od}(s)$	Duty-cycle to output-current transfer function (flyback converter)
$G_{og}(s)$	Line-voltage to output-current transfer function
$i_{BD}(t)$, $i_{FD}(t)$	Buck- and flyback-diode current sources

$i_{BS}(t)$, $i_{FS}(t)$	Buck- and flyback-transistor current sources
k_{BD}	$G_{Bd}(s)$ transfer function gain
k_{BG}	$G_{Bg}(s)$ transfer function gain
k_{BDG},k_{BDB}, k_{BDD}	Buck-converter diode small-signal current sources
k_{BSG},k_{BSB}, k_{BSD}	Buck-converter transistor small-signal current sources
k_{FDB},k_{FDB}, k_{FDO}	Flyback-converter diode small-signal current sources
k_{FSB},k_{FSD}	Flyback-converter transistor small-signal current sources
p_B, p_F	Instantaneous buck- and flyback converters input power
p_{BB}, p_{DO}	Transfer function poles
r_{BDSon}, r_{FDSon}	Buck- and flyback-transistor on-state resistance
T_s	Switching period
V_{BF}, V_{FF}	Buck- and flyback-diode forward voltage drop
$Y_i(s)$	Input admittance transfer function
$Y_o(s)$	Output admittance transfer function
$Z_i(s)$	Input impedance transfer function

Chapter 6

CR	Dimming –or contrast, ratio
CR_{max}	Maximum dimming ratio
d_{avg}	Dimming duty cycle average value
d_{D_max}	Minimum dimming duty cycle
d_{D_min}	Maximum dimming duty cycle
D_L	Snubber free-wheeling diode
H_0	Feedback sensor gain
I_{AVG}, $I_{o<AVG>}$	Average output current (dimmed)
I_{PK}	Output-current peak value
L_S	Snubber inductor
P, $P_{o<AVG>}$	Output power
R_L	Snubber series resistor
t_D	Delay time (converter lag)
t_{SD}	Falling edge time
t_{SU}	Rising edge time
V_{err}	Error signal
V_H	Sensor signal
V_R, V_{RP}	Reference signal
V_{reg}	Control signal
V_{RD}	Dimming ratio reference
ϕ_D	Luminous output (dimmed)
ϕ_K	Luminous output (full power)

Chapter 7

C_{Bridge}	EMI filter capacitor
C_{o_min}	Minimum output capacitor
C_{oss}	Transistor output capacitance
C_S	Snubber capacitor
C_{x1}, C_{x2}, C_{y1}, C_{y2}	EMI filter capacitors
di_F/dit	Slope of diode forward current
d_{max}	Maximum duty cycle
D_5, D_6, D_7, D_8, D_9	Diodes

i, k	Indices
$i_{BUS}(t)$	IBFC-bus output current (time varying)
$i_{CB}(t)$	Bus-capacitor current (time varying)
$i_r(t)$	Output-current reference (time varying)
$I_{D1}, I_{D2}, I_{D3}, I_{D4}$	Diode currents
I_{Davg}	Diode average current
I_{Drms}	Diode rms current
I_g	Line current
I_S	Drain current
I_{Srms}	Transistor rms current
I_{v_avg}	Average luminous intensity
$K(t)$	Controller function (time varying)
$K_z(z)$	Discretised controller
$K_{z30}(z), K_{z60}(z)$	Discretised controller for the 1x30/2x30, and 1x60 configurations
L_{CM}, L_{CM1}	Common-mode chokes
$LFFI$	Low-frequency flicker index
$LFPF$	Low-frequency percent flicker
n	Transformer turns ratio
N	Number of series-connected LEDs; sample size
p	Number of paralleled-strings
P_{DIM}	Output power in dimmed operation
P_{Don}	Diode conduction losses
P_{min}, P_{max}	Minimum and maximum output power
P_{nom}	Nominal output power
P_{Son}	Transistor conduction losses
P_{sw}	Switching losses
R_{Dmin}, R_{Dmax}	Minimum and maximum dynamic resistance
R_{Dnom}	Nominal dynamic resistance
R_{DSon}	Transistor on-resistance
R_s	Shunt resistor
R_{SNUB}	Snubber resistor
T	Line period
$\hat{u}_B$	Unitary bus-voltage ripple
U_{Bmin}, U_{Bmax}	Minimum and maximum bus voltage
U_{Bnom}	Nominal bus voltage
V_{Dnom}	Nominal LED forward voltage
U_{DS}	Drain-to-source voltage
W_{on}, W_{off}	Energy dissipated in the on and off transitions
X_{avg}	Light source luminous output
X_{trunc}	Truncated Fourier decomposition of luminous output
z	Digital variable
δI_v	Luminous intensity ripple
δU_B	Unitary bus-voltage ripple
η	Efficiency
ψ	Forward-current deviation
$\bar{\ }$	Unitary/specific magnitude

Chapter 1

Introduction to Electronic Lighting

In this chapter, a brief introduction to electronic lighting is provided in order to allow for a better and deeper understanding of the concepts involved in lighting.

Firstly, the main theoretical concepts in general lighting, such as the magnitudes, e.g. luminous flux or intensity, and the physical background will be introduced and explained. Secondly, the main mechanisms of luminous emission will be covered. Then, the most usually employed lamps will be listed, as well as their most important features and applications. Afterwards, a comparison among the most common artificial light sources, in terms of luminous efficacy, life span, typical rated power, etc. will be provided. After that, Light Emitting Diodes (LEDs) will be dealt with, since these light sources are the aim of this work. As the light emission mechanism of LEDs is different from any other lighting source already available, this issue will be deeply and thoroughly discussed, together with other relevant considerations in order to design an LED fixture successfully

Moreover, LED devices exhibit an electrical behaviour different from that of incandescent or gas-discharge lamps. Therefore, the behaviour of these devices as a power load will be taken into consideration, introducing the three basic schemes for driving LED lamps, as well as the LED models. In addition, extra features of an electronic lighting fixture will be introduced, such as the luminous flux control, i.e. dimming, which is a very interesting functionality, allowing for energy efficiency and rational use of energy. The two main techniques will be covered: i) Analogue or Amplitude Modulation (AM) dimming and ii) Pulse-Width Modulation (PWM) dimming.

Finally, the different LEDs commercially available will be classified according to their power consumption and other features, also introducing the binning that manufacturers perform to commercial devices. Finally, the chapter ends gathering the main characteristics of the LEDs chosen for this study.

1.1. Introduction

There is a rising concern about energy efficiency in all aspects of modern life due to economic and sustainability reasons. As an example, the energy consumption in Spain in 2010 rose up to 260.6 TWh [1.1], of which around a 25% is assumed for lighting appliances. Therefore, the importance of energy efficiency in lighting is increasing significantly. Improving the efficiency of such appliances, not only the amount of carbon dioxide emitted to the atmosphere – which is considered the main responsible for Global Warming – would be lowered, but also the energy dependence of the country would be further reduced.

Light Emitting Diodes (LEDs) have lately been undergoing a great improvement in many features, such as luminous flux, efficacy, life span, thermal resistance, etc. Nowadays, the efficacy of these devices has broken the 100 lm/W barrier [1.2], so they have become a highly interesting luminous emitter for general applications, as backlighting [1.3]-[1.6], permanent emergency lighting systems (PELS) [1.7], [1.8], general indoor/outdoor and architectural lighting [1.9]-[1.14], street lighting [1.15]-[1.17], automotive lighting (including headlamps) [1.18], among others.

With the newest energy efficiency regulations becoming more demanding and tighter [1.19], it is even more necessary to increase the research investments and efforts in this field so that the efficacy of luminaries takes advantage of the increase in efficacy that LEDs have performed. This purpose can be achieved through a multiple fold approach accounting for an adequate thermal design and management [1.20], [1.21], as well as the optimisation of the LED driver [1.16], among others. Nevertheless, one of the most promising research fields involves development of smart techniques for light usage by means of luminous flux control, i.e. dimming, which assures that the illumination levels are matched to the actual needs in any kind of application [1.22]-[1.32]. This is why LEDs are gaining attention in research today, as they are a promising technology but still under development, with unlimited boundaries for research.

1.2. Key concepts in lighting

This section will cover the main concepts of lighting that will be of help in order to face the design of a basic lighting research project.

1.2.1. Light

Light is an electromagnetic radiation that carries an amount of energy that is visible by the human being. As an electromagnetic radiation, there is a relation between the energy of the particle – in this case, the photon, and the wavelength of the associated electromagnetic wave, given by:

$$E = h \cdot \frac{c}{\lambda} = hv \tag{1.1}$$

where h is the Planck constant, c is the propagation speed of the particle in vacuum, v, its propagation speed in a medium, and λ, the wavelength of its associated electromagnetic wave, which is in the range visible by the human eye.

1.2.2. Electromagnetic spectrum

The classification of the different electromagnetic radiations in terms of their wavelength constitutes the electromagnetic spectrum, as can be seen in Fig. 1.1.

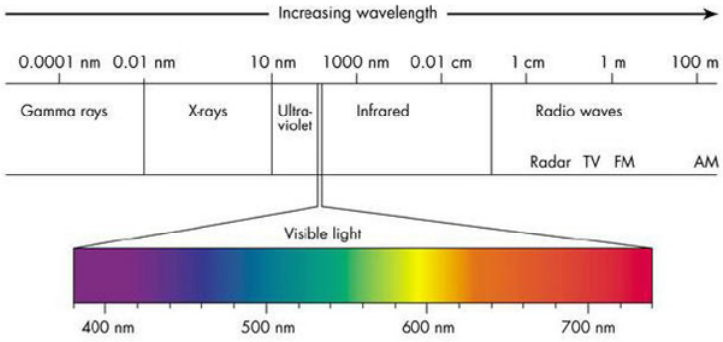

Fig. 1.1. Electromagnetic spectrum

The human retina is sensitive to a narrow band of wavelengths, which is the visible spectrum. This is shown in Fig. 1.2. Besides, the human eye sensitivity is not constant for the entire visible spectrum. Indeed, it varies with the wavelength and the amount of light available.

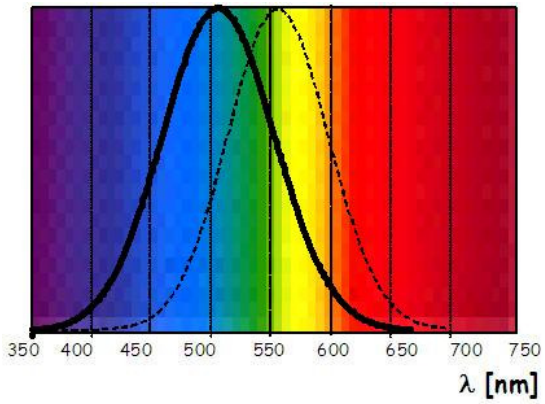

Fig. 1.2. Visible spectrum and sensitivity of the human eye, photopic (dashed line), and scotopic (solid line).

In this way, under strong lighting conditions, the so-called photopic vision takes place, with its maximum sensitivity at 555 nm, whereas under low levels of illumination, the sensitivity curve shifts towards the UV region, namely, the scotopic vision.

1.2.3. Light emission mechanisms

The different light emission mechanisms can be classified according to the way in which the electrons are excited. There are two main mechanisms: thermal radiation –or incandescence, and luminescence.

1.2.3.1. Thermal radiation

Thermal radiation could be defined as the emission of electromagnetic radiation due to the thermal motion of electrons caused by the material temperature. If this electromagnetic energy emission falls into the visible spectrum is called incandescence.

The interaction between the electrons in an emitter body are intensified as long as the temperature is increased, so the feasible energy levels grow, being the emission spectrum continuous as a result of this. The higher the body temperature is, the higher amount of energy is emitted within the visible spectrum, as can be seen in Fig. 1.3.

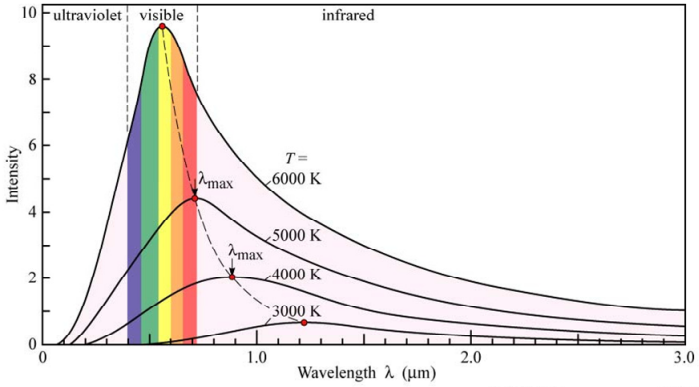

Fig. 1.3. Black body radiation curves (Planck curves). The visible spectrum is highlighted.

1.2.3.2. Luminescence

Essentially, luminescence is the emission of electromagnetic energy radiated from a body due to electron excitation produced by a foreign agent. In this case, the emission intensity in discrete energy levels is much higher than that of the body temperature, resulting in a discontinuous emission spectrum.

According to the excitation source, luminescence could be categorised into the following types:

- Electroluminescence: generated by the action of an electric field inside a substance. Examples of lamps that generate light by electroluminescence are some discharge lamps, light emitting diodes (LEDs), etc.
- Photoluminescence: generated by the absorption of photons radiated with different wavelength, this can in turn be divided into the following sub-categories: fluorescence, phosphorescence, LASER, etc.
- Chemiluminescence: generated by chemical reactions.
- Bioluminescence: produced by living organisms.
- Triboluminescence: generated by a mechanical action on a body.
- Etc.

1.2.4. Colour Temperature (CT) and Correlated Colour Temperature (CCT)

The Colour Temperature (CT) of a light source represents its thermal appearance, expressed in Kelvin (K). This appearance –indeed, the colour, depends on the spectral composition of the visible spectrum of the light emitted. Every body, when heated up to a certain temperature, start to emit a redish light. As long as its temperature increases, this light turns towards whitish. This phenomenum establishes a relation between the temperature of the light source and its colour appearance, so the parameter that characterises the colour of a light source is called Colour Temperature.

The CT of a light source is determined by comparison with a pattern. This pattern is based on a lamp with emitting properties close to that of the black body. The different temperatures of a black body establish the so-called Planck Locus inside the CIE chromaticity diagram, as shown in Fig. 1.4.

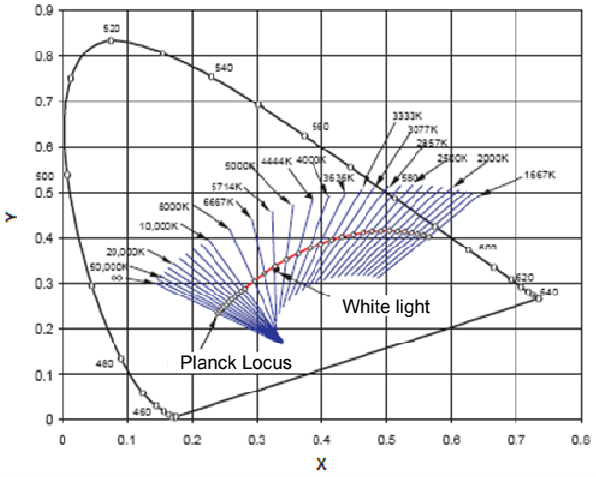

Fig. 1.4. CIE 1931 Chromaticity Diagram, Planck Locus and Correlated Colour Temperature lines.

For those light sources not emitting in a continuous spectrum, their colour is outside the Planck Locus, and the concept of Colour Temperature is no longer valid. In these cases, the applicable concept is the Correlated Colour Temperature, which shows the colour of the light as if it were emitted as a continuous spectrum, but gives no information about the spectral composition. The CCT lines in Fig. 1.4 allow this parameter to be known.

1.2.5. Colour Rendering Index (CRI)

The Colour Rendering Index (sometimes known as Colour Rendition Index) shows the ability of a given light source to reproduce colours faithfully as compared to a black-body pattern light source with the same CT. The IRC values are comprised between 0 and 100, being the higher, the better reproduction of colours.

1.2.6. Basic units and magnitudes in lighting

Below, there is a list of the main magnitudes most commonly used in lighting:

- Luminous flux (Φ): is the radiant power emitted, $F_r(\lambda)$, weighted with the human eye response curve, $V(\lambda)$, generally in photopic conditions. Its unit is lumen, *lm*.

$$\Phi = 683 \int F_r(\lambda) V(\lambda) d\lambda \tag{1.2}$$

- Luminous intensity (I_v): luminous flux emitted within a solid angle in a given direction. Its unit is candela, *cd*.
- Illuminance: luminous flux per square metre. Its unit is lm/m^2, or *lux*.
- Luminance: relation between the luminous intensity of a light source in a given direction and the surface of the light source in that direction. Its unit is candela per square metre, cd/m^2.
- Luminous efficiency, efficiency, or efficacy: ratio between the luminous flux emitted by a light source and its energy consumption. Its unit is lumen per watt, *lm/W*.
- Life span: period of time elapsed until a light source does not satisfy the operation requirements, typically a 70% lumen maintenance of its rated lumen output in the case of LEDs.
- Mean life: period of time elapsed until the 50% of the samples reach a failure condition.

1.3. Types of lamps

In this section, the main types of lamps commercially available will be briefly introduced, as classified by its light emission mechanism: thermal radiation and luminescence.

1.3.1. Incandescent lamps.

Incandescent lamps generate light by thermal radiation as a consequence of the flow of a current through a tungsten filament. A great amount of that energy is emitted out of the visible region, actually in the IR range, and therefore, the efficacy of such lamps is low, between 8 and 20 lm/W. Featuring a continuous emission spectrum, the CT of the light emitted is determined by the temperature of the tunsgten filament. Fig. 1.5 shows the emission spectra of two incandescent lamps with their filamentes at different temperatures.

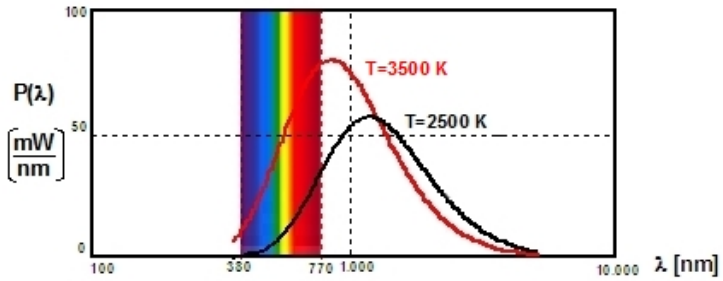

Fig. 1.5. Emission spectra of two incandescent lamps with their filament at different temperatures.

The CT of incandescent lamps corresponds to warm white (as much as 3000 K), the CRI is 100, and their life span ranges 1000 – 2000 hours.

1.3.2. Halogen incandescent lamps

This kind of lamps are essentially incandescent lamps, but with a halogen-based additive in the filling gas, generally iodine or bromine. This additive allows the halogen cycle to occur, which consists of the recombination of the halogen with the filament steaming tungsten, and performs a regenerative effect that prevents deposition of tungsten on the bulb and allows the filament to work at higher temperatures, increasing the mean life, around 3000 or 4000 hours, the luminous output and therefore, the efficiency, which is as high as 25 lm/W. Their CT is as high as 4200 K in some automotive applications.

1.3.3. Low-pressure gas discharge lamps.

Gas discharge lamps emit light produced by the luminescence mechanism. In this case, the luminescence mechanism takes place inside a plasma through the action of an external electric field that induces the excitation of the plasma atoms.

Low-pressure gas discharge lamps are characterised by an emission in a discontinuous spectrum depending on the atomic structure of the plasma and the pressure inside the bulb. This is a consequence of the excitation of valence electrons in discrete energy levels, so the electromagnetic emission corresponds to the resonance lines, which are characteristic of each material, gas and additives.

Low-pressure gas discharge lamps are composed of a gas confined in a bulb at pressures around 1 Pa. The electric field is generally produced between two or more electrodes at each side of the bulb, although there are electrodeless lamps commercially available [1.33]. The

action of this electric field induces the ionisation of the gas until the disruptive discharge is reached. At this point, the current through the gas increases rapidly, so a current-limiting ballast is used in order to limit the lamp current to an appropriate value. A characteristic of low-pressure lamps is the low heating induced by the flow of the current in a low-pressure gas.

The most common low-pressure lamps are:

- **Low-pressure mercury lamps (fluorescent lamps):** characterised by the emission of UV radiation at 185 and 253.7 nm corresponding to the resonance lines of mercury. In a second step, this UV emission is converted into visible light by a phosphor coating on the inner wall of the bulb. This wavelength conversion by different phosphors allows for an extremely wide range of CCT, ranging between 2600 and 8000 K and with an excelent CRI up to 97. The efficacy of these lamps reaches values around 100 lm/W. Fluorescent lamps generally feature a very low power density.
- **Low-pressure sodium lamps (LPS):** characterised by the narrow emission of the sodium atom, these lamps emit the 90% of the radiation in two wavelengths corresponding to the so-called D-lines: 589 and 589.6 nm, very near to the maximum sensitivity of the human eye under photopic conditions, 555 nm, making these lamps the most efficient of all light sources with an efficiency reaching up to 180 lm/W. However, the light emitted by these lamps is highly monochromatic, and therefore, the rendering index is rather poor.

1.3.4. High-pressure gas discharge lamps (HID lamps)

The pressure of the filling gas is a decisive parameter in the light-emission performance of gas discharge lamps. When the pressure in a gas rises, the temperature also rises due to the energy transfer produced by the collisions between atoms and electrons within the ionised plasma. At such high temperatures, the electrons own enough energy to ionise the gas.

The higher temperature is reached in the centre of the discharge arc, being a temperature gradient established between the centre of the discharge and the surface of the bulb, so the greatest amount of energy is radiated from the centre of the arc.

The main difference with low-pressure lamps lies on the different spectral composition of the light emitted, as the emission lines tend to broaden since the electrons are excited at additional energy levels due to the increase in pressure. As a result, the emission lines become emission bands, with an emission spectrum which is almost continuous. This improves the CRI of the lamp, but as a consequence of the higher pressure, higher temperatures are achieved, which induces a decrease of the efficiency as a consequence of a higher fraction of energy radiated as heat.

The most common HID lamps are:

- **High-pressure mercury vapour lamps (HPM-HME)**: these lamps were the first high-pressure lamps commercially available, and were the most common choice in street lighting for a large time extent. However, due to their relatively low efficiency (around 50 lm/W) they are nowadays overcome by high-pressure sodium and metal-halide lamps in such applications. The pressure reaches values around 200 and 2000 kPa and therefore, emission bands within the visible region, as well as a continuous spectrum, appear. Nevertheless, there is a lack of emission in the red region, so the CRI of this kind of lamps is low. In order to improve this issue, two techniques are employed: the earliest one, consisted in the addition of an incandescent filament, which greatly lowers

the efficiency and reliability, and more lately, was the addition of fluorescent-like phosphors, which introduces a wide range of different CRI and CCT.

- **High-pressure sodium lamps (HPS-SON)**: as the pressure rises, the emission lines of sodium are split into two emission bands and separated towards red and green. The emission spectrum is filled with some green and blue emission by the addition of mercury. These lamps feature a CCT around 2000 K with a CRI around 40 and a luminous efficiency around 120 lm/W or slightly higher, but in the white sodium lamps (SON), the CRI can be as good as 85 and the CCT can rise up to 2800 K, although the efficacy is reduced as a consequence of the higher pressure of such lamps, being below 60 lm/W.
- **Metal-halide lamps (MH)**: these lamps stem from HPM lamps with the addition of metallic halides and rare earth salts that radiate within the visible spectrum in order to improve both the quality of the light and the efficacy. The CCT of such lamps usually ranges between 3000 and 5500 K, depending on the additives used, the CRI is as good as 95, and its efficacy surpasses 100 lm/W in some devices.

1.3.5. Light-Emitting Diodes

Light-Emitting Diodes (LEDs) are solid-state devices, where the light is generated by electroluminescence. There is a wide range of CRI, CCT and luminous efficiency values. Regarding the CRI, the most usual are around 75 up to 95. The CCT goes from 3000 K to 8000 K or even higher for some cool white devices, and the luminous efficiency has surpassed the 100 lm/W for cool white devices. Their life span is extremely long, higher than 50,000 hours in continuous operation for a luminous maintenance of 70% [1.34]. However, this life span, as well as the performance of LEDs, is highly affected by two main factors, namely operation current and junction temperature. Their high efficiency together with many other interesting features such as their dimmability have led LEDs to be one of the most emerging technologies in lighting nowadays.

Since this work is focused on solid-state street and general lighting with white LEDs, more information will be provided in depth in subsequent sections.

1.3.6. Comparison among lamps

This section will briefly compare the main characteristics of the most common lamps used in general applications, including a comparison according to the following characteristics: CRI, CCT, luminous efficiency, and life span. These data are gathered in Table I.I. It should be noted that these values are illustrative and may vary from different manufacturers.

1.4. Light-Emitting Diodes

This section will introduce a brief insight on solid-state lighting, starting from the operation principles of LEDs, and covering the most important issues in supplying LED lamps.

LEDs have undergone an impressing improvement in several characteristics such as efficacy, thermal resistance and light maintenance. Other advantages of LEDs are the absence of IR and UV radiation in the radiating output.

However, LEDs still feature some drawbacks such as the loss of efficiency at high temperature, which is worsened by the fact that most of the heat generated in the *p-n* junction is dissipated by conduction through the slug of the device.

TABLE I.I.
MAIN CHARACTERISTICS OF COMMERCIAL LAMPS (TYPICAL)

Lamp	***CRI***	***CCT* (K)**	***Efficacy* (lm/W)**	***Life span* (h)**
Incandescent	100	~2700	~10	~1000
Halogen	100	~3600	<25	<4000
Fluorescent	<97	2600-8000	~100	~20k
LPS	-	~1700	<180	~20k
HPM- HME	20-50	4000-7000	10-60	~20k
HPS-SON	20-85	2000-2800	50-140	~20k
MH	65-95	3000-5500	~100	6k-20k
LEDs cool white	~70	~5500	>100	~50k
LEDs neutral white	~85	~4000	~100	~50k
LEDs warm white	~95	~3000	<100	~50k

1.4.1. Operation principles of LEDs

The light emission mechanism in LEDs is the so-called luminescence injection. This takes place by the radiative recombination of a hole-electron pair through the band gap of the semiconductor as the *p-n* junction is excited by means of an external electric field.

There are two different carriers in a semiconductor: electrons and "holes"- this is, absence of an electron in a covalent link, which induces a positive charge. Under an external electric field or due to thermal excitation, electrons in the valence band can achieve enough energy to "*jump*" to vacant energy levels in the conduction band, creating a hole in the valence band. Fig. 1.6 shows the bands diagram, which sketches the semiconductor energy levels at which electrons can be found according to their occupation probability. This figure illustrates a recombination process, where the electrons reach the conduction band after having absorbed an amount of energy E_a, greater than E_c-E_v, where E_c is the minimum energy level at the conduction band and E_v is the maximum energy level at the valence band.

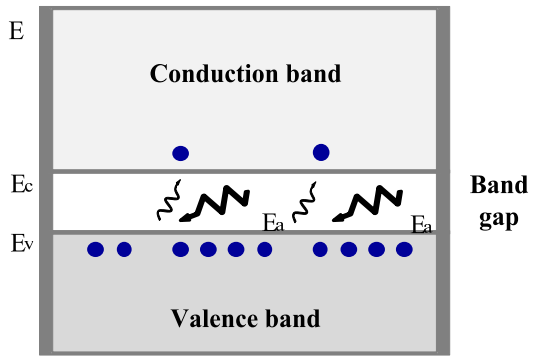

Fig. 1.6. Energy bands in an intrinsic semiconductor. Vertical axis: electrons energy, in eV.

As a consequence of an external electric field applied, electrons gain an amount of energy $q\Delta V$, where q is the charge of the electron and ΔV is the electric field, and they are in constant motion across the lattice interacting among them, resulting in a loss on their kinetic energy. Due to the loss on kinetic energy, electrons reach lower energy levels in the conduction band. Fig. 1.7 shows the energy bands in a semiconductor under an external electric field applied.

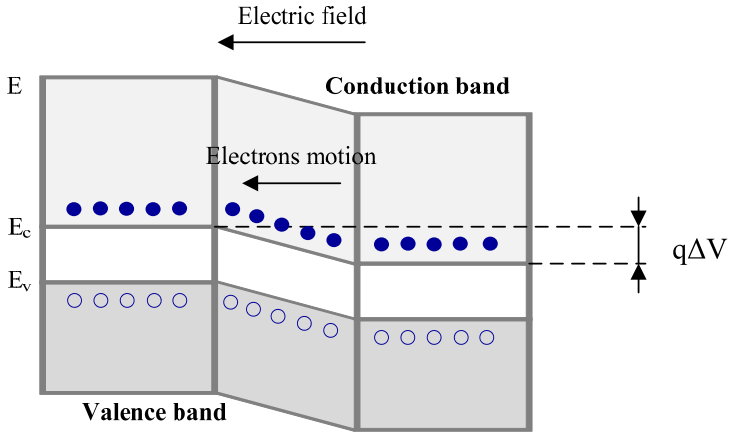

Fig. 1.7. Energy bands in an extrinsic semiconductor under an external electric field that supplies an energy $q\Delta V$. The motion of electrons and loss of energy is also shown.

In the case of extrinsic semiconductors, donor and acceptor impurities induce a variable concentration of carriers along the lattice, which produces diffusion currents and, in turn, internal electric fields. Then, the energy bands undergo a bending, as if an external electric field were applied.

When an electron has reached the lowest possible energy in the conduction band, the only way to keep losing energy is by a recombination, since there are no feasible energy states within the band-gap. In this process, the electron occupies a hole, this is, one of the vacant energy states in the valence band. In order for this to occur, the electron has to release an amount of energy at least equal to the band gap energy, as there is no feasible energy state inside the band gap. This energy release can be produced by either a radiative recombination, by the emission of a *photon*; or by non-radiative recombination, by a *phonon* –a vibration in the lattice that yields to heat losses. Thus, the wavelength of the electromagnetic radiation released, λ, will be determined by the band gap of the semiconductor, E_g, as the energy of an electromagnetic radiation is related to its wavelength, as can be seen from (1.1). In the case of LEDs, this band gap ranges from approximately 1.89 eV for 650 nm emitters and around 3 eV for 450 nm emitters. As it will be mentioned in subsequent sections, the emission spectrum has a relatively narrow bandwidth.

As stated before, recombination may be radiative or non-radiative. A radiative recombination is characterised by a similar kinetic momentum at both the minimum energy level at the conduction band and at the highest energy level at the valence band. This implies that the electron releases energy at the recombination, but not kinetic momentum. This can be satisfied by the emission of a photon. Its wavelength will be determined by the energy released. On the contrary, if the kinetic momentum at the highest energy level at the valence band and the lowest energy level at the conduction band are different, the release of energy cannot be produced by the emission of a photon. This is caused because the electrons have to release energy and kinetic momentum. In such case, the energy is released by a vibration of the lattice, which is known as *phonon*.

Radiative recombinations are predominant in direct-gap semiconductors, whereas non-radiative recombinations are those predominant in indirect-gap semiconductors. Fig. 1.8 shows the *E-k'* (energy-kinetic momentum across the lattice) for direct- and indirect-gap semiconductors.

In Fig. 1.8 it can be seen how the recombination implies a change in both the energy and the kinetic momentum for the Silicon, whereas GaAs features no loss in kinetic momentum and therefore, only the gap energy is to be released.

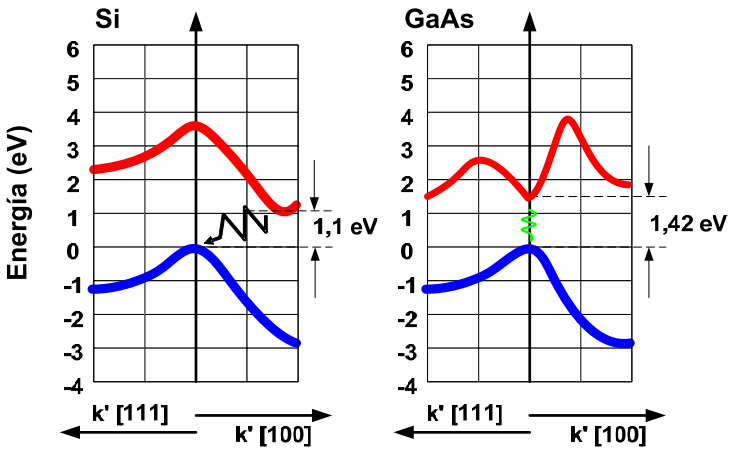

Fig. 1.8. *E-k'* diagram for Silicon (left) and Gallium Arsenide (right).

Nevertheless, by means of an adequate doping, impurities can be introduced in the lattice in order to create deep-level states, which establish an intermediate recombination. This intermediate recombination can happen through a deep level close to the conduction band, where the electrons releases a small amount of energy and its kinetic momentum –an indirect recombination, and in a subsequent recombination, a direct gap may be created, or analogously, an electron can release most of its energy through a direct intermediate recombination from the conduction band to a deep-level state close to the valence band, and subsequently, can lose a small amount of energy and its kinetic momentum by an indirect gap from the deep-level state to the valence band.

1.4.2. III-V Semiconductor Alloys

LEDs are built with alloys between chemical elements of Groups III and V (typically, although there also are II-VI alloys). The most usually employed elements of Group III are Aluminium (Al), Indium (In), or Gallium (Ga), whereas the most usual elements of Group V are Nitrogen (N), Phosphorus (P), or Arsenic (As), among others. These alloys actually form direct-gap semiconductors for a wide range of elements ratio. These alloys are binary, ternary, or quaternary, depending on the amount of chemical elements in the lattice. Ternary elements are the result of the combination between two binary alloys with a common chemical element, whereas quaternary elements are the result of the combination of three binary alloys with a common element or two ternary alloys with two common elements. The most common alloys nowadays are AlInGaP for yellow, amber and red LEDs, InGaN for blue, green, phosphor-converted amber [1.35], phosphor-converted white LEDs, AlGaN or AlInGaN for UV LEDs [1.36], [1.37]. Fig. 1.9 shows the III-V InGaN system diagram with the corresponding band-gap energy, wavelength, and the lattice constant regarding the different ratios between the alloys. The lattice constant indicates the distance between atoms in the crystal lattice. Also, the two most commonly used substrates, besides GaN, are shown: SiC and ZnO.

A keystone in the performance of III-V alloys relies on the correlation between the lattice constant of the binary alloys and the substrate used. In case of a different lattice constant

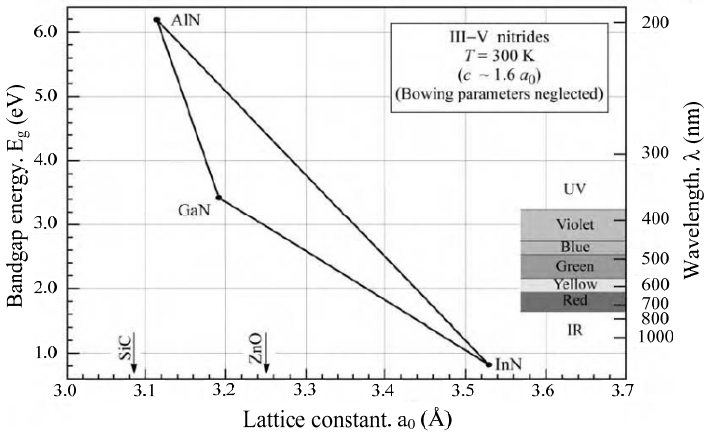

Fig. 1.9. Diagram of the III-V InGaN material.

between the binary elements, there is a lattice mismatch at the interfaces and strong internal electric fields appear, which become centres of non-radiative recombinations.

Theoretically, InGaN chips could reach the entire visible spectrum. However, there are structural issues when a high In ratio is required. Moreover, one of the most interesting features of the InGaN chip is its low sensitivity to high density of lattice dislocations, with no drop in quantum efficiency due to the high lattice mismatch between the substrate, the active layers, and the confining layers that GaN-based chips feature [1.38].

1.4.3. Characteristics of the emission spectrum

The emission spectrum of LEDs depends on the band-gap energy of the active layer, which determines the wavelength of the emitted photon. However, carriers are neither uniformly distributed along the conduction and valence bands nor mainly at the energy levels closest to the gap. The concentration of carriers at the conduction and valence bands is determined by the product of the function of states density, *g(E)*, and the Fermi-Dirac function, *f(E)*. This function accounts for the occupation probability at a certain energy level, where energy levels at lower energy than the Fermi level account for higher occupation probability. This is shown in Fig. 1.10 along with three possible recombinations between different energy levels.

The concentration of carriers has a strong effect on the emission spectrum. Thus, a recombination with a release of energy equal to E_g is rather unlikely, since the concentration of electrons at the lowest energy level within the conduction band and at the highest energy level within the valence band tends to zero. Moreover, the function $g(E)f(E)$ reaches a maximum at the energy level $E_c+1/2kT$ for the electrons, where E_c is the lowest energy level at the conduction band, whilst the maximum for the holes corresponds to $E_v-1/2kT$, where E_v is the lowest energy level at the conduction band. As a consequence of this, the most likely recombination will take place between these two energy levels, and therefore, the peak wavelength would correspond to the energy level E_g+kT. This is shown in Fig. 1.11 for the three recombinations depicted in Fig. 1.10.

Nevertheless, it should be noted that the doping of the semiconductor also affects the emission spectrum, since the presence of impurities may introduce feasible energy states inside the band-gap of the semiconductor which might reduce the effective band-gap of the semiconductor.

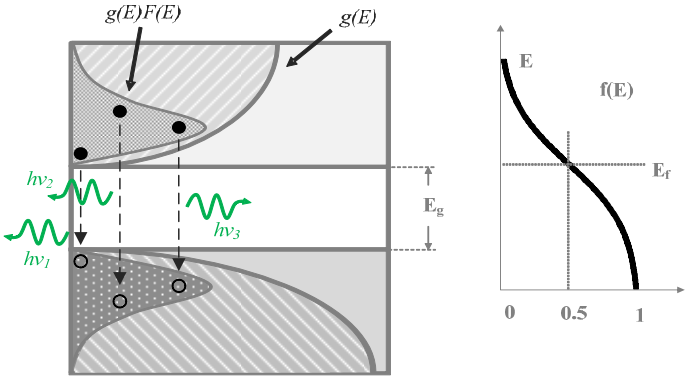

Fig. 1.10. Energy band diagram of a semiconductor. The density of states function, *g(E)*, as well as the Fermi function, *f(E)*, are shown.

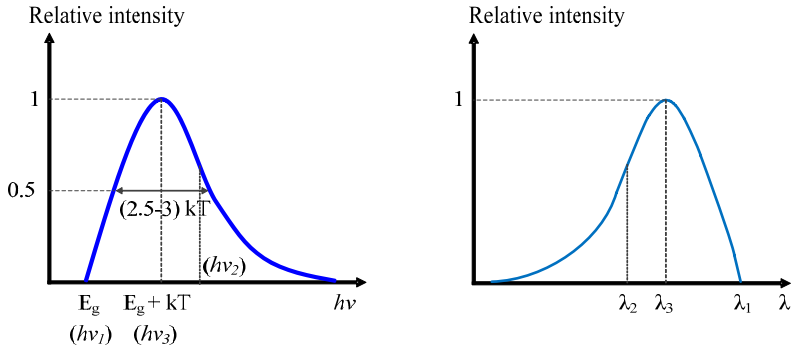

Fig. 1.11. Relative luminous intensity as a function of the energy released in the recombination. Left: Relative intensity versus photon energy, *hν*. Right: relative intensity versus photon wavelength, *λ*.

1.4.4. Double Heterojunctions and Multiple Quantum Wells

A *p-n* junction where the two regions with different doping are made of the same semiconductor material is a homojunction. This kind of *p-n* junctions is characterised by the same band-gap energy for both regions. However, since the photons are released with equal or greater energy than the band-gap energy, they are likely reabsorbed by the other region, thus reducing the quantum efficiency.

In order to overcome this issue, heterojunctions are composed of two different materials for each region, in the way that the active layer has a lower band-gap energy than the other regions. This implies that the photons emitted have always lower energy than the non-active layers band-gap and therefore the absorption is not feasible in those regions, since the absorption of a photon is possible only if it has higher energy than that of the semiconductor band-gap. This structure increases the quantum efficiency. Moreover, as the refraction index of semiconductors depends on the band-gap energy, it is possible to use the neutral regions as light guides. Fig. 1.12 sketches a DH LED built with two semiconductors featuring a different band-gap and the likely recombination, taking place only in the active region. An example of such structure would be an InGaN/GaN LED, where the InGaN band-gap is lower than that of the GaN region and therefore the former acts as the active layer.

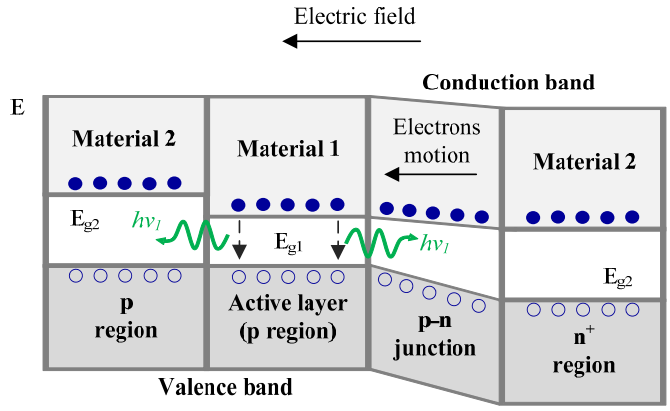

Fig. 1.12. Energy bands in an extrinsic double-heterojunction semiconductor under an external electric field. The different band-gaps are shown.

As a consequence of this effect, most High-Brightness LEDs (HB-LEDs) are built with very thin *p* layers, in order to avoid self-absorption of photons, a heavily doped *n*+ region to create enough electrons, and an active region in between, where light is created, which is either a double heterojunction (DH) or multiple quantum wells (MQWs) [1.39]. In addition, confining layers and electron-blocking layers are located between the DH or MQWs and the doped regions of the chip in order to prevent electrons from escaping the active region. The formers feature an active region that has lower band-gap energy than the rest of the layers. This is also the principle of MQWs [1.37], [1.40], where the active region is composed of several layers of a semiconductor with a lower band-gap energy interleaved with thin layers of a higher band-gap energy in a sandwich-like structure. The layers featuring a higher band-gap energy are known as confining layers, since their higher potential and band-gap energy prevents from diffusion of carriers and absorption of photons, acting as well as light guides.

1.4.5. Characteristics of light emission: droop

The luminous flux emitted by HB-LEDs is highly linear with forward current. However, there is a saturation phenomenon in GaN-based LEDs that arises as the forward current is increased from low values to high values under constant junction temperature operation. This can be seen in Fig. 1.13, where the luminous flux vs. forward current curve of the XLamp XP-G device from Cree is depicted [1.2].

As can be seen, there is a trend towards lowering the slope of the curve as the current is increased. In other words, the higher the forward current, the lower the quantum efficiency of the LED. This phenomenon is called “droop”, and is one of the most important challenges in LED lighting for general purposes, being one of the fields in LED lighting attracting more research efforts. It was firstly attributed to the presence of radiative recombination centres caused by the heterogeneous concentration of In-rich clusters in the active region, which become saturated at high currents. However, it still is a controversial point, with several hypothesis pointed out, such as the leakage of carriers from the quantum wells, which induces a drop of radiative recombinations as the electrons recombine in the *p* region [1.41], [1.42]. Nevertheless, although these effects have been demonstrated, the most popular theory for droop lies on Auger recombination, which is the interaction of an electron and a hole with a third carrier that is propelled to higher energy states, without the emission of light [1.43], [1.44]. Some recent works have put together both theories, obtaining realistic results in simulation [1.45].

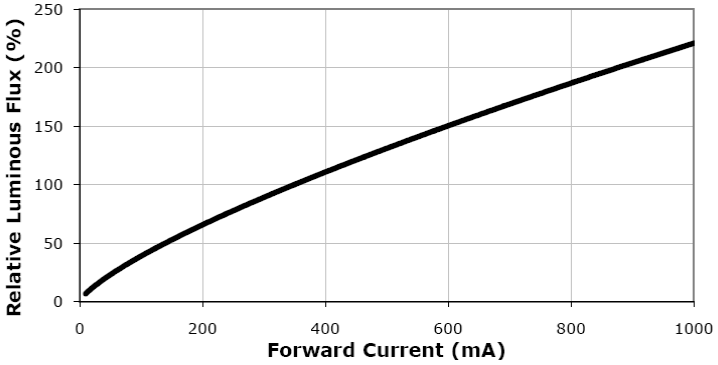

Fig. 1.13. Luminous flux vs. forward current for the XLamp XP-G device from Cree at a junction temperature of 25 ºC.

As a consequence of this effect, the operation current will have to be chosen as a trade-off between efficacy, thermal performance and desired number of emitters.

1.4.6. Electrical characteristic of LEDs

The electric behaviour of LEDs, as well as any other kind of diodes, is far from a resistor-like device. As in regular diodes, the *I-V* curve is determined by the depletion region, where the carriers from the *n* and the *p* region are diffused to the other region prior to recombination. As a consequence of this, there is an internal electric field in the depletion region, namely the diffusion voltage, or built-in voltage. This electric field actually features a "barrier of potential" to be overcome by the carriers in order to reach the opposite region.

When an LED is forward-biased, a qV energy is applied to the depletion region in such a way that the Fermi level of the semiconductor is modified, bringing the energy levels of conduction and valence closer and allowing the injection of carriers to the opposite region, so forward current is increased. In case of reverse-biasing an LED, the energy levels are moved away from each other and thus ceasing the injection of carriers, although a temperature-dependent inverse current caused by minority carriers is kept. This current is called inverse saturation current, I_s. The *I-V* curve of LEDs can be described by the Shockley equation:

$$I_D = I_S(e^{\frac{qV_D}{kT}} - 1) \tag{1.3}$$

Where I_D is the forward current, I_S is the inverse saturation current, and V_D is the applied voltage. Nevertheless, for real diodes, a modification of (1.3) is used, which introduced the ideality factor, η, a parameter that depends on the physical region where the recombinations take place. This parameter ranges from 1 for ideal diodes to more than 6 for GaN-based LEDs.

$$I = I_S e^{\frac{qV_D}{\eta kT}} \tag{1.4}$$

However, this equation would satisfactorily fit an experimental *I-V* curve only for ideal diodes. However, there are several non-ideal and parasitic elements in a real diode. The most comprehensive simplification –not considering capacitive parasitic effects, accounts for the effects of the parallel – due to side recombination across the surface of the chip, and series resistive effects, due to ohmic contacts and *p* and *n* neutral layers:

$$I - \frac{(V_D - IR_s)}{R_p} = I_S e^{\frac{q(V_D - IR_s)}{\eta kT}} \tag{1.5}$$

where R_p is a resistance in parallel to the *p-n* junction and R_s is a resistance in series with R_p and the *p-n* junction. This is shown in Fig. 1.14.

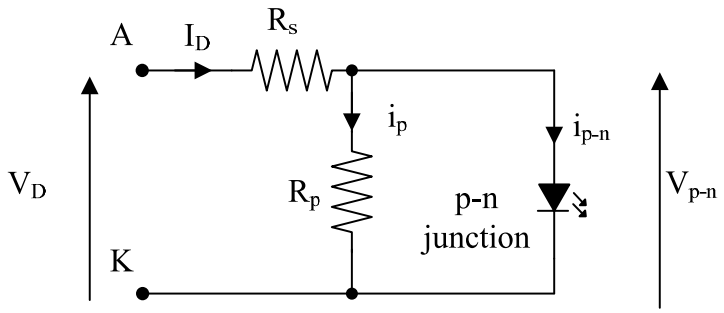

Fig. 1.14. Parasitic effects added: series and parallel resistances, R_s and R_p, respectively.

Finally, it should be noted that the *I-V* curve highly depends on the junction temperature, as will be introduced in the following section.

1.4.7. Influence of junction temperature on the *I-V* curve of LEDs

The temperature in the active region, namely the junction temperature, T_j, is a critical parameter on the performance of LEDs due to its large influence on the efficiency, electric behaviour, and life span. Indeed, the heating in the active region is caused both by the increase of non-radiative recombinations – phonons, and Joule effect in the parasitic elements of the chip.

The effects of the junction temperature could be classified into two main aspects:

- On the one hand, the junction temperature affects the emission spectrum and the quantum efficiency of the LED, and
- On the other hand, the junction temperature affects the *I-V* curve: built-in voltage, inverse saturation current, ideality factor, etc.

Actually, the rise in junction temperature provides the carriers with more energy, inducing a narrowing in the energy gap of the semiconductor. This phenomenon makes the peak wavelength to be displaced towards lower energy levels, i.e. the peak emission is shifted to the red as the temperature is increased. Moreover, as a consequence of the carriers being higher thermally energised, an emission broadening effect is observed [1.46]. It has also been demonstrated that this effect is prevalent over the shift towards lower wavelengths produced by the higher excitation as the current is increased [1.47]. However, in phosphor-converter white LEDs, it has been reported that the effect of the phosphor is prevalent at low forward currents, and therefore a higher shift in the emission spectrum is assumed due to the forward current, with a lower thermal effect [1.48].

In addition, the junction temperature affects the diffusion constant of carriers, the average life of carriers, and the state-density function in both the valence and conduction band. These are all parameters determining the inverse saturation current, which has been extensively reported to be increased as the junction temperature rises. Moreover, the term *kT* also affects the *I-V* curve, as can be seen in (1.5). In conclusion, an increase in the junction temperature will

induce a lower built-in voltage, as the energy gap is reduced, lower parasitic resistances, as carriers have higher excitation, and a lower forward voltage for the same forward current.

1.4.8. Generation of white light in LEDs

There are several approaches to generate white light from the monochromatic light of LEDs, but all rely on the same principle: a mixture of different wavelengths in order to produce excitation in the three different cones of the retina. Therefore, two main strategies may be distinguished: by colour mixture or by wavelength conversion.

Regarding the colour mixture approach, some techniques are:

- By dichromatic devices, where a mixture of two complementary colours is performed, generally blue and yellow.
- By trichromatic or RGB devices, which are employed in screens and in lighting applications were colour tuning and/or high CRI are needed.
- Tetrachromatic and pentachromatic devices, barely used due to their higher complexity, although their CRI is better than that of RGB solutions.

With regard to the wavelength conversion, the three main techniques are:

- Phosphor-converted white LEDs: where light at a given wavelength is emitted by the chip and partially absorbed by a phosphor, which has a broad emission band at higher wavelengths. This is the most common technique and will be discussed later in more detail.
- Semiconductor-converted white LEDs: where a primary active region is electrically excited and the light emitted is partially absorbed by a secondary optically-excited active region, which re-emits the light absorbed at lower energy levels – higher wavelengths.
- Dye-converted white LEDs: where organic molecules are used instead of phosphors in order to perform the wavelength conversion. This solution is rarely used, as dyes lack of long term stability [1.49].

The solution employed in HB-LEDs nowadays is almost exclusively based on phosphor-converted blue LEDs, where a semiconductor emits blue light by electroluminescence and optically excites a monochromatic phosphor that absorbs a portion of the blue light and re-emits light at a broad emission band at higher wavelengths. The most commonly used phosphors are the so-called *garnets*, of which the most usual one is the *YAG* phosphor, an Yttrium-Aluminium garnet. The phosphor doping elements usually are rare earths, rare earth oxides or any other rare earth compounds, Cerium being the doping used for blue chips YAGs. Fig. 1.15 shows the typical emission spectrum of a GaN-based white LED, highlighting the chip emission, the phosphor emission, and the resulting spectra.

The overall efficacy for such technique is higher than 100 lm/W for cool white devices, featuring an acceptable CRI of 70, which rises up to 90 for warm-white commercially-available devices [1.50].

Another approach is the emission in the UV-A range (200 – 320nm) or emission in the UV-C or violet range (320 – 410nm) by AlInGaN/AlGaN- or AlGaN/GaN-based chips and the subsequent conversion by trichromatic phosphors, featuring higher efficacy, colour rendering and thermal stability [1.37]. However, AlGaN/GaN structures still feature important challenges

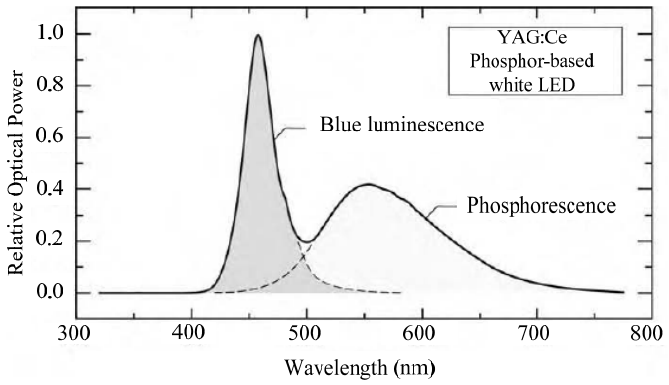

Fig. 1.15. Emission spectrum of a GaN-based White LED with a blue chip and wavelength conversion by a Ce-doped Yttrium-Aluminium garnet.

in terms of lattice mismatch and efficacy, which might be solved by quaternary AlInGaN devices emitting in the near UV [1.52].

1.5. Light-Emitting Diodes as a Power Load

The photometric, electric and thermal characteristics of LEDs are different from any other light source currently available. Moreover, these characteristics vary from one LED manufacturer to other. Therefore, there are several considerations that must be taken into account in order to develop a satisfactory solid-state ligthing luminaire that reaches all the manufacturer claims in terms of efficacy, luminous output, lifespan, and lumen maintenance. Otherwise, LED products will fail in attaining the claimed figures of merit, offering misleading results [1.53].

1.5.1. Issues on supplying LED fixtures

With regard to the photometric characteristics, the highly linear dependency between current and luminous flux that LEDs feature make current-controlled driver the best choice por HB-LEDs, albeit current-limiting circuits are generally used in the lowest-power systems [1.38]-[1.52], [1.54].

Regarding the electrical characteristics, proper supply methods need to account for the *I-V* characteristic of LEDs. As can be demonstrated from the Shockley equation (1.5)-(1.6), the dynamic resistance, i.e. the inverse of the *I-V* curve slope, is very reduced for LEDs, so small variations in forward voltage will induce large variations in forward current. Therefore, it is needed to supply the LED lamp with a current-controlled driver, or at least, to limit the maximum current in order to prevent the forward current to exceed the lamp maximum admisible values [1.55], [1.56].

Concerning the thermal characteristics of LEDs, it is critical for the proper performance of the LED fixture, to account for the thermal behaviour of LEDs. As was explained in Section 1.4.7, the junction temperature has an effect on the built-in voltage and the effective resistance of the chip. This effect implies that, for a given forward voltage, the rise on junction temperature will induce a higher current, which will induce higher heating of the p-n junction, which in turn will produce a rise on the forward current until a thermal equilibrium is reached. If there is no current-limiting circuit, the increase in junction temperature will induce a non-controlled rise in both forward current and junction temperature, even leading to the total failure

of the luminaire. This is sketched in Fig. 1.16 for a generic GaN-based LED at three different junction temperatures, where the highest junction temperature implies a more than threefold forward current.

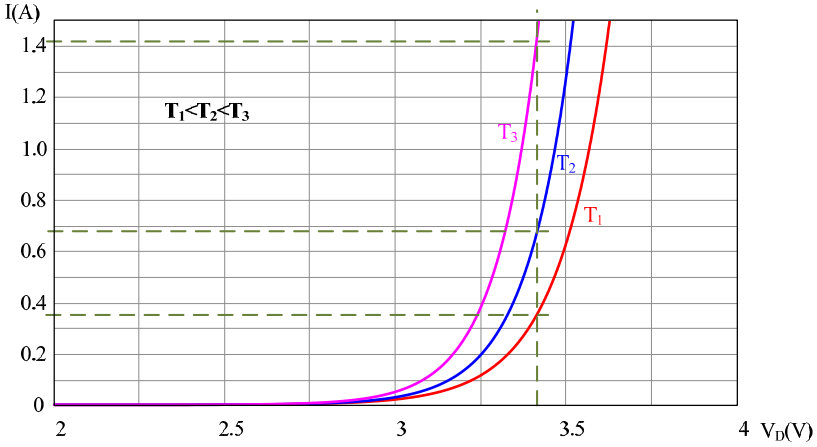

Fig. 1.16. Illustrative example of the theoretical variation of the *I-V* curve with junction temperature for a generic GaN-based LED, T_1 being the nominal operation point.

Manufacturers usually provide the data for the V_D-T_j variation, by either a chart or a parameter that is the slope of the V_D-T_j curve, assumed linear. This parameter, negative, is in the range of few mV/ºC [1.35], [1.50], [1.57], [1.58].

Due to the reasons exposed above, LED lamps are to be supplied by a current scheme, or at least, LED drivers have to implement a current-limiting feature.

1.5.2. Current-control and current-limiting schemes for LED lamps

In order to manage the supply issues of LED lamps exposed in the previous section, several techniques have been developed, either disipiative or non-disipative.

Firstly, the most employed solutions are those implemented by Switched-Mode Power Supplies (SMPS) such as buck-, buck-boost-, and boost-based converters with a proper current-control scheme. The range of application of this topologies covers from low-voltage battery-supplied applications such as Permanent Emergency Lamps [1.8], or automotive applications [1.59], to off-line high-power street-ligthing applications where Power Factor Correction (PFC) is mandatory [1.16]. The most remarkable advantages of these converters are their great flexibility to suit any application or operation mode, such as PFC or dimming, and their high efficiency, even greater than 90%. However, in low-power, low-performance lighting fixtures other driving solutions are used.

If a tigth control of the LED forward current is still needed, a current-regulating dissipative scheme is achieved by the use of either a series or shunt linear regulator. However, only LED lamps with a forward voltage lower than the supply voltage can be used. The main disadvantage of this technique is the low efficiency likely to be achieved, as the linear regulator dissipates the excess of power. Nevertheless, this technique has been employed together with SMPS supplying mid-power LED lamps with several parallelled strings to balance the current through each string. This technique has shown a good performance combined with an adaptive voltage scheme so the power dissipation in the series linear regulator is kept as low as possible [1.60].

Finally, the simplest and most cost-effective dissipative scheme is based on placing a current-limiting resistor in series to the lamp in order to decrease the slope of the *I-V* curve and thus minimise the forward current shift due to forward voltage variations. However, this scheme is valid only for low-power lamps, as a considerable amount of power is dissipated as heat in the resistor [1.55], [1.56]. Other disadvantages are the lack of current regulation and the impossiblity to supply lamps at forward voltages higher than the supply voltage.

1.5.3. LED modelling

Due to the non-linear electrical behaviour of LEDs as a power load, it is necessary to use an adequate model in order to predict large- and small-signal variations at the operation point accurately. Two models are distinguished: small-signal models, which are needed for obtaining the small-signal dynamic model of the LED driver, and large-signal models, which are used to determine the operation point of the LED driver.

1.5.3.1. Large-signal models

These models are used to determine the operation point of the LED driver. The simplest model found in the literature uses the static equivalent resistance of the LED lamp at a single operation point [1.61]. This is, given the forward voltage of the LED lamp, V_D, and the forward current I_D, the equivalent resistance is calculated as:

$$R_{EQ} = \frac{V_D}{I_D} \tag{1.6}$$

However, this model introduces huge errors if used to determine the small-signal dynamics of the converter, as the static equivalent resistance may greatly differ from the equivalent small-signal resistance at a given operation point, this is, the dynamic resistance [1.62]. This model is sketched in Fig. 1.17.

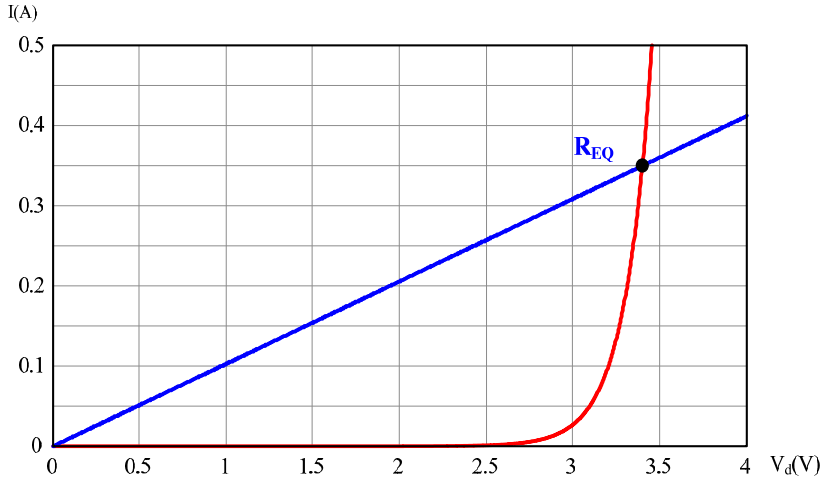

Fig. 1.17. Static equivalent resistance of an LED at the operation point.

The most commonly employed model is the so-called linear model, where the exponential *I-V* curve of the LED is approximated by the combination of a voltage source, which accounts for the built-in voltage and represents the threshold voltage, V_γ, and a series resistor, which represents the dynamic resistance – i.e. the inverse of the *I-V* curve slope, R_D, at high injection

currents [1.56], [1.62], [1.63]. Thus, the output voltage as a function of the forward current, I_D, can be expressed as:

$$V_D = V_\gamma + I_D R_D \tag{1.7}$$

Where the dynamic resistance is calculated as the inverse of the slope of the tangent at the operation point:

$$R_D = \frac{\Delta V_D}{\Delta I_D} = \frac{1}{\tan \alpha} \tag{1.8}$$

However, since R_D is usually calculated at high injection currents, its value will tend to converge to the LED series resistance. This fact will introduce considerable errors for lower currents, as depicted in Fig. 1.18.

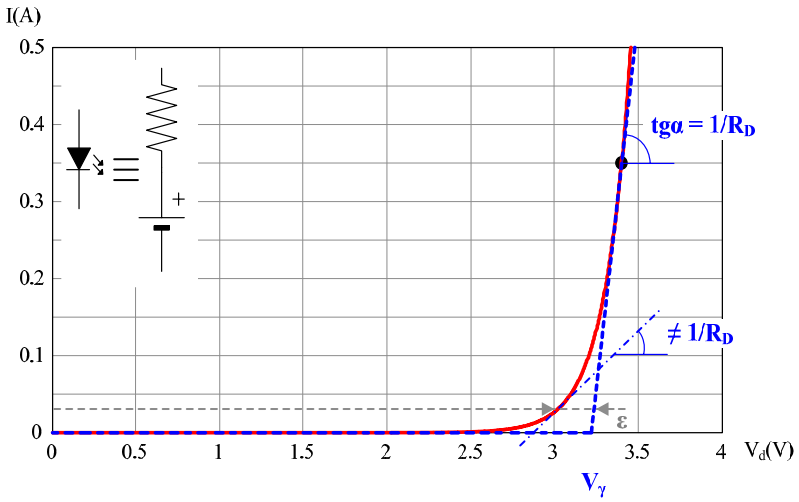

Fig. 1.18. Linear approximation of an LED at the operation point. The mismatch and error between the *I-V* curve and the linear model at low current levels is highlighted. The elements of the linear model are shown in the graph inset.

Fig. 1.18 also shows the slope of the actual *I-V* curve at low currents together with the error ε introduced in order to determine the static operation point at low current levels.

As can be seen from the figure, this approach offers an extremely good approximation at the operation point, but lacks of accuracy at lower current levels, where it shows a noticeable mismatch with the actual *I-V* curve. Therefore, the linear approximation has to be determined for the nominal operation point. However, piece-wise approximations have been developed in order to determine an accurate linear approximation for several operation points [1.63].

1.5.3.2. Small-signal models

Several comprehensive small-signal models have been proposed in order to account for the parasitic effects in the chip, such as parasitic inductances in the wires and leads of the package, series resistance variations due to skin effect and electrical contacts, parallel resistances due to surface recombinations, junction capacitance due to the charge stored in the junction during the forward polarisation, etc [1.64]. These models link not only the optical, electrical and thermal characteristics [1.20], [1.65], but also thermal characteristics of the LED and its internal quantum efficiency [1.21], [1.66]. In the small-signal model proposed in [1.65], the parasitic impedances are considered. This model is shown in Fig. 1.19.

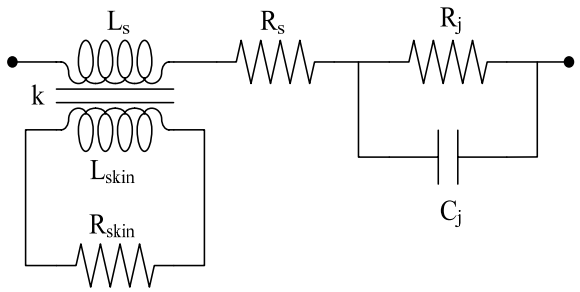

Fig. 1.19. Small-signal model proposed in [1.65].

However, for the high current injection levels used in lighting applications, the dynamic resistance calculated for a given operation point as in the previous section is enough to model the small-signal dynamics of an LED lamp accurately [1.62], [1.63], [1.67], [1.68]. Other publications consider this small-signal approach, but also introduce the effects of the junction temperature on the small-signal behaviour [1.25], where the dynamic resistance is experimentally determined for the DC current and operation point as follows:

$$r_D(\hat{\imath}_{AC}, I_D) = \left.\frac{\hat{u}_{AC}}{\hat{\imath}_{AC}}\right|_{I_D,T_j} \tag{1.9}$$

where r_D is the small-signal resistance, I_D is the output current, $\hat{\imath}_{AC}$ is the AC current perturbation, $\hat{u}_{DC}$ is the measured output voltage perturbation, and T_j is the junction temperature of the LED array.

1.6. Dimming of Light-Emitting Diodes

As already commented, luminous output control, or dimming, is a very interesting feature in multiple applications, not only aimed at energy savings in situations where a lower luminous output is needed, such as in street or general lighting, but also in those applications where the so-called ambiance intelligence is an important issue, where several scenarios are pursued for each single situation by varying the illuminace level, the CCT or both, among others.

One of the most valuable features of LEDs is their high dimmability. This is achieved by several techniques that will be introduced in subsequent Sections, owing to their almost instantaneous light-up and their wide dimming ratio. As a consequence of this capability, a great research effort is currently being developed on this topic for every application, such as in backlighting [1.69]-[1.72], or in general lighting for DC-supplied drivers [1.73], TRIAC-based off-line commercial drivers [1.74], or off-line PFC converters for general illumination [1.75]. The fundamental dimming techniques are presented below.

1.6.1. Analogue dimming

Amplitude-modulated dimming, also known as AM dimming or simply analogue dimming, is the simplest technique to control the luminous output. It is based on the fair linearity existing between forward current and luminous flux. Thus, by varying the DC current with which the LED lamp is supplied, the luminous flux is varied accordingly. Fig. 1.20 shows the luminous flux vs. forward current relation for the Philips Lumileds Luxeon Rebel device [1.50] along with an ideal linear relation between the nominal and lowest forward current levels.

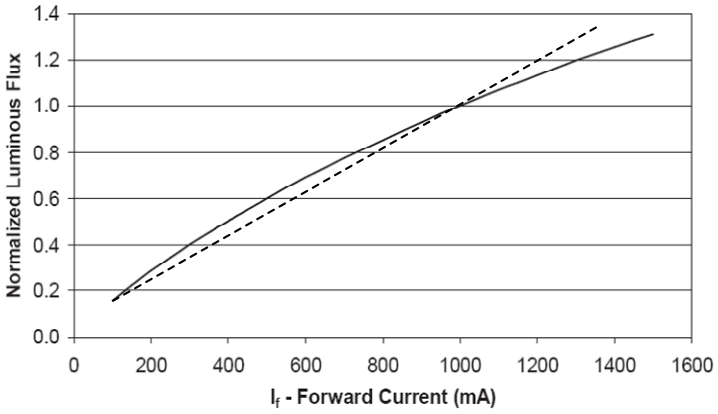

Fig. 1.20. Luminous flux vs. forward current for the Philips Lumileds Luxeon Rebel device at 25ºC junction temperature (solid line). The dashed line represents an ideal linear relation adjusted between the minimum current level and the nominal forward current.

The main advantages of this method rely on its simplicity and cost-effectiveness, being applicable to any LED driver, as it is achieved by just varying the output current reference. Moreover, due to the droop effect explained is Section 1.4.5 [1.39], the efficiency of the LED lamp is increased as long as the output power is reduced, enhancing the energy savings. Another advantage of analog dimming is the absence of EMI perturbances [1.75].

However, this technique features two main disadvantages. On the one hand, there is a shift induced in the chromatic coordinates and in the CRI as shown in [1.76], due to the dependence in drive current that these parameters feature in GaN-based, phosphor-converted LEDs. This chromaticity shift is produced due to both the own GaN chip [1.48] and the phosphor [1.75] response against forward current. To illustrate this issue, Fig. 1.21 shows the chormaticity shift diagram for the Osram Golden Dragon device under constant junction temperature. However,

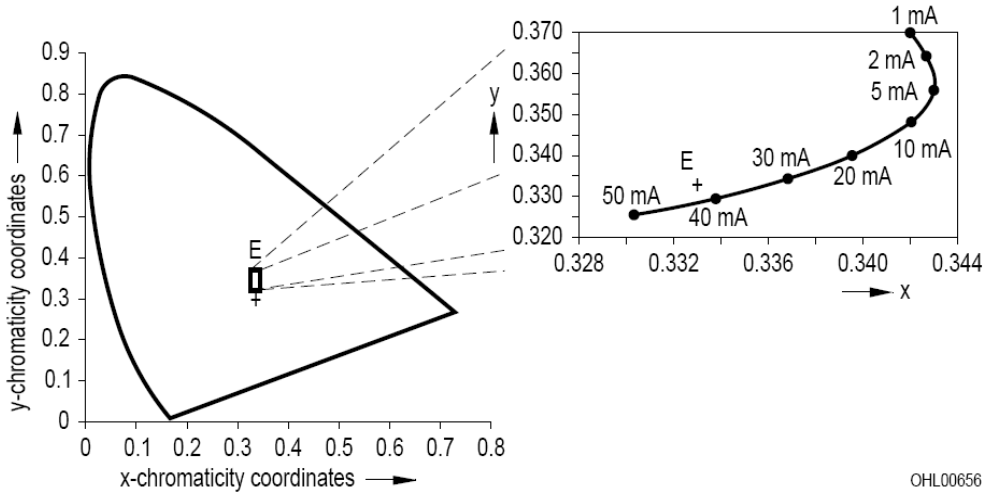

Fig. 1.21. Chromaticity coordinates shift due to changes in forward current for a Golden Dragon device by Osram.

the change in junction temperature derived from a different drive current induces an effect in the opposite direction to that of the forward current, which partially compensates the chromaticity coordinates shift [1.77]. On the other hand, this technique features a lack of linearity due to the

droop effect [1.26], [1.39], the dispersion in electro-optical characteristics at low current levels, which may lead to a luminous flux mismatch within the array, and the difficulties to reach output levels lower than 10% of the nominal due to the *I-V* curve of LEDs [1.78], derived from the problems to sense low-level currents accurately.

1.6.2. Pulse-Width Modulated dimming

As opposed to analog dimming, Pulse-Width Modulated dimming is based on varying the average current level but keeping the peak value constant in order to avoid the chromaticity coordinates shift induced by the forward current change. Thus, the LED lamp is supplied by a current square wave with a peak value which is the same as the DC current level, but by varying the time in which the LED lamp is lit on over the period of the pulse train, the average value of the output current is modified. This is sketched in Fig. 1.22, where the dimming period, T_{DIM}, the lit-on time, t_{ON}, the peak current value, I_D and the average value, I_{AVG} are highlighted.

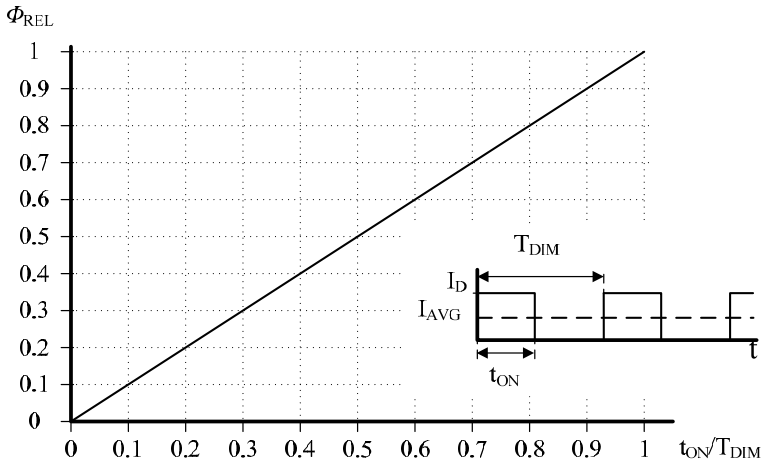

Fig. 1.22. Relative luminous flux as a function of the lit-on time of the Pulse-Width Modulation technique. The pulse train current is shown in the graph inset, where the dimming period, the lit-on time, the peak current value, and the average value are highlighted.

If this pulse train has a frequency higher than the *critical flicker fusion frequency* (CFFF), the human will perceive a decrease in the luminous intensity which is proportional to the square wave average value, instead of the flicker [1.48], [1.75], [1.76]. This CFFF is generally considered between 35 and 40 Hz [1.79], although depends on several biological factors. However, the minimum dimming frequency recommended is 120 Hz in order to avoid or at least minimise the stroboscopic effect [1.75], although higher frequencies are recommended by authors: 200 Hz [1.48], 300 Hz [1.80], [1.83], or even 400 Hz in screen and video recording [1.79]. Moreover, dimming frequencies above 20 kHz are also recommended in order to avoid the undesirable effects of low-frequency PWM dimming, such as non-visible flicker [1.82], stroboscopic effect in moving objects [1.75], or audible noise [1.75], [1.83].

As the peak current is kept constant, this technique is intended to minimise the chromaticity coordinates shift, although this characteristic is still affected by the junction temperature [1.26], so the chromaticity coordinates shift is actually reduced but not completely avoided [1.77]. Other advantages are a higher linearity between dimming reference and luminous output, and higher dimming ratio [1.26].

A combination of both AM and PWM dimming called "Bilevel Current Driving Technique" is intended to enhance the colour stabitility of LED lamps [1.85].

Dimming of LEDs will be covered in more detail in Chapter 6.

1.7. Commercially-available LEDs

LEDs exhibit an extremely high flexibility for several applications. However, different kinds of devices may be classified according to the nominal power or their package. In this way, the different kinds of LEDs could be classifed as follows:

1.7.1. Low- and mid-power LEDs

These LEDs, also known as signalling LEDs, or Superflux LEDs, among others names, are characterised by a current level in the range of tens of milliamps, but always lower than few hundreds of milliamps, typically lower than 150 mA, although LEDs operating at such currents are also known as mid-power LEDs. The power dissipation is usually limited to the range of tens to few hundreds of milliwatts. Examples of this kind of LEDs are the TopLED by Osram –up to 50 mA, Superflux by Philips Lumileds, Seoul Semiconductor, Everlight or Cree –up to 70 mA, SnapLED by Philips Lumileds, Everligth or Cree –up to 150 mA, Z-Power P9, by Seoul Semiconductor –up to 150 mA, etc. Fig. 1.23 shows some of these devices.

Fig. 1.23. Low-power LEDs. Left: Superflux LEDs by Philips Lumileds. Centre: TopLED by Osram. Right: SnapLED by Philips Lumileds.

These emitters are available in red/amber colour for automotive applications as well as in white colour, reaching efficacies up to 80 lm/W for the AlInGaP devices and 100 lm/W for the InGaN ones.

1.7.2. 1 W LEDs

These LEDs, also known as Power-LEDs (P-LEDs) or High-Brightnes LEDs (HB-LEDs) are characterised by a 1 mm^2 chip, which is GaN-based for white, green and blue devices, and AlInGaP-based for yellow, amber and red emitters. The nominal operation current of these devices is 350 mA, which yields to a power dissipation around 1 W at 25 ºC junction temperature. That is the reason why these LEDs are called "1W LEDs", although these devices generally have operation currents up to 1000-1500 mA, which corresponds to power dissipations around 5 W. These LEDs were the first commercially available devices in breaking through the 100 lm/W barrier, corresponding this figure of merit to the Z-Power P4 by Seoul Semiconductor. Examples of such devices are the Luxeon K2, Luxeon A, Luxeon C, and Luxeon Rebel by Philips Lumileds, XLamp XR-E, XLamp XP-E, or XLamp XP-G by Cree, Z-Power P4, Z-Power P8, or Z-Power Z1 by Seoul Semiconductors, NVSW by Nichia, among many others. Fig. 1.24 shows some of these devices together with the dimensions of the Z-Power P4 by Seoul Semiconductor.

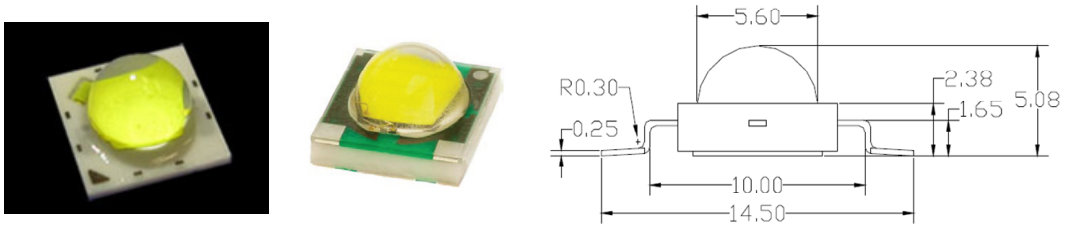

Fig. 1.24. Power-LEDs. Left: NVSW by Nichia. Centre: XLamp XP-G by Cree. Right: dimensions of the Z-Power P4 by Seoul Semiconductors, in mm.

Currently, these kind of LEDs perform efficiencies above the 100 lm/W barrier, such as the XLamp XP-G by Cree [1.2].

1.7.3. High-Power LEDs

These kind of LEDs have recently been developed in order to overcome one of the biggest issues of P-LEDs, namely, the relative cost per lumen derived from the large number of emitters in order to fulfill the lumen requirements for the highest power applications. In this way, one of the first devices in being launched was the Diamond Dragon by Osram, consisting of a larger chip and capable of withstanding up to 2 A, which leads to a total power dissipation up to 7 W, and emitting 311 lm at 1400 mA. Afterwards, multi-chip devices become available, consiting of multiple single chips in the same package. Two examples are, on the one hand, the XLamp MC-E by Cree, composed by four 1 mm^2 chips and emitting up to 700 lm at 10 W – 2800 mA if the chips are connected in parallel. On the other hand, the High-Power Multi-Chip emitters, composed of several parallel strings of a number of chips in series. Some examples of the latter are the Sharp Mega Zenigata, featuring 38 V at 1 A; the Bridgelux devices, where the most powerful device, the RS Array, reaches 100 lm/W typical luminous efficiency at 85 W power dissipation, or the Altilon by Lumileds, especially intended for forward-lighting automotive applications. Fig. 1.25 shows three of these devices.

Fig. 1.25. High-Power LEDs. Left: RS Array by Bridgelux. Centre: Diamond Dragon by Osram. Right: XLamp MC-E by Cree.

These devices were especially suited, optimised, and intended for the higher power applications, such as retail ligthing, commercial down lights, high bay, outdoor and street lighting, etc.

1.7.4. Other Power-LEDs

Other Power-LEDs refers to those that are not classifiable within one of the previous types. This can be applied to multi-chip LEDs featuring special characteristics. An example of this are the Acrich or Acrich2 devices, AC LEDs by Seoul Semiconductor; or High-Voltage 1W LEDs, such as the HV LED by Everlight or the XLamp XM-L High Voltage by Cree, shown in Fig. 1.26.

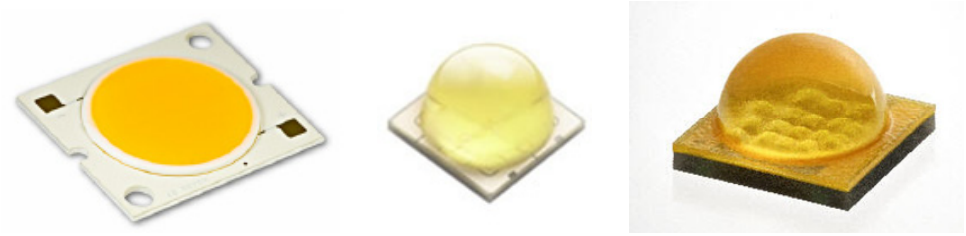

Fig. 1.26. Other Power-LEDs. Left: Acrich2, AC LED by Seoul Semiconductors. Centre: HV LED, high voltage device by Everlight. Right: XLamp XM-L, high voltage LED by Cree.

The AC LEDs by Seoul Semiconductor are directly plugged to the mains supply, operating at 100-110/220-230V - 50/60Hz. This is achieved by an antiparallel connection of two strings of several series LEDs. These devices feature a luminous output up to 700 lm in warm white at 120 V_{rms} and 15 W power consumption, available in different packages and arrays, including Chip on Board (CoB) packages.

The high-voltage LEDs are especially intended for halogen-donwligths retrofits, where the energy conversion from the mains voltage down to few volts may induce serious efficiency and/or performance constraints. These LEDs generally are 1 W to 4 W devices operating at voltages around few tens of volts and currents in the range of tens of milliamps. The HV LED by Everlight features 20 mA or 40 mA operating currents at differents forward voltages: 47-55 V or 95-111 V at 20 mA, leading to 1-2 W power consumption, and 95-111 V at 40 mA, leading to 4 W power consumption. The efficacy of such devices approaches 100 lm/W for the 1 W device. The XM-L device by Cree nominal operation is 46 V at 44 mA, emitting up to 240 lm and at efficacies above 100 lm/W. The maximum power consumption of such device is 6 W.

1.8. Binning & Labelling

Binning and labelling refers to the characteristics variation that LEDs feature within the same manufacturing process. As with any other process or technology, semiconductor technology is subject to variations in the process that lead to a range in performance that is Gaussian or approximately Gaussian [1.34] around the typical value. Fig. 1.27 sketches the distribution of devices vs. the relative performance over a typical value, applied to the luminous flux.

In order to provide the designers with a useful tool to design LED fixuters, manufacturers usually classify –"bin" their products according to their relative performance in terms of luminous flux, chromaticity coordinates, forward voltage, CCT, and CRI, into several ranges. Thus, Fig. 1.27 sketches 5 bins for luminous flux for the Luxeon K2 device, where the higher production volume corresponds to the typical bin, and the extreme values correspond to the higher and the lower performance bin, as a Gaussian distribution implies. However, some

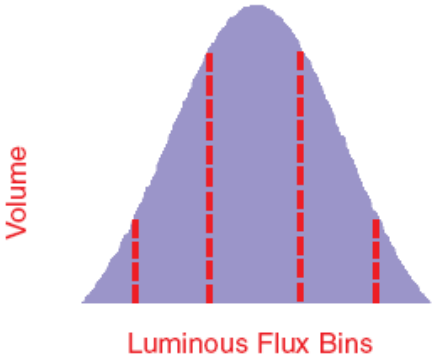

Fig. 1.27. Luminous flux vs. production volume for the Luxeon K2 device by Philips Lumileds [1.34].

manufacturers do not offer a tight binning or binning at all for some features such as forward voltage or luminous flux.

1.9. LEDs selected for this work

Four LEDs from different manufacturers were chosen in order to compare their figures of merit and also the deviations in performance of the LED driver that different devices would introduce. These LEDs are:

- Golden Dragon Plus by Osram [1.57],
- Luxeon K2 with TFFC by Philips Lumileds [1.34]–nowadays discontinued and replaced by the Luxeon Rebel [1.50],
- Z-Power P4 by Seoul Semiconductor [1.84], and
- XLamp XR-E by Cree [1.58],

as they were the most efficient commercial LEDs available, with an efficacy around or greater than 100 lm/W. In addition, the construction of LED luminaires with discrete emitters instead of with a multichip high-power array has been an extended trend in Street Lighting in recent years. This configuration introduces some benefits regarding the aesthetics and freedom of design, since custom designs are easily achievable. Their main characteristics are gathered in Table I.II showing, among others, the typical luminous flux at the test current, thermal resistance, typical forward voltage, maximum current, thermal resistance, and forward voltage bin, as this is an interesting parameter in order to design the output voltage of the LED driver and if parallelled strings are required.

1.10. Conclusions

This chapter presented an overview about general topics in lighting, and solid-state lighting in particular. The fundamentals on lighting and light emission mechanisms have been covered, highlighting the various kinds of commercially available lamps assorted by their emission mechanism. Finally, a rough classification on commercial devices is provided, covering practical issues such as the binning and labelling performed by manufacturares, and introducing the four devices that have been employed for the development of this work.

LEDs are to be supplied according to their *I-V* curve and its photometric characteristics. This way, and as has already been stated in this Chapter, small changes in forward voltage lead to huge changes in forward current, whereas the forward current determines the luminous

output. In addition, the junction temperature also affects the forward voltage for a given forward current. As a consquence of this, DC current-controlled electronic drivers are needed, either switched-mode for high-performance, high power applications, or dissipative regulators or at least current-limiting ballasts, for low-performance, low-power applications. With regard to the photometric characteristics, the luminous output of LEDs feature a highly linear dependence on forward current, although there is a lose of linearity for high currents, phenomenom known as "*droop*". This implies that the driving current has to be chosen as a trafe-off between number of emitters – and subsequently cost, and efficiency. Regarding the thermal effects on LEDs, and besides the shift on forward voltage that the junction temperature introduces, the chromatic coordinates are affected, the life span is reduced and an excessive temperature eventually leads to the device failure. Therefore, there is a high need for a proper thermal design in order to assure a maximum junction temperature not just below the absolute maximum junction temperature, but within a given range that optimises the trade-off between efficiency, life span and size and cost of the lighting fixture. Therefore, a proper LED fixture design must account for cost, efficiency, reliability and size in order to set the forward current and junction temperature so a trade-off between those parameters is achieved.

TABLE I.II.
MAIN CHARACTERISTICS OF THE LEDS UNDER STUDY

Characteristic	**LED**			
	Golden Dragon Plus	***Luxeon K2 with TFFC***	***Z-Power P4***	***XLamp XR-E***
Part	LUW W5AM KYLX-6P7Q	LXK2-PWC4-0200 TW0H	SSCW42180U2-SVOH	XREWHT-L1-0000-00D01
***Test current* (mA)**	350	1000	350	350
***Maximum Current* (mA)**	1000	1500	1000	1000
***Luminous Flux* (lm)**	82 - 97	95 (typ.@350mA)	100 - 109	107 – 114
Luminous Flux Bin	KY	0200	U	Q5
***Thermal Resistance* (K/W)**	11	5.5	6.9	8
***CCT* (K)**	6500 (typ)	6500 (typ.)	6300 (typ.)	5000-10000
CRI		-	70 (typ.)	75 (typ.)
***Typical Forward Voltage* (V)**	3.2	3.65	3.25	3.3
***Typical Forward Voltage at 350mA* (V)**	3.2	3.3	3.25	3.3
Forward Voltage Range	2.7 – 3.8	3.03 – 4.71	2.9 - 4	3.9 (max)
Voltage Bin	-	H (3.99 – 4.23)	H (3 – 3.25)	-
***Forward Voltage Thermal Coefficient* (mV/ºC)**	-	-2.8	-	-4 (@350mA)
***Maximum Junction Temperature* (ºC)**	125	150	145	150

Table I.II shows the LEDs parameters at the test current, unless otherwise specified.

Concerning the regulation of the luminous output, i.e. dimming, there are basically two main techniques that have been covered: AM dimming and PWM dimming. The advantages of AM dimming lie on its simplicity and low cost, and lamp improved efficiency at low current levels. However, the dimming ratio and linearity is lower than those of the PWM, and the chromaticity coordinates are effected by the change in current and junction temperature.

Nertheless, these effects have been reported to mitigate each other. On the contrary, PWM dimming presents a higher dimming ratio provided that an adequate control scheme is implemented and the linearity is somewhat higher, but generally needs extra circuitry and the chromaticity coordinates are affected by the junction temperature shift. Therefore, the adoption of each technique will have to be evaluated for each lighting project, according to the particular requirements of the given application.

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Chapter 2

Light-Emitting Diodes Modelling

In this chapter, the thermal characterisation of four commercially-available GaN-based phosphor-converted white LEDs from the most representative manufacturers will be covered in order to test their electrical behaviour and its dependence on temperature. Firstly, the parasitic effects of a p-n junction will be discussed in Section 2.2 in order to determine the best fitting curves for the I-V characteristic. Afterwards, the properties of the LEDs under study will also be introduced. The thermal dependence of the I-V curve and the dynamic resistance will also be covered in Section 2.3. In Section 2.4, different considerations about the dynamic resistance, such as its derivation from the I-V and the linear model, will be discussed.

Section 2.5 will briefly list the different methods for determining the junction temperature of an LED lamp. Section 2.6 will describe the procedure for determining the I-V characteristic for a wide range of junction temperatures, which is considered one of the most accurate methods for the junction temperature estimation. Then, Section 2.7 will introduce the electrical properties of the LEDs under study for obtaining the statistical significance of the tests.

Section 2.8 will cover the I-V and V_D-T_j test performed, introducing the workbench, and exposing the obtained experimental results, also studying all the parameters considered in the curve fitting procedure. Section 2.9 will introduce the R_D-T_j analysis, describing the experimental procedure and the workbench developed for the laboratory tests, and discussing the experimental results. In this Section the implications of the dynamic resistance shift will be discussed by an illustrative example of a generic LED driver.

Finally, Section 2.10 will summarise the conclusions achieved in this work

2.1. Introduction

Light-Emitting Diodes (LEDs) have become an outstanding technology in lighting due to their extremely long life span –several thousands of hours for a lumen maintenance of 70%, i.e. L70 [2.1], [2.2], under the IES LM-80-08 procedure [2.3], and their continually increasing luminous efficacy, which has recently overcome that of CFLs and Metal-Halide lamps.

Nowadays there is a growing trend towards replacing existing solutions with LED lamps in many applications, e.g. indoor lighting [2.4], automotive lighting [2.5], street lighting [2.6], architectural lighting [2.7], etc. However, the electrical behaviour and life span of LEDs greatly differ from that of incandescent bulbs or discharge lamps, such as Compact Fluorescent Lamps (CFLs), which are widely spread in general and indoor lighting. This has given rise to the need for different strategies in order to develop suitable, reliable, and cost-effective LED drivers while accounting for the non-linear electrical behaviour of LEDs. In this way, several works have been developed in order to achieve a deeper insight into their behaviour as a power load, such as [2.8]-[2.10]; or into the existing link between their thermal, optical and electrical characteristics as a non-linear lighting device [2.11]-[2.14].

Due to the non-linear electrical behaviour of LEDs, it is very important to consider an accurate model in order to design an LED driver properly. As it has been discussed in Chapter 1, the simplest choice is the equivalent resistor at the operation point. However, this approximation is valid only for the operation point, leading to errors in a small-signal analysis [2.9]. The most usually employed model in designing LED drivers is the linear approximation [2.9], [2.10], as previously introduced in Chapter 1. Besides, as the junction temperature affects their *I-V* curve lowering the voltage drop for a given injected current as the temperature rises, it is widely assumed that the best control technique for power LEDs relies on a current-controlled scheme [2.15].

As a result of thermal effects on the *I-V* curve of LEDs, the operation point of closed-loop converters will undergo small variations around the operation point. Moreover, the forward voltage variation affects the DC gain of the duty-ratio to LED-current small-signal transfer function, and in the case of buck-boost- and boost-based converters, the right half-plane (RHP) zero is also affected [2.9]. Manufacturers usually provide the designers with the temperature coefficient for the forward voltage related to a junction temperature of 25 ºC, so the expected forward voltage can be calculated using:

$$V_D = V_D(25ºC) + k(T_j(ºC) - 25) \tag{2.1}$$

where k is the temperature coefficient of forward voltage, i.e. $\partial V_D/\partial T_j$. Nevertheless, there are few studies about the thermal effects on the LED dynamic resistance, such as [2.16]. These variations could likely have a great impact on the closed-loop dynamics, depending on this parameter temperature sensitivity. Therefore, the need for a better understanding of LEDs small-signal behaviour and its junction temperature dependency arises.

This Chapter will study the thermal characterisation of LED diodes, focusing on the dynamic resistance change related to the junction temperature of the four commercial devices from the most representative manufacturers considered in this work and already introduced in Chapter 1: Osram Golden Dragon Plus [2.17], Lumileds Luxeon K2 with Thin Film Flip Chip (TFFC) [2.18], Seoul Semiconductors Z-Power P4 [2.19], and Cree XLamp XR-E [2.20]. The four devices are GaN-based, phosphor-converted cool white LEDs featuring a luminous efficacy around or greater than 100 lm/W. Their main characteristics are recalled in Table II.I, where T_j

is the maximum junction temperature, I_D is the maximum forward current, $R_{\theta jc}$ is the junction-to-case thermal resistance, and k is the temperature coefficient of forward voltage, as extracted from the datasheets [2.18], [2.20].

TABLE II.I:
MAIN TYPICAL CHARACTERISTICS OF THE LEDS UNDER TEST

LED	T_j *(max.)* (ºC)	I_D *(max.)* (A)	$R_{\theta jc}$ (ºC/W)	k (mV/ºC)
Golden Dragon Plus	125	1.0	11 (max.)	Chart [2.17]
Luxeon K2 with TFFC	150	1.5	5.5	-2.8
Z-Power P4	145 (@0.7A)	1.0 (@90ºC)	6.9	Chart [2.19]
XLamp XR-E	150	1.0	8	-4

The lamps built for this study feature a power level in the range of 60-70 W, with an output luminous flux around 5,000 lm, as this is an adequate power level for many street-lighting applications and several indoor/outdoor commercial uses [2.21], [2.22]. Also, single LEDs will be tested. Even though nowadays there are multi-chip devices at power levels up to 100 W or higher, specifically designed for street-lighting, single-chip LEDs are still suitable for making LED lamps in the mid-power range.

2.2. Effects of the parasitic elements on the *I-V* Curve

As introduced in Chapter 1, Section 1.3.1.6, the Shockley equation states the ideal *I-V* curve of a *p-n* junction under high forward voltage bias conditions, which also applies to the DH (double heterojunction) and MQW (multiple quantum wells) LEDs structure described in Chapter 1, Section 1.4.1.4:

$$I_D = I_S e^{\frac{q}{\eta k_B T} V_D} \tag{2.2}$$

where I_S is the reverse saturation current, q is the electron charge – $1.602 \cdot 10^{-19}$ C, η is the ideality factor, k_B is the Boltzmann constant – $1.381 \cdot 10^{-23}$ J/K, and T_j is the *p-n* junction temperature in K. However, in a real diode, there are several non-ideal and parasitic elements. The most comprehensive simplification not considering capacitive parasitic effects accounts for the parallel resistive effect, due to side recombination across the surface of the chip, and the series resistive effect, due to ohmic contacts and *p* and *n* neutral layers [2.23]:

$$I_D = \frac{V_D - R_S I_D}{R_p} + I_S e^{\frac{q}{\eta k_B T}(V_D - I_D R_S)} \tag{2.3}$$

where R_p and R_s are the parallel and the series resistance, respectively. The model considering this parasitic effects is shown in Fig. 2.1.

The parasitic effects due to side recombinations across the surface of the chip would introduce the same phenomenon as if a resistor were placed in parallel to the *p-n* junction, thus enabling an additional path for the current to flow across the chip for forward voltages below the built-in voltage of the semiconductor. Nevertheless, it is assumed that the effect of the parallel resistance might be negligible in HB-LEDs [2.24]. In order to check this statement, the influence of the parallel resistance on the *I-V* curve of an LED will theoretically be calculated.

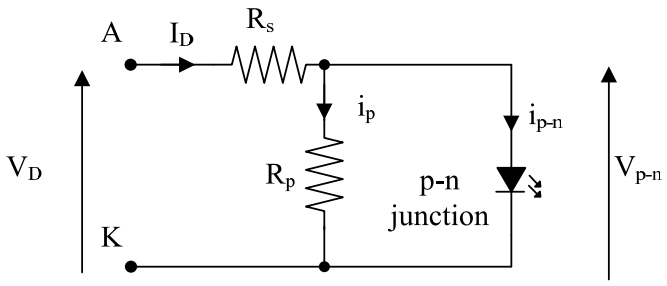

Fig. 2.1. Non-idealities of a *p-n* junction: series and parallel parasitic resistances.

Thus, a hypothetical LED with parameters likely to be found on commercial devices such as an reverse saturation current of 10^{-12} A and an ideality factor of 6, with no series resistance, will be used for determining the *I-V* curve for several parallel resistance values ranging from 10 Ω to 100 kΩ. In this way, the curve of the ideal diode could be plotted by using (2.2). Regarding the current across the parallel resistance, I_P, the following expression can be used:

$$I_P = \frac{V_D}{R_P} \tag{2.4}$$

In addition, the expression for the *I-V* curve of the *p-n* junction featuring parallel resistance can be obtained from (2.3) by making the series resistance equal to zero:

$$I_D = \frac{V_D}{R_P} + I_S e^{\frac{q}{\eta k_B T}(V_D - I_D R_S)} \tag{2.5}$$

The semilog plots of the *I-V* curves for the ideal diode as well as for the parallel resistance and the device including the parallel resistance are depicted in Fig. 2.2

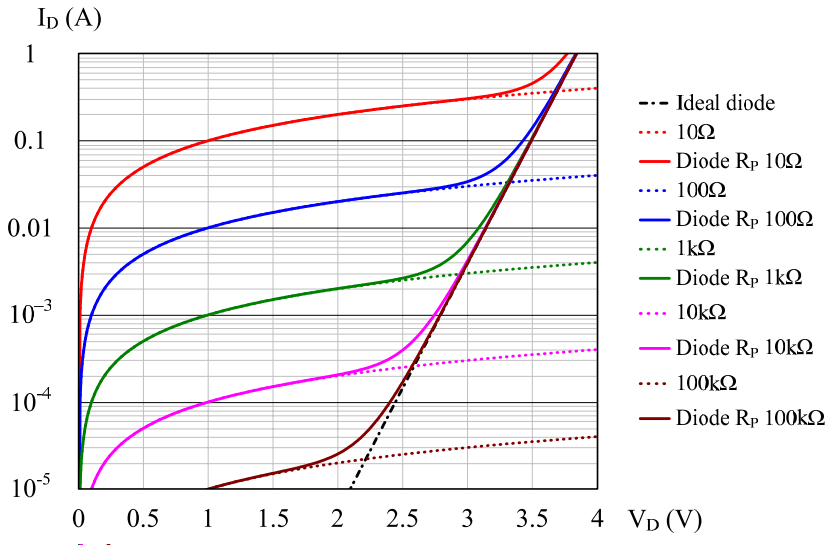

Fig. 2.2. Semilog plot of the *I-V* curve with parallel resistance (solid lines), parallel resistance (dotted lines), and ideal diode (dashed lines) for different parallel resistance values.

As can be seen, only low parallel resistance values in the same order of magnitude as the equivalent resistance of the LED will affect the *I-V* curve. Indeed, as can be seen from Fig. 2.2, for a forward voltage of 3.5 V, the forward current is 0.1 A giving 35 Ω of equivalent resistance

and only the 10 Ω parallel resistance induces a noticeable effect on the *I-V* curve. Moreover, the 100 Ω resistance does affect the curve, but to a much lesser extent, whereas parallel resistance values from 1 kΩ and above only affect the *I-V* curve for current values below few tens of milliamps. In conclusion, due to the forward current levels that will be employed for both the experimental characterisations and the nominal operation of the LED lamps, and provided that the parallel resistance for commercially-available HB-LEDs is much larger than the series resistance [2.23], the effect of the parallel resistance for the subsequent calculations and fittings can be neglected without any negative effects on accuracy.

With regard to the ohmic behaviour of contacts and the intrinsic resistance of cladding layers, *p* and *n* regions, and current-spreading layers, among others, a series-resistance effect appears. The presence of such a parasitic element will introduce a two-fold effect on the performance of LEDs. On the one hand, the optical efficiency of the LED will decrease as long as the forward current is increased as a consequence of a higher fraction of the input power being dissipated on the series resistor instead of on the *p-n* region, with the additional issue of higher junction temperatures due to extra losses. On the other hand, the *I-V* curve of the LED will be affected since a higher voltage drop will be produced due to the contribution of such a parasitic element. This will also produce more heating due to the power dissipation generated at the ohmic layers, with an effect on the forward voltage drop, which could be more or less pronounced depending on the physical situation of the parasitic elements [2.14], [2.25]. Since the former effect has been exhaustively reported in literature [2.14], [2.25]-[2.27] and is out of the scope of this work, only the latter effect will be taken into consideration in order to determine the optimal fitting of the experimental curves obtained in the laboratory tests.

In order to check the effect of the series resistance on the *I-V* curve of an LED, the same procedure will be followed. Thus, for the same theoretical diode, the effect of a series resistance R_S will be calculated for values ranging from 0.05 Ω to 10 Ω. As the previous case, the ideal curve of a diode defined by (2.2) is plotted. Regarding the effect of the series resistance, by neglecting the term related to the parallel resistance in (2.3), the following expression is obtained:

$$I_D = I_S e^{\frac{q}{\eta k_B T}(V_D - I_D R_S)} \tag{2.6}$$

However, this non-linear expression introduces computational issues. Further rearrangement of (2.6) leads to:

$$V_D = R_s I_D + \frac{\eta k_B T}{q} \cdot ln\left(\frac{I_D}{I_S}\right) \tag{2.7}$$

which allows the *I-V* curve to be determined with a lower computational burden [2.29]

The semilog plots of the *I-V* curves for the ideal diode and the effect of adding several values of series resistance are depicted in Fig. 2.3.

As can be seen from the figure, the effect introduced in the *I-V* characteristic is a rise in the forward voltage as a result of the addition of the voltage drop due to the *p-n* junction –i.e. the ideal diode, and the voltage drop in the series resistor. Moreover, even low-value series resistors will induce a noticeable effect on the *I-V* curve for the forward current range that will be taken into account in both the laboratory experimental tests and the nominal operation of the LED lamp. Therefore, it can be concluded that the series resistance effect is to be taken into account for subsequent calculations and fittings of the experimental *I-V* curve.

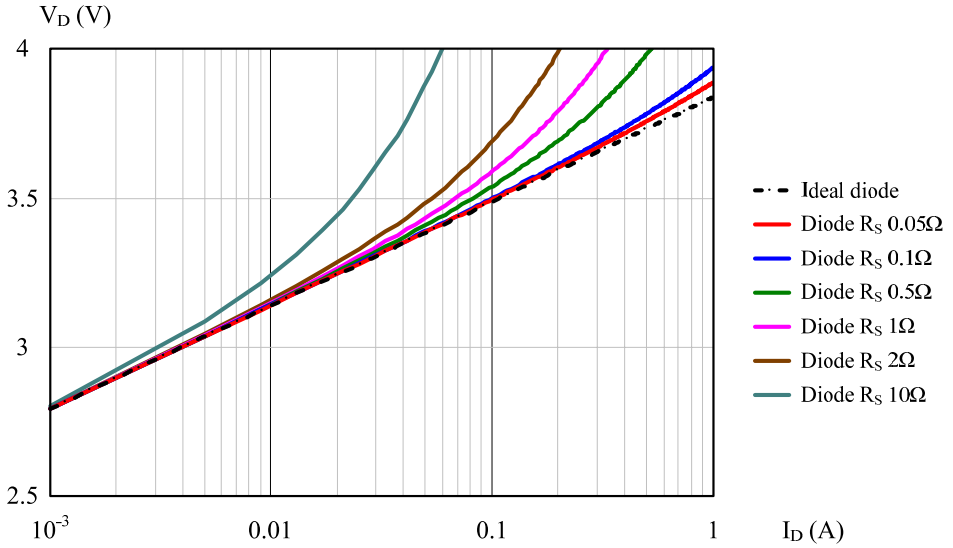

Fig. 2.3. Semilog plot of the *I-V* curve with series resistance (solid lines), series resistance (dotted lines), and ideal diode (dashed lines) for different series resistance values.

In addition, it can be concluded that the term related to the parallel resistance in (2.3) can be neglected, as this parasitic element is higher than the series resistance by several orders of magnitude. Therefore, the current through the *p-n* junction will virtually be the forward current. Thus, it can be assumed that (2.7) will accurately determine the *I-V* curve for the current range that will be taken into account in the experimental tests.

2.3. Effects of the Junction Temperature on the *I-V* curve.

The effect of the junction temperature on the *I-V* curve can be inferred from the study of the Shockley-derived equation accounting for the parasitic effects (2.3). As can be seen, it is directly affected by the junction temperature. In addition, other parameters that are temperature-dependent are also present. Thus, the reverse saturation current depends on the carriers diffusion constants, the bandgap energy, and the effective density of states, all temperature-dependent [2.28], [2.30]. In addition, the ideality factor is also a temperature-dependent parameter in GaN-based devices [2.24]. Moreover, the parasitic resistances are likely dependent on temperature as a consequence of the effects of increasing temperature on charge carriers –further activating them in *p*-type materials [2.24], and contacts, reducing their parasitic resistance.

2.4. Considerations on the dynamic resistance

The calculation of the dynamic resistance for each operation point is obtained by straightforward derivation of (2.7) with respect to the forward current:

$$R_D = \frac{\partial V_D}{\partial I_D} = R_S + \frac{\eta k_B T}{q} \cdot \frac{1}{I_D} \tag{2.8}$$

The effect of the series resistance on the dynamic resistance is illustrated in Fig. 2.4 for the ideal *p-n* junction considered in this theoretical analysis together with a *p-n* junction featuring several series resistance values ranging from 10 mΩ to 1 Ω

As can be seen from Fig. 2.4, the effect of the series resistance on the dynamic resistance shall not be neglected. Moreover, examination of (2.8) shows that the dynamic resistance is

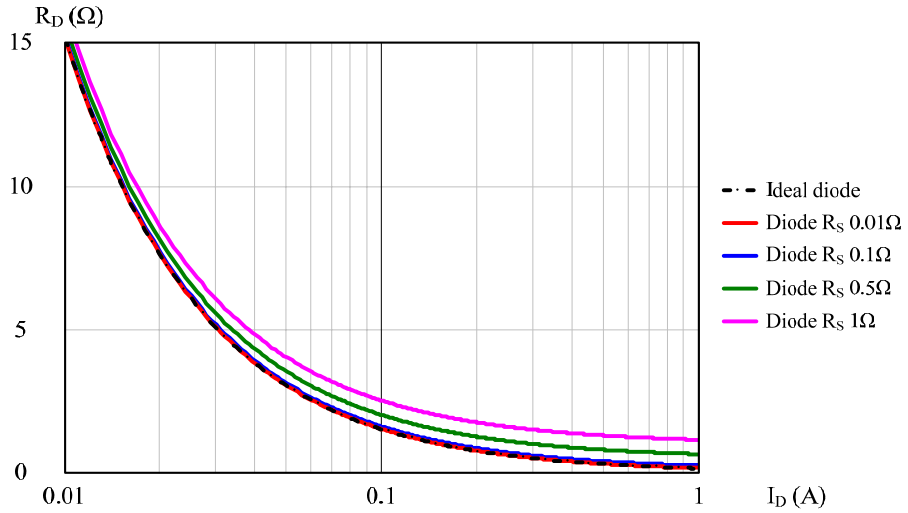

Fig. 2.4. Semilog plot of the dynamic resistance (solid lines) of a *p-n* junction with several values of series resistance. The ideal diode is also shown (dashed line).

affected by the forward current and by the junction temperature. Regarding the former, the second term in (2.8) is inversely proportional to forward current. Therefore, a decreasing dynamic resistance with rising forward current will be expected. Regarding the latter, the behaviour of the dynamic resistance will depend on which parameter variation is predominant: either the ideality factor, the series resistance or the junction temperature.

Once the dynamic resistance corresponding to each forward voltage and junction temperature has been calculated, the linear model of an LED lamp can be obtained for each operation point *i* under a given forward current and junction temperature:

$$V_{Di} = V_{\gamma i} + I_{Di}R_{Di} \tag{2.9}$$

where V_{Di} is the forward voltage, $V_{\gamma i}$ is the threshold voltage, and R_{Di} is the dynamic resistance. The threshold voltage is easily calculated by the measured forward voltage and dynamic resistance corresponding to each operation point.

2.5. Methods for thermal characterisation of LEDs

Junction temperature is a critical parameter in the operation of LEDs, as it affects the luminous maintenance, and also the electrical characteristics are subjected to changes. Therefore, it is important to measure the junction temperature. There are several methods for thermally characterising the *I-V* curve of LEDs. The simplest method just estimates the junction temperature by applying the one-dimensional equivalent electrical circuit [2.26], [2.31], as the power dissipation, P_D, and the thermal resistance from junction to case are known parameters and other temperatures, such as the board temperature, T_B, are easily measurable. Then, the junction temperature can be estimated as:

$$T_j = T_B + R_{\theta jc}P_D \tag{2.10}$$

However, this methodology gives only approximate results, as it is necessary to measure the actual power dissipation and the heat-spreading is not accounted for, neglecting the thermal resistance between the LED case and the board measured point [2.26], [2.32]. Moreover, the thermal resistance from junction to case is power-dependent, as has been exhaustively reported

in [2.14], [2.25], [2.26], [2.32]. Consequently, several methods have been developed in order to determine the junction temperature accurately:

a) Micro-Raman spectroscopy [2.33], based on the inelastic scattering of monochromatic light that interacts with the matter.
b) Threshold current measurement –in Laser Diodes, [2.34], which is temperature-dependent. However, it is not applicable to LEDs.
c) Thermoreflectance and reflectance modulation [2.35], based on the changes on reflectance that a change in the bulk temperature induces.
d) Study of the thermally-induced refractive index by photoluminescence [2.36].
e) Non-contact method based on the shift of the spectral power distribution (SPD) [2.37].
f) Forward-voltage method, based on the dependency of the *I-V* curve on temperature [2.38].
g) Non-contact method based on the drop of radiometric power [2.39].

Methods a) to d) provide quite accurate measurements of the junction temperature, although they require expensive and complex laboratory equipment and the implementation of such techniques for measuring an LED lamp leads to complex arrangements. On the contrary, methods e) to g) provide lower accuracy but the laboratory equipment is simpler and cheaper. In the case of methods e) and g), a CCD is needed in order to register the spectral power distribution, whereas method f) only uses a voltage probe. However, these low-cost methods demand the LED lamp thermal characterisation unless a comprehensive, detailed model of the DUTs is available. Since the forward-voltage is considered the simplest and most accurate low-cost method [2.30], [2.39], it has been chosen for the subsequent stages of the thermal characterisation. This method will be comprehensively introduced in the following section.

2.6. Thermal characterisation of LEDs: the Forward-Voltage Method

It has extensively been reported that the most accurate procedure for determining the junction temperature at a given injected current is the method consisting of a pulsed operation of the LED in a temperature-controlled chamber [2.30], [2.38]-[2.41]. In this method, the device under test (DUT) is placed in a temperature-controlled room and tested under pulsed-current injection with a very small duty cycle. It is assumed that provided that the duty cycle is small enough, typically 0.1% according to the literature [2.30], the self-heating of the *p-n* junction is negligible [2.38]-[2.41], [2.42], and therefore, the junction temperature will be the same as the board and heatsink temperatures, which at steady state will be the same as the ambient temperature. Therefore, after measuring the forward voltage drop for each injection current at each ambient temperature, the V_D-T_j characteristic of the DUT can be determined for each forward current with an accuracy around ±3 ºC [2.30], as opposed to the ±24 ºC accuracy of the SPD-based non-contact methods [2.40].

2.7. Description of the LED lamps under study

Two different studies were carried out: first, with a single chip, and after that, an entire lamp composed by 60 LEDs was built. The main difference between the four LED types chosen for this work lies on the binning: the Z-Power P4 and the Luxeon K2 with TFFC are binned for luminous flux and forward voltage. Therefore, the characteristics of whatever two devices chosen from the same reel are very close to each other. On the contrary, the Dragon Plus and the XLamp XR-E are unbinned for forward voltage, causing a likely noticeable difference in the electrical characteristics among devices in the same reel. As this section aims to design the LED

lamp from the point of view of a power load, the binning of luminous flux will not be taken into account.

The LEDs will be connected in series in order to avoid any luminous mismatch among paralleled strings, which also helps to reduce the complexity of the electronic driver, since balancing circuits are not required [2.9], [2.43], [2.44]. The main disadvantage of this solution is the resulting lamp high voltage. The forward voltage characteristics of the four LEDs considered are gathered in Table II.II.

TABLE II.II
BINNING OF THE LEDS CONSIDERED IN THE STUDY

LED	V_D (V)			V_{Dtyp} (V) @350mA	Bin		
	Min.	*Typ.*	*Max.*		*Code*	V_{Dmin} (V)	V_{Dmax} (V)
Dragon Plus	2.7	3.2 (@350mA)	3.8	3.2	-	-	-
Luxeon K2	3.03	3.65 (@1A)	4.71	3.3	H (@1A)	3.99	4.23
Z-Power P4	2.9	3.25 (@350mA)	4	3.25	H (@350mA)	3	3.25
XLamp XR-E	-	3.3 (@350mA)	3.9	3.3	-	-	-

The first step will be focused on the forward voltage deviation for a given sample size, obtained from the data provided by the manufacturer. This first estimation will allow the statistical deviation from the typical value to be determined in order to consider whether the average forward voltage obtained from the 60 LEDs sample size is a good estimator of the electrical behaviour of the LED under study for subsequent tests and the development and design of an LED lamp and the driver. Moreover, a proper statistical modelling could determine the feasibility of a parallel-connected lamp without the need for equalising circuitry [2.43]. This topic is covered ahead in Chapter 7. In this way, the characteristics of LEDs follow a statistical distribution that is approximately Gaussian [2.18], [2.43]. However, some skewness – i.e. asymmetry, can be observed from the minimum, maximum and typical forward voltage data provided by the manufacturers, as the typical forward voltage is different from the median value. This could likely be modelled by the addition of two Gaussian distributions, one corresponding to the forward voltage drop due to the energy gap, and another one corresponding to the forward voltage drop due to the effect of parasitic series resistances. However, this is just a supposition and further experimentation should be done in order to verify this point. Nevertheless, it can be considered that the assumption of a Gaussian distribution is satisfactorily accurate even for a narrow bin [2.43] or simply, by the Central Limit Theorem, a Gaussian distribution could be assumed. In order to calculate the expected forward voltage deviation, two different approaches are to be taken depending on the binning of LEDs.

2.7.1. Unbinned LEDs

If the LEDs are unbinned, the Probability Distribution Function (PDF) will resemble a Gaussian distribution with some amount of skewness. As the manufacturers only provide the minimum, maximum and typical value, it would be necessary to test a large sample of LEDs in order to estimate the mode, median and mean value of the LEDs population. Therefore, and starting from the data provided by the manufacturer, the Central Limit Theorem will be applied. This theorem establishes that given a random variable, X, from a given population with an

average value μ, and variance σ^2 – where σ is the standard deviation, the average value of a sample, ξ, with size n, will approximately follow a Gaussian distribution of average value μ, and variance σ^2/n. This is, the probability distribution function of:

$$\frac{\xi - \mu}{\sigma/\sqrt{n}} \tag{2.11}$$

is approximately Gaussian. In other words, the probability, P, of a random variable X of being lower than b, is approximately:

$$P(X \leq b) \approx P\left(Z \leq \frac{b - \mu}{\sigma/\sqrt{n}}\right) \tag{2.12}$$

where Z is a standard normal random variable. This approximation increases its accuracy as long as the sample size is increased, being 30 a practical minimum sample size for the application of the Central Limit Theorem.

In a normal distribution, the expected value $E(X)$ corresponds to the average of the distribution, μ, and σ is defined as $P(X \leq 3\sigma)=0.999$. Therefore, in the case of LEDs, which are characterised by a minimum and a maximum forward voltage, V_{Dmin} and V_{Dmax}, respectively, X would be the voltage of any device, and σ is defined as [2.43]:

$$\sigma = \frac{V_{Dmax} - V_{Dmin}}{6} \tag{2.13}$$

Nevertheless, this procedure assumes a symmetric PDF. Given that the manufacturers only provide with the values for typical, minimum, and maximum forward voltage values, an acceptable assumption would be to define the standard deviation, σ, in a way that either the sample size or the typical forward voltage deviation are overestimated, leading to a conservative design. Such a definition for σ would be:

$$\sigma = max\left(\frac{V_{Dmax} - V_{Dtyp}}{3}, \frac{V_{Dtyp} - V_{Dmin}}{3}\right) \tag{2.14}$$

Fig. 2.5 depicts the PDF and the cumulative probability distribution (CPD) for the Golden Dragon Plus forward voltage, X, obtained from the data contained in the data sheets, but σ being calculated both as in [2.43], and by (2.14).

As can be seen, if the standard deviation is calculated from (2.14), the probability distribution function is lower for the central values, while slightly higher for those values at the wings of the Gaussian bell. This would imply more conservative results in subsequent calculations. With the procedure described in this section, the statistical functions for the four LEDs considered in this work were calculated and are gathered in Table II.III.

Fig. 2.6 shows the probability distribution function for the devices under test, assuming a symmetric normal random variable.

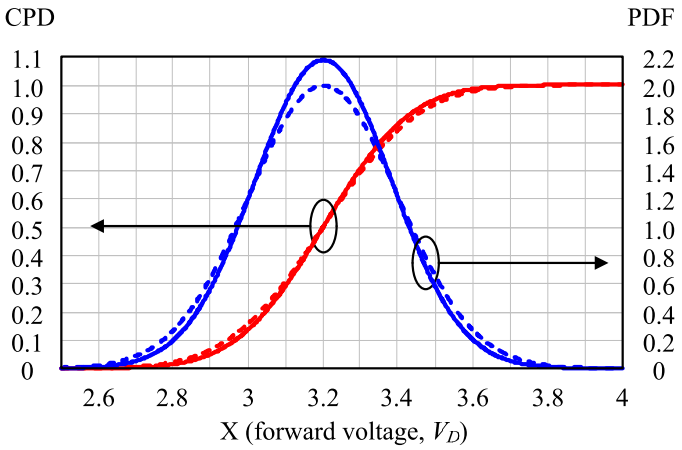

Fig. 2.5. CPD and PDF for a Golden Dragon Plus device. Solid lines show the probability functions with standard deviation calculated as in (2.13), whereas dashed lines show the probability functions with standard deviation calculated as in (2.14).

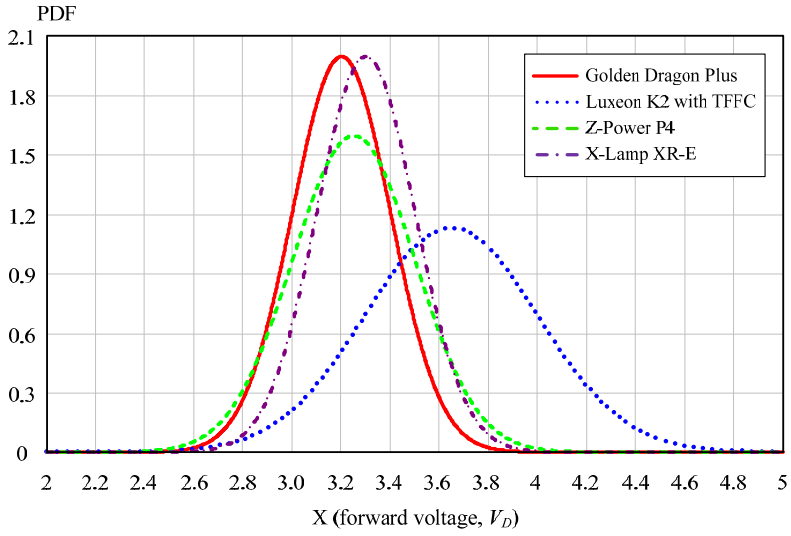

Fig. 2.6. Theoretical PDF estimated for the four devices under test as estimated from the data extracted from the data sheets. All the devices are binned at 350 mA except for the Luxeon K2, which is binned at 1000 mA.

TABLE II.III
AVERAGE VALUE AND STANDARD DEVIATION FOR THE LEDS UNDER STUDY

LED	μ	σ
Golden Dragon Plus	3.2	0.2
Luxeon K2 TFFC	3.65	0.353
Z-Power P4	3.25	0.25
XLamp XR-E	3.3	0.2

2.7.2. Binned LEDs

In the case of binned LEDs, the Central Limit Theorem could be straightforwardly applied in order to determine the forward voltage deviation for a large enough sample size [2.43]. However, the typical value for a single bin would not necessarily be the median of the bin. By

inspection of Fig. 2.5, it could easily be seen that for a bin ranging from 3.4 to 3.6 V, the average value would be lower than 3.5 V, as the probability density function is much higher between 3.4 and 3.5 V than from 3.5 to 3.6 V. In this case, both the expected value and the standard deviation are to be calculated from the PDF between the minimum and maximum forward voltage corresponding to the actual bin, assuming that all the LEDs will be contained within those voltage limits. Therefore, the expected value of the random variable *T* corresponding to the forward voltage of any LED included in a single bin, *E(T)*, will be calculated as:

$$E(T) = \int_{V_{Dmin}}^{V_{Dmax}} x \frac{1}{P(N(\mu,\sigma) \leq V_{Dmax}) - P(N(\mu,\sigma) \leq V_{Dmin})} \frac{1}{\sqrt{2\pi}\sigma} e^{-\frac{(x-\mu)^2}{2\sigma^2}} dx \qquad (2.15)$$

where $N(\mu,\sigma)$ is the Gaussian distribution corresponding to the unbinned LED, as stated in Table II.III, and V_{Dmin} and V_{Dmax} are the corresponding minimum and maximum voltage values for the actual bin, as gathered in Table II.II. After that, the variance of the distribution can be calculated as:

$$Var(T) = E(T^2) - E(T)^2 \qquad (2.16)$$

where $E(T^2)$ can be calculated as:

$$E(T^2) = \int_{V_{Dmin}}^{V_{Dmax}} x^2 \frac{1}{P(N(\mu,\sigma) \leq V_{Dmax}) - P(N(\mu,\sigma) \leq V_{Dmin})} \frac{1}{\sqrt{2\pi}\sigma} e^{-\frac{(x-\mu)^2}{2\sigma^2}} dx \qquad (2.17)$$

Finally, the standard deviation is calculated as the square root of the variance.

By following the described procedure, the following values gathered in Table II.IV for the expected value, variance and standard deviation are obtained.

TABLE II.IV
EXPECTED VALUE, VARIANCE, AND STANDARD DEVIATION FOR THE BINNED LEDS

LED	*E(T)*	*Var(T)*	*σ*
Luxeon K2 TFFC	4.093	4.552E-3	0.067
Z-Power P4	3.135	4.978E-3	0.071

The probability distribution function for both devices is sketched in Fig. 2.7 together with the cumulative probability distribution.

Once the probability distribution functions have been calculated, the confidence interval can be estimated for a given sample size, as will be introduced in the following section.

2.7.3. Determination of the confidence interval for the lamps under study

The purpose of this section is to determine whether the lamps used in the electrical characterisation are a valid sample for determining the electrical behaviour of any lamp with the same characteristics –i.e. the same device, number of LEDs in series and binning, as the characterisation results for average voltage, ξ, are kept within a tight tolerance around the population average, μ. Provided that by the Central Limit Theorem, the random variable *X* –or *T* in the case of binned LEDs, approximately follows a normal distribution for a large enough sample size, the tolerance between the theoretical values and a sample, as well as the confidence

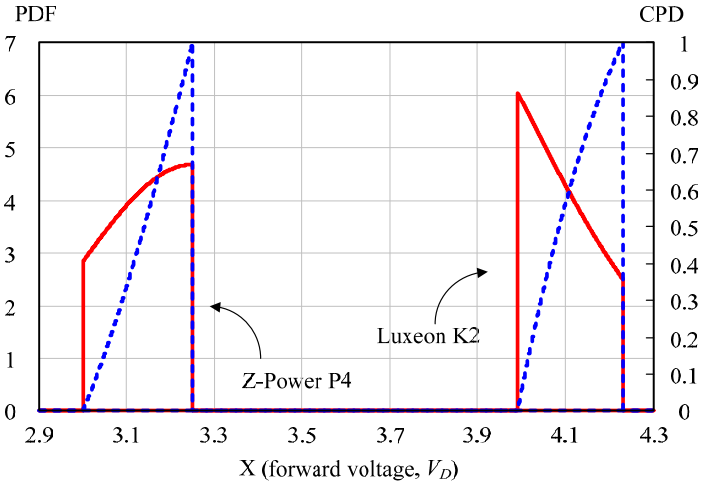

Fig. 2.7. Theoretical PDF (solid line) and CPD (dashed line) estimated for the binned Luxeon K2 and Z-Power P4 devices.

interval, can be determined for a given confidence level. In this way, the probability of the sample average value, ξ, to be kept within an interval defined as a tolerance, ε, over the typical voltage for a given random variable, can be determined for a 95% probability, which is considered reasonable, as:

$$P\left(\frac{|\xi-\mu|}{\sigma/\sqrt{n}} \leq \frac{\varepsilon\cdot\mu}{\sigma/\sqrt{n}}\right) = 0.95 \tag{2.18}$$

By checking in a look-up table for a normal random variable for a 95% probability and solving for ε, the maximum expected deviation at a 95% probability is obtained for an n size sample:

$$\varepsilon = \frac{1.96\sigma}{\mu\sqrt{n}} \tag{2.19}$$

The obtained maximum expected deviation from the typical value for each LED at a 95% probability is gathered in Table II.V together with the typical value for both binned and unbinned LEDs for a 60 series LEDs sample size. The forward voltage deviation is expressed as a percentage over the typical forward voltage value.

TABLE II.V
MAXIMUM EXPECTED FORWARD VOLTAGE DEVIATION AT A 95% PROBABILITY

LED	μ *unbinned* (V)	ε (%)	μ *binned* (V)	ε (%)
Golden Dragon Plus	3.2	1.58	-	-
Luxeon K2 TFFC	3.65	2.45	4.093	0.42
Z-Power P4	3.25	1.95	3.135	0.57
XLamp XR-E	3.3	1.53	-	-

Table II.VI shows the minimum sample size, n, obtained for several forward voltage variation values, expressed as percentages over the typical forward voltage, ranging from 1% to 10% for a 95% confidence level.

However, these results are valid as long as the unbinned LEDs are supposed to feature a normal distribution. On the contrary, these results have been obtained by the Central Limit

TABLE II.VI
MINIMUM SAMPLE SIZE FOR A GIVEN VOLTAGE DEVIATION AT A 95% CONFIDENCE LEVEL

LED	1%	2%	5%	10%
Golden Dragon Plus	151	38	7	2
Luxeon K2 TFFC (unbinned)	360	90	15	4
Z-Power P4 (unbinned)	228	57	10	3
XLamp XR-E	142	36	6	2
Luxeon K2 TFFC binned	11	3	1	1
Z-Power P4 binned	20	5	1	1

Theorem for those LEDs that are binned, assuming that the actual single bins follow whatsoever probability distribution function. Therefore, unless more information about the PDF of single bins is obtained, the minimum sample size in order to assure the validity of these results should be large enough to apply the Central Limit Theorem, of which a practical minimum sample size is 30.

To summarize up, the 95% of the LED lamps built with 60 series LEDs will feature a forward voltage drop kept in the range of $\mu \pm \varepsilon\mu$. As can be seen in Table II.VI, the tolerance values will be lower than 2% for the unbinned LEDs and lower than 1% for the binned LEDs, which is considered a reasonable value. Therefore, it is assumed that the electrical characteristic of the LED lamps under study will be representative of a generic LED lamp built with the same number of series LEDs from the same bins. Moreover, the average values obtained from the 60 LEDs tests can be used to obtain the typical LED forward voltage values in order to design a generic LED lamp with a given number of series-connected emitters. In addition, these typical values can also be used in the determination of the minimum emitters per string in the case of paralleled-strings LED lamps.

Two complementary studies were developed: firstly, single LEDs were tested in order to verify the previous assumptions about the effects of junction temperature in forward voltage and dynamic resistance. Secondly, the differences between DUTs can be determined. Additionally, the 60-series LED lamps were more deeply tested in order to determine the typical characteristics of the devices and to check the possible variations and differences between a single emitter and an entire fixture composed of several emitters.

2.8. Thermal Characterisation of LEDs: V_D-T_j and I-V curves.

This test was performed in order to determine the I-V curves for each temperature of the LEDs. Afterwards, these curves are easily transformed to V-T curves. This will allow the junction temperature to be calculated by just measuring the forward voltage.

2.8.1. Description of the Workbench

The workbench differed slightly for the two experimental tests. Firstly, for the single LED test, one sample of each device was fixed to a Metal Core PCB (MCPCB) with thermal bond. A K-type thermocouple was attached to the MCPCB in order to measure the board temperature. Then, the entire fixture was placed inside a temperature-controlled chamber. By means of a specific driver, a 20 μs-width current pulse was injected to the DUT for each target current level at each target temperature. The devices were tested from 100 mA up to 1A in 100 mA steps, plus the nominal current, i.e. 350 mA, for an ambient temperature ranging from -20 ºC to 120 ºC in 10 ºC steps, plus 25 ºC. The experimental arrangement for this test is shown in Fig. 2.8.

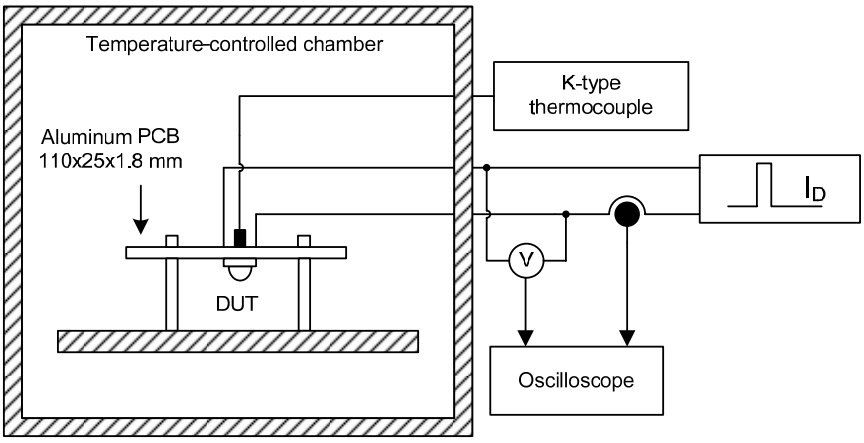

Fig. 2.8. Experimental arrangement used to obtain the forward voltage versus junction temperature characteristic (or curve) for a single DUT test.

The pulse width was chosen as a trade-off between high Signal-to-Noise Ratio (SNR) and negligible LED self-heating due to the energy applied to the *p-n* junction, provided that the pulse width is much lower than the thermal time constant of the LEDs. This thermal time constant is considered to be in the several hundreds of microseconds to few milliseconds range for the chip [2.8], [2.14], [2.24], [2.31], [2.45]. Thus, both the electrical noise due to the switching of the DUT and the self-heating of the *p-n* junction can be avoided. In order to check whether a 20 µs width current pulse would induce a non-negligible self-heating to the DUT, a 1000 mA current step was applied to a Cree XLamp XR-E device, measuring the forward voltage drop for a long time period. Fig. 2.9 shows the results of the test, from which it can be

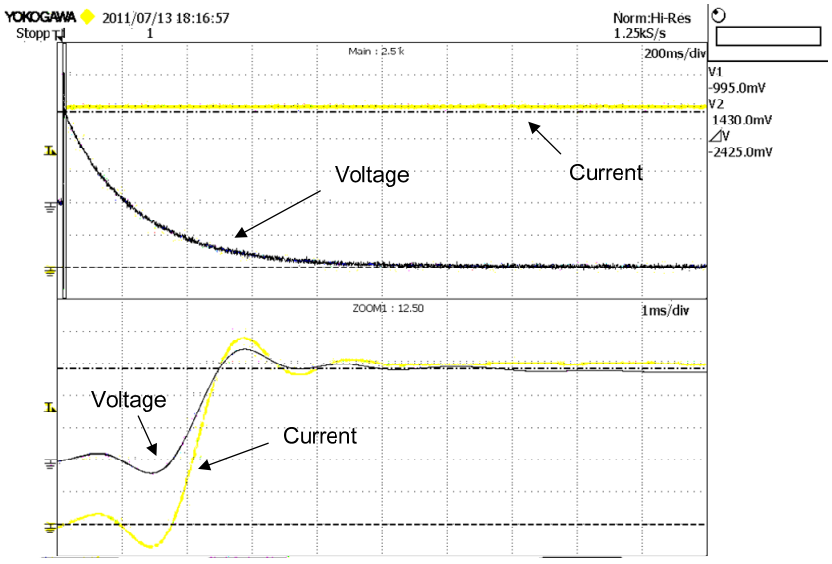

Fig. 2.9. 1000 mA current pulse test to determine the forward voltage drop of the Cree XLamp XR-E device. Upper: forward current and forward voltage of the DUT. Vertical scale: 200 mA/div, 500 mV/div. Horiz. scale: 200 ms/div. Lower: zoom of the pulse rising edge. Vertical scale: 200 mA/div, 500 mV/div. Horiz. scale: 1 ms/div. AC coupling.

assumed that the forward voltage drop of the DUT can be considered negligible for a pulse width of less than 20 μs.

Secondly, the 60-LEDs lamp tests followed the same procedure. The arrangement is illustrated in Fig. 2.10. The 60-LEDs lamps are shown in Fig. 2.11.

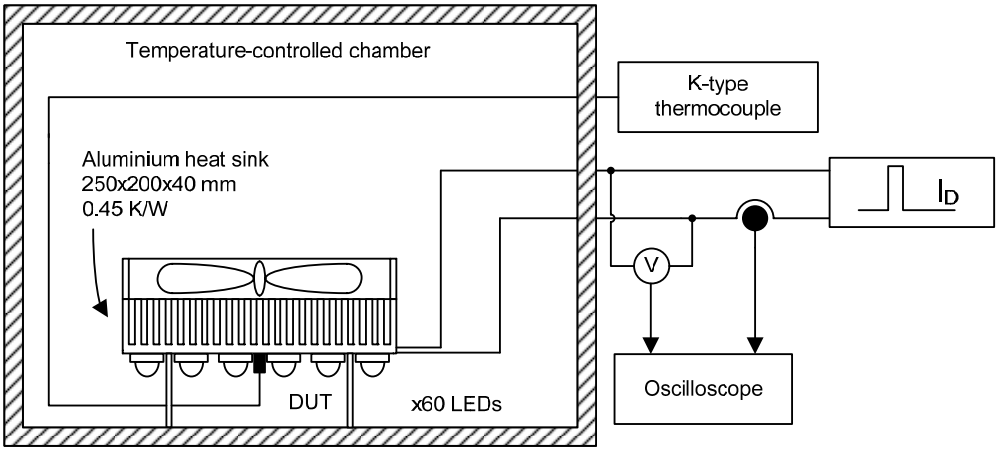

Fig. 2.10. Experimental arrangement in order to obtain the forward voltage versus junction temperature relation for the 60-series LEDs lamps.

The LEDs were directly attached to a heatsink by thermal bond in order to reduce the thermal resistance from the junction to the ambient. The heatsinks chosen were 250x200x40 mm finned aluminium heatsinks from Aavid Thermalloy, featuring a 0.45 K/W thermal resistance under natural convection conditions. A K-type thermocouple was screwed into the hottest point of the heatsink, this is, the centre point of the LEDs side, so the heatsink

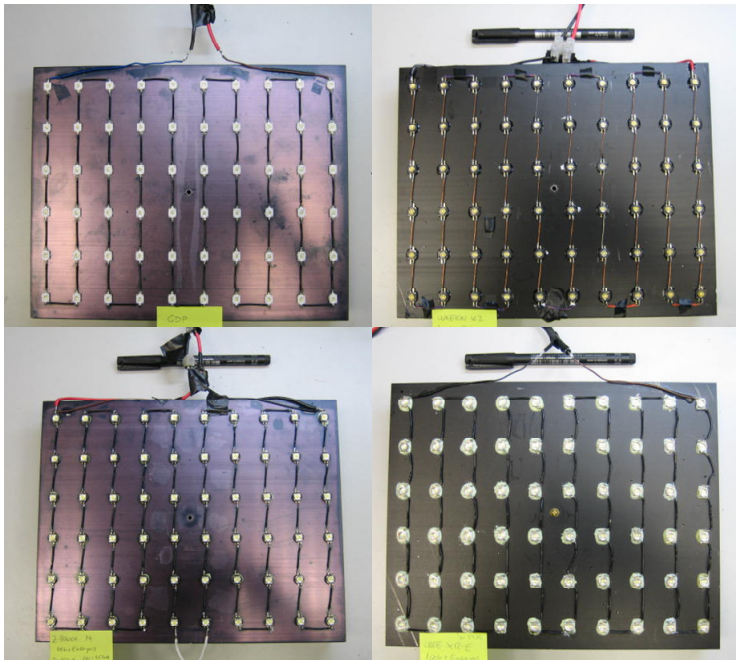

Fig. 2.11. LED lamps tested: a) top, left: Osram Golden Dragon Plus; b) top, right: Philips Lumileds Luxeon K2 with TFFC; c) bottom, left: Seoul Semiconductor Z-Power P4; d) bottom, right: Cree XLamp XR-E.

temperature could be measured. Moreover, slight forced convection was added. Then, the entire fixture was placed inside the temperature-controlled chamber. A specific driver was built to provide 1000 mA up to 250 V. The current range was set from 10 mA to 200 mA in 50 mA steps and from 300 mA to 1000 mA in 100 mA steps. The ambient temperature was varied from -10 ºC to 120 ºC. The pulse width was increased to 40 µs in order to get rid of electrical noise at the lowest test currents.

2.8.2. Experimental Results: *I-V* curve

As only forward voltage and current typical values were pursued, the experimental results were calculated by averaging sixteen measurements of ambient temperature, board – and therefore, junction temperatures, forward current, and forward voltage for each current and temperature operation points. In addition, and although both the single LEDs and the entire lamps were tested following the same procedure, only the results obtained from the latter were used to fit the *I-V* curve and thus to obtain the typical electrical behaviour. The test average junction temperatures, T_A, are gathered in the Appendix A in Table A.I, together with their standard deviation, σ.

The experimental results obtained from the *I-V* characterisation are shown in the Appendix A in Fig. A.1. The experimental curves were fitted by (2.7) for each temperature for a 95% confidence level. These results are shown through Fig. 2.12 to Fig. 2.15. The semilog curves, i.e. *lnI-V*, of the experimental data and the fitting curves are shown in the Appendix A in Fig. A.2

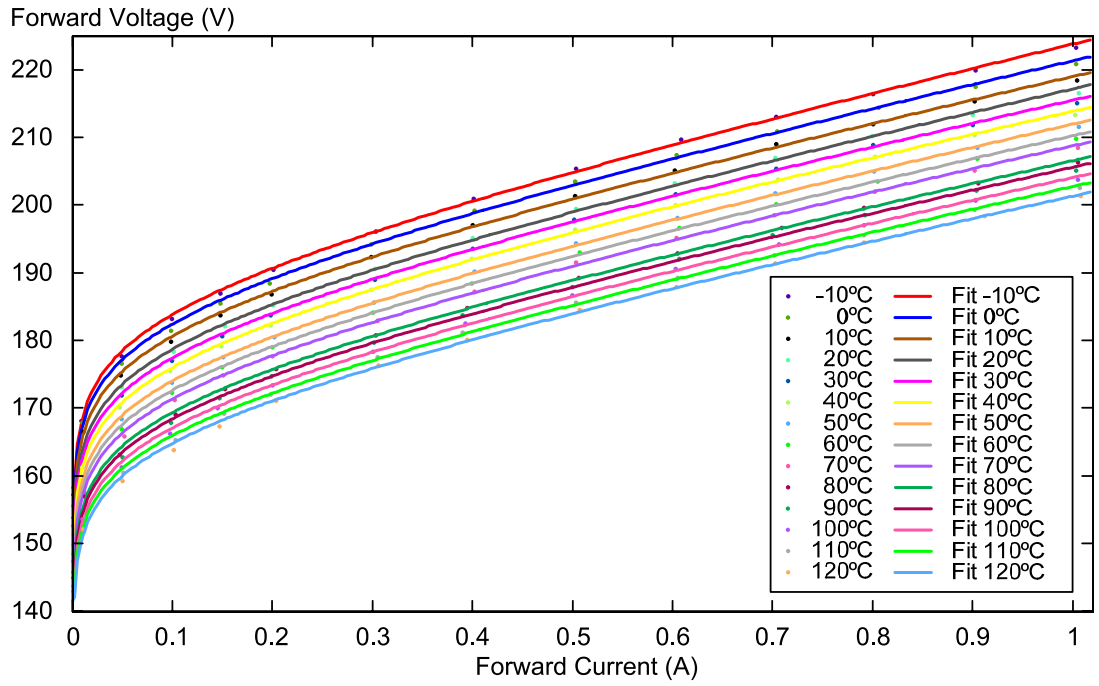

Fig. 2.12. *I-V* fit for the Osram Golden Dragon Plus device for several junction temperatures.

The fitting curve (2.7) allows the reverse saturation current, the ideality factor, and the series resistance of the DUTs to be extracted. These results are gathered from Table A.II to Table A.VI in the Appendix A for the 60-LEDs lamps together with the fitted values for a single average diode. The correlation coefficient, r^2, is also shown. These LED parameters are also depicted in Fig. A.3 in a linear scale.

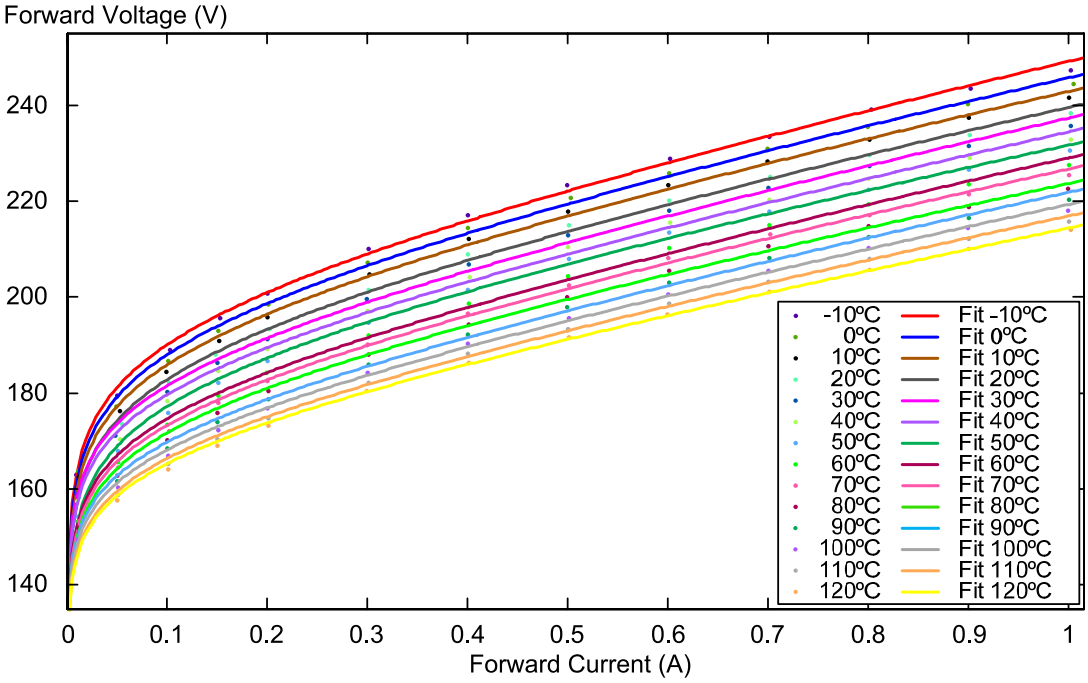

Fig. 2.13. *I-V* fit for the Philips Lumileds Luxeon K2 with TFFC device for several junction temperatures.

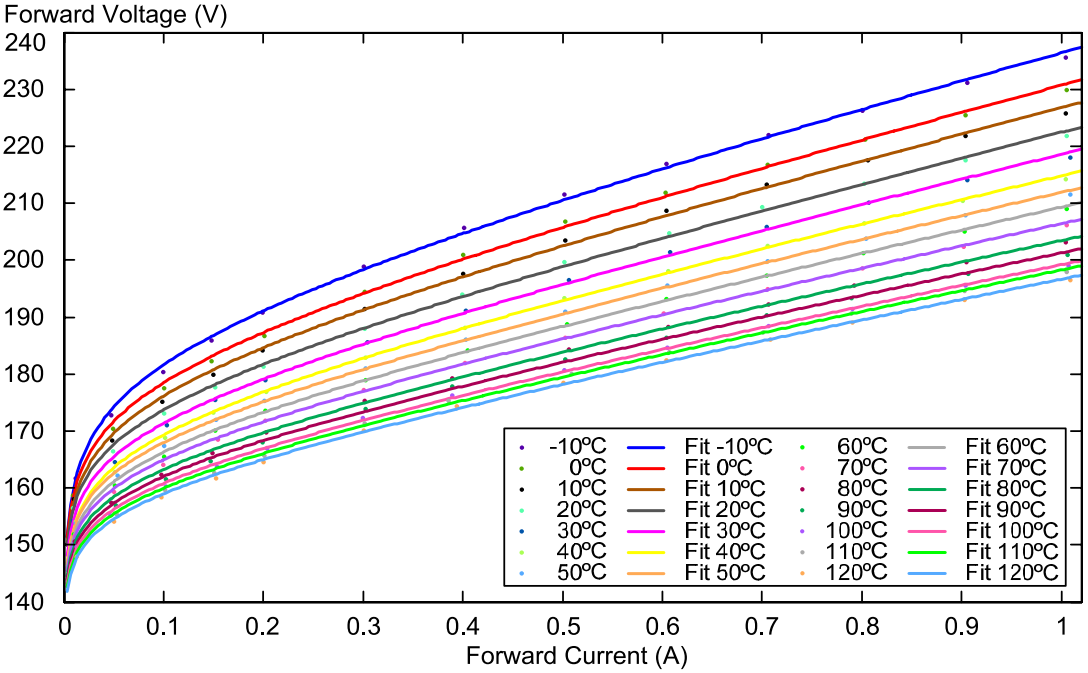

Fig. 2.14. *I-V* fit for the Seoul Semiconductor Z-Power P4 device for several junction temperatures.

Moreover, the dynamic resistance can be determined from the experimental *I-V* fitting by substitution in (2.8). Therefore, the behaviour and the thermal dependence of the dynamic resistance can be predicted and compared to the experimental results obtained in the subsequent tests. The dynamic resistance values were calculated for the two most common operation currents for HB-LEDs, i.e. 350 and 700 mA at the test temperatures. The results are shown in Fig. 2.16 and gathered in Table A.VI in the Appendix A.

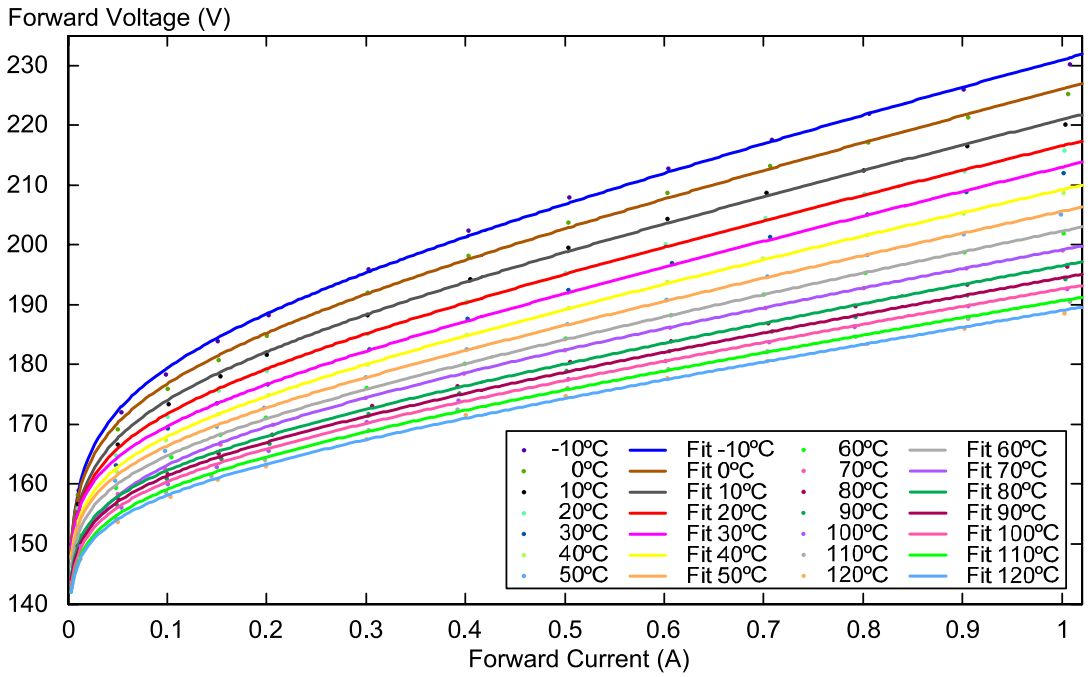

Fig. 2.15. *I-V* fit for the Cree XLamp XR-E device for several junction temperatures.

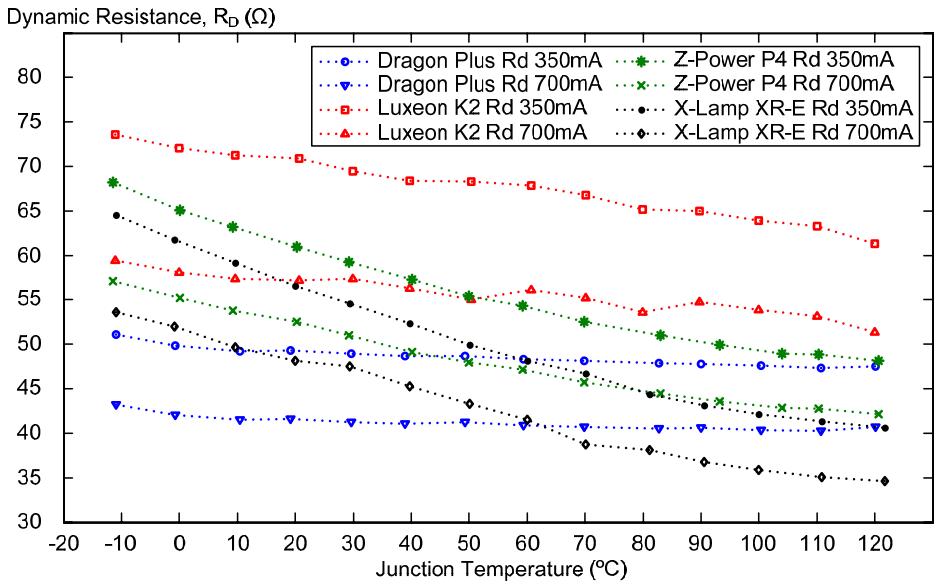

Fig. 2.16. Dynamic resistance theoretically calculated at 350 and 700 mA.

As can be seen from the experimental results, the thermal dependence of the *I-V* curve has been obtained, confirming the results previously reported in the literature: a decrease of the ideality factor with increasing temperature [2.24], and a decrease on the series resistance with increasing temperature [2.42]. However, erratic values are produced for the reverse saturation current, with a thermal dependence that has been obtained contrary to the actual behaviour of this parameter, which is assumed to double each 10 ºC of temperature increase. In addition, the fitting of the experimental *I-V* curves is worsened at the lowest injection currents, as can be seen from Fig. 2.12 to Fig. 2.15 and in Fig. A.2 and from Table A.II through Table A.VI in the Appendix A. This issue would likely be owed to the experimental setup loss of accuracy at low

currents and the lack of measurement points for such low currents. Therefore, a new fit was performed for a reduced data set by excluding the 10 mA current level. The fits for the reduced data set of the lamps under study are shown from Fig. 2.17 to Fig. 2.20.

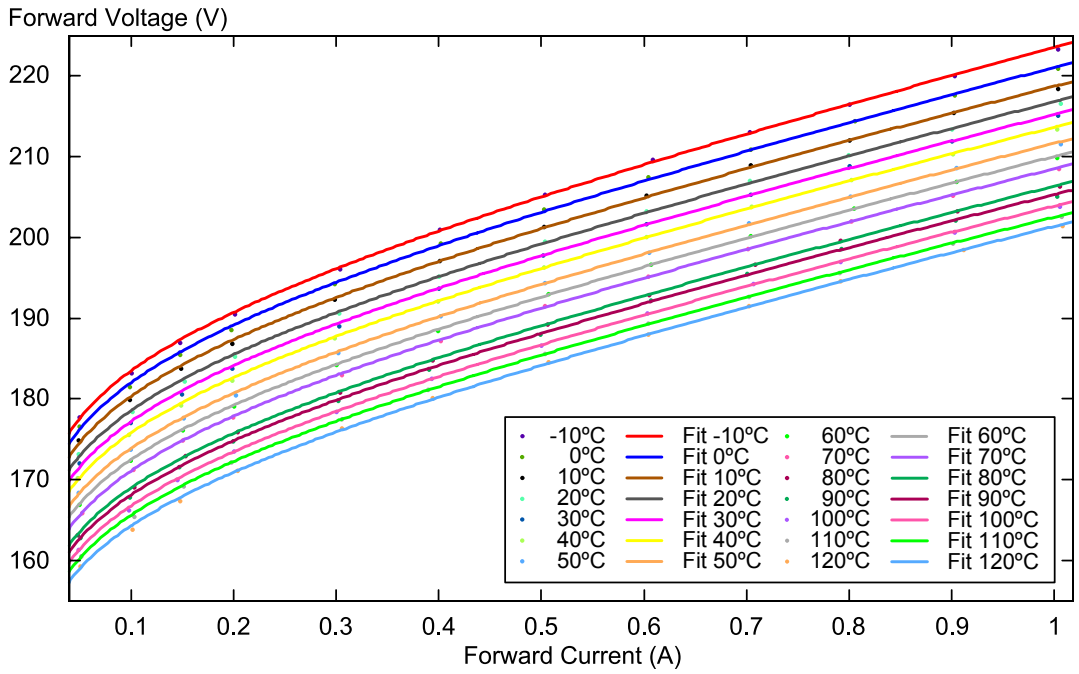

Fig. 2.17. *I-V* fit for the Osram Golden Dragon Plus device for several junction temperatures, reduced data set.

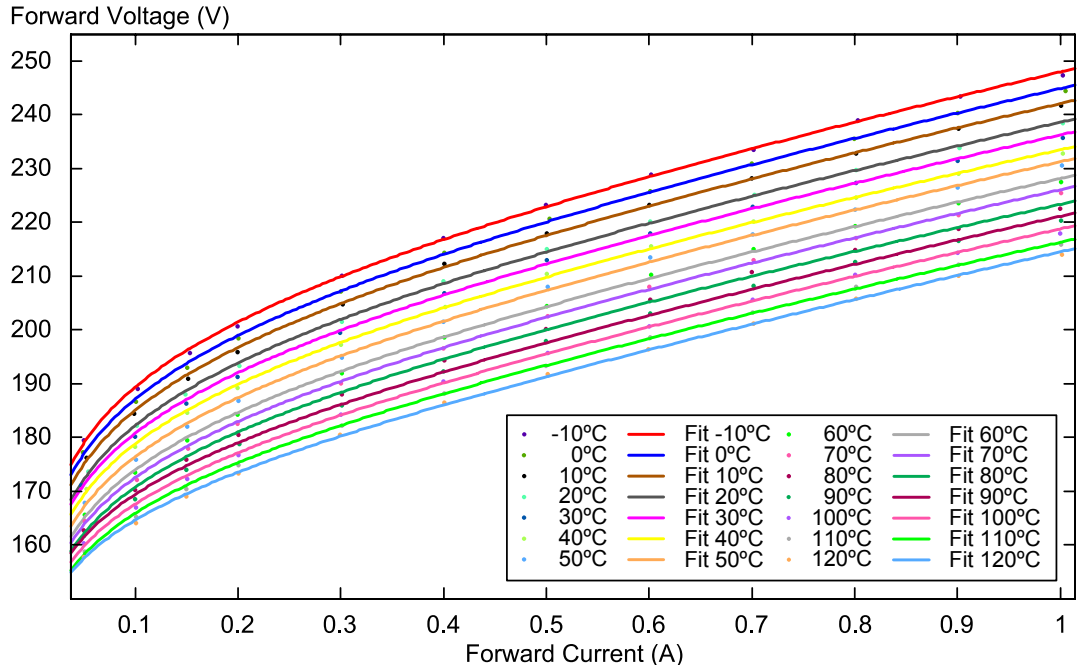

Fig. 2.18. *I-V* fit for the Philips Lumileds with TFFC device for several junction temperatures, reduced data set.

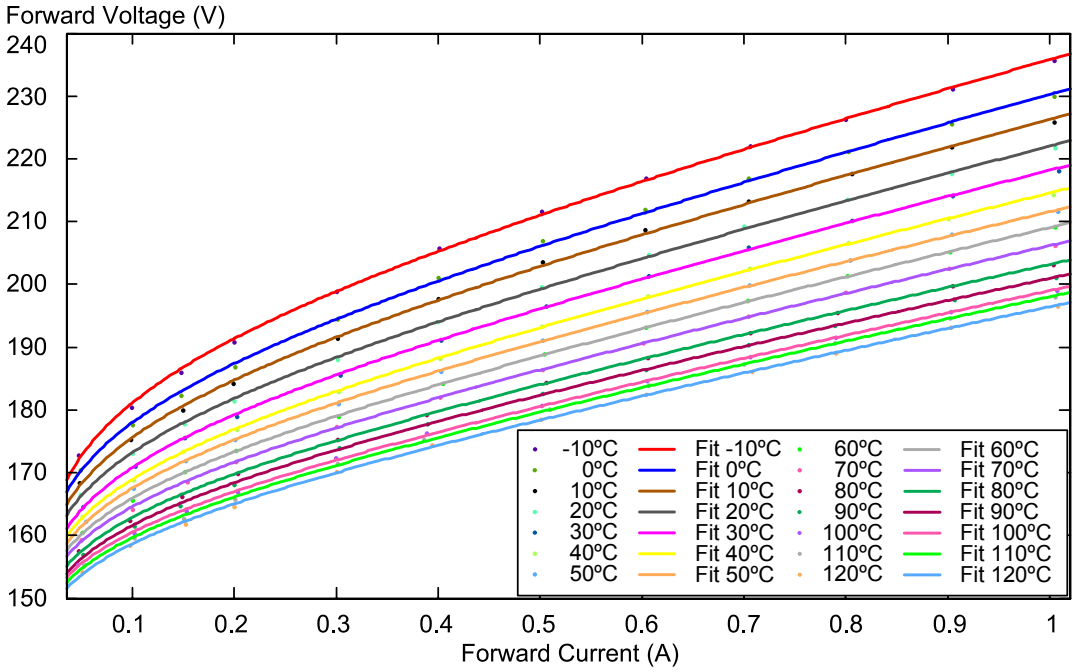

Fig. 2.19. *I-V* fit for the Seoul Semiconductor Z-Power P4 device for several junction temperatures, reduced data set.

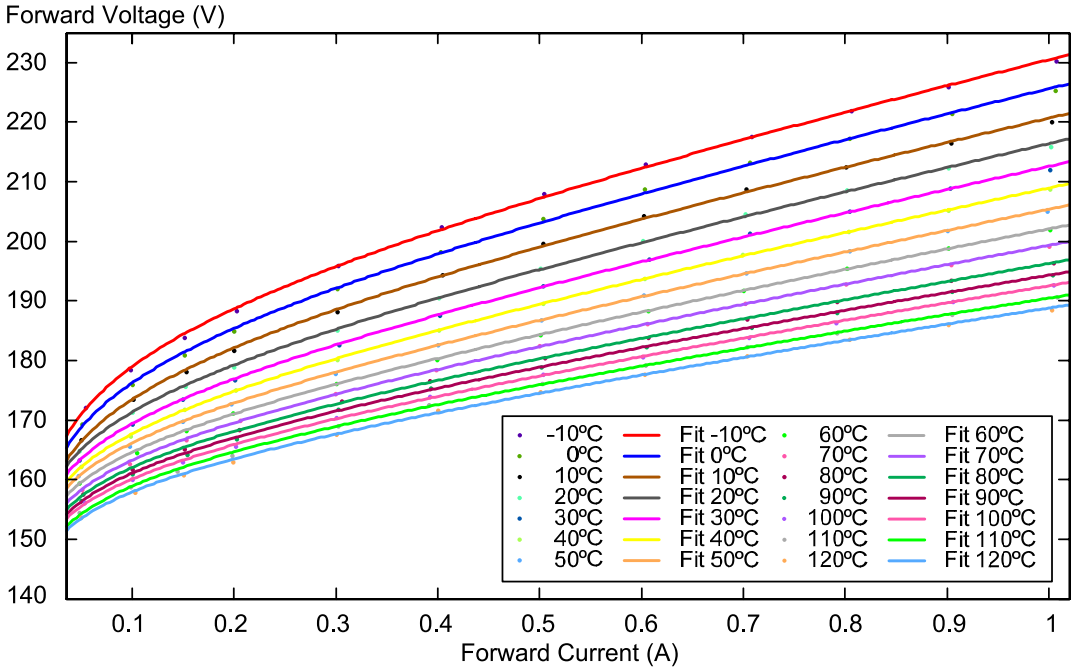

Fig. 2.20. *I-V* fit for the Cree XLamp XR-E device for several junction temperatures, reduced data set.

The results obtained for the reverse saturation current, the ideality factor and the series resistance are gathered from Table A.VII to Table A.X in the Appendix A together with the fit for an average diode. The correlation coefficient, r^2 is also shown. In addition, the experimental

data and the fits are depicted in a semilog graph in Fig. A.4 in the Appendix A. As can be seen, the fit accuracy is greatly improved, with correlation coefficients above 0.999.

The experimentally calculated parameters, i.e., reverse saturation current, ideality factor and series resistance are depicted in Fig. A.VI in the Appendix A. As happened with the entire data set, the values obtained for the reverse saturation current are erratic and show a trend which is contrary to the actual thermal dependence of such parameter, due to the lack of experimental points at low current levels. As in the previous case, the dynamic resistance is calculated by (2.11) with the parameters obtained from the reduced data set fit. The results for 350 and 700 mA are shown in Fig. 2.21.

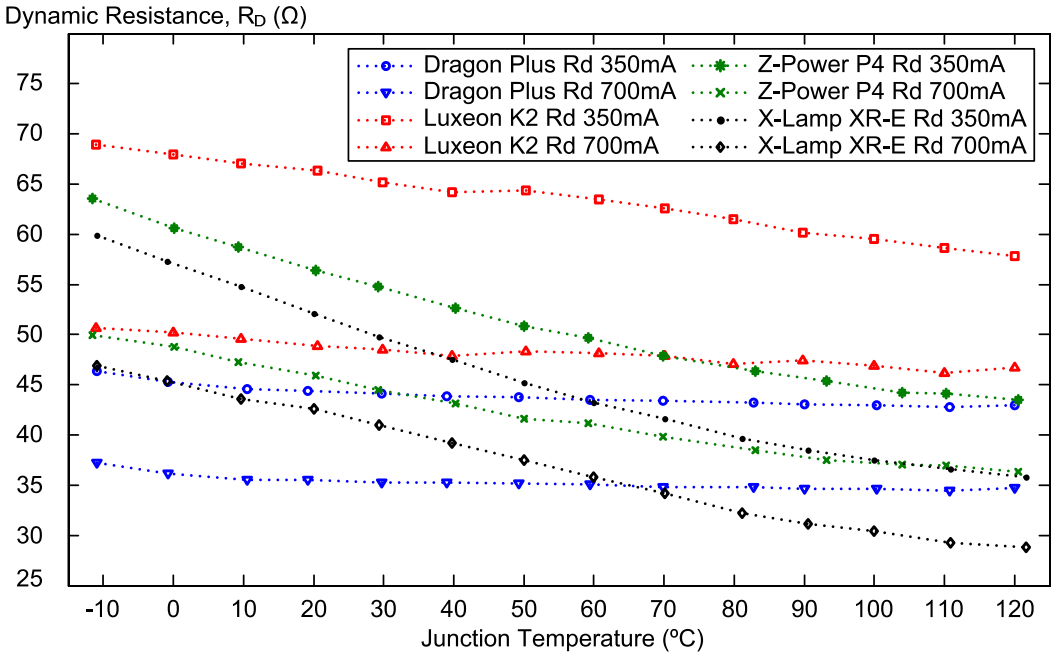

Fig. 2.21. Dynamic resistance theoretically calculated at 350 and 700 mA, reduced data set.

The theoretically calculated values for the dynamic resistance are gathered in Table A.XI in the Appendix A.

2.8.3. Experimental Results: V_D-T_j curve

The V_D-T_j curves show the relation between junction temperature and forward voltage drop for a given forward current. Thus, once the fitting is obtained for a given DUT at a given operation forward current over a wide range of temperatures, the junction temperature is easily measured by the forward voltage. The V_D-T_j curves were calculated from the experimentally obtained *I-V* fitting curves in both experimental tests: for the four single devices and for the four entire lamps. Regarding the low standard deviation in ambient temperatures and the dispersion in currents achieved, and in order to reduce the impact of individual deviations in the parameters extraction, the *I-V* fittings of the Reduced Data Set were employed in the case of the 60-LEDs lamps in order to obtain the forward voltage for each junction temperature for a given forward current, given the higher correlation coefficient obtained for those fittings. As the V_D-T_j data sets show a non-linear relation, second order polynomials will be used.

These experimental tests rose up some differences for both the single LED tests and the 60-LEDs lamps characterisation, as there were two devices featuring a fairly linear temperature dependence: the Golden Dragon Plus and the Luxeon K2 with TFFC, whereas the other two

devices showed a more pronounced quadratic relation. This experimental results have already been reported in [2.30], [2.38], [2.48] for the linear relation, and in [2.42] for the non-linear dependence, where the authors attribute this phenomenon to the major contribution to the series resistance of *p*-regions, *p*-waveguide and *p*-superlattice layers acting as cladding layers in GaN Laser Diodes (LDs), the latter not being present in LEDs that show a linear relation.

In the case of the single emitter test, the polynomial fits were obtained for currents from 100 mA to 1000 mA, plus 350 mA. Fig. 2.22 shows the experimental data along with the 2nd order polynomial fit obtained from the single emitter tests for the Golden Dragon Plus, Luxeon K2 with TFFC, Z-Power P4 and XLamp XR-E devices, respectively.

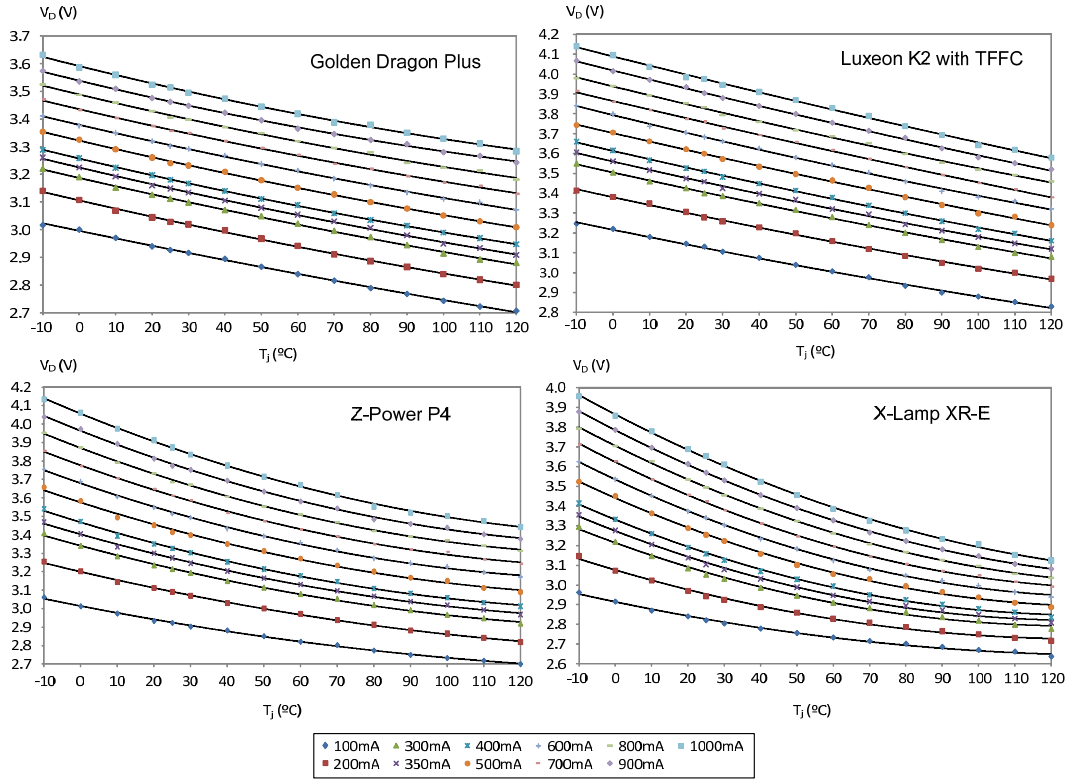

Fig. 2.22. Experimental results for the forward voltage as a function of the junction temperature for single emitter tests.

Tables A.XII to A.XVI show the 2nd order polynomial fit of the forward voltage drop related to junction temperature for each target current. These tables correspond to Golden Dragon Plus, Luxeon K2, Z-Power P4 and XLamp XR-E devices respectively. The correlation coefficient, r^2, is also shown. A good fit was achieved, with correlation coefficients around 0.999 and always above 0.995. These polynomials allow the calculation of the forward voltage for a given junction temperature, and inversely, the junction temperature can be estimated after measuring the forward voltage for a given injected current. Finally, a linear fit following (2.1) was also developed, in order to estimate the junction temperature more easily, and compared with the data provided by the manufacturers. The forward voltage temperature coefficient, *k'*, calculated from the experiments, the value provided by manufacturers, *k*, the fitting interval, and the correlation coefficient, r^2, are gathered in Table II.VII.

TABLE II.VII
EXPERIMENTAL TEMPERATURE COEFFICIENT OF FORWARD VOLTAGE (LINEAR FIT, SINGLE EMITTER TEST)

LED	*k'* (mV/ºC)	*Fitting Interval*	r^2	*k* (mV/ºC)
Golden Dragon Plus	-2.65	@ 350mA -10ºC ≤ Tj ≤ 120 ºC	0.9964	Chart [2.17]
Luxeon K2 TFFC	-4.30	@1000mA -10ºC ≤ Tj ≤ 120 ºC	0.9976	-2.8
Z-Power P4	-3.41	@350mA 25ºC ≤ Tj ≤ 100 C	0.9877	Chart [2.19]
XLamp XR-E	-3.40	@350mA 25ºC ≤ Tj ≤ 100 C	0.9749	-4

In the case of the 60-LEDs lamps, the V_D-T_j curves were calculated from the *I-V* fits for all the current levels considered in the experimental test. The V_D-T_j curves are depicted in Fig. A.6 in the Appendix A. However, only the V_D-T_j curves will be considered for the two most representative operation currents for these devices, i.e. 350 and 700 mA. However, the Luxeon K2 with TFFC V_D-T_j values will additionally be taken into account, as this is the manufacturer test current, in order to compare the results obtained in the single emitter and the entire-lamp test. Table A.II.-15 in the Appendix A shows the voltage values for each temperature at each forward current. These results are depicted in Fig. 2.23 for operation under 350 mA and Fig. 2.24 for 700 mA.

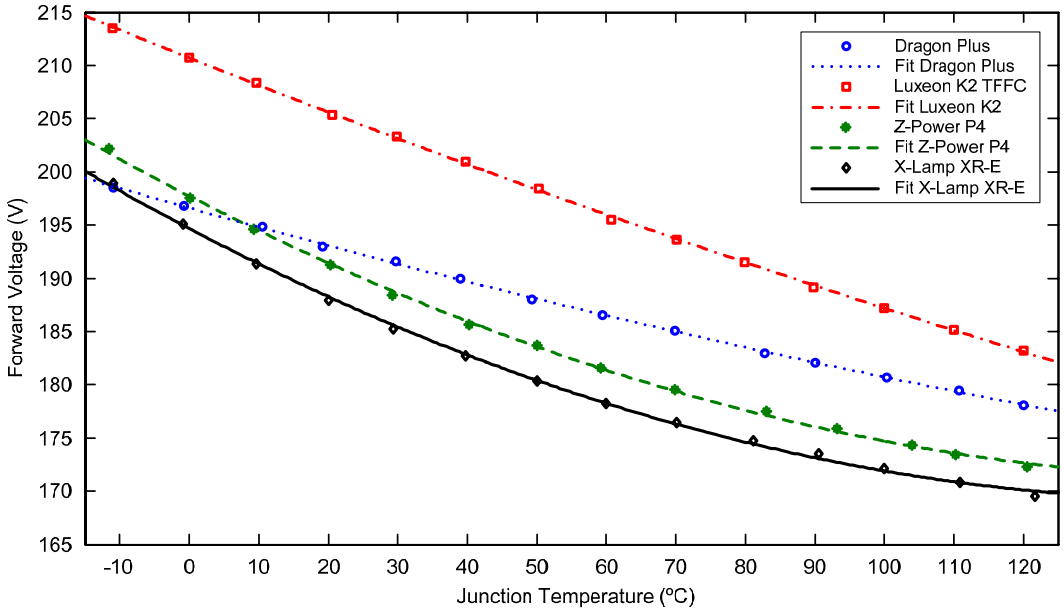

Fig. 2.23. V_D-T_j curves calculated from the *I-V* fits for the 60-series-LEDs lamps at 350 mA.

The 2nd order fitting polynomials are gathered in Table A.XVII and Table A.XVII in the Appendix A. In addition, linear fits were performed in order to estimate the junction temperature more easily. These results are shown in Table II.IX under 350 mA operation.

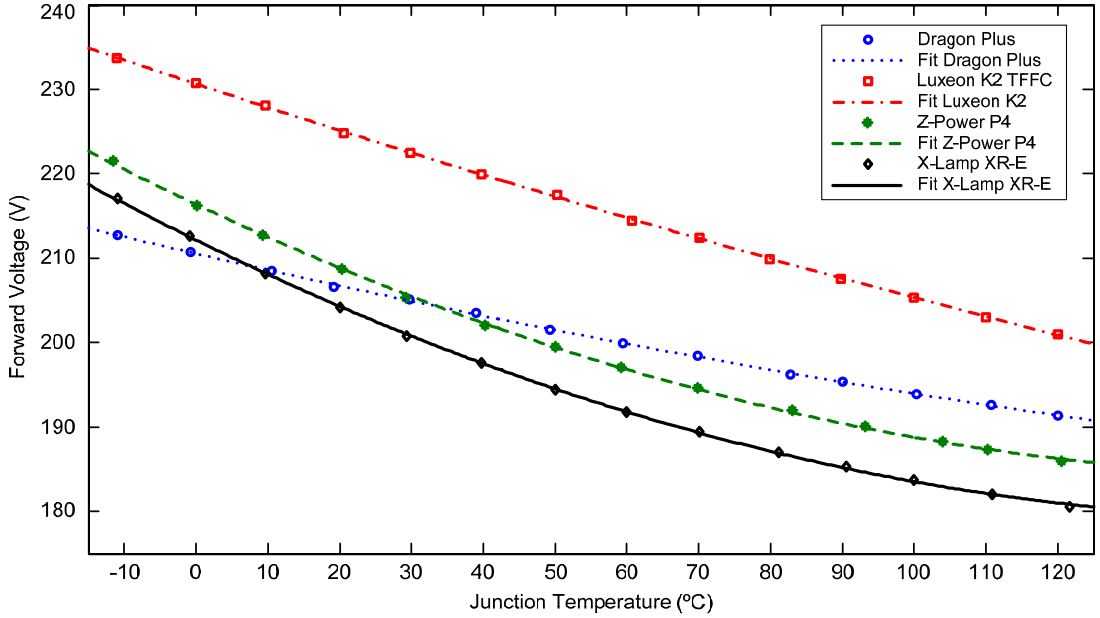

Fig. 2.24. V_D-T_j curves calculated from the *I*-*V* fits for the 60-series-LEDs lamps at 700 mA.

Finally, given the high linearity of the V_D-T_j curve of the Golden Dragon Plus and Luxeon K2 with TFFC devices, their linear fit is gathered in Table A.XIX for 350 and 700 mA operation currents for the entire temperature range.

In conclusion, the V_D-T_j curves of the LEDs under test have been experimentally obtained for a single emitter as well as for 60-series-LEDs lamps. Two different behaviours have been observed: whereas the Dragon Plus and the Luxeon K2 devices performed quite linearly, the Z-Power P4 and the XLamp XR-E featured a quadratic relation. Afterwards, the V_D-T_j curves have been fitted by 2nd order polynomials in order to achieve good accuracy. These polynomials allow for the junction temperature determination by measuring the forward voltage at a given forward current in subsequent tests.

2.9. Thermal Characterisation of LEDs: R_D-T_j curve

The variation of the dynamic resistance was discussed in Section 2.4, considering both the forward current and the junction temperature. Provided that the change in dynamic resistance and forward voltage induced by current and temperature modify the load connected to an electronic driver, this issue could cause a great impact on the closed-loop dynamics, depending on the sensitivity of this parameter to junction temperature. With the purpose of testing these implications, a small-signal characterisation was performed.

2.9.1. Description of the Workbench

The dynamic resistance of the four samples was measured using the following procedure, which has previously been introduced in [2.16]: each DUT is driven at different levels of forward current. A sinusoidal perturbation, i_{ac}, is superimposed to the DC current by using a specific driver. The amplitude of this sinusoidal perturbation is set to a given percentage over the DC current, I_{DC}, whereas the frequency is set to 1 kHz in order to avoid thermal effects due to the AC component. Then, the junction temperature of the DUT is modulated in the temperature-controlled chamber by the ambient temperature. Afterwards, the junction

TABLE II.VIII
EXPERIMENTAL TEMPERATURE COEFFICIENT OF FORWARD VOLTAGE (LINEAR FIT, 60-LEDS LAMPS TEST)

LED	*k'* (mV/ºC)	*Fitting Interval*	r^2
Golden Dragon Plus	-156.5	@ 350mA -10ºC ≤ Tj ≤ 120 ºC	0.9967
Luxeon K2 TFFC	-232.8	@350mA -10ºC ≤ Tj ≤ 120 ºC	0.9983
	-256.9	@1000mA -10ºC ≤ Tj ≤ 120 ºC	0.9977
Z-Power P4	-186.5	@350mA 25ºC ≤ Tj ≤ 100 C	0.9898
XLamp XR-E	-183.7	@350mA 25ºC ≤ Tj ≤ 100 C	0.9871

temperature is determined by measuring the forward voltage and using the fitting polynomials obtained in the previous section and gathered in the Appendix A.

Consequently, the small-signal dynamic resistance, r_D, can be calculated for each operation point as:

$$r_D = \frac{v_{ac}}{i_{ac}}\Big]_{I_D,T_j} \tag{2.20}$$

where v_{ac} is the AC voltage measured across the LED. Therefore, the variables to be measured are the AC voltage and AC current, in order to obtain the dynamic resistance; DC current to set the operation point; and DC voltage, in order to determine the junction temperature.

This procedure was applied to both the single emitters and the 60-series-LEDs lamps. Regarding the single-emitters test, the 1 kHz sinusoidal perturbation was set to a 10% over the DC current level. The test DC currents were the three rated ones of the devices, i.e. 350, 700 and 1000 mA. The ambient temperature was varied from -30 ºC to 80 ºC by 10 ºC steps, plus 25 ºC. Forced convection was applied in order to reduce the board-to-ambient thermal resistance and the thermal impedance. The workbench is sketched in Fig. 2.25.

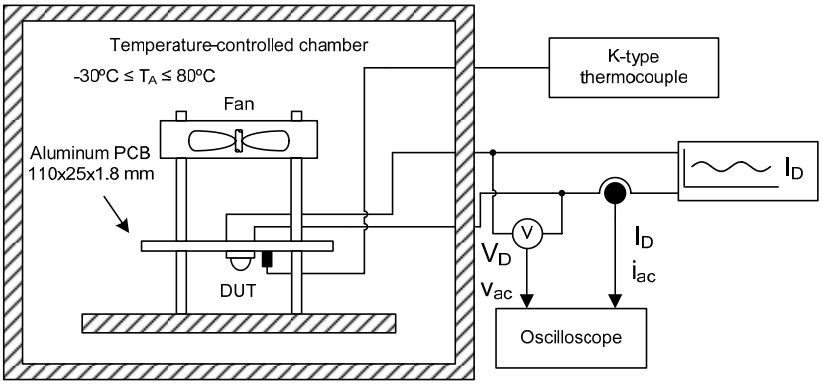

Fig. 2.25. Experimental arrangement in order to determine the dynamic resistance versus junction temperature relation for a single DUT test.

With regard to the 60-LEDs lamps test, only operation under 350 mA and 700 mA was considered, as the operation under 1000 mA leads to a total power dissipation greater than 240 W, which is out of the scope of this work. In addition, the current ripple superimposed was varied from 10% to 40% of the DC current level in 10% steps in order to check whether the peak-to-valley value affects the dynamic resistance due to the intrinsic *I-V* curve non-linearity and due to thermal effects. The AC component was kept at 1 kHz. However, as both Integrated-Single-Stage Converters (ISSC) and Single-Stage Converters (SSC) feature an output current low-frequency ripple at twice the line frequency, the same test was developed with an AC perturbation at 100 Hz in order to check the performance under these conditions in the worst case, which is the 50 Hz European mains supply.

The ambient temperature was varied from -20 ºC to the level at which 120 ºC junction temperature was reached in every case, in 10 ºC steps. The junction temperature was measured by the forward voltage and the polynomials obtained in the previous section. The experimental values are gathered in Table A.XVII and Table A.XVIII in the Appendix A. The experimental workbench is sketched in Fig. 2.26.

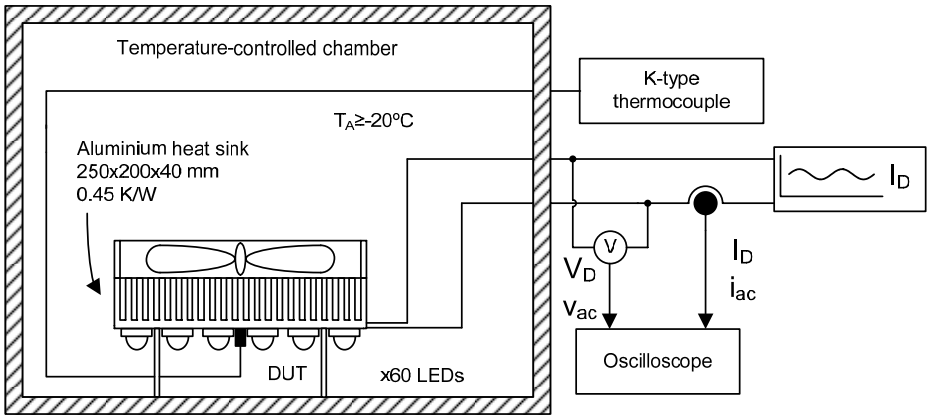

Fig. 2.26. Experimental arrangement in order to establish the dynamic resistance versus junction temperature relation for the 60-series-LEDs lamps.

As the measured parameters were the forward voltage and the dynamic resistance of the ensemble i.e. the entire lamp, [2.26], [2.32], the individual values obtained may vary depending on the physical position on the PCB due to the surface temperature gradients produced across the PCB and the heatsink. In order to minimise this issue, forced convection was applied. However, even assuming that the thermal gradient has been minimised, there would still exist some dispersion in the junction temperature caused by the inherent dispersion of the LEDs thermal resistance among emitters. Nevertheless, this gives the average figure of merit for a generic lamp according to the Gaussian distribution assumed for the LEDs parameters, as described in Section 2.7.

2.9.2. Experimental Results

With respect to the dynamic resistance related to the forward current, all the devices performed as previously expected, since the dynamic resistance underwent a drop as the injected current was stepped up at constant temperature in both tests. Nevertheless, there are slight differences between the four samples tested. In the single-emitter tests, it can be seen in Fig. 2.27 that in those devices featuring a more quadratic V_D-T_j dependence –this is, the XLamp XR-E and the Z-Power P4 devices, the dynamic resistance values were overlapped for different

current levels at different junction temperatures, especially for the XLamp XR-E device. However, for the devices performing a more linear V_D-T_j relation –this is, the Luxeon K2 and the Golden Dragon Plus devices, the dynamic resistance values were clearly delimited for each current level at the whole temperature range, with no dynamic resistance overlap for the entire junction temperature range.

Nonetheless, noticeable differences among the different LEDs – in both the single-emitter test and the 60-LEDs lamps tests, were found regarding the behaviour of the dynamic resistance versus the junction temperature under constant forward current. Thus, in the single-emitter tests, all the devices except for the Golden Dragon Plus experienced a decrease on the dynamic resistance as the junction temperature was increased for the three current injection levels: 350 mA, 700 mA, and 1000 mA, as can be seen in Fig. 2.27.

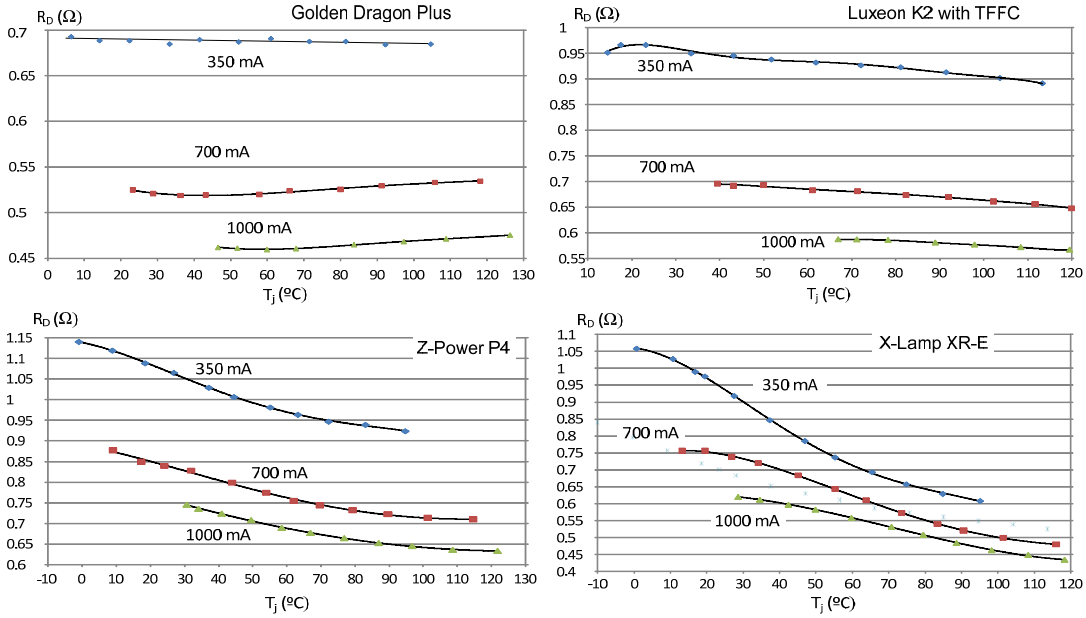

Fig. 2.27. Experimental results for the dynamic resistance as a function of the junction temperature for single-emitter tests.

Considering the Golden Dragon Plus device, the dynamic resistance at the 350 mA test remained fairly constant for the entire temperature range, up to approximately 105 ºC, whereas for the 700 mA and 1000 mA test featured a decrease at the lowest ambient temperatures followed by an increase with lowering slope after a minimum corresponding to an ambient temperature of -10 ºC.

Regarding the Luxeon K2 with TFFC device driven at 350 mA, the dynamic resistance showed a maximum at junction temperatures around 25 ºC, decreasing towards low and high temperatures. At the injection current levels of 700 and 1000 mA, the dynamic resistance seemed to reach a maximum at the lowest ambient temperatures and a decrease with increasing slope, as can be seen in Fig. 2.27. Finally, and as in the V_D-T_j characterisation, the XLamp XR-E and the Z-Power P4 devices experienced a very similar behaviour. Both featured a fall in dynamic resistance as the junction temperature rose, with decreasing slope at the lowest and highest temperatures, suggesting maximums and minimums at those levels, respectively.

The R_D-T_j curves were linearly fitted in the case of the Golden Dragon Plus at 350mA due to the fairly flat curve achieved, whereas second order polynomials were used in the case of the

Golden Dragon Plus device at 700 and 1000 mA, Luxeon K2 with TFFC, and Z-Power P4 at 700 and 1000 mA. Finally, in the case of the Z-Power P4 at 350 mA and the XLamp XR-E at all currents, third-order polynomials were employed. This is justified by a trade-off between the lowest-order and best-fitting polynomial. The results are gathered in Table II.IX. In addition, as the Golden Dragon Plus dynamic resistance at 350 mA featured a fairly flat value, the average value could also be considered. In this way, the average dynamic resistance for the entire temperature ranges is 687.7 mΩ with only 2.67 mΩ of standard deviation.

TABLE II.IX
DYNAMIC RESISTANCE: POLYNOMIAL FIT, SINGLE-EMITTER TEST

LED	$R_D = a \cdot T_j^3 + b \cdot T_j^2 + c \cdot T_j + d$ (Ω)				r^2
	a (mΩ/ºC^3)	b (mΩ/ºC^2)	c (mΩ/ºC)	d (Ω)	
Golden Dragon Plus 350mA	0	0	-0.05	0.6904	0.3804
Golden Dragon Plus 700mA	0	0.003	-0.2	0.5256	0.8947
Golden Dragon Plus 1000mA	0	0.002	-0.2	0.4644	0.9577
Luxeon K2 TFFC 350mA	0	-0.002	-0.4	0.9684	0.9599
Luxeon K2 TFFC 700mA	0	-0.002	-0.2	0.7065	0.9907
Luxeon K2 TFFC 1000mA	0	-0.003	0.1	0.5926	0.9937
Z-Power P4 350mA	2E-4	-0.010	-2.7	1.1404	0.9983
Z-Power P4 700mA	0	0.010	-3.1	0.9063	0.9943
Z-Power P4 1000mA	0	0.010	-3.0	0.8259	0.9993
XLamp XR-E 350mA	6E-4	-0.070	-4.2	1.0706	0.9981
XLamp XR-E 700mA	4E-4	-0.080	1.0	0.7600	0.9993
XLamp XR-E 1000mA	3E-4	-0.060	1.5	0.6190	0.9997

The highest shift in dynamic resistance corresponds to the XLamp XR-E device at 350 mA, with a drop from 1.06 Ω down to 0.61 Ω, i.e. a 42%. On the contrary, the lowest drop in dynamic resistance was featured by the Golden Dragon Plus, with a fairly constant curve at 350 mA for the entire test temperature range.

Regarding the 60-LEDs lamp tests at 1 kHz, the same general results were obtained, as all devices featured a lower dynamic resistance at 700 mA. However, the dynamic resistance values slightly varied according to the current ripple, as can be seen in Fig. 2.28 for the Golden Dragon Plus device, Fig. 2.29 for the Luxeon K2 device, Fig. 2.30 for the Z-Power P4 device, and Fig. 2.31 for the XLamp XR-E device. These values of dynamic resistance for each current and current ripple are gathered in Table A.XX through Table A.XVII.

In this way, the general trend shows an increase in the dynamic resistance as the current ripple is increased, this phenomenon being more noticeable for the 350 mA current level, especially in the case of the Golden Dragon Plus and the Luxeon K2 with TFFC, whereas it is almost imperceptible at 700 mA in all devices.

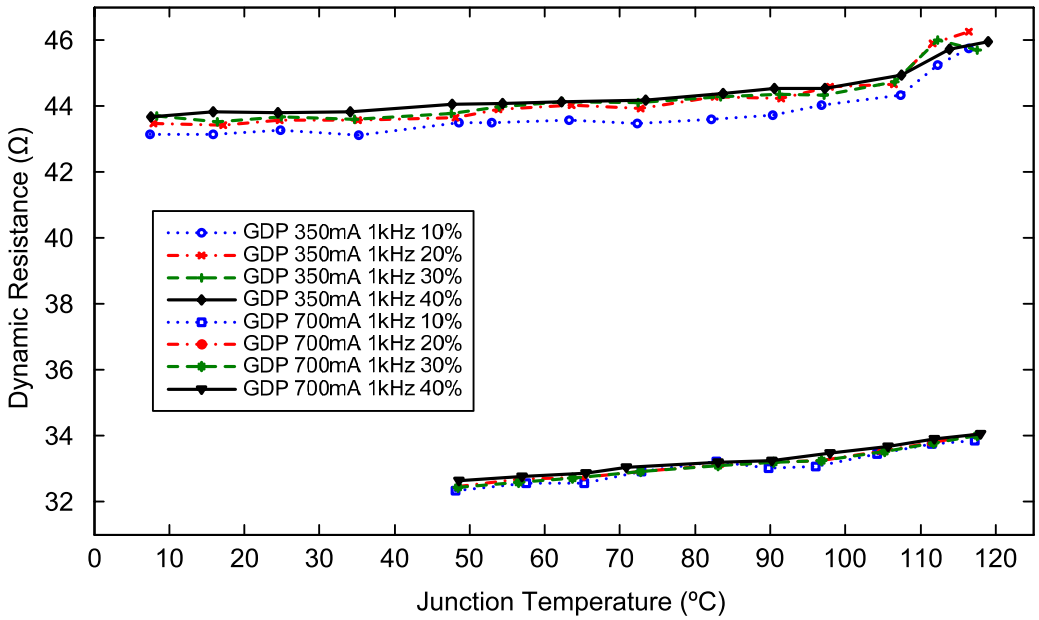

Fig. 2.28. Experimental results for the dynamic resistance as a function of the junction temperature and the current ripple for the Golden Dragon Plus device.

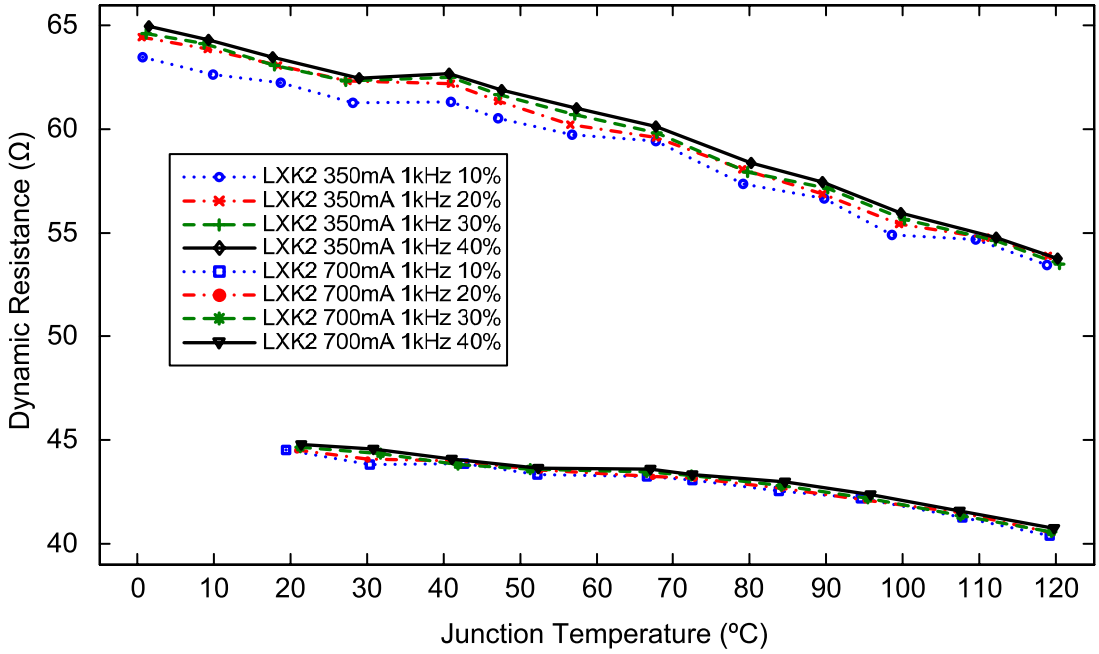

Fig. 2.29. Experimental results for the dynamic resistance as a function of the junction temperature and the current ripple for the Luxeon K2 device.

In the case of the variation of dynamic resistance due to temperature changes, it should be noted that, due to the higher power dissipation and the limitations on thermal resistance of the heatsinks used in the tests, it was impossible to reach such low temperatures as in the single-emitters tests for the 700 mA current level. However, the LEDs performed exactly as the single-emitter tests showed for the entire temperature range, except for the Golden Dragon Plus at 350 mA. In this case, the dynamic resistance underwent an increase as the junction temperature was increased, with a sharp increase from approximately 105 ºC onwards. This result is also contrary to the dynamic resistance shift predicted for this device, since the theoretically-determined

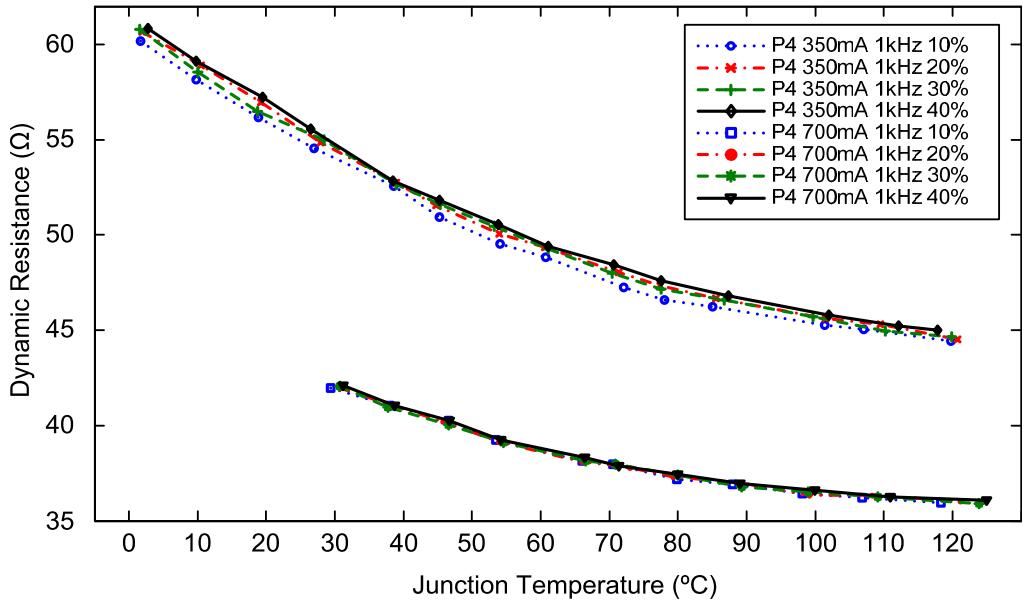

Fig. 2.30. Experimental results for the dynamic resistance as a function of the junction temperature and the current ripple for the Z-Power P4 device.

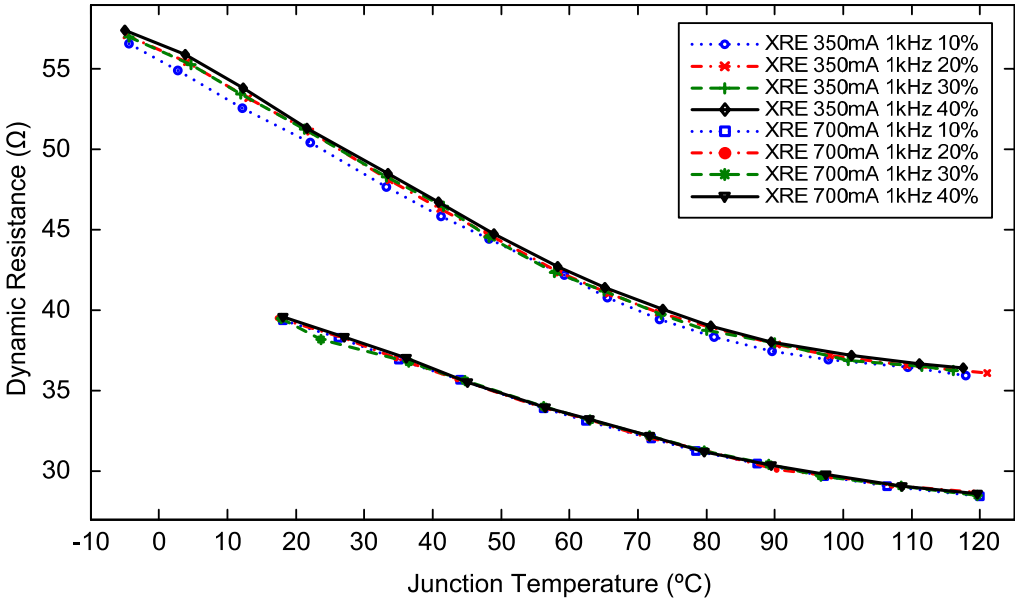

Fig. 2.31. Experimental results for the dynamic resistance as a function of the junction temperature and the current ripple for the XLamp XR-E device.

dynamic resistance curve was found to feature a falling characteristic as the temperature rises. Nevertheless, up to approximately 100 ºC, the change in dynamic resistance is lower than 1 Ω for the entire lamp.

Finally, as in the single-emitter tests, the dynamic resistance was fitted by the lowest-order, best-fitting polynomial. These results are gathered in Table II.X. Only the 10% current ripple results will be fitted, since the high-frequency ripple in most applications is generally small.

These fits are shown in Fig. 2.32 for the 350 mA operation current, and Fig. 2.33 for the 700 mA operation current.

TABLE II.X
DYNAMIC RESISTANCE: POLYNOMIAL FIT, 60-LEDS LAMPS TEST, 1 KHZ, 10% CURRENT RIPPLE

LED	$R_D = a \cdot T_j^3 + b \cdot T_j^2 + c \cdot T_j + d$ (Ω)				r^2
	a (mΩ/ºC^3)	b (mΩ/ºC^2)	c (mΩ/ºC)	d (Ω)	
Golden Dragon Plus 350mA	0	0.3134	-21.79	43.49	0.8648
Golden Dragon Plus 700mA	0	0.1003	4.421	31.93	0.9359
Luxeon K2 TFFC 350mA	0	-0.3427	-43.12	63.26	0.9865
Luxeon K2 TFFC 700mA	0	-0.2828	2.302	44.28	0.9767
Z-Power P4 350mA	0	1.0420	-259.3	60.67	0.9991
Z-Power P4 700mA	0	0.6766	-168.1	46.41	0.9979
XLamp XR-E 350mA	8.366E-3	-0.4035	-233.0	55.55	0.9996
XLamp XR-E 700mA	3.811E-3	-0.1819	-146.7	42.11	0.9999

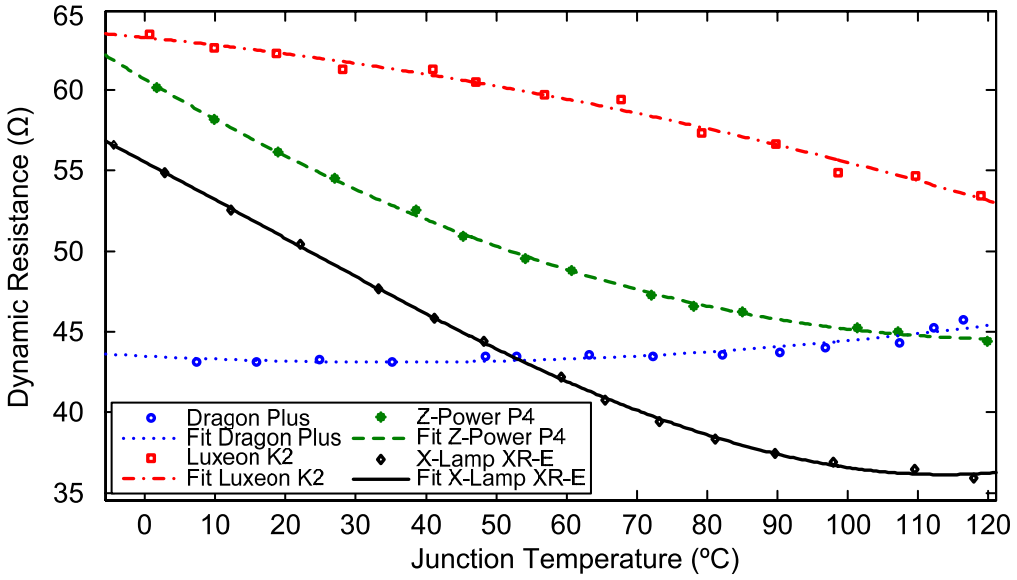

Fig. 2.32. Polynomial fit of the dynamic resistance at 350 mA, 1 kHz current ripple.

Moreover, careful inspection of the Golden Dragon Plus device fit at 350 mA can conclude that, for junction temperatures below 100 ºC, an acceptable linear fit may be obtained in the shape $c \cdot Tj(ºC)+d$ with $c = 8.455$ mΩ/ºC and $d = 43.01$ Ω, featuring an $r^2 = 0.8395$ and a Sum of Square Errors (SSE) of 0.126. Moreover, even when considering the average value for junction temperatures below 100 ºC the SSE is 0.7854 for an average value of 43.46 Ω. Therefore, a constant dynamic resistance between 10ºC and 100ºC can be considered without a significant lack of accuracy.

With regard to the 100 Hz test, it is important to remark that, since the thermal time constant of LEDs is in the range of milliseconds, as the period of the low-frequency ripple, thermal effects are expected due to this AC component. Thus, the junction temperature would not be constant through the low-frequency ripple period, featuring a low-frequency modulation induced by the AC current component, with higher temperatures during the peak-current periods

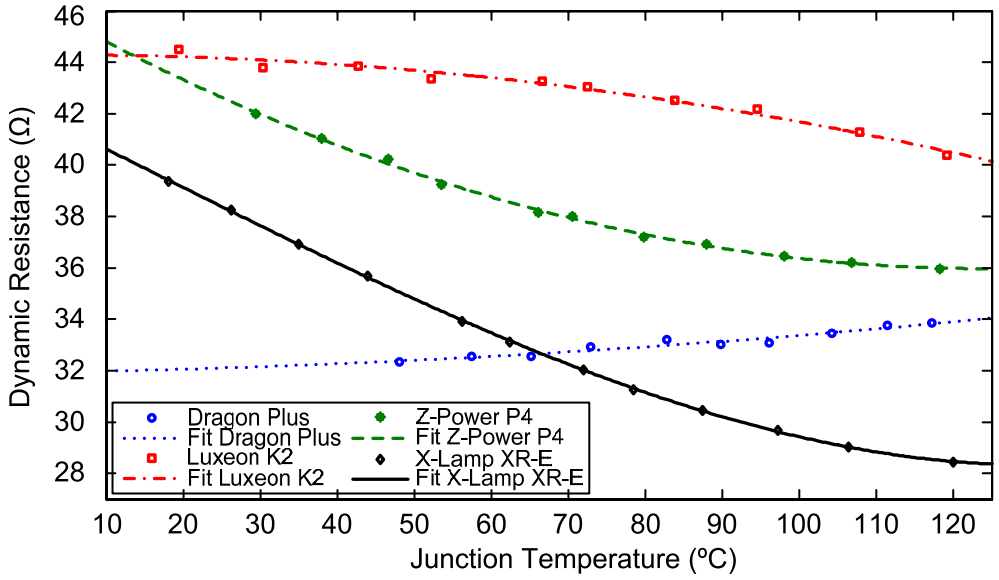

Fig. 2.33. Polynomial fit of the dynamic resistance at 700 mA, 1 kHz current ripple.

and lower during the valley periods. A higher junction temperature for the peak values of the AC ripple implies that the *I-V* curve would experience a drop in the forward voltage, whereas the junction temperature would remain lower at the valley AC ripple, inducing a rise in forward voltage if compared to a high-frequency ripple with no junction temperature modulation. The main consequence is that the average junction temperature would be the nominal temperature, but different from those values at the peak and the valley AC ripple due to this temperature modulation effect, leading to a shift in the small-signal *I-V* curve slope. This would induce a change in the dynamic resistance for those periods. Since the drop in forward voltage at high currents with a rise in forward voltage at low currents yields to a higher slope, an average lower dynamic resistance is expected. Fig. 2.34, Fig. 2.35, Fig. 2.36, and Fig. 2.37 show the experimental results of the 100 Hz test for the Dragon Plus, Luxeon K2, Z-Power P4, and XLamp XR-E devices, respectively, at 350 and 700 mA together with the fitting polynomials used for each current ripple at each current level. In addition, the experimental values are gathered from Table A.XVIII to Table A.XXXV in the Appendix A.

Since this test is intended to predict the behaviour of the LEDs under significant low-frequency ripples, such as those likely to be found on the output currents or voltages of ISSCs and SSCs, the dynamic resistance curves were also fitted according to the current ripple. The results are gathered in Tables A.XXXVI to Table A.XXXIX in the Appendix A for the Golden Dragon Plus, Luxeon K2 with TFFC, Z-Power P4 and XLamp XR-E lamps, respectively. In addition, the same procedure as in the case for the 1 kHz AC perturbation can be followed in order to achieve an acceptable linear fit for a defined temperature range. Thus, for junction temperatures below 100 ºC, a linear fit can be established, the results being gathered in Table A.XL in the Appendix A.

As can be seen from the figures, the four LED lamps behaved as in the 1 kHz test, with decreasing values as the current was increased and decreasing values for rising temperature except for the Golden Dragon Plus at 350 mA. The latter underwent an increase in dynamic resistance as the junction temperature was raised with a sharper slope from approximately 110 ºC onwards. In addition, increasing dynamic resistance values for higher current ripples at 350 mA effect, which was found to be negligible at 700 mA, were observed as in the 1 kHz test.

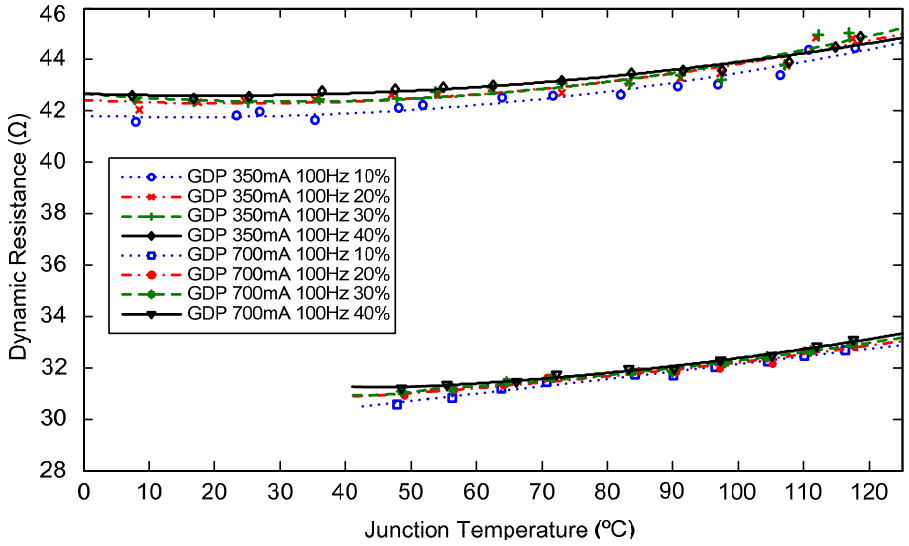

Fig. 2.34. Experimental results and polynomial fits for the dynamic resistance as a function of the junction temperature and the 100 Hz current ripple for the Golden Dragon Plus device.

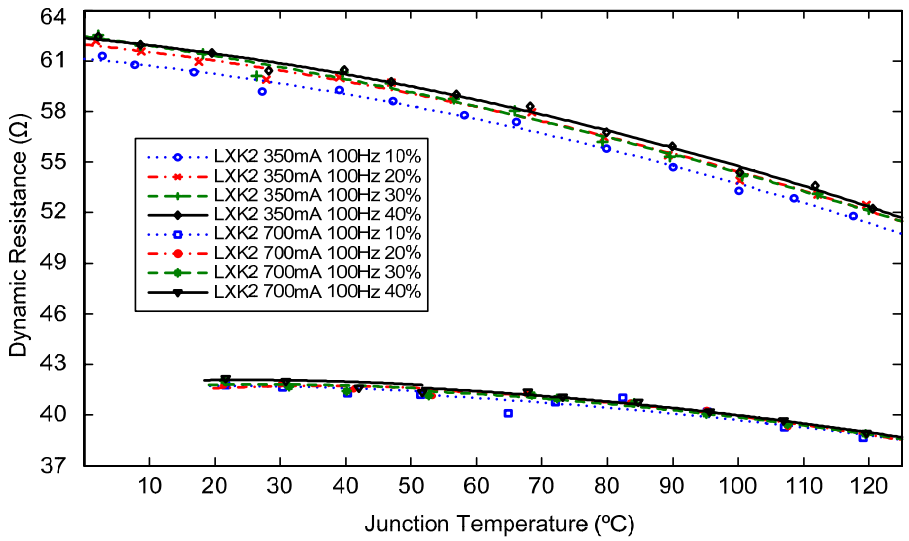

Fig. 2.35. Experimental results and polynomial fits for the dynamic resistance as a function of the junction temperature and the 100 Hz current ripple for Luxeon K2 device.

Finally, as can be seen, the dynamic resistance values are lower at the 100 Hz test than those at the 1 kHz test, confirming the supposition of a lower dynamic resistance due to thermal effects. This can also be verified from the waveforms obtained in both small-signal tests. Fig. 2.38 shows the waveforms corresponding to the Z-Power P4 device at 350 mA, 40% current ripple at 1 kHz and 100 Hz as well as the *X*-*Y* diagram for both operation points showing the AC current vs. the AC voltage, i.e. the small-signal dynamic resistance.

As can be seen from Fig. 2.38, the low-frequency ripple imposed by the ac-current component induces a thermal shift in the *p*-*n* junction within the disturbance period, leading to a higher forward voltage drop at the peak currents. This yields a phase shift between the AC current and the AC voltage, which can be noted from the *X*-*Y* diagram: whereas the 1 kHz small-signal disturbance features a pure resistive behaviour, the *X*-*Y* diagram shows an "ellipsoidal" characteristic in the case of the low-frequency disturbance, due to an *I*-*V* curve

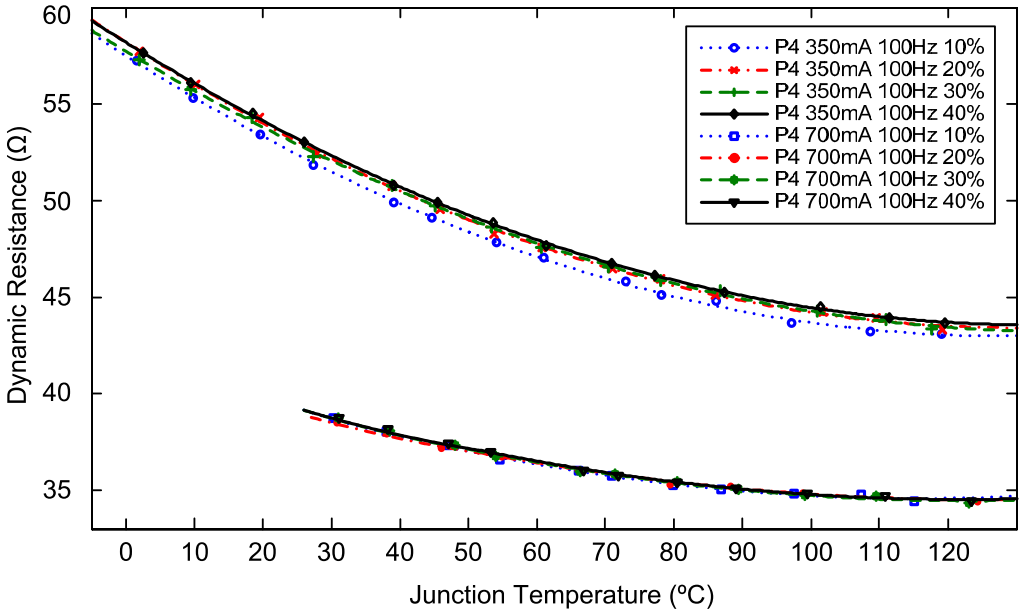

Fig. 2.36. Experimental results and polynomial fits for the dynamic resistance as a function of the junction temperature and the 100 Hz current ripple for the Z-Power P4 device.

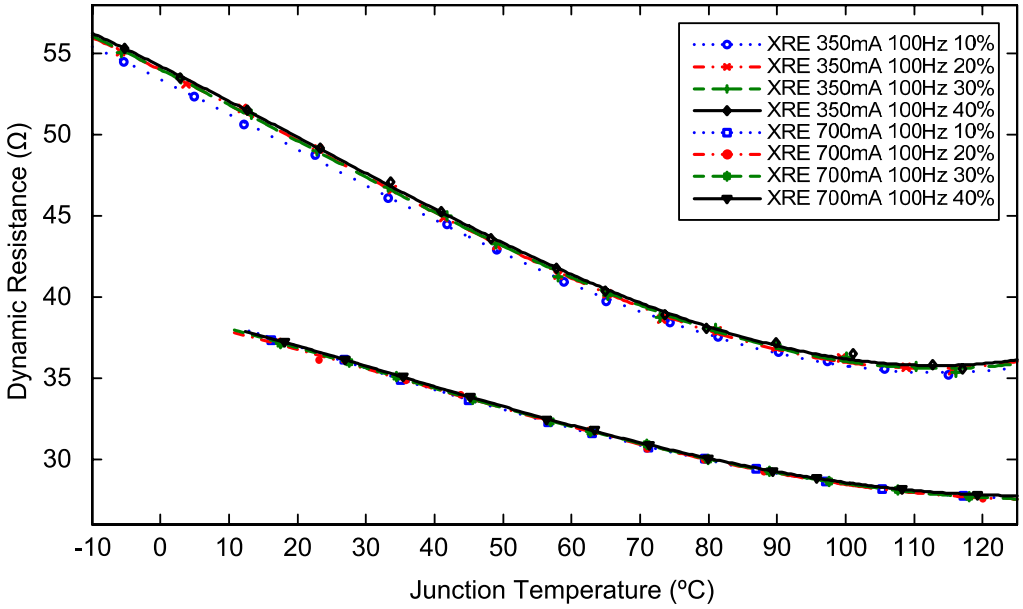

Fig. 2.37. Experimental results and polynomial fits for the dynamic resistance as a function of the junction temperature and the 100 Hz current ripple for the XLamp XR-E device.

shifted to higher forward voltage drop at the peak currents, and an *I-V* curve shifted to lower forward voltage drop at the valley currents, leading to a "reactive-like" behaviour with phase-leaded voltage at low frequencies.

2.9.3. Discussion

Several experimental tests were performed in order to check the theoretical calculations and the deviation in characteristics. Thus, the temperature of the LED lamp was measured by IR

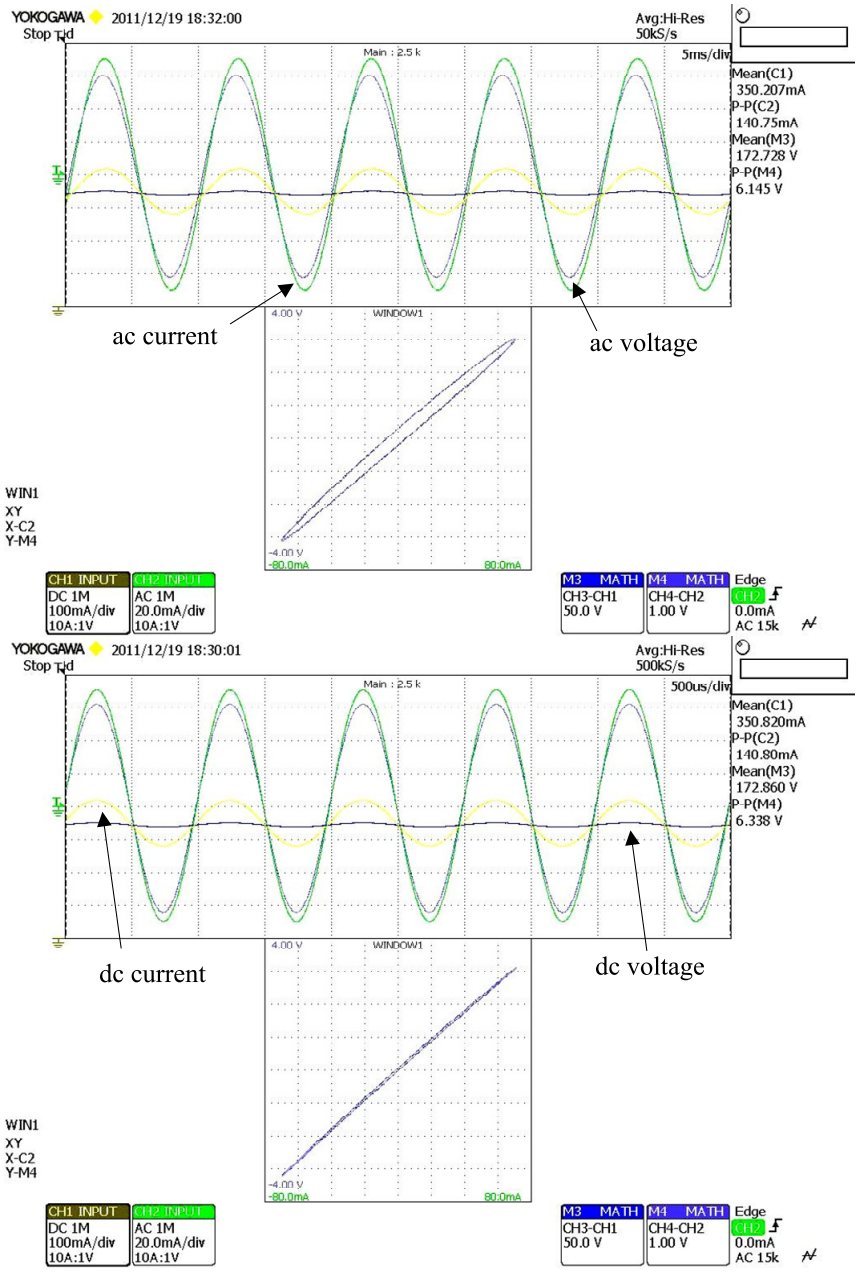

Fig. 2.38. Small-signal waveforms of the 100 Hz (upper screen snap-shot) and 1 kHz (lower screen snap-shot) test. Upper trace: dc voltage (50 V/div), AC voltage (1 V/div), dc current (100 mA/div), and AC current (20 mA/div). Horizontal scale: 5 ms/div (upper screen snap-shot), 500 µs/div (lower screen snap-shot). Lower trace: X-Y diagram of AC voltage vs. AC current. Horizontal scale: 80 mA/div. Vertical scale: 4 V/div.

thermography, and the characteristics obtained from the single-emitter and the 60-LEDs tests were contrasted.

2.9.3.1. Junction temperature measurement by IR thermography

In order to compare whether the performance of the 60-LEDs lamps, as well as that of single emitters, matches the average predicted values, the lamp temperature was measured by infrared (IR) thermography in steady-state operation at 350 mA under natural convection. Besides, the ensemble voltage drop was recorded in order to calculate the average junction temperature, and the individual voltage drop of each LED composing the lamp was recorded in

order to check whether the fitting polynomial is applicable to single-LEDs, either binned or unbinned, for accurately determining the junction temperature. The workbench developed for this test is shown in Fig. 2.39. The temperature contour plots are depicted in Fig. 2.40.

Fig. 2.39. Experimental workbench for measuring the lamp temperature by IR thermography.

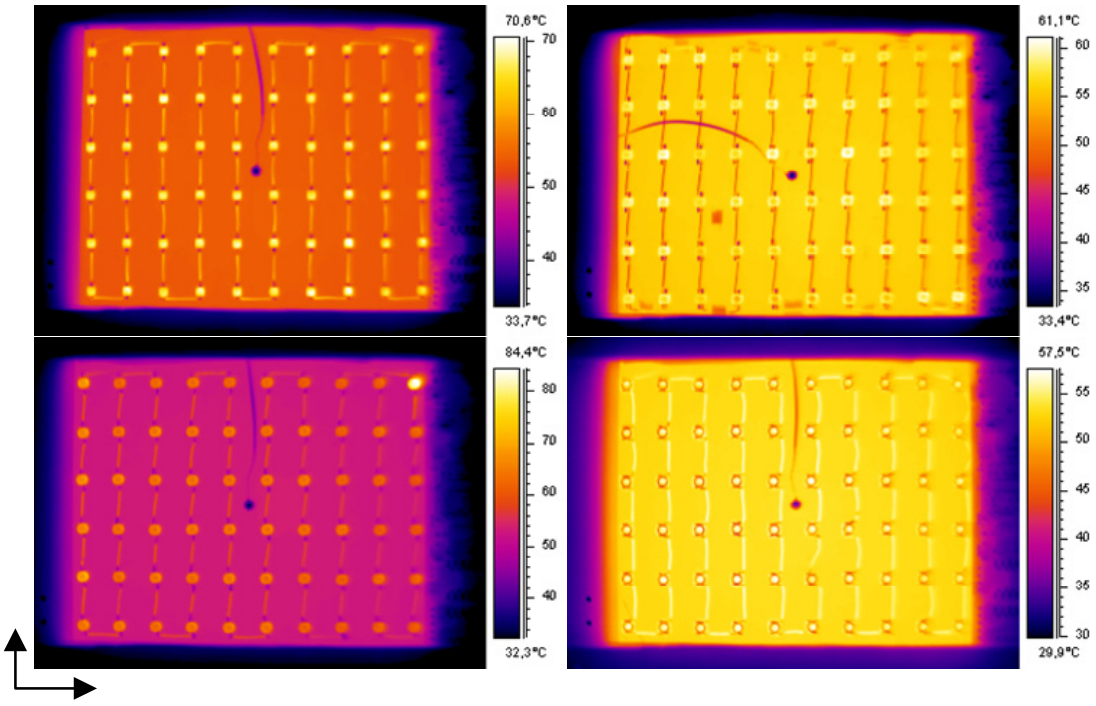

Fig. 2.40. Temperature contour plot by IR thermography. Upper left: Golden Dragon Plus. Upper right: Luxeon K2 with TFFC. Lower left: Z-Power P4. Lower right: XLamp XR-E.

These contour plots were obtained once the temperature was stabilised. The board temperature was also measured at the centre of the heatsink by a K-type thermocouple screwed into it, corresponding to the dark point seen in the figure. The lamp forward voltage was measured in order to predict the ensemble junction temperature by using the fitting polynomials obtained in the previous sections. As can be seen from the figure, an even temperature distribution is reached throughout the heatsink, being around 50 – 55 ºC for the four LED lamps. This result seems reasonable, since the power dissipation level was similar in all the

LED lamps and the four heatsinks were identical. However, substantial differences regarding the LEDs were found. Firstly, it can be seen that, depending on the LED package, IR thermography measures either the case or the lens temperature, but not the junction temperature. This can be observed from the captions corresponding to the Luxeon K2 with TFFC and the Z-Power P4, since the temperature measured for the case is higher than the value registered for the centre of the package, this is, the lens, whereas the XLamp XR-E and the Golden Dragon Plus devices showed higher temperatures at the lens than those corresponding to the case. Since there is a significant thermal resistance between the junction and the case, it can be concluded that IR thermography allows the junction temperature calculation by estimation after the power dissipation and the thermal resistance are determined.

Secondly, the thermal resistance from the junction to the case of each device can be compared, since the temperature gap is higher in those LEDs featuring a higher thermal resistance. This procedure also allows the thermal resistance to be compared within the same array provided that there is an even temperature distribution at the heatsink. Thus, it can be seen that the highest thermal resistance corresponds to the Golden Dragon Plus, with the largest temperature gap between the heatsink surface and the hottest point in the case. On the other side, the other lamps showed lower thermal resistances, since the temperature at the hottest point was closer to that of the heatsink. Moreover, it has to be remarked that this technique allows thermal failures to be predicted, since information about the thermal resistance of a single LED can be estimated. Thus, it can be seen that in the case of the Z-Power P4 lamp, there is an LED working at higher temperatures than the rest of the lamp, whereas the heatsink features an even temperature distribution. This was found to be caused by partial detachment of the LED from the thermal bond, leading to a higher thermal resistance and thus, a higher junction temperature.

Table II.XI gathers the experimental results corresponding to the entire lamp measurements and from measuring LED by LED. With regard to the first measurements, the following variables could be obtained:

- the ensemble forward voltage, V_D *(ensemble)*;
- the ensemble junction temperature obtained from the ensemble voltage, T_j *(ensemble)*;
- the ambient temperature, T_A;
- the board temperature, T_B;
- the total power dissipation, P_D;
- the junction-to-board thermal resistance, $R_{\theta j\text{-}b}$, calculated from (2.13).

With regard to the results obtained by measuring LED by LED values, Table II.XI shows the minimum and maximum LED forward voltage for each lamp, V_{Dmin} and V_{Dmax}, respectively; the sample average LED forward voltage obtained as the average of each LED forward voltage individually measured, V_{Davg}; the sample standard deviation of forward voltage, S_V; the average junction temperature calculated as the average of each single LED temperature, T_{jAVG}, which in turn has been obtained by applying the fitting polynomials introduced in Section 2.8.3 to each LED forward voltage; the minimum and maximum LED junction temperature for each lamp, T_{jmin} and T_{jmax}; the sample standard deviation of junction temperature, S_T; the entire-lamp forward voltage calculated as the sum of each LED forward voltage, V_D (total); and the junction temperature obtained by applying the fitting polynomials to the total forward voltage, T_j (total). The values in parenthesis are those corresponding to the Z-Power P4 lamp after discarding the partially-detached LED.

TABLE II.XI
EXPERIMENTAL RESULTS FROM THE IR THERMOGRAPHY TEST

LED	Golden Dragon Plus	Luxeon K2 TFFC	Z-Power P4	XLamp XR-E
V_D *(ensemble)* (V)	184.46	190.57	181.32	179.98
T_j *(ensemble)* (ºC)	75.4	84.2	60.3	51.9
T_A (ºC)	26.1	25.9	24.4	25.6
T_B (ºC)	51.1	53.5	54.1	50.0
P_D (W)	65.2	67.3	64.0	63.6
$R_{\theta j\text{-}b}$ (ºC/W)	22.4	27.4	5.8	1.8
V_{DAVG} (V)	3.076	3.174	3.022 (*3.024*)	2.986
V_{Dmin} (V)	2.982	3.082	2.888 (*2.928*)	2.896
V_{Dmax} (V)	3.293	3.299	3.085	3.369
S_V (V)	0.069	0.040	0.042 (*0.039*)	0.101
T_{jAVG} (ºC)	74.8	85.0	61.2 (*60.4*)	58.5
T_{jmin} (ºC)	-8.2	51.5	43.6	-20.4
T_{jmax} (ºC)	110.9	110.8	113.4 (*92.6*)	85.4
S_T (ºC)	26.4	10.9	13.4 (*11.6*)	23.5
V_D *(sum)* (V)	184.56	190.43	181.32 (*178.43*)	179.19
T_j *(sum)* (ºC)	74.8	84.9	60.3 (*59.7*)	55.5

Fig. 2.41 shows the 3D temperature surface plot obtained by IR thermography, where the board, case and lens temperatures can be seen (on the left). It also shows the junction temperature bar plot obtained from measuring the forward voltage drop of each individual LED and estimating its junction temperature with the fitting polynomials obtained in Section 2.8.3 (on the right). The bar plot is observed from the same point of view as the 3D surface plot. As can be observed from Fig. 2.41, the maximum temperatures obtained by IR thermography are close, yet lower, to the ensemble junction temperature obtained by estimation using each LED-lamp fitting polynomials. Thus, it can be concluded that IR thermography actually measures the lens temperature, which features its own thermal resistance between the chip and the ambient, thus introducing a temperature gradient. Moreover, it can be noticed that the application of the normalised fitting polynomials to the calculation of the junction temperature by measuring each individual LED forward voltage drop yields misleading results, even in the case of binned LEDs, although the measurements are closer to the ensemble temperature measured. This way, although a general trend can be observed, especially in the case of the partially-detached Z-Power P4 LED, there is a large difference in individually-estimated junction temperature between the LEDs in the lamp, even though their case temperature is similar. In addition, it can be seen from Table II.XI that the average value of the individual junction temperatures calculated by each LED forward voltage drop tends to the value obtained from the ensemble measurements.

The junction temperature, as introduced in Section 2.5, can be estimated by (2.10) once the power dissipation, the board temperature and the thermal resistance between the junction and

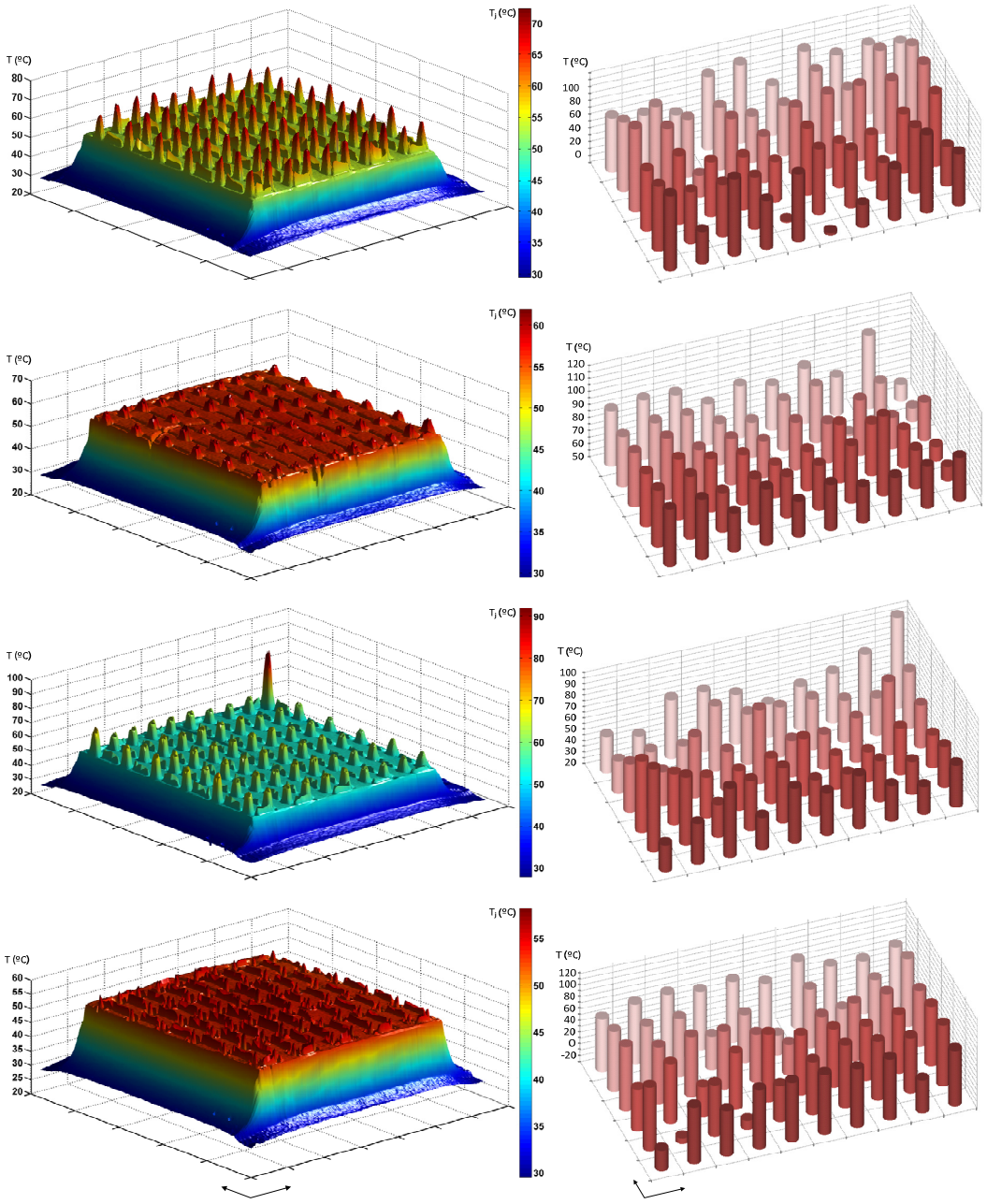

Fig. 2.41. Left: lamp temperature surface plot obtained by IR thermography. Right: junction temperature bar plot obtained by forward voltage measurement of each LED. First on top: Golden Dragon Plus. Second on top: Luxeon K2 with TFFC. Third: Z-Power P4. Bottom: XLamp XR-E.

the board are known. As the forward voltage of each LED and the board temperature have already been measured, the forward current is known, and the thermal resistance is provided by the manufacturer and gathered in Table II.I, the junction temperature can be estimated. This is shown in Fig. 2.42. It can be noticed from Fig. 2.42 that the junction temperature deviation within the same array is almost negligible. However, the junction temperature estimated by this method also shows misleading results, as the estimated values are always lower than those calculated by the fitting polynomials. It has to be taken into account that the thermal resistance introduced by the thermal bond is not considered as it can usually be considered negligible provided that its value is much lower than the junction-to-case thermal resistance. As a result of this, it can be seen that the values for junction-to-case thermal resistance obtained from the

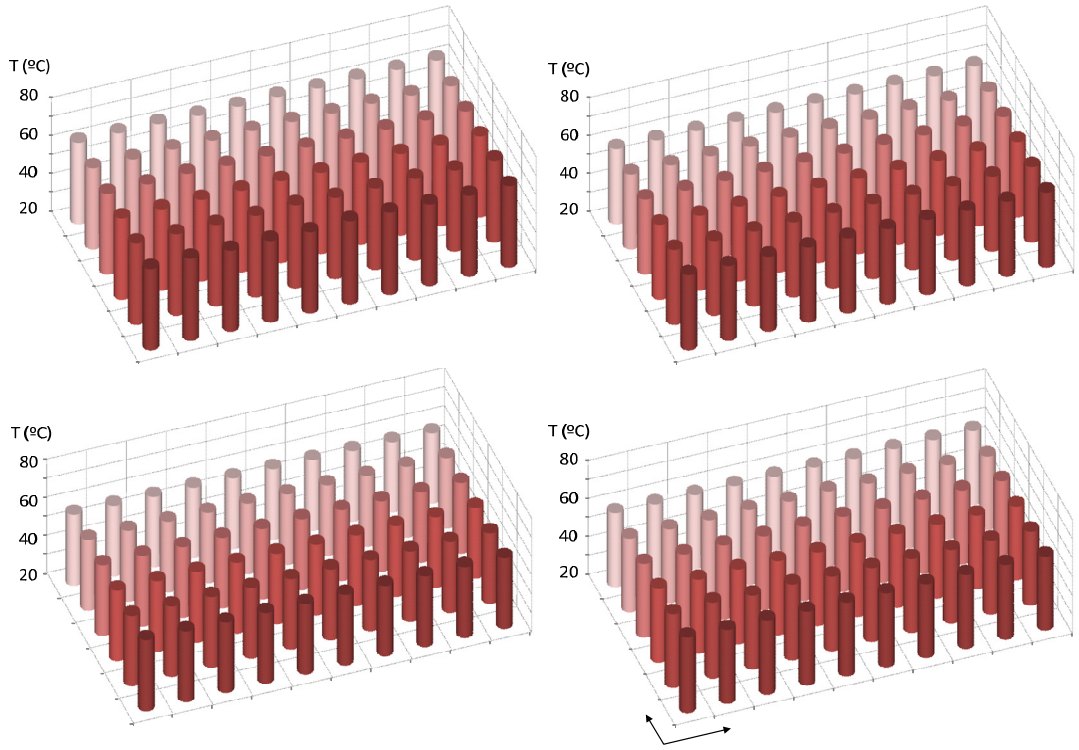

Fig. 2.42. Junction temperature bar plot calculated from (2.10) for each LED. Top left: Golden Dragon Plus. Top right: Luxeon K2 with TFFC. Bottom left: Z-Power P4. Bottom right: XLamp XR-E.

experimental results, neglecting the bond thermal resistance, and gathered in Table II.XI greatly differ from those provided by the manufacturer and gathered in Table II.I, especially in the case of the Golden Dragon Plus and Luxeon K2, by excess, and the XLamp XR-E, of which thermal resistance was calculated lower than the value provided by the manufacturer. Finally, the Z-Power P4 shows a similar value, disregarding the effects of the partially-detached LED.

As can be seen from the information obtained from Fig. 2.41 and Fig. 2.42 and comparing these results with the results gathered in Table II.XI, some conclusions can be highlighted:

a) First, an even temperature distribution throughout the heatsink surface can be confirmed for the four LED lamps.

b) Second, it can be seen that the case temperature is smoothly distributed across each lamp, confirming a variable but delimited thermal resistance. Moreover, the difference in case temperature among LEDs does not necessarily imply a higher junction temperature. Thus, if comparing the surface plots on the left of Fig. 2.41 with their corresponding junction temperature, it can be seen that, although the Luxeon K2 with TFFC and the XLamp XR-E devices feature a case temperature much closer to the heatsink temperature than the Golden Dragon Plus and the Z-Power P4 devices, the estimated thermal resistance for the Luxeon K2 is the highest, whereas the XLamp XR-E features the lowest. In addition, it can be seen that the case temperature is close to the estimated junction temperature in all the lamps except for the Luxeon K2 with TFFC, which shows a thermal gap around 30 ºC. This implies that a good knowledge about the package is needed in order to estimate the junction temperature from the case temperature. Nevertheless, the smooth distribution of case temperature throughout the

LED lamps validates the supposition of a smoothly-distributed junction temperature within the same lamp.

c) Third, from close examination of Fig. 2.41, it can be seen that the junction temperature estimated for each single LED cannot be accurately determined by the fitting polynomials due to the forward voltage variation present even in binned LEDs. Thus, it can be seen from Table II.XI that although the average estimated junction temperature obtained by averaging the single LED temperatures tends to the average value obtained by measuring the ensemble forward voltage, the temperature swing and the standard deviation obtained are around 60 ºC and 10 ºC, respectively, for the best case, corresponding to the binned LEDs, namely Luxeon K2 and Z-Power P4, which feature a lower forward voltage swing between LEDs. It should be remarked the case of unbinned LEDs, especially the XLamp XR-E device, where junction temperatures as low as -20 ºC are estimated, confirming the unsuitability of this method due to the strong single-LED forward voltage deviation from the average value unless tight binning is assured.

d) Finally, from the experimental results and Fig. 2.42, it can be seen that estimation of the junction temperature by measuring the board temperature and calculating the former by (2.10) could lead to unacceptably inaccurate temperature values unless the actual package and thermal-bond thermal resistance values are known, or at least, can be estimated.

Finally, the experimental test show a good agreement between the forward voltage sample standard deviation obtained from the experimental tests and the theoretical values gathered in Table II.III and Table II.IV for the unbinned and binned devices. In addition, a 95% confidence interval containing the theoretical average value, μ, can be estimated as:

$$\xi \pm 1.96\frac{S_V}{\sqrt{n}} \tag{2.21}$$

where ξ stands for the sample average value, $V_D\,(total)$. The average value at the test junction temperature will be contained in the confidence interval at a 95% probability. The lower and upper confidence interval limits (LCI and UCI), as well as the average value and the sample standard deviation, are shown in Table II.XII. The data corresponding to the partially-detached LED are discarded.

TABLE II.XII
95% CONFIDENCE INTERVAL AT THE TEST JUNCTION TEMPERATURE

LED	*LCI* (V)	*Average* (V)	*UCL* (V)	S_V (V)
Golden Dragon Plus	3.058	3.076	3.093	0.069
Luxeon K2 TFFC	3.164	3.174	3.184	0.040
Z-Power P4	3.014	3.024	3.034	0.039
XLamp XR-E	2.961	2.986	3.012	0.101

For instance, in the case of the Golden Dragon Plus operating at around 75ºC the datasheet gives a forward voltage drop around 150 mV from a 3.2 V nominal voltage, which is kept within the confidence level calculated. It can also be remarked that for this sample size, the sample standard deviation values for the four DUTs are lower than those corresponding to the population

2.9.3.2. Comparison between single-emitter and average values

In order to compare the single-emitter test with the tests comprising 60-series LEDs, which have more statistical relevance, the forward voltage coefficient results obtained from the single-emitter and the 60-LEDs lamps tests are recalled in Table II.XIII. Thus, the experimental typical values, *k'*, and the manufacturer data, *k*, can be compared. The data corresponding to the 60-LEDs lamps are normalised to a single averaged emitter.

As can be seen, the temperature coefficient of forward voltage in the single-emitter tests are quite close to the average values obtained from the 60-LEDs lamp tests, especially fitted in the case of the Luxeon K2, which is binned, and the Golden Dragon Plus, the Z-Power P4 and XLamp XR-E featuring a higher deviation.

TABLE II.XIII
EXPERIMENTAL TEMPERATURE COEFFICIENT OF FORWARD VOLTAGE (LINEAR FIT, SINGLE-EMITTER, NORMALISED LED, MANUFACTURER DATA)

LED	*k'* (mV/ºC)	*Fitting Interval*	r^2	*k* (mV/ºC)
Golden Dragon Plus (single)	-2.65	@ 350mA -10ºC ≤ Tj ≤ 120 ºC	0.9964	Chart [2.17]
Golden Dragon Plus (normalised)	-2.61		0.9967	
Luxeon K2 TFFC (single)	-4.30	@1000mA -10ºC ≤ Tj ≤ 120 ºC	0.9976	-2.8
Luxeon K2 TFFC (normalised)	-4.28		0.9983	
Z-Power P4 (single)	-3.41	@350mA 25ºC ≤ Tj ≤ 100 C	0.9877	Chart [2.19]
Z-Power P4 (normalised)	-3.11		0.9898	
XLamp XR-E (single)	-3.40	@350mA 25ºC ≤ Tj ≤ 100 C	0.9749	-4
XLamp XR-E (normalised)	-3.06		0.9871	

With regard to the V_D-T_j curves and fitting polynomials, the experimental results obtained from the single-emitter tests, the theoretical V_D values obtained from the *I-V* characterisation, the polynomial fit obtained from the single-emitter test, and the normalised polynomial fit obtained from the 60-LEDs lamp tests, are depicted in Fig. 2.43 for 350 and 700 mA. Only the polynomials corresponding to the 1 kHz test at 350 and 700 mA will be considered. As can be seen, the values that have been obtained from the single-emitter test and the 60-LEDs lamps tests after normalisation are very close to each other and within the standard deviation values. The fitting polynomial parameters are gathered in Table A.XLI for the single-emitter test and the normalised LED obtained from the 60-LEDs test at 350 and 700 mA operation.

Regarding the theoretically-calculated dynamic resistance and the experimental values obtained, as seen in Fig. 2.16 and Fig. 2.21 respectively and recalled in Fig. 2.44 for comparative purposes, it can be concluded that the experimental *I-V* fit allows the determination of the dynamic resistance with an acceptable accuracy, except for the Golden Dragon Plus, which showed an unpredicted behaviour in the small-signal analysis. Thus, in the case of the Luxeon K2, the dynamic resistance is determined with an error of approximately 5 Ω for 60 series LEDs, less than 100 mΩ for a single emitter at 350 mA. This accounts for less than a 10% error. In the case of the Z-Power P4 and XLamp XR-E, the theoretical calculation of the dynamic resistance is much more accurate, especially in the case of the Z-Power P4, very close to the experimental results at all currents, but especially at 350 mA. Nevertheless, in the case of the Golden Dragon Plus device, it could be assumed that the average value of the theoretically

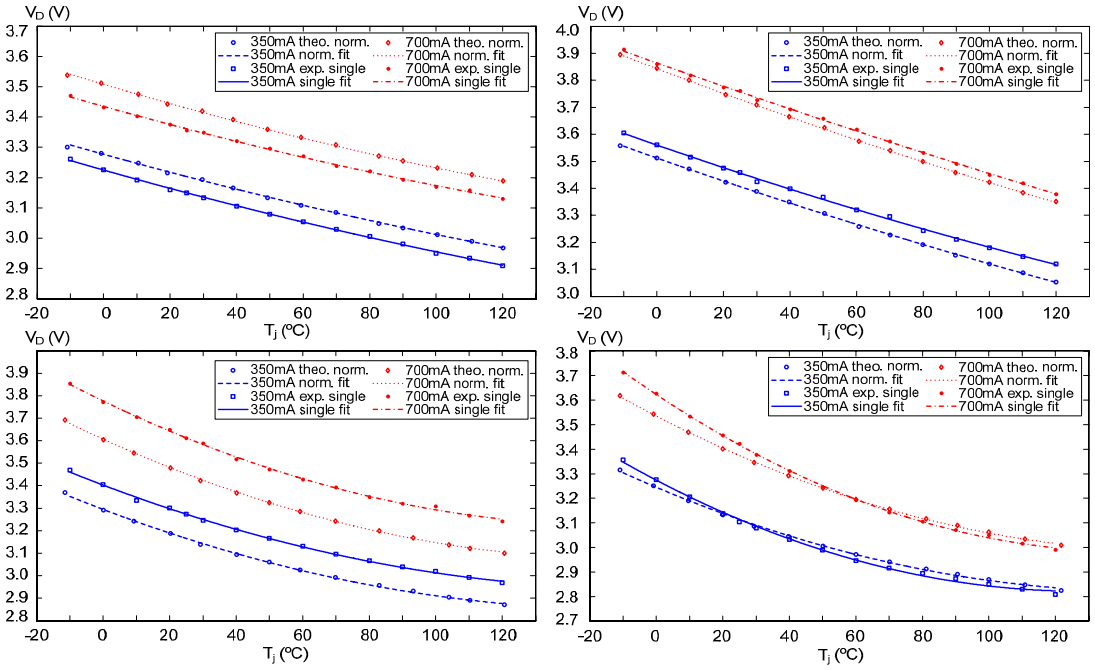

Fig. 2.43. V_D-T_j curves at 350 and 700 mA obtained from the single-emitter experimental test, single-emitter polynomial fits, 60-LEDs lamps *I-V* characterisation and normalised polynomial fits. Upper left: Golden Dragon Plus; upper right: Luxeon K2 with TFFC; lower left: Z-Power P4; lower right: XLamp XR-E.

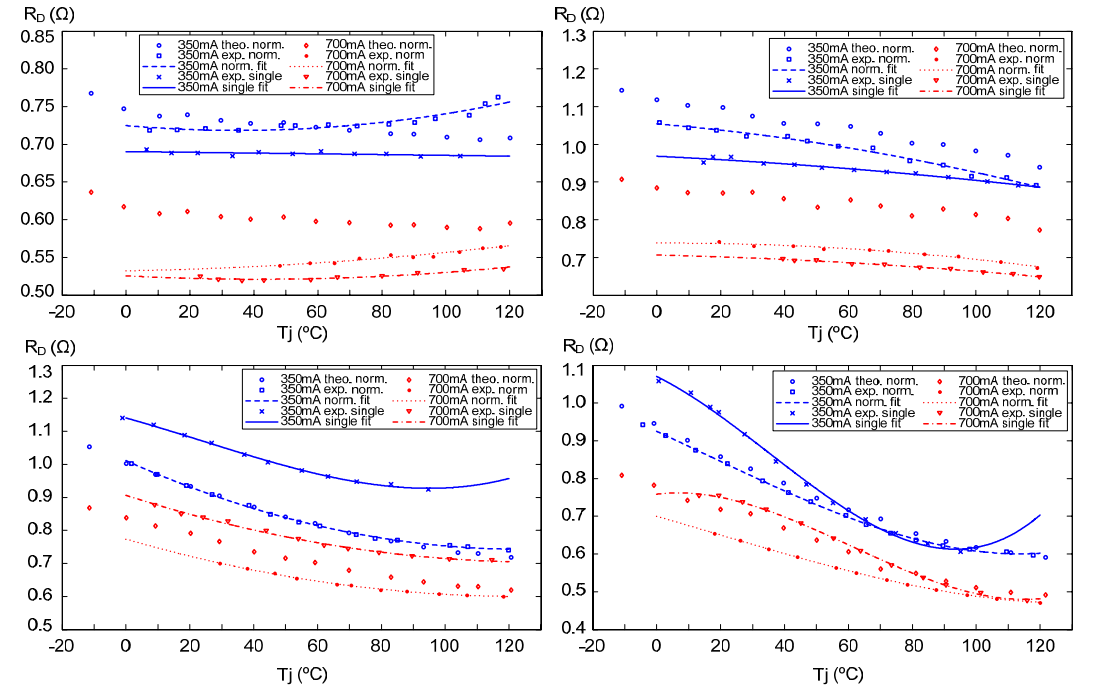

Fig. 2.44. R_D-T_j curves at 350 and 700 mA obtained from the single-emitter experimental test, single-emitter polynomial fits, 60-LEDs lamps *I-V* characterisation, 60-LEDs experimental test, and normalised polynomial fits. Upper left: Golden Dragon Plus; upper right: Luxeon K2 with TFFC; lower left: Z-Power P4; lower right: XLamp XR-E.

calculated dynamic resistance could be a fair estimator of the experimentally-determined average dynamic resistance at 350 mA for junction temperatures below 100ºC. Finally, it should

be remarked that in the case of the XLamp XR-E, a more quadratic behaviour was found at the single-emitter test, although the trend is similar.

Finally, regarding the experimentally-determined dynamic resistance in the single-emitter and the 60-LEDs lamps tests performed, the fitting polynomials obtained for the single emitter and a normalised LED at 350 and 700 mA are shown in Table A.XLII in the Appendix A.

As can be seen, the fitting polynomials show a high deviation in parameters from the single-emitter and the 60-LEDs tests. This can be attributed to experimental deviations in the single-emitter tests which are cancelled in the 60-LEDs tests. This could be the reason why the correlation coefficient of the normalised polynomials is higher than that of a single-emitter test.

Finally, with the experimental procedures described in this paper, the actual linear model as

$$V_D]_{T_j} = V_\gamma]_{T_j} + R_D]_{T_j} I_D \tag{2.22}$$

can be obtained for a given device in a wide range of operating junction temperatures, T_j, where V_D, V_γ, and R_D are the forward voltage, the threshold voltage, and the dynamic resistance respectively, under a given forward current, I_D. This linear model can be used in order to model a whole lighting fixture –LED driver together with LED lamp– dynamically for a wide range of operating ambient temperatures. This can be done by setting the expected limit values of forward voltage, V_D, and dynamic resistance, R_D. Table II.XIV shows the average parameters of the linear model at a junction temperature of 25 ºC at 350 mA for the four samples under test, as well as the result obtained from the single-emitter test.

TABLE II.XIV
EXPERIMENTAL LINEAR MODEL AT 350MA, 25 ºC

LED	V_γ (V)	R_D (Ω)
Golden Dragon Plus (single)	3.15	0.69
Golden Dragon Plus (avg)	3.20	0.72
Luxeon K2 with TFFC (single)	3.46	0.96
Luxeon K2 with TFFC (avg)	3.41	1.03
Z-Power P4 (single)	3.26	1.07
Z-Power P4 (avg)	3.17	0.91
XLamp XR-E (single)	3.11	0.95
XLamp XR-E (avg)	3.11	0.83

2.9.4. Implications of the dynamic resistance shift

Since the dynamic resistance has been proven to be temperature-dependent, a sharp change in the operation temperature, which could even compromise the operation of an LED driver, may be predicted and accounted for. This issue could be critical in lamps with several LEDs in series, since not only the DC operation point but also the poles of the transfer function are affected by a shift in the dynamic resistance [2.9]. In addition, the low-frequency AC ripple would likely be increased out of the specifications with certain output capacitor designs, even leading to unnoticeable but biologically affecting flickering [2.49].

a) Considerations over the output current ripple

As an example, a single-stage current-controlled discontinuous conduction mode (DCM) flyback LED driver featuring power factor correction (PFC) could be considered running a 60-series XLamp XR-E LED lamp at 350 mA, such as in Fig. 2.45. In this case, a junction

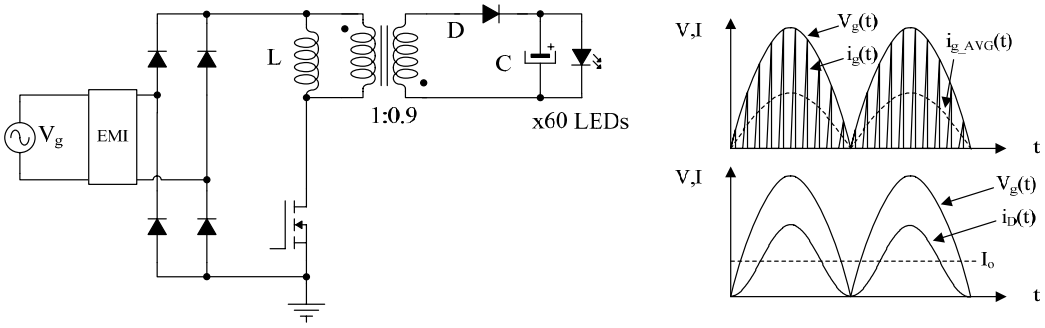

Fig. 2.45. Typical PFC DCM flyback LED driver (left) and its ideal main waveforms (right).

temperature rise from ambient temperature -i.e. 25 ºC, to a steady state temperature of 100 ºC on this lamp would imply a shift in the dynamic resistance from 48.5 Ω down to approximately 36 Ω, considering the fitting polynomials calculated for a 30% low-frequency ripple. In other words, the final dynamic resistance would be the 67% of the initial value.

As it is widely known, the output capacitor has to be sized in order to assure an admissible low-frequency output-current ripple. The averaged current through the output diode, D in Fig. 2.45, of an off-line DCM flyback converter can be expressed as [2.50]:

$$i_D(t) = \frac{V_g^2 d^2}{LfV_o} sin^2(\omega_L t) \tag{2.23}$$

V_g being the AC supply rms voltage, d the duty cycle, f the switching frequency, V_o the output voltage, L the inductance of the flyback primary inductor, and ω_L, the line angular frequency. This expression is obtained from the processing of power from the rectified line voltage, being characterised by a DC level and an AC component at twice the line frequency. The duty cycle is considered constant to feature PFC with no harmonics in the input current. This expression can be simplified by substituting the squared sine by its trigonometric equality. Thus:

$$i_D(t) = \frac{V_g^2 d^2}{2LfV_o} - \frac{{V_g}^2 d^2}{2LfV_o} cos\, 2\omega_L t \tag{2.24}$$

The first term stands for the DC output current, I_o, whereas the second term stands for the double-line-frequency AC component, $i_{ac}(t)$, which will be filtered by the output capacitor, C. The main waveforms are depicted in Fig. 2.45, where the line voltage, $V_g(t)$, the average input current, $i_{g\_AVG}(t)$, the actual input current, $i_g(t)$, the output diode current, $i_D(t)$, and the output average current, I_o, are highlighted. The averaged output equivalent circuit of the DCM flyback PFC is also sketched in Fig. 2.46. This equivalent circuit can be divided into two equivalent subcircuits corresponding to the DC current level, namely I_o, and the AC component, $i_{ac}(t)$. The AC component through the output diode is the sum of the AC current through the output capacitor, $i_c(t)$, and the LED load, $i_o(t)$:

$$i_{ac}(t) = i_C(t) + i_o(t) \tag{2.25}$$

The minimum capacitor for a given output-current ripple can be obtained by accounting for the AC components and using phasor calculus. The AC component through the output diode, $\bar{I}_{ac}$, is the sum of the AC current through the output capacitor, $\bar{I}_C$, and the LED load, $\bar{I}_o$:

$$\bar{I}_{ac} = \bar{I}_C + \bar{I}_o \tag{2.26}$$

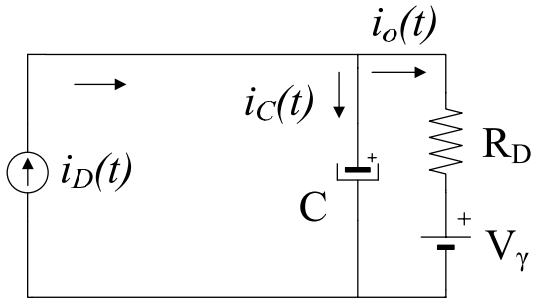

Fig. 2.46. Averaged output equivalent circuit of the DCM flyback PFC.

First, a ripple factor relating the output-current ac-component amplitude to the DC component can be defined as:

$$\delta = \frac{\|\bar{I}_o\|}{I_o} \tag{2.27}$$

Second, considering that the output voltage will be determined by the product of the AC output current and the parallel impedance, Z_o, composed of the output capacitor and the dynamic resistance of the LED load at twice the line frequency, and as it will match the product of the dynamic resistance and the AC output current, the following equality is achieved:

$$Z_o\|\bar{I}_{ac}\|\angle\phi_{ac} = R_D\|\bar{I}_o\|\angle\phi_o \tag{2.28}$$

Where ϕ_{ac} and ϕ_o stand for the diode-current AC component and the output-current AC component phase shifts, respectively. In addition, the output voltage, $\|\bar{U}_o\|$, can also be expressed as:

$$\|\bar{U}_o\| = R_D\|\bar{I}_o\|\angle\phi_o \tag{2.29}$$

As it will match the product of the dynamic resistance and the AC output current, by combining (2.28) and (2.29), and solving for the output current the following equality is achieved:

$$\|\bar{I}_o\|\angle\phi_o = \frac{Z_o\|\bar{I}_{ac}\|\angle\phi_{ac}}{R_D} \tag{2.30}$$

By using phasor calculus, the phase angle between the currents and the complex impedances can be ignored in order to determine the minimum output capacitor for a given ripple factor, considering only the modulus. Since the purpose of this Section is to check the output-current ripple variation due to the thermal effects on LED lamps, and provided that the equivalent series resistance (ESR) of low-ESR capacitors is much lower than the LED lamp dynamic resistance, the capacitor ESR is neglected in this example for the sake of simplicity. Thus, by taking the absolute values in (2.30), substituting (2.27) in (2.30) and rearranging:

$$\delta\frac{{V_g}^2 d^2}{2Lf(V_\gamma + R_D I_D)} = \frac{\dfrac{{V_g}^2 d^2}{2Lf(V_\gamma + R_D I_D)}\dfrac{R_D}{\sqrt{1 + 4{\omega_L}^2 C^2 r_D^2}}}{R_D} \tag{2.31}$$

After re-arranging and solving for the minimum capacitance value, C_{min}, for a given low-frequency output current ripple, the following expression is given by:

$$C_{min} = \sqrt{\frac{1-\delta^2}{4\delta^2 {\omega_L}^2 R_D^2}} \tag{2.32}$$

which, as can be seen, depends on the dynamic resistance of the LED lamp, with decreasing minimum capacitance values for increasing dynamic resistance. This suggests that decreasing dynamic resistances will induce higher output current ripple values. It has to be noted that R_D stands for the dynamic resistance at any given operation point. The calculations can be done at any operation currents, just by setting the proper value for R_D.

b) Considerations over the closed-loop dynamics

With regard to the dynamic behaviour of the DCM Flyback converter, its transfer function can be obtained from the analysis of the DC component of the output equivalent circuit depicted in Fig. 2.46. Provided that low ESR values introduce a high-frequency zero, and this example illustrates the closed-loop operation of a slow-dynamics LED driver, this simplification could be considered accurate enough in order to predict the most significant effects of thermal variation in the LED lamp. Thus:

$$\langle i_D \rangle(t) = \langle i_C \rangle(t) + \langle i_o \rangle(t) \tag{2.33}$$

where the chevron symbol, ⟨ ⟩, stands for the averaged variables. Developing (2.35):

$$\frac{\langle v_g \rangle^2 \langle d \rangle^2}{2Lf\,\langle v_O \rangle} = C\frac{d}{dt}\langle v_O \rangle + \langle i_o \rangle \tag{2.34}$$

Substituting (2.25) in (2.36):

$$\frac{\langle v_g \rangle^2 \langle d \rangle^2}{2Lf\left(V_\gamma + R_D\langle i_O \rangle\right)} = R_D C\frac{d}{dt}\langle i_O \rangle + C\frac{d}{dt}\langle V_\gamma \rangle + \langle i_o \rangle \tag{2.35}$$

Perturbing and linearising:

$$R_D C\frac{d}{dt}\langle \widehat{i_O} \rangle + \langle \widehat{i_O} \rangle = \frac{2V_g^2 d^2}{2LfV_o}\langle \hat{d} \rangle - \frac{V_g^2 d^2 R_D}{2LfV_o^2}\langle \widehat{i_O} \rangle \tag{2.36}$$

Rearranging and taking the Laplace transform, the following transfer function is yielded:

$$G(s) = \frac{i_o(s)}{d(s)} = \frac{2 \cdot \frac{I_o}{dR_D C}}{s + \frac{V_o + I_o R_D}{V_o R_D C}} \tag{2.37}$$

where I_o, d, R_D, C, and V_o are the output current, duty cycle, dynamic resistance, output capacitor and output voltage at the operation point, respectively. As can be seen, the pole and the static gain transfer function depend on the output voltage and the dynamic resistance, both temperature-dependent variables.

The block diagram sketched in Fig. 2.47 will be considered in this example, where *r(s)* is the output current reference, *e(s)* is the error signal, *C(s)* is the controller, *d(s)* is the control

signal applied to the DCM flyback converter, *G(s)*, *H(s)* is the feedback block, and $I_o(s)$ is the output current. Unity feedback is considered for the sake of simplicity.

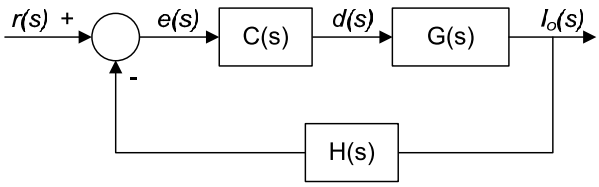

Fig. 2.47. Closed loop block diagram of the proposed illustrative example.

A proportional-integral compensator will be considered in this illustrative example. The transfer function of this compensator is as follows:

$$C(s) = K_{dc}\frac{1+zs}{s} \tag{2.38}$$

where *1/z* is the compensator-zero corresponding angular frequency and K_{dc} is the static gain of the compensator.

c) Illustrative example of the dynamic-resistance shift implications.

This example will show a converter designed for a nominal junction temperature of 25 ºC, featuring a 0.35 duty cycle, 500 µH primary flyback inductor, 49 Ω dynamic resistance, 187 V output voltage, and 180 µF output capacitor for approximately a 30% peak-to-peak output-current ripple target, as calculated from (2.32). The compensator will be designed for a 60 degrees phase margin for the nominal junction temperature in order to achieve a fast transient response and -20dB gain at 100 Hz in order to prevent the 100 Hz low-frequency ripple from affecting the duty cycle and thus, the power factor (PF). With this constraint, the static gain would be K_{dc} = 105.44 V^{-1}, considering a unity-gain PWM modulator, and the zero would be located at 432 rad/s.

Moreover, the case of 0 ºC and 100 ºC of junction temperatures will also be considered in order to analyse the implications of the dynamic resistance shift on the performance of the converter. The open loop Bode diagrams of the DCM flyback converter for the three cases are shown in Fig. 2.48. Considering these temperatures, the actual output voltages will be 194.7 V and 171.9 V for 0º C and 100 ºC respectively, and the dynamic resistance values will be 54 Ω and 36 Ω, for those temperatures, respectively.

As can be seen from Fig. 2.48, the pole of the transfer function would be located at 125 rad/s, and its static gain would be 1.81 A at a junction temperature of 25 ºC. However, if the junction temperature rose up to 100 ºC, the transfer function pole would be moved to 165.6 rad/s, and the static gain would be shifted to 1.93 A, as the output voltage would have dropped to 171.9 V and the dynamic resistance would have been lowered down to 36 Ω. On the other side, if the junction temperature drops down to 0 ºC, the static gain would be 1.78 A, and the pole would be displaced to 112.9 rad/s. This issue might be critical in those designs where the feedback control is designed for only one single operating point, since not only the change over time of the closed loop parameters, but also the change in the thermal operation point could lead to instabilities as the low-frequency poles and the output impedance are affected.

Fig. 2.49 shows the *C(s)G(s)H(s)* loop-gain transfer function with unity feedback for the three junction temperatures considered. As can be noticed, the phase margin is reduced from

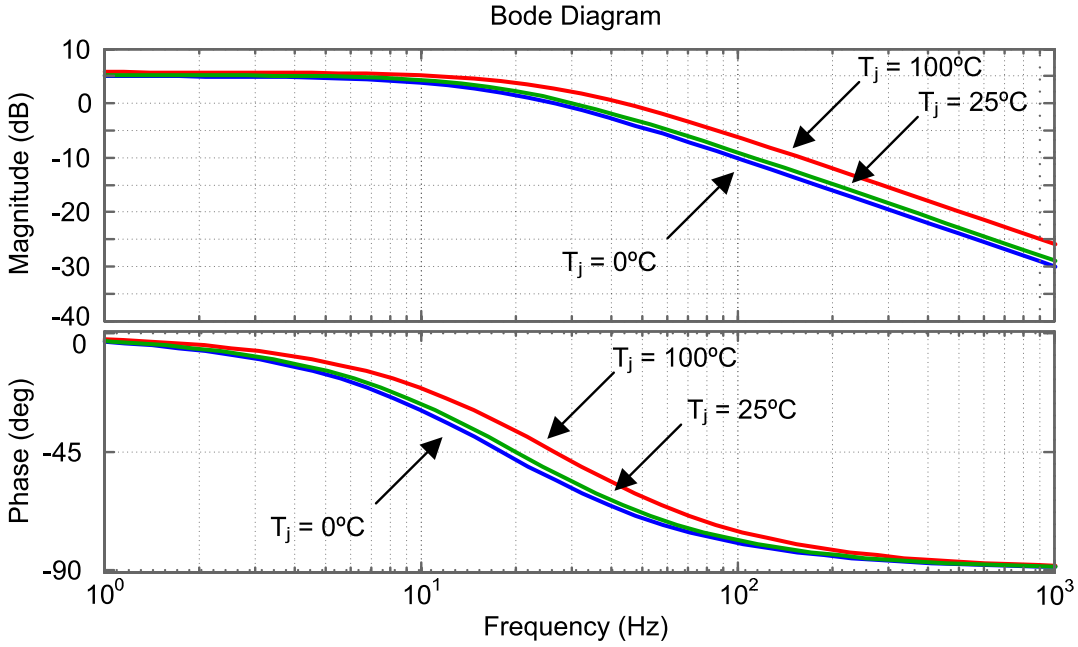

Fig. 2.48. DCM Flyback Bode diagrams for 0, 25 and 100ºC junction temperatures.

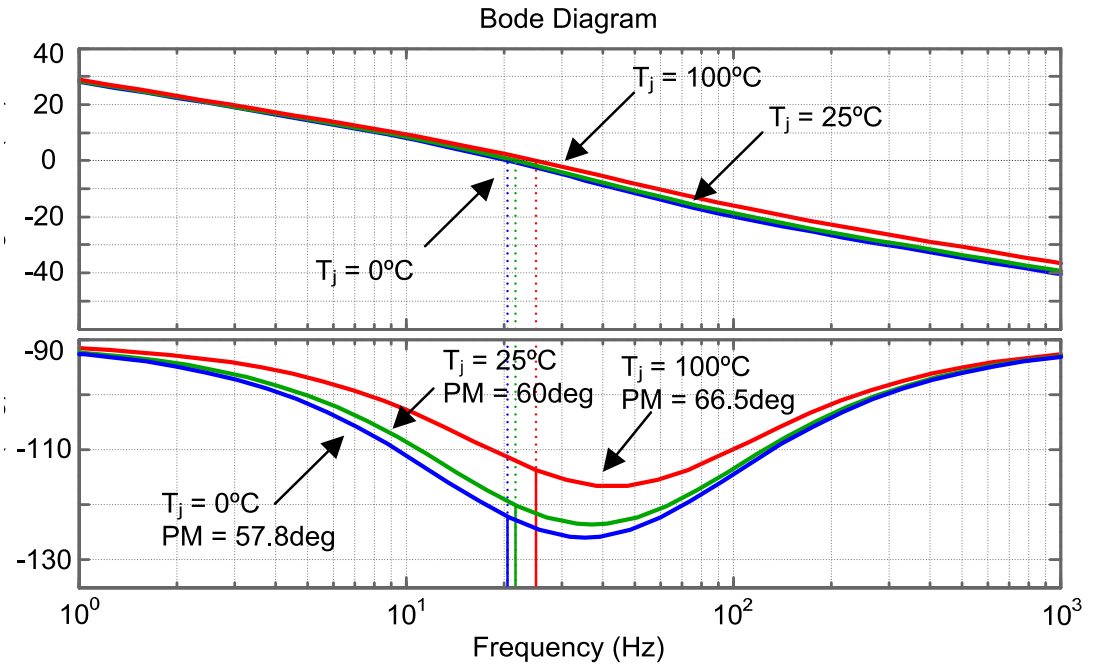

Fig. 2.49. Loop gain Bode diagrams for 0, 25, and 100 ºC junction temperatures.

66.5 degrees at a junction temperature of 100 ºC, down to 57.8 degrees as the temperature decreases to 0 ºC.

In order to check the implication of the phase margin shift due to thermal effects, a closed-loop step response under the three junction temperatures considered will be investigated. The results are shown in Fig. 2.50. As can be seen, as the phase margin is boosted, corresponding to a lower dynamic resistance due to a rise in junction temperature, the closed-loop system becomes less oscillatory and features a lower overshoot, the settling time being also reduced.

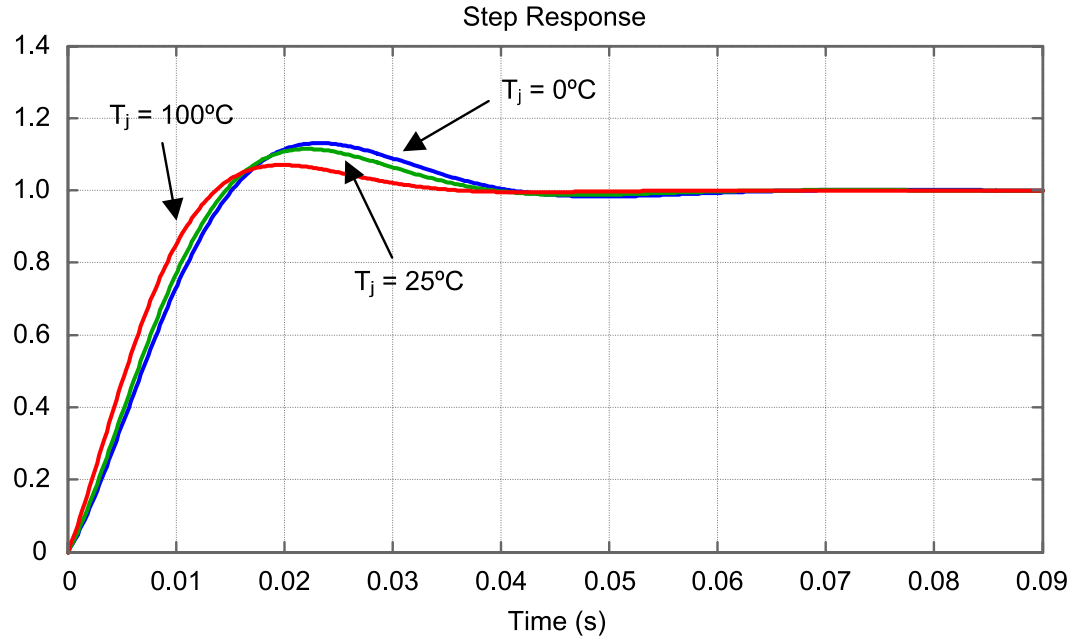

Fig. 2.50. Step responses for 0, 25, and 100 ºC junction temperatures.

On the contrary, as the junction temperature is decreased inducing a higher dynamic resistance value, which corresponds to a lower phase margin, the step response becomes more oscillatory, with higher overshooting and larger settling times.

Regarding the implications of the junction temperature shift on the output current ripple, it has to be noted that the target value was a 35% at a junction temperature of 25 ºC. In this case, rearranging (2.32), the following value for the current ripple is achieved:

$$\delta = \frac{1}{\sqrt{1 + 4\omega_L{}^2 C^2 R_D^2}} \tag{2.39}$$

With a 180 µF output capacitor, the low-frequency output-current peak-to-peak ripple is set at a 36% of the DC value at nominal operation, whereas the ripple is raised up to 48% at a junction temperature of 100 ºC. On the contrary, as the dynamic resistance is increased as long as the junction temperature is decreased, the ripple will be lower at 0 ºC, being a 32% over the DC current.

Fig. 2.51 shows the output current ripple under closed-loop operation at the three junction temperatures. As can be seen from this figure, the peak-to-peak output-current ripple is set to approximately 130 mA at the nominal junction temperature, which represents around a 37% peak-to-peak current ripple. However, the output-current ripple swings from around 120 mA at 0 ºC to more than 170 mA at 100 ºC, corresponding to a 34% and a 50% over the DC value, respectively, thus confirming the theoretical calculations and discussions.

As can be seen from this example, the dynamic resistance shift caused by the junction temperature change induces two effects on the closed-loop operation of an LED driver. On the one hand, decreasing dynamic resistances as a consequence of a junction temperature change would lead to increasing low-frequency output-current ripples. On the other hand, increasing dynamic resistances as a consequence of a junction temperature shift would lead to a more underdamped response.

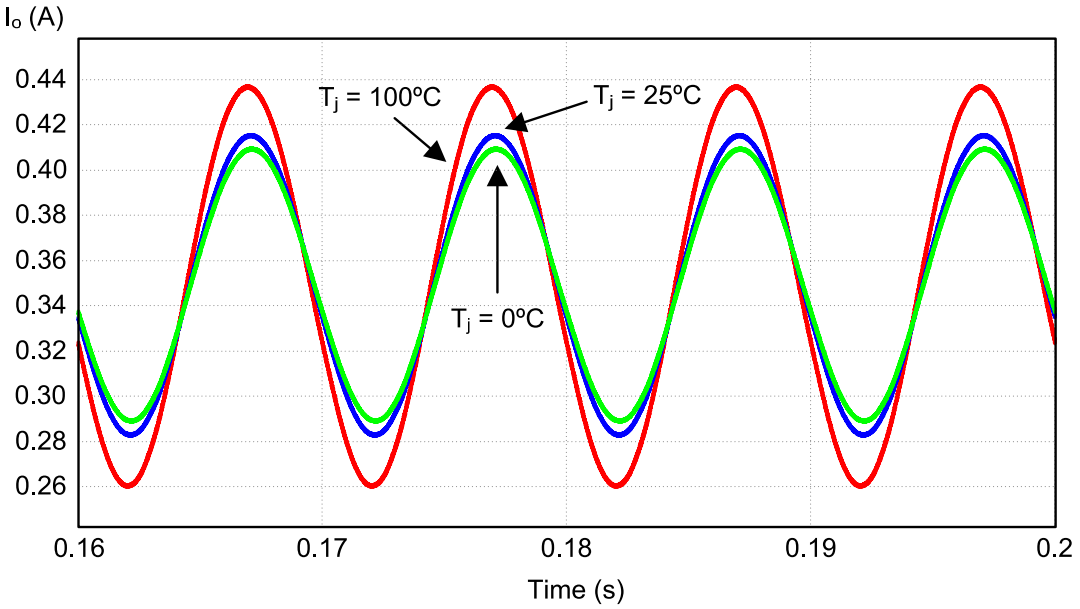

Fig. 2.51. Closed-loop output-current ripple simulation for 0, 25, and 100 ºC junction temperatures.

2.10. Conclusions

The effects of the junction temperature on the electrical behaviour of LEDs have been tested in this Chapter. Firstly, four commercial GaN-based, phosphor-converted white LEDs from four of the main manufacturers have been chosen for the experimental work. In order to determine the influence of parasitic elements on the *I-V* curve of HB-LEDs, the effect of the series and parallel resistances on a *p-n* junction has been theoretically determined. The theoretical studies can conclude that, for commercial LEDs, only the series resistance can be considered without a noticeable lack of accuracy on the fits. Prior to the experimental tests, the statistical properties of the Gaussian distribution assumed to LEDs properties have been studied. It has been concluded that for a sample size of 60 LEDs connected in series, the experimental results obtained are representative and have statistical relevance.

Afterwards, the LEDs have been characterised using the voltage-temperature method in order to determine the *I-V* curve corresponding to each junction temperature, so this parameter could be accurately estimated in subsequent tests. Two different tests have been carried out: first, the *I-V* curve single emitters was characterised in order to obtain the V_D-T_j curve. Moreover, 60-series-LEDs lamps built with the four LEDs considered were characterised in order to obtain the *I-V* curve parameters such as the reverse saturation current, ideality factor, and series resistance, and the dynamic resistance for each junction temperature and current operation. With regard to the *I-V* curve parameters, reasonable results were obtained, as these parameters feature a decrease with rising temperature. However, the reverse saturation current showed an erratic dependence on temperature, likely caused by the lack of measuring points at the lowest current levels. In addition, the dynamic resistance was theoretically determined for the 60-LEDs lamps.

Secondly, the experimental results have shown that all the devices tested featured a quadratic dependency of the forward voltage drop as opposed to the junction temperature for a given injected current. However, two different behaviours were checked: whereas the Golden Dragon Plus and the Luxeon K2 with TFFC performed more linearly, the Z-Power P4 and the

XLamp XR-E featured a more pronounced quadratic dependency. These results refute the linear dependency generally assumed for a wide temperature range. Nevertheless, the experimental results agree with the non-linear forward voltage-junction temperature relation provided by some manufacturers and reported by some authors. The V_D-T_j curves were fitted in order to determine the junction temperature in subsequent experiments.

Then, the influence of the junction temperature on the LEDs electrical behaviour has been tested and evaluated. In this way, a small-signal analysis has been performed at three injection current levels for the single emitters, and two injection current levels for the 60-LEDs lamps and variable junction temperature in order to determine the junction temperature and the dynamic resistance. The experimental results confirm that the dynamic resistance does feature a shift due to changes in the junction temperature. However, the change in the dynamic resistance has shown different trends, as the dynamic resistance underwent a drop as the junction temperature was raised only in three of the LEDs tested. In the remaining device the actual change in the dynamic resistance did happen as opposed, since this parameter was increased as the junction temperature rose up at the highest test currents, whereas remained fairly constant at the lowest test current for the whole temperature range. These results were theoretically predicted with fairly good agreement in either test: single-emitter and 60-LEDs lamps. However, the trend showed by the Golden Dragon Plus device was opposed as predicted. In addition, a small-signal, low-frequency test was performed with the 60-LEDs lamps, confirming that such low-frequency disturbances induce a temperature shift in the *p-n* junction, leading to a variation in dynamic resistance compared to the high-frequency test and introducing a reactive-like small-signal behaviour. Moreover, it has been checked that the dynamic resistance also varies with the current ripple for the 350 mA current level. The dynamic resistance curves have been fitted in order to determine the dynamic resistance for a given operation current and junction temperature, taking into account the current ripple at low frequency.

With the experimental procedures described in this chapter, a linear model can be obtained for a wide range of operating junction temperatures, providing the designer with the actual linear model for each injection current at each junction temperature, so either the power stage or the feedback loop could be optimised for a wide range of operation conditions of the final lighting product or fixture

Finally, the experimental results achieved show that depending on the commercial device and the LED lamp design, a sharp change in the operation temperature could even compromise the operation of both the LED fixture and the LED driver due to a large shift in the dynamic resistance of several series-connected LEDs. This may cause a decrease in the phase margin of the system that could yield to a more underdamped response of the output current as the junction temperature decreases, as well as an increase in the output current ripple, showing that these effects must be taken into account and a trade-off between both effects should be achieved, especially when the lighting fixture satisfactory performance under a wide range of operation temperatures is required.

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Chapter 3

High Power Factor Off-line Power Supplies for LED Lighting

This chapter deals with the supply from the AC mains. Thus, the first important concept in AC power supplies is presented: power factor correction. The IEC 61000-3-2:2005 Class C regulations, which apply to any kind on lighting equipment but incandescent lamps with integrated dimmers will be briefly covered.

Second, the several techniques for power factor correction (PFC) will be summarised, making a classification between passive and active techniques. With regard to active techniques, the two possible divisions are listed: either sinusoidal input current or non-sinusoidal input current PFPs.

Since passive solutions are not interesting for high-power applications, universal-range operation, or high-performance lighting equipment, active solutions will be taken into account. Thus, the different operation modes that can be found on literature will be explained: continuous conduction mode (CCM), discontinuous conduction mode (DCM) or boundary conduction mode (BCM). In addition, some considerations regarding the control loop will be included for each conduction mode.

After that, the different architectures of active solutions that can be found in the literature will be listed: one-stage, two-stage, three-stage or single-stage integrated converters. Regarding the latter, the integration process will be briefly covered.

Finally, the behaviour of sinusoidal input-current and non-sinusoidal input-current PFC converters will be studied, comparing both solutions for performing PFC.

3.1. Introduction

As has already been introduced in Chapter 1, HB-LEDs, or Power LEDs, are to be supplied at constant current in order to assure an efficient, flexible and high-performance operation of the LED fixture. This is generally achieved by the use of electronic drivers [3.1], although passive LED drivers have been proposed, such as in [3.2], which consume energy from the AC line and supply the LED lamp with DC current. Nevertheless, there are exceptions, such as the Acriche LED by Seoul Semiconductor described in Chapter 1.

In addition, there are several features that are highly desirable in outdoor lighting, street lighting, or indoor lighting applications due to the enhancement in energy efficiency and flexibility they introduce, such as universal input-voltage supply or dimming operation, so the LED fixture can properly operate worldwide under several operation conditions while providing an accurate current control [3.3]. However, these features are only achieved by the use of electronic drivers.

Since these drivers are supplied from the AC mains, the amount of line harmonic distortion and displacement between AC mains voltage and current shall be kept as low as possible in order to maximise the deliverable energy. In addition, the amount of non-linear loads has been increasing considerably in the few past decades. Thus, the regulations have been being tightened since the IEC 555-2, published in 1982. Nowadays, lighting appliances must comply with European IEC 61000-3-2:2005 Class C equipment mandatory regulations –or equivalent, such as the Japanese JIS 61000-3-2, which refer to lighting systems, in terms of harmonic content and power factor (PF) [3.4]. In addition, other programs such as the Energy Star developed by the US Department of Energy and the US Environmental Protection Agency require at least 0.9 and 0.7 power factor for commercial and residential applications, respectively [3.5].

This chapter compiles a brief survey on all the solutions generally used for supplying solid-state lighting fixtures from the AC mains prior to introducing the topology that will be proposed in this work.

3.2. Definition of power factor (PF)

IEC 61000-3-2 regulation limits the harmonic content rather than the power factor. However, as the third harmonic is defined by the power factor, and the Energy Star program requires a minimum value, this parameter is to be properly defined.

Power factor is the ratio of real power, P, to apparent power, S [3.6]:

$$PF = \frac{P(W)}{S(VA)} = \frac{P_{avg}}{V_{rms}I_{rms}} = \frac{\frac{1}{T}\int_0^T v(t)i(t)dt}{\sqrt{\frac{1}{T}\int_0^T v(t)^2dt}\sqrt{\frac{1}{T}\int_0^T i(t)^2dt}} \tag{3.1}$$

where P_{avg} refers to the real power averaged over a period T, V_{rms} is the rms value of the input voltage, $v(t)$, and I_{rms} is the rms value of the input current, $i(t)$. The classical definition of power factor, applicable to pure sinusoidal waveforms accounts for the phase shift between voltage and current, ϕ. Thus [3.7]:

$$PF = \cos\phi \tag{3.2}$$

This definition is also referred to as the displacement factor (*DispF*). However, as many electronic power supplies feature non purely-sinusoidal input current waveforms, the PF may be

reduced even though voltage and current are in phase, but some amount of distortion is present. In this case, a distortion factor (DF) can be defined [3.6]:

$$DF = \frac{I_1}{I_{rms}} \tag{3.3}$$

where I_1 stands for the fundamental harmonic of current. Assuming that the line voltage is a pure sine wave, which is reasonable in AC power supplies with power factor correction, the DF can be expressed as a function of the input current total harmonic distortion, THD_I [3.6], [3.7]:

$$DF = \frac{1}{\sqrt{1 + THD_I^2}} \tag{3.4}$$

The total input current harmonic distortion can be defined as follows, according to the IEC61000-3-2 regulation [3.4]:

$$THD_I = \frac{\sqrt{\sum_{n=2}^{40} I_n^2}}{I_1} \tag{3.5}$$

where I_1 and I_n stand for the first- and nth-harmonic amplitude, respectively.

Therefore, an extended definition for *PF*, accounting for both the phase shift and the harmonic distortion present in the input current can be set as:

$$PF = \frac{\cos\phi}{\sqrt{1 + THD_I^2}} \tag{3.6}$$

where $cos\phi$ applies to the line-current first harmonic[3.6]. As can be seen from (3.6) and provided that there is no phase shift, high power factor and THD can simultaneously coexist.

3.3. IEC 61000-3-2:2005 regulations

The IEC 61000-3-2:2005, or its equivalent EN61000-3-2:2006, refers to the electromagnetic compatibility and is aimed at setting levels for harmonic current injection back to the AC mains supply, applied to all electrical and electronic equipment with an input current up to 16 A per phase [3.4], [3.8]. This standard distinguishes four classes depending on the application:

- Class A: balanced three-phase equipment; household appliances excluding equipment identified as Class D; tools, excluding portable tools; dimmers for incandescent lamps; audio equipment; and all other equipment, except those stated in one on the other following classes.
- Class B: portable tools; except professional arc welding equipment.
- Class C: lighting equipment.
- Class D: PCs, PC monitors, radio or TV receivers with input power lower than 600 W.

Since lighting equipment is classified as Class C, this class limits will be those to take into account and, therefore, will be covered in this section. Class C limits are set to two levels depending on the input power, greater than 25 W or smaller or equal than 25 W.

3.3.1. Input power greater than 25 W

Class C for input power greater than 25 W establishes relative limits that are given as a percentage of the fundamental harmonic amplitude, as shown in Table I, second column. However, there are two exceptions applying to incandescent and discharge lamps with integrated dimmers.

3.3.2. Input power smaller or equal than 25 W

Class C for input power smaller or equal than 25 W establishes two conditions: either the harmonic current limits corresponding to Class D and expressed as maximum admissible current per watt, as gathered in Table I, third column, or a given waveform defined by a third and fifth harmonic amplitudes that shall not exceed 86% and 61% of the fundamental current, besides other considerations about the waveform shape [3.4].

TABLE III.I: LIMITS FOR CLASS C EQUIPMENT

Harmonic order **n**	**Maximum permissible harmonic current expressed as a percentage of the input current at the fundamental frequency (P > 25 W)** **%**	**Maximum permissible harmonic current per watt** **mA/W**
2	2	-
3	30·λ*	3.4
5	10	1.9
7	7	1.0
9	5	0.5
11	3	0.35
$13 \leq n \leq 39$ (odd harmonics only)		3.85/n

* λ is the circuit power factor

3.4. Power factor correction (PFC) techniques

Power factor correction and harmonic reduction can be performed by several techniques [3.8] achieving sinusoidal input current or just limiting the input current harmonic content [3.9]. The most commonly employed ones are either passive or active solutions, the latter known as power factor pre-regulators (PFP) or power factor correctors (PFC) [3.9]. A brief survey is listed as follows.

3.4.1. Passive techniques

Passive PFC techniques employ passive and/or reactive elements such as line-filters implemented by inductors, resistors and/or capacitors cascaded to the input rectifier.

3.4.1.1. Passive filters

PFC by means of passive filters, also referred to as passive PFC, consists of using passive devices such as inductors, resistors and capacitors together with non-controlled rectifiers, as sketched in Fig. 3.1. It introduces high impedance for the considered input current harmonics, reducing their amplitude and smoothing the input current waveform [3.8]. This solution offers

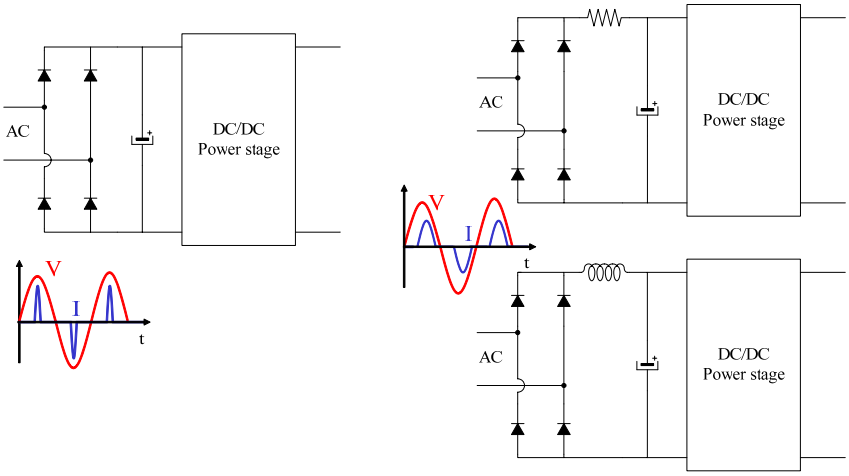

Fig. 3.1. Left, rectifier bridge with capacitive energy storage and corresponding input voltage and current. Right, passive filters for improving PF: RC filter (top) and LC filter (bottom) with the corresponding input voltage and current.

an attractive trade-off between efficiency and cost and does not generate electro-magnetic interferences (EMI). However, due to the high size of the passive devices it is a good solution only for low power levels. In addition, the input current harmonic content is usually very close to the limit and it is difficult to optimise for universal input voltage range [3.9].

3.4.1.2. Valley-fill circuits

A simple, passive solution widely employed for discharge lamps supply that overcomes the disadvantages of passive filters is the use of the valley-fill topology. This solution has the advantages of not requiring control circuitry and is capable of reaching 0.95 PF, although the total harmonic distortion of the input current (THD_I) ranges from more than 25% up to around 40% [3.10], [3.11]. The operation of the valley-fill circuit is aimed to increase the input current conduction time in order to make the input current come closer to a sine wave. The simplest valley-fill topology is composed by two capacitors and three diodes, as shown in Fig. 3.2.

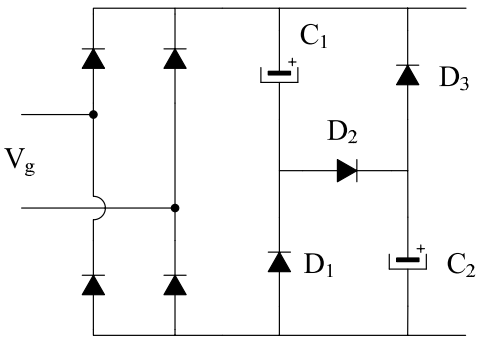

Fig. 3.2. Typical valley-fill topology.

Assuming that valley-fill capacitors feature the same capacitance, they will be charged though diode D_2 up to $V_g/2$ at the line peak value while the load is simultaneously supplied by the AC line. Once the line voltage goes below the valley voltage, i.e. $V_g/2$, the rectifier bridge diodes become reverse-biased and the valley fill capacitors supply the load through diodes D_1 and D_3. This solution has extensively been used for fluorescent lamp ballasts [3.10]-[3.12] and

HID lamps [3.13], although has also been applied for LED drivers, as a passive PFC in passive drivers [3.2], or as a decoupling stage in active LED drivers [3.14] in order to avoid an electrolytic-capacitor based DC-link.

Other passive solutions, such as tuned circuits, are covered in [3.7].

3.4.2. Active techniques

The other way to comply with regulations consists of using high power factor (HPF) DC-DC converters as power factor pre-regulators (PRP), or power factor correctors (PFC), between the rectifier bridge and the load, reaching high efficiency and high power factor. Since these converters draw constant averaged power from the AC line, the input energy is pulsating at twice the line frequency and therefore has to be stored [3.7], [3.7]. Fig. 3.3 sketches the average waveforms of a sinusoidal-input current PFC, highlighting the average input current and voltage as well as the average and DC output power. Nevertheless, these converters are complex, more expensive and generate electromagnetic interferences (EMI). Yet, these topologies are considered the best solution for high power levels and for operating within the universal input voltage range [3.9], [3.14]-[3.18].

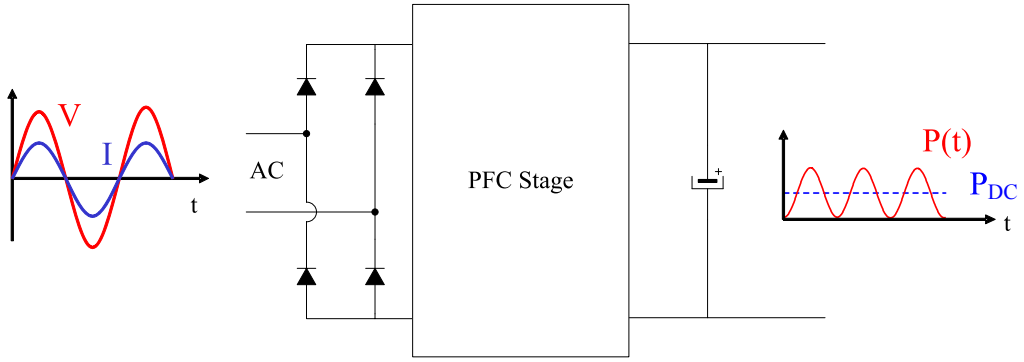

Fig. 3.3. Averaged waveforms of a sinusoidal-input-current PFC stage.

According to the input current, two PFC stages can be listed: (i) sinusoidal input current and (ii) non-sinusoidal input current.

3.4.2.1. Sinusoidal input current: Ideal PFC Stages

These converters emulate, from the point of view of the AC line, the behaviour of a resistor, drawing an in-phase instantaneous current proportional to the instantaneous line voltage. Therefore, if the input voltage is sinusoidal, the current will also be sinusoidal. These PFC converters guarantee the compliance of any regulation, since almost unity factor and very low THD_I are achieved. There are several solutions for implementing a sinusoidal PFC, the more significant being listed as follows:

- **Resistor emulator:** in this kind of PFPs, the line current is shaped by a sinusoidal reference signal synchronised to the AC line. Therefore, the input current is kept sinusoidal and in phase with the line voltage. This is achieved by sensing the line voltage in order to generate a current reference which is modified by an error amplifier in order to keep the output voltage constant. A widely-used resistor emulator is the boost converter operating in continuous conduction mode (CCM) with double control loop, sensing the input current and the output voltage and generating a reference with a

multiplier [3.7]. Any converter featuring a gain greater than unity can be used as a resistor emulator with a proper control scheme.

- **Voltage follower:** some converters intrinsically behave as a voltage follower if operating in discontinuous conduction mode (DCM) since the input port behaves as a constant resistor. Thus, there is no need for the multiplier control and the inner loop can be eliminated while maintaining sinusoidal input current. Suitable converters for this approach are the buck-boost, SEPIC, Çuk and ZETA.

A more comprehensive classification including the current-sink emulator, parallel and bidirectional energy processing approach, among others, can be found in [3.7] and [3.9].

3.4.2.2. Non-sinusoidal input current: Quasi-PFC Stages

These converters feature either a non-sinusoidal input current with limited harmonic content or a sinusoidal input current only within a given interval inside the half line period, resulting in a highly-distorted, discontinuous input current but meeting the harmonic content imposed by the regulations. There are several solutions for implementing non-sinusoidal or Quasi-PFC converters, the more significant being listed as follows:

- **DC-DC converters:** some DC-DC converters inherently behave as a Quasi PFC depending on the control loop and/or the operation mode, providing HPF and limited harmonic content. Examples of such converters are the boost PFP in DCM, which shows a significant third harmonic due to the input-current modulation imposed by the discharge time of the choke inductor, which depends on the output voltage; or the buck PFP with whichever current control [3.19]. Buck-based PFP topologies feature a crossover distortion since the buck converter is not capable of processing energy when the instantaneous input line voltage is lower than the output voltage.
- **Input current shapers (ICS):** this approach consists of a topology transformation by means of the connection of an additional output of the converter, generally from the converter transformer, between the input line and the bulk capacitor. This way, the load is directly supplied by the AC line but by means of the auxiliary output, some amount of energy is recycled, allowing for the conduction angle enlargement, but penalising the efficiency [3.20]-[3.22].

A more comprehensive classification can be found in [3.7] and [3.9].

3.4.3. Active techniques: operation modes

Regarding the active PFC solutions, three different operation modes could be distinguished according to the inductor conduction mode, which will determine the behaviour of the converter as PFC stage.

3.4.3.1. Continuous conduction mode (CCM)

In this operation mode, the inductor current is continuous and always greater than zero. There are mainly two approaches for CCM front-end PFPs: either a resistor-emulator or an input-current-clamped converter. The main difference among them relies on the input current waveform. Whereas the former features an almost unity power factor, sinusoidal input current, having been widely studied in the literature, the latter features a constant input current reference, which approaches a square-wave input current, but still fulfilling the IEC 61000-3-2 regulation.

Front-end PFC CCM clamped-current buck converter has been reported in [3.23]-[3.25], whereas a CCM clamped-current boost was first proposed and studied in [3.23] and [3.26].

The main advantages of CCM operation rely on a low EMI provided that the input-current high-frequency ripple is kept at a low level and, therefore, the EMI filter size will also be favoured. In addition, due to the low rms current through the transistors, their losses are kept at a low level.

However, since the inductors are operated in CCM, there is hard switching in the high-frequency diode turn-off due to the reverse recovery, which increases the losses in this device, increasing the radiated EMI too. In addition, in the case of resistor-emulator converters, the double-line frequency ripple in the output voltage forces the control loop to feature a low-pass filter, which implies a slow dynamic response [3.27].

3.4.3.2. Discontinuous conduction mode (DCM)

In this operation mode, the inductor current reaches the zero level, i.e. the inductor gets completely discharged. Several converters naturally behave as a voltage follower when operated at DCM under constant duty cycle, achieving almost unity factor with a single control loop. These converters are the buck-boost and flyback, SEPIC, ZETA, Ćuk, and buck-based topologies [3.28].

The main advantages of such operation mode rely on a simpler circuitry and control, which implies a lower cost compared to the CCM solution [3.29]. In addition, since the inductor gets fully discharged, the transistor turn-on and the diode turn-off achieve zero current switching (ZCS), thus reducing the transistor turn-on losses and the diode turn-off losses due to the reverse recovery. However, the rms value of the currents is much higher, increasing conduction losses and penalising the size of the EMI filter due to the higher current requirements.

3.4.3.3. Boundary conduction mode (BCM)

In boundary conduction mode, the inductor operates at the boundary between DCM and CCM. This implies that the inductor current starts being charged again at the instant when it reaches zero current and is fully discharged. Since the AC line voltage varies sinusoidally, this is only achieved by variable frequency operation.

This operation mode allows voltage-follower PFPs to be implemented with any converter topology, including the boost converter. Compared to the DCM operation, the transistor conduction losses are reduced since the current rms values are lower owing to the variable frequency operation. In addition, zero-voltage switching (ZVS) in the transistor is achievable with no additional circuitry, thus improving the overall efficiency [3.30], [3.31].

The main drawbacks of BCM operation are the higher complexity of both the control loop and the design of the EMI filter, since it has to be sized for the whole frequency swing if compared to DCM. The light-load efficiency is also penalised derived from the increase in operation frequency [3.30].

3.4.4. Active PFC architectures

The most usually employed topologies for performing PFC are listed as follows. LED drivers use typical DC-DC converter topologies but conveniently adapted to the supply of LED lamps.

3.4.4.1. Single-stage converters (SSC)

The simplest active PFC circuits consist of a unique stage converter that performs power factor correction and supplies the load. Single-stage PFPs are also called front-end PFPs or front-end PFCs. The most common one-stage topologies used are the boost converter, the buck-boost, or buck-boost derived topologies such as the flyback converter, the latter usually working in DCM [3.17], [3.29], [3.33], [3.34]. Flyback-based topologies are usually employed in cost-effective, low-power solutions, since it performs as a voltage follower with a simple control, features galvanic isolation and offers an extra degree of freedom from the transformer turns ratio [3.35]-[3.37]. Another advantage of single-stage PFPs is their high efficiency, since the energy is processed only once. This architecture is depicted in Fig. 3.4.

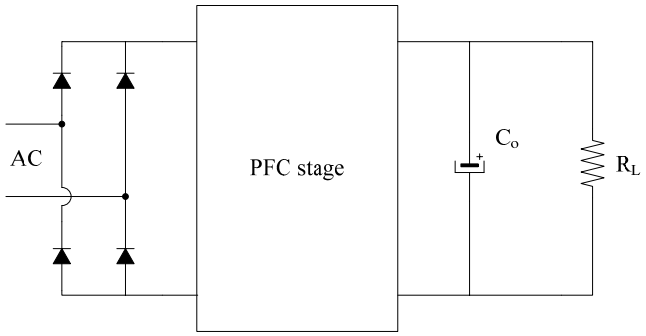

Fig. 3.4. Typical front-end PFP.

The main drawbacks of these pre-regulators are, on one hand, the high peak current stresses and EMI problem caused by the DCM operation and, on the other hand the energy storage at twice the line frequency at the output capacitor, which implies the use of huge electrolytic capacitors that worsens the dynamics and the life-span and reliability of such converters [3.29].

Moreover, Pulse-Width Modulation (PWM) dimming of LEDs must be carried out at frequencies above 125 Hz. Therefore, when PWM dimming operation is required, these single stage solutions are not feasible for traditional techniques due to their slow dynamic response unless an extra stage is added [3.3], [3.38], or more advanced PWM dimming techniques are implemented, such as the one proposed in [3.39], which will be covered in depth in Chapter 6.

3.4.4.2. Two-stage converters

In those applications demanding a universal-range input voltage and dimming feature, a two-stage architecture is needed in order to perform power factor correction properly and to obtain a fast enough output dynamics. This system implementation consists of a front-end PFP, which processes the energy from the AC line and stores it at the DC-link, followed by a cascaded DC-DC converter, which processes the energy stored at the DC-link driving the LED load with a much faster dynamics [3.28]. Fig. 3.5 sketches this architecture.

This scheme is usually implemented by means of a boost converter for the first stage and forward, buck-boost derived topologies or flyback converters for the output converter [3.3], [3.32]. In addition, even buck converters may be used for the former [3.6], [3.19], [3.23][3.24][3.25]. These topologies are a very good solution especially for high power levels, reaching unity power factor if boost or buck-boost topologies are used as PFPs, and providing fast output dynamics. However, the size of the converter is increased, and therefore, the cost is increased too. In addition, the efficiency is generally lower than the single-stage approach, since

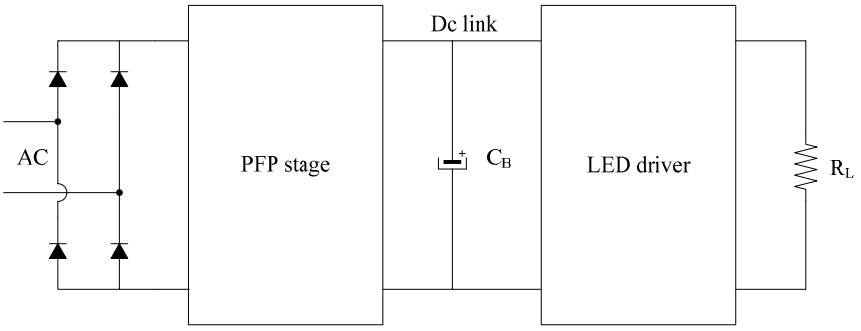

Fig. 3.5. Two-stage architecture.

the energy is processed twice [3.27], [3.29]. Two-stage architecture is a common solution in LED lighting when other features such as dimming operation or electrolytic capacitor avoidance are expected [3.3], [3.40].

3.4.4.3. Three-stage converters

This architecture is generally applied to point-of-load LED drivers, where a first stage is dedicated to perform PFC and is cascaded by a second stage implemented by a voltage-controlled DC-DC converter, either isolated or not, that implements a DC bus to which several current-controlled LED drivers are connected. This architecture is sketched in Fig. 3.6.

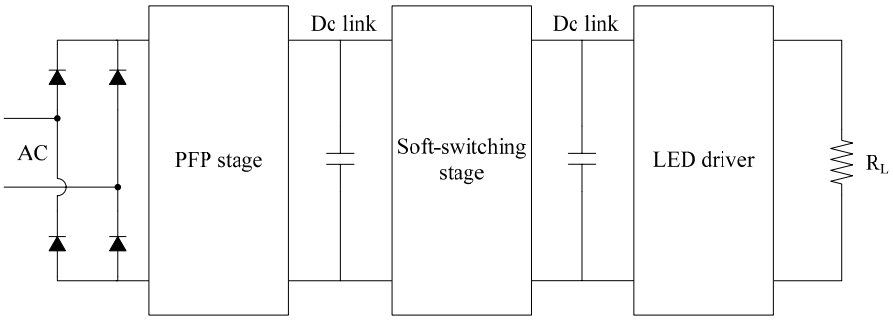

Fig. 3.6. Typical three-stage converter.

Moreover, in high-power LED lighting applications where high efficiency is pursued, this architecture is also applied by employing soft-switching converters. In [3.41] a three-stage solution is proposed for LED street lighting where each stage is optimised for a single purpose. Thus, the PFP stage is implemented by an electrolytic-capacitor less BCM boost converter optimised for high efficiency disregarding regulation, since a high voltage ripple is allowed from the electrolytic-less condition. The second stage is intended only to perform galvanic isolation by means of a ZVS-ZCS electronic transformer optimised for high efficiency to the detriment of the regulated bus voltage. Finally, Twin-Input buck (TIB) converters are used to drive several LED strings. The TIB converters are intended only for eliminating the low-frequency ripple and regulating the current through the LED string, achieving high-efficiency provided that the stress on the components is highly reduced. Authors report 92% efficiency at full load.

3.4.4.4. Integrated power converters (IPCs)

A good solution is to implement the so-called integrated power converters (IPCs) or integrated single-stage converters (ISSCs), which is based on the two-stage architecture by the integration of the PFC stage together with the DC-DC converter [3.9], [3.15]-[3.18], [3.33], [3.42]. This is achieved by eliminating one transistor and sharing the remaining transistor between the two stages, which operate with the same duty cycle, but can operate either in DCM or CCM [3.42], [3.48]. However, if both stages are operated in DCM, the converter intrinsically behaves as a voltage follower and the bus voltage is not load-dependent [3.42]. A 90 W BCM with Synchronous Rectifier (SR) flyback-based IPC has been reported in [3.43], where the efficiency of such converter is above 90% for the entire universal input voltage.

These topologies are not only a good solution when high power factor is needed, but also they can provide a satisfactorily fast output dynamic response if compared to a two-stage PFC converter, and are suitable for universal input-voltage operation. In addition, the size of the whole converter is reduced and therefore, cost, complexity and weight are reduced too [3.9]. However, although the efficiency is usually satisfactory in case of operation under narrow input voltage range conditions because part of the power is processed only once, or just a small part is processed twice within a single switching period [3.44], the efficiency is usually lower than that of the two-stages approach due to the integration process: the stages are integrated either in an over-voltage or over-current cell, leading to higher electrical stresses and losses if compared to the non-integrated topology [3.43], [3.45], [3.48].

The DC-DC converters used for integration vary widely [3.42]. Buck-boost or flyback PFPs integrated with any kind of converter have been presented in [3.43], [3.45], [3.46]; boost PFPs integrated with other topologies have been reported in [3.47]; buck converter integrated with a flyback converter has been firstly reported in [3.48].

3.5. Analysis of Voltage-Follower PFPs

Voltage follower converters will be considered due to the control simplicity and their suitability at the low power range, where the losses produced by the high rms values across transistors and diodes are less significant. This way, their behaviour as PFP will be studied and compared, prior to analyse the IBF converter as the power supply for LEDs

This section will cover the study of voltage-follower PFPs operating in DCM, attending to the input current achieved: either purely sinusoidal –Ideal PFC stages, or sinusoidal with limited harmonic current –Quasi PFC stages. A generalised study will be considered based on the loss-free resistor concept [3.52]. This forthcoming study has partially been published in [3.53].

3.5.1. Ideal PFP Stages

In this kind of PFPs, the input port of the converter behaves as a constant resistor, namely R_g, not depending on any other parameter but line voltage and duty cycle, which is considered constant. Therefore, the current is proportional to the line voltage, resulting in a sinusoidal waveform. The instantaneous power, p_g, extracted from the line can be expressed as:

$$p_g = \frac{v_g^2}{R_g} = \frac{V_g^2 \sin^2(\omega_L t)}{R_g} = \frac{V_g^2}{2R_g}(1 - \cos 2\omega_L t) \tag{3.7}$$

where v_g refers to the instantaneous line voltage, V_g the line peak voltage value and ω_L the line angular frequency.

Given the loss-free resistor concept and discarding low-frequency storage elements, it can be stated that the input and output power will be equal for an averaged switching period. Therefore, the output current –the bus current in two-stage architectures, i_B, can be calculated as:

$$i_B = \frac{p_g}{V_B} = \frac{V_g^2}{2V_B R_g}(1 - \cos 2\omega_L t) \tag{3.8}$$

Where V_B stands for the output voltage, which in turn is the bus voltage, also known as DC-link voltage.

As can be seen from (3.7), the output current features a DC component, I_B, and an AC component at twice the line frequency, $\hat{I}_B$, both of the same amplitude:

$$I_B = \hat{I}_B = \frac{V_g^2}{2V_B R_g} \tag{3.9}$$

In typical applications, such as switching-mode power supplies (SMPS), nearly all the AC component will flow through the bus capacitor equivalent reactance, X_B, generating an AC voltage ripple, $\hat{V}_B$. Its value can be calculated as:

$$\hat{V}_B = \hat{I}_B X_B = \frac{\hat{I}_B}{2\omega_L C_B} = \frac{\hat{I}_B}{4\pi f_L C_B} \tag{3.10}$$

Taking into account that the average power, P_g, processed by the PFC stage is equal to $V_g^2/2R_g$, the following expression for the voltage ripple normalised to the bus voltage, $\hat{v}_B$, can be obtained:

$$\hat{v}_B = \frac{\overline{I_n}}{C_n} \tag{3.11}$$

where $\overline{I_n}$ is the specific current, I_B/V_B, measured in A/V, and C_n is the specific bus capacitor, $4\pi f_L C_B$, measured in A/V.

Fig. 3.7 shows a chart where the bus voltage ripple can be obtained as a function of the bus capacitor for different bus current per bus voltage ratios operation at 50 Hz line frequency.

It can be seen from (3.11) and Fig. 3.7 that the higher the bus current per bus voltage ratio, the higher the capacitor needed for the same bus voltage ripple, and inversely, the higher the bus current per bus voltage ratio, the higher the bus voltage ripple for the same line frequency and bus capacitor. In addition, the lower bus voltage ripple would be achieved at the highest bus voltage achievable by the converter for a given bus current.

3.5.2. Quasi-PFC Stages

Quasi PFC Stages also behave as loss-free resistors. However, there are two effects in Quasi PFC Stages: the input resistance behaves either as a resistor only within a given interval inside the half-line period, as a variable resistor, or both. This is the case of buck- and boost-based voltage-follower converters.

The boost converter has been widely used for general SMPS and even LED drivers in two- and three-stage architectures [3.3] due to its suitability for PFC under universal input-voltage range with HPF. Regarding the DCM boost PFP, it continuously draws current from the AC line

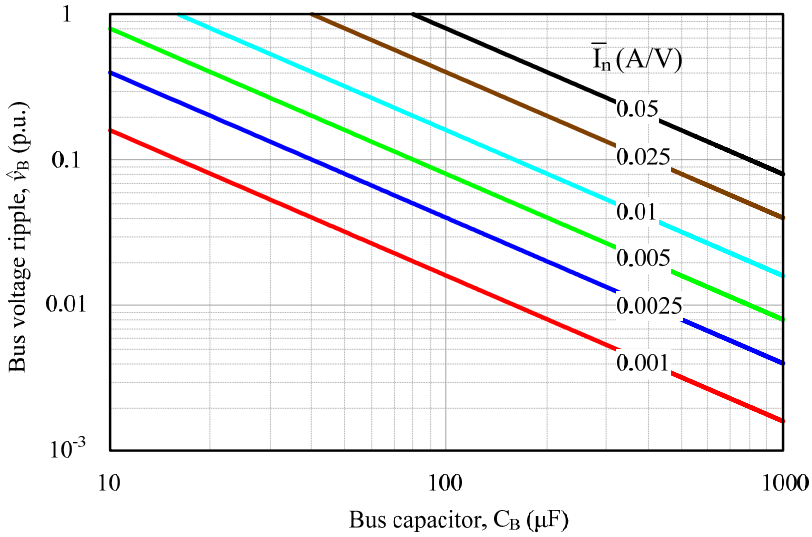

Fig. 3.7. Ideal PFC stage: normalised bus voltage ripple as a function of bus capacitor for different values of specific current. Line frequency 50 Hz.

as the buck-boost PFP, but its instantaneous input-port equivalent impedance changes depending on the line voltage, unlike the latter. This leads to a sinusoidal current with a harmonic content depending on the converter gain due to the input current modulation induced by the dependence of the choke-inductor discharging time on the bus voltage [3.55]. Thus, for achieving low THD_I and high PF, high gain ratios are to be used, yielding to bus voltages beyond 400 V for the European line voltage. This high voltage also induces a negative effect on the efficiency of the downstream converters, as the higher bus voltage increases the switching losses. This effect is especially noticeable at light-load conditions, where the switching losses dominate [3.6].

As opposed to the boost converter, the buck converter only draws current from the AC mains while the line voltage is higher than the bus voltage, leading to a conduction interval that in angular scale could be expressed as $[\alpha, \pi\text{-}\alpha]$ for a half line period, α being the dead angle within which the line voltage is lower than the bus voltage. During this interval, the input current can be written as follows:

$$i_g = \frac{v_g - V_B}{R_g} = \frac{V_g \sin(\omega_L t) - V_B}{R_g} \tag{3.12}$$

Since the buck PFP draws current from the line supply only for a certain conduction angle, θ, it is necessary to set the dead angle, α, for which the Class C requirements are satisfied. Due to the lower output voltage featured by the buck PFP and its better suitability to light-load operation, the performance of such converter will be studied in terms of THD_I and output capacitor according to the dead angle. This study will assume that the bus-voltage ripple is negligible compared to the bus-voltage value determined by the dead angle, so the bus voltage will be considered as a pure DC voltage and therefore, no effects on the input current will be taken into account. The first step will be to determine the buck equivalent resistor as a function of the conduction angle. The instantaneous input power within the conduction interval can be calculated as follows:

$$p_g = v_g i_g = \frac{V_g^2}{R_g}\sin^2(\omega_L t) - \frac{V_g V_B}{R_g}\sin(\omega_L t) \tag{3.13}$$

where α denotes the angle at which the line voltage reaches the bus voltage, $V_B = V_g\, sin(\alpha)$. Therefore, substituting in (3.13) and performing some algebra, the input power can be expressed as follows:

$$p_g = \frac{V_g^2}{2R_g}(1 - \cos(2\omega_L t) - 2\sin(\alpha)\sin(\omega_L t)) \tag{3.14}$$

By integrating (3.14) within a half line period, the average power processed by the input stage is calculated:

$$P_g = \frac{V_g^2}{2R_g}\left(1 - \frac{2\alpha + \sin 2\alpha}{\pi}\right) \tag{3.15}$$

Expression (3.15) also yields the equivalent loss-free resistor for a given line voltage and power processed as a function of the dead angle.

Therefore, the input current can be expressed as a function of the dead angle. Thus, from (3.12) and (3.15), the following expression is achieved for the input current:

$$i_n = \frac{2P_n}{\left(1 - \frac{2\alpha + \sin 2\alpha}{\pi}\right)}(\sin(\omega_L t) - \sin(\alpha)) \tag{3.16}$$

Expression (3.16) has been expressed as a power per line-voltage ratio, or specific power, $P_n = P_g/V_g$, measured as W/V in order to study the input current and the THD_I independently of line voltage and input power.

Fig. 3.8 shows the input current for different dead angles for the same specific power, and for several normalised power levels under the same dead angle. Line voltage, as well as bus voltage, is shown in a normalised voltage scale, V_n. Normalised bus voltage is expressed as V_B/V_g. The minimum value shown for the specific power is 0.08 W/V, since this power is that corresponding to the minimum input power considered in Class C requirements, namely 25 W, for 230 V_{rms} line voltage. On the contrary, 25 W input power at 90 V_{rms} line voltage would lead to a specific power of 0.2 W/V.

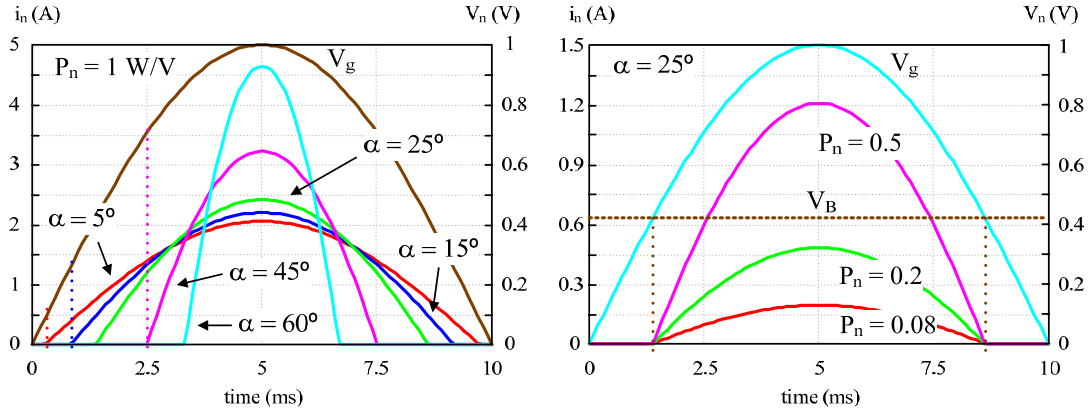

Fig. 3.8. Buck PFC stage: specific input current as a function of the dead angle at constant specific power (left) and as a function of the specific power drawn from the line under constant dead angle (right). Line frequency 50 Hz.

It can be seen from Fig. 3.8 that the higher the dead angle, the higher the bus voltage and the input current peak value, since the converter draws current from the AC line only when the bus voltage is lower than the instantaneous input voltage, eventually leading to higher harmonic distortion. The normalised bus voltage corresponding to each dead angle is highlighted by a dotted line in the left graph in Fig. 3.8. Moreover, it can also be seen from the right graph in Fig. 3.8 that the higher the input power, the higher the input-current peak value. However, the bus voltage is kept constant, not depending on the input power but on the conduction angle.

In order to determine the maximum dead angle for complying with the requirements, the power factor and the THD_I will be obtained from applying (3.1) and (3.6), respectively, to the normalised input current calculated in (3.16). The results are shown in Fig. 3.9.

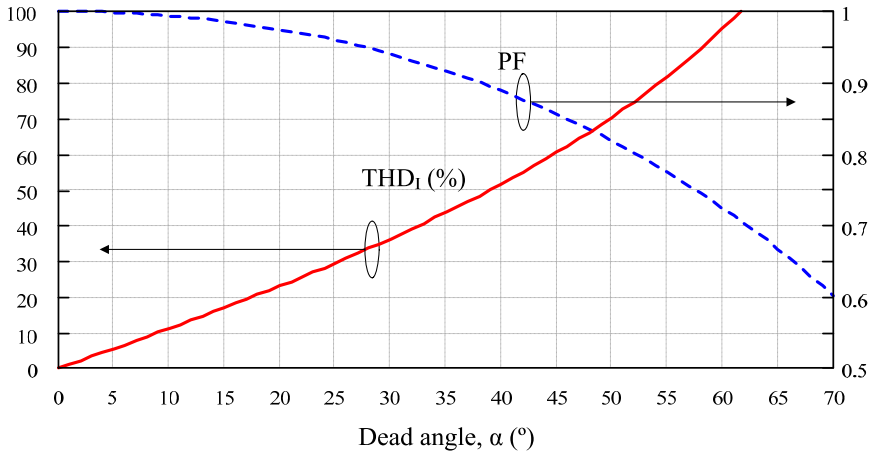

Fig. 3.9. Buck PFC stage: total harmonic distortion (red solid line) and power factor (blue dashed line) as a function of the dead angle. Line frequency 50 Hz.

As can be seen from Fig. 3.9, the Energy Star requirements for commercial applications are fulfilled with about 37º dead angle, achieving almost 50% THD_I. However, this is only valid if the PF limitation is accounted for. In order to comply with IEC61000-3-2 Class C requirements, the relative amplitude of each individual harmonic related to the fundamental frequency has to be checked. Thus, by applying the Fourier Transform (FT) to the base current obtained in (3.16), a normalised harmonics map can be obtained. This is shown in Fig. 3.10, together with the Class C limits. As can be seen from Fig. 3.10, the maximum dead angle for complying with Class C requirements is approximately 25º, limited by the third harmonic. This is coherent with the results reported in [3.54].

With regard to the output capacitor calculation, the bus voltage ripple can be obtained from the total charge injected to the bus capacitor, ΔQ, as follows:

$$\hat{V}_B = \frac{\Delta Q/2}{C_B} = \frac{1}{8\pi f_L C_B} \int_0^{\pi} |i_B - I_B| \, d\theta \tag{3.17}$$

where i_B is the instantaneous output current of the PFC stage and I_B its average value. As both currents can be calculated from (3.14) and (3.15) as p_g/V_B and P_g/V_B respectively, using (3.14), (3.15) and (3.17), the following expression is obtained for the peak value of the bus voltage ripple normalised to the bus voltage, $\hat{v}_B$:

$$\hat{v}_B = \frac{\overline{I_n}}{2C_n}\left[2\alpha + \int_{\alpha}^{\pi-\alpha}\left|\frac{1-\cos 2\theta - 2\sin\alpha\sin\theta}{1-\frac{2\alpha}{\pi}-\frac{\sin 2\alpha}{\pi}} - 1\right| d\theta\right] \tag{3.18}$$

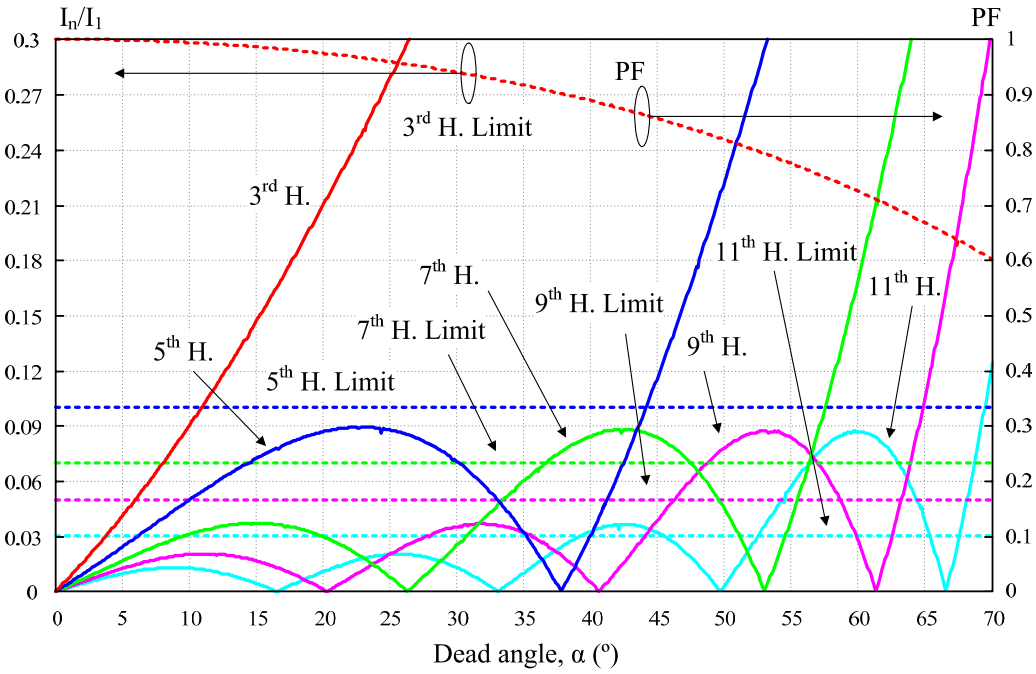

Fig. 3.10. Buck PFC stage: normalised harmonics map up to 11th harmonic and Class C limits. Line frequency 50 Hz.

Where, as in the Ideal PFC Stage case, $\overline{I_n}$ is the specific current, I_B/V_B, measured in A/V, and C_n is the specific bus capacitor, $4\pi f_L C_B$, measured in A/V. Fig. 3.11 shows a chart from which the bus voltage ripple can be obtained as a function of the bus capacitor for different bus current per bus voltage ratio considering two different dead angles, α = 10º and α = 25º, since the latter is the highest dead angle for which Class C regulations are met for input power levels higher than 25 W. Operation at 50 Hz line frequency is considered.

As can be seen from Fig. 3.11, the higher the bus current per bus voltage ratio, the higher the capacitor needed for the same bus voltage ripple, and inversely, the higher the bus current per bus voltage ratio, the higher the bus voltage ripple for the same line frequency and bus capacitor. In addition, it can be seen that a lower dead angle implies a lower bus voltage ripple. However, this leads to lower bus voltage levels, and therefore, to higher specific currents, so the results for different dead angle values are not comparable. The behaviour of the bus voltage ripple can be studied as a function of the dead angle for a given specific power. Thus, a new definition shall be done for a constant specific power ratio. This way, by expressing (3.18) as a function of bus power:

$$\hat{v}_B = \frac{\overline{P_n}}{2C_n\sin^2\alpha}\left[2\alpha + \int_{\alpha}^{\pi-\alpha}\left|\frac{1-\cos 2\theta - 2\sin\alpha\sin\theta}{1-\frac{2\alpha}{\pi}-\frac{\sin 2\alpha}{\pi}} - 1\right| d\theta\right] \tag{3.19}$$

where $\overline{P_n}$ is the specific bus power, P_B, related to the input voltage, P_B/V_g^2, measured in W/V^2, in order to study the unitary bus voltage ripple as a function of the output power and dead angle,

independently of the bus and line voltages. This expression is charted in Fig. 3.12 for a 100 µF bus capacitor several specific power levels as a function of the dead angle.

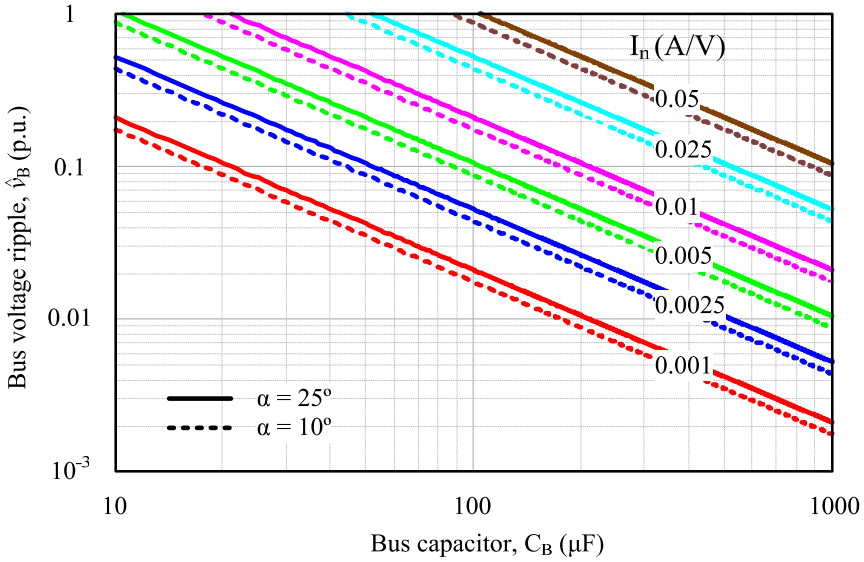

Fig. 3.11. Buck PFC stage: normalised bus voltage ripple as a function of bus capacitor for different values of specific current. Line frequency 50 Hz.

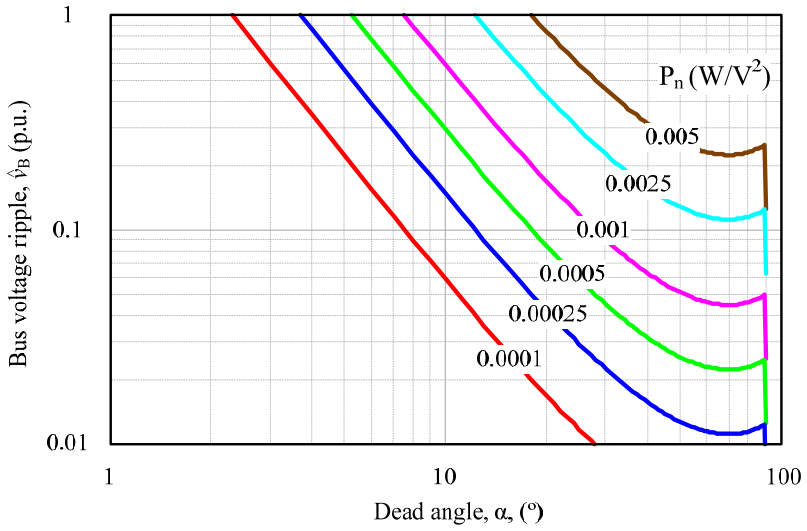

Fig. 3.12. Buck PFC stage: normalised bus voltage ripple as a function of dead angle for different values of specific bus power assuming a 100 µF bus capacitor. Line frequency 50 Hz.

As can be seen from Fig. 3.12, for a constant bus power, lower dead angles imply higher bus voltage ripple. This is reasonable, since lower dead angles induce lower bus voltages and therefore, higher bus currents for the same specific power, so the bus capacitor has to be increased in order to keep the voltage ripple constant.

3.6. Proposed PFP topology

The topology proposed in this work for performing the PFC and supplying the LED load is the high power factor (HPF) integrated buck-flyback converter (IBFC) developed in previous works [3.15], [3.16], [3.45], [3.46]. It is composed by a buck converter performing PFC

integrated with a flyback DC-DC converter supplying an LED lamp. The buck converter must be operated in DCM so that high power factor can be achieved at the input while the converter behaves as a current source at the output with simple control loop. The buck-flyback converter is sketched in Fig. 3.13 before integration. Since the main purpose of this Chapter is to present a brief survey on the most remarkable PFC techniques, LED drivers architectures and PFP topologies, the integration process, as well as the operation of the IBF converter, will be deeply covered and discussed in the next Chapter, the present one only giving considerations about the PFC Stage.

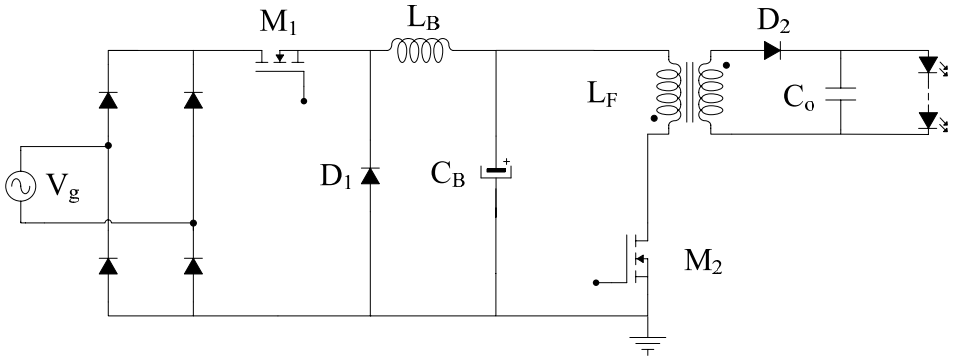

Fig. 3.13. Two-stage buck-flyback converter for supplying an LED load.

The main advantages of buck-based topologies over boost-based PFPs lie in several aspects [3.6]. Firstly, the bus voltage is much lower than that of boost or buck-boost based converters, with lower downstream voltages. This improves reliability and efficiency due to the use of lower-voltage MOSFETs with better figures of merit, and results in lower common mode (CM) noise. In addition, a lower DC bus voltage requires a lower voltage rating for the bulk capacitor, featuring a lower ESR device and longer life if adequately sized. Other advantages include a lower PFC inductance value, higher control easiness and inherent stability, and a natural protection against no-load or short-circuit operation.

On the disadvantages of the buck PFC over boost-based topologies, the more remarkable are the inherent cross-over distortion that limits THD_I and PF and larger bulk capacitors due to the lower bus voltage and therefore higher current levels for the same output power, which in turn induces higher bus voltage ripple, and higher losses if the bus voltage is too low [3.6]. Indeed, if comparing the bus capacitor needed for a 0.1 unitary bus voltage ripple for 0.001 normalised current in the case of a buck-boost and a buck PFP, it can be seen from Fig. 3.7 and Fig. 3.11 that the output capacitor needed will be around 15 μF and 20 μF in the case of the buck-boost and the buck converter, respectively.

With regard to the PFC performances, it can be seen from Fig. 3.10 that conduction angles above approximately 130º will fulfil Class C requirements while requiring bus voltage levels high enough not to compromise the efficiency due to high rms currents in the downstream stages. Precisely, inspection of Fig. 3.12 shows that the lower the dead angle, the higher the ripple due to the decrease on bus voltage and its subsequent increase in output current. Therefore, it can be concluded that the optimal design relies on dead angles around 20 – 25º, so the Class C requirements are satisfactorily fulfilled whereas the bus voltage ripple is kept at the low level, allowing for the use of smaller bus capacitors or even, allowing for the employment of non-electrolytic devices, which further increases the reliability of the PFP stage and in turn the LED driver.

3.7. Conclusions

In this chapter, the need for power factor correction has been introduced since the main purpose of this work is to develop an integrated converter for supplying LED lamps in the range of 50 – 100 W from the AC mains. Thus, the concept of power factor and harmonic content has been introduced, and the existent IEC 61000-3-2:2005 Class C regulations for lighting products have been covered, taking into account both the luminaries with an input power lower than and greater than 25 W. Since the LED lamps used in this work feature power dissipation in the range of 60 – 70 W, the efforts have been focused on the limits for 25 W or more. Therefore, the most usually employed and most significant techniques for limiting the harmonic content have been covered and discussed. This way, passive and active PFC techniques have been studied and discussed. However, since LED lighting products for such a power range are intended to be high-performance products, only active PFC has been taken into account for subsequent work. With regard to active PFC, a brief but deep revision about the performance of PFP circuits – either ideal PFC or Quasi PFC stages, operation mode of converters, and architecture of PFC circuits in general and LED drivers from the AC mains supply in particular, has been developed. This revision has been carried out assuming that the bus-voltage ripple is negligible compared to the bus voltage, and therefore, the effect of the bus-voltage ripple on the buck-converter input current can be neglected. Regarding the architecture of the LED driver solution, the most important contributions have been presented, namely one-stage, two-stage and third-stage converters, as well as IPCs for PFC and LED supply. Moreover, both ideal- and quasi-PFC voltage-follower stages have been analysed in terms of harmonic content and output capacitor requirements, bringing the focus to the buck PFP. Finally, provided that this topology shows several advantages over boost-based PFPs, and since the low bus voltage also allows for operation from an UPS unit or DC bus, the topology finally chosen relies on the buck PFP.

3.8. References

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[3.55] Liu, K.-H.; Lin, Y.-L.; "Current waveform distortion in power factor correction circuits employing discontinuous-mode boost converters," in Records of the 20th Annual IEEE Power Electronics Specialists Conference, 1989. PESC '89, vol. 2, pp. 825 – 829. Milwaukee, Wisconsin, US. 14 – 17 October 1996.

Chapter 4

Study of the High-Power-Factor Off-line Integrated Buck-Flyback Converter for LED Lighting Applications.

This chapter introduces the study and analysis of the integrated buck-flyback converter (IBFC) proposed in this work. First, the two-stage buck-flyback converter is presented, highlighting its main advantages over other topologies. After that, the integration technique developed by T.-F. Wu et al. will be briefly covered prior to presenting the IBFC. Then, the IBFC will be statically analysed for two operation modes: Full DCM and DCM/CCM, the former characterised by the operation of both inductors in DCM, whereas the latter characterised by the DCM operation of the buck inductor and the CCM operation of the flyback inductor. The buck converter is operated in DCM so PFC is achievable by a voltage-follower approach.

Second, both operation modes are compared according to their suitability for supplying LED lamps from the AC mains supply. After that, the study of the IBFC as an LED driver supplied from the AC mains will be covered.

Finally, a case study will be included, where a Full-DCM IBFC is proposed for supplying a 70 W LED lamp under universal input-voltage range.

4.1. Introduction

As stated in the previous Chapter, the simplest architecture for implementing an LED driver performing PFC consists of a front-end PFP that directly supplies the LED load. This architecture assures very high efficiency while being the simplest, most cost-effective solution for power levels beyond 25 W, since PFC is compulsory to be performed in order to fulfil the Class C requirements. However, two- and three-stage architectures are widely used in the medium-to-high power-level lighting applications. Although the power is processed more than once, the efficiency achieved by such architectures can be fairly high, since the design of each stage can be optimised for a given task, namely PFC, bus voltage regulation, constant-current supply, or dimming. Nevertheless, this increases the complexity of the LED driver and the Bill of Materials (BoM), thus increasing cost.

As stated in the previous Chapter, a good solution that comes from the two-stage architecture is to implement the so-called Integrated Power Converters (IPCs), or Integrated Single-Stage Converters (ISSCs) by the integration of the active switches corresponding to each stage, in the way that both stages share a single synchronous transistor. This integration technique yields a single-stage HPF converter with a satisfactorily fast output dynamic response, and the capability of operation under universal input-voltage range. However, these converters have one degree of freedom less than the equivalent two-stage converter, showing also higher electrical stresses due to the integration process, which can lead to lower a efficiency.

The topology proposed in this work is the high power factor (HPF) integrated buck-flyback converter (IBFC) firstly described in [4.1] as a DC-DC converter, and developed in previous works as an HPF off-line power supply [4.2], as an HPF ballast for MH lamps [4.7], [4.8], and for HPS lamps [4.9]. It is composed by a buck converter performing PFC integrated with a flyback DC-DC converter supplying an LED lamp. Since the buck converter works as a voltage follower, it must be operated in DCM so that high power factor can be achieved at the input while the converter behaves as a current source at the output with a simple control loop. With regard to the second stage, the flyback converter allows the LED load to be supplied by means of a low component-count, isolated converter, which is well suited for low-to-medium power applications, such as street, commercial or indoor lighting. The flyback converter can operate either in DCM or CCM, but in the latter case the bus voltage is load-dependent. The buck-flyback converter is sketched in Fig. 4.1 before integration.

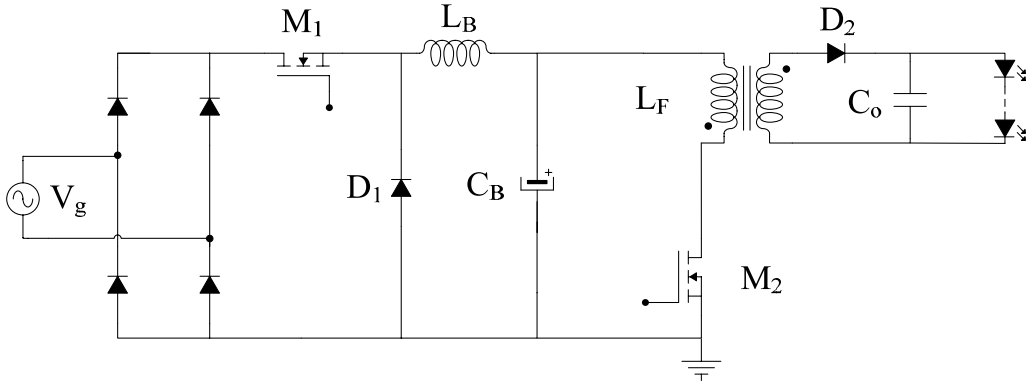

Fig. 4.1. Two-stage buck-flyback converter for supplying an LED load.

The converter integration technique pursues the generation of one-stage – or single-stage converters, from two cascaded converters, either DC–DC or DC–AC for achieving a high gain range while reducing the component count and, therefore, the cost of the converter. Although many integrated converters were previously proposed, such as [4.1] or [4.2]-[4.4], among many others, the integration technique was generalised in [4.5].

This technique is applicable when the transistors of both stages feature a common node, although topological transformations are possible in order to fulfil this requirement, and work synchronously with the same duty cycle. There are four different types of synchronous transistor connections, which are depicted in Fig. 4.2.

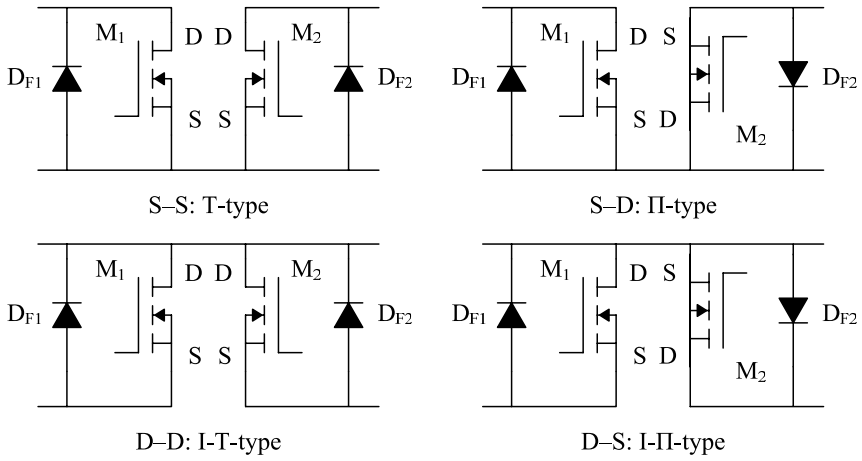

Fig. 4.2. Different possible connection between transistors in a two-stage converter.

In this case, the two transistors are replaceable by a single synchronous transistor plus four diodes, which allow the current to be bidirectional, block voltage differences and manage the current unbalance between both converters. It has to be noted that the diodes highlighted as D_{F1} and D_{F2} in Fig. 4.2 allow the current to be bidirectional. Therefore, only two blocking diodes are to be added, which will block the voltage difference between M_1 and M_2 in the synchronous transistor M_S. The four synchronous transistors are depicted in Fig. 4.3.

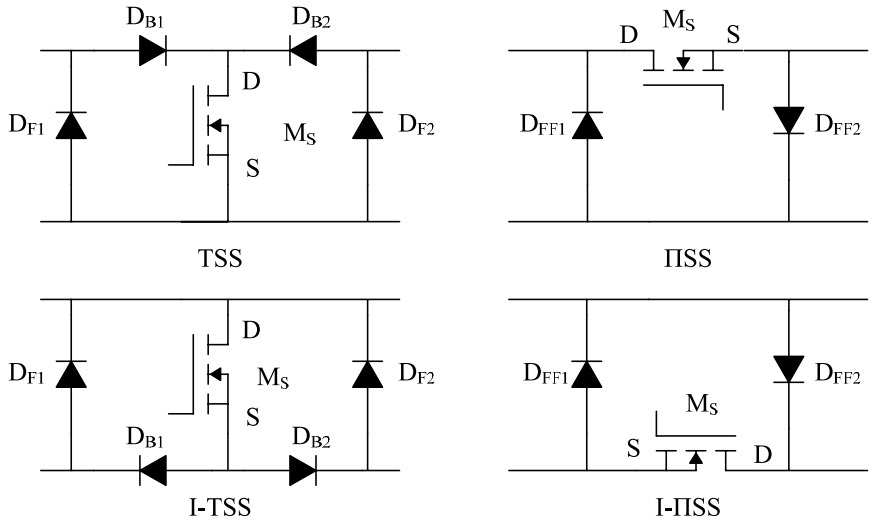

Fig. 4.3. Synchronous transistors after integration.

4.1.1. Proposed topology: Integrated Buck-Flyback Converter

As previously stated, the converter proposed in this work is derived from the integration of a buck front-end PFC cascaded with a flyback converter for supplying an LED lamp. In order to develop the integration, first, the transistors of both stages have to share a common node. This is sketched in Fig. 4.4, where the secondary side of the flyback converter and the AC line source are disregarded for the sake of simplicity.

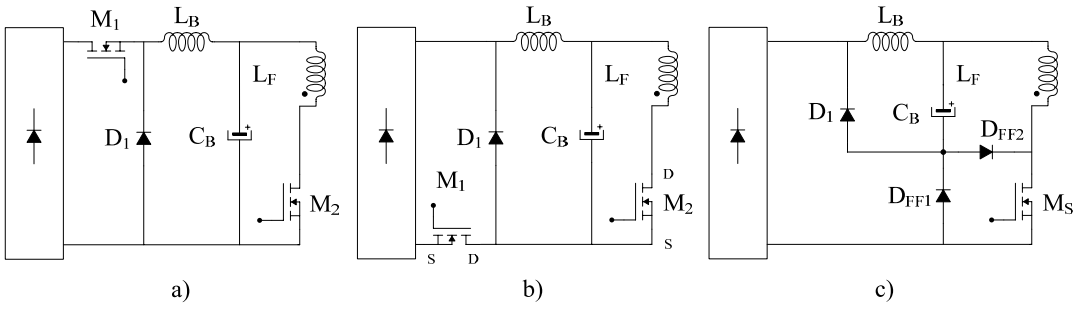

Fig. 4.4. Integration process of the buck-flyback converter: a) original circuit; b) relocation of the buck transistor; c) buck-flyback topology with synchronous transistor.

The common node is achieved by replacing the buck transistor, M_1 in Fig. 4.4, so the drain of M_1 and the source of M_2 share the same node, also with the buck-freewheeling diode and bus capacitor anodes. This is shown in Fig. 4.4 b). As can be seen from Fig. 4.2 and Fig. 4.4, the D-S connection corresponds to an I-Π-type synchronous transistor. By applying the I-ΠSS synchronous transistor depicted in Fig. 4.3, the result shown in Fig. 4.4 c) is achieved. The entire topology of the IBFC for supplying an LED load is depicted in Fig. 4.5.

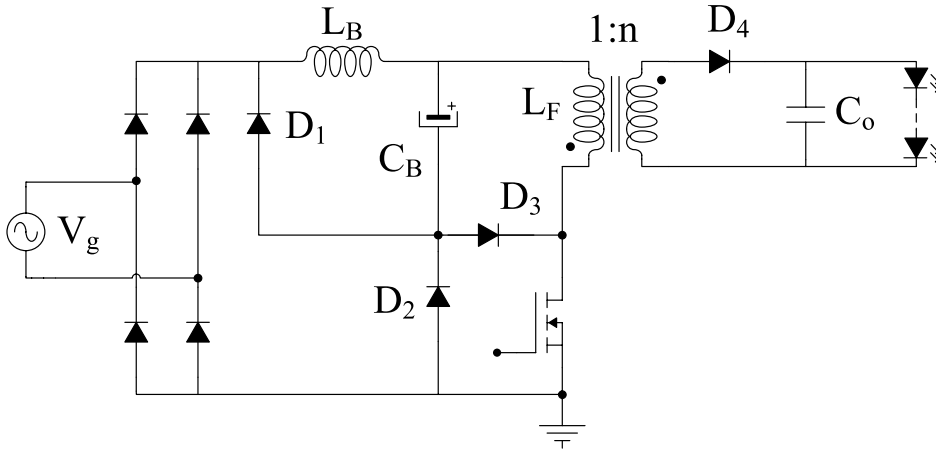

Fig. 4.5. Integrated buck-flyback converter.

The main advantages of the buck PFC over boost-based PFPs lie in several main aspects [4.10], which have been outlined in the previous Chapter. Another advantage of the IBFC over boost- and buck-boost- based topologies is that in the proposed ballast, the switch only handles the highest of the buck or flyback current, not the addition of both currents, as happens in other integrated single-stage converters [4.8], [4.9]. This point, together with the better efficiency of buck-based PFPs at light load [4.10], helps to keep the losses at a reasonable level, including at dimmed operation, where it is expected to overcome the performance of ISS boost-based LED drivers.

4.2. Analysis of the Integrated Buck-Flyback Converter (IBFC)

This section will cover the analysis of the integrated buck-flyback converter from a DC supply attending to its operation in Full DCM, i.e. both the buck and flyback inductors in DCM, and in DCM/CCM, where the buck inductor is operated in DCM and the flyback inductor is operated in CCM. This is aimed to deeply understand the operation of the converter prior to extending the analysis to an AC supply. The converter will be directly studied for supplying LED lamps. For the sake of simplicity and comprehensiveness, the secondary side of the IBFC will be referred to the primary side considering a generic turns ratio *n*. Therefore, the Integrated Buck-Buck-Boost Converter will be the case of study. The currents and voltages in the IBFC components are shown in Fig. 4.6.

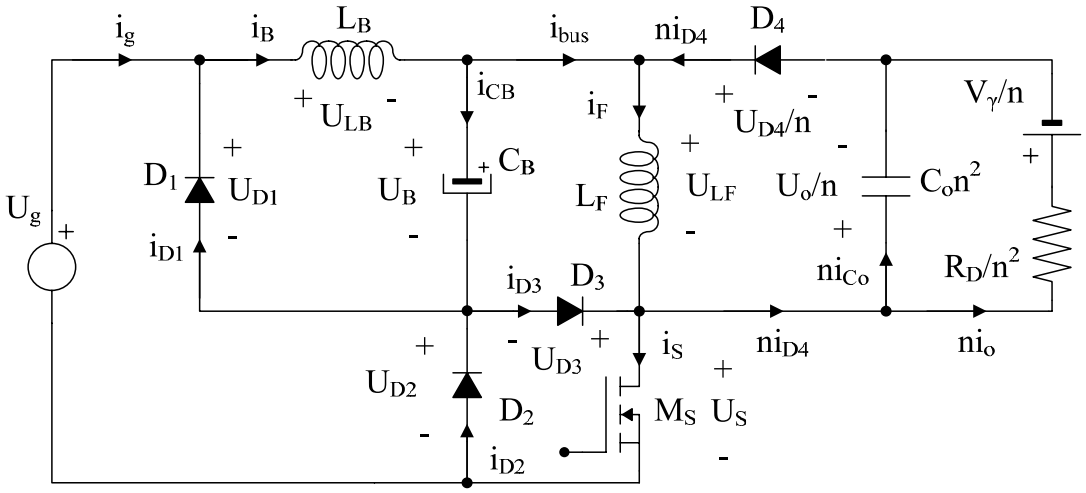

Fig. 4.6. Currents and voltages in the IBFC. The secondary side of the flyback converter is transferred to the primary side.

From here onwards, the second-stage converter will be referred to as buck-boost or flyback with no distinction, whether this stage is composed of an *n*-turns ratio flyback converter or by a buck-boost. The subsequent analysis is performed under the assumptions of a lossless converter and a supply voltage greater that the bus voltage at any time.

The relations between the different currents are shown in (4.1).

$$\begin{aligned} i_g &= i_B - i_{D1} & \qquad i_{CB} + i_{D2} &= i_{D1} + i_{D3} \\ i_F &= i_{bus} + n i_{D4} & \qquad i_F + i_{D3} &= i_S + n i_{D4} \\ i_B &= i_{CB} + i_{bus} & \qquad i_{Co} + i_o &= i_{D4} \end{aligned} \tag{4.1}$$

Some considerations shall be taken for fully understanding the operation of the IBFC. First, as the first stage is a buck converter, the IBFC will draw current from the supply only when the transistor is in the on state and the supply voltage, U_g, is higher than the bus voltage, U_B. In case of U_B being higher than U_g, the converter will work as a flyback cell, not drawing energy from the power supply, but from the bus capacitor and therefore, the bus voltage will drop. Another interesting issue is that the current through the synchronous transistor, M_S, will be the higher of the buck or the flyback current, not the sum of both, as stated in [4.6]. This partly compensates for the increased electrical stresses in the transistor, as the IBFC is built on an over-voltage cell [4.5], [4.7], penalising the efficiency to a lower extent compared to other integrated topologies [4.8]. Consequently, as the current through the synchronous transistor will be the higher of both

cell currents, two situations will be considered: first, higher buck current: $i_B > i_F$, and second, higher buck-boost current, $i_F > i_B$. It would also be interesting to analyse the role of diodes D_2 and D_3. These diodes could be considered as in parallel to two current sources: the buck inductor, and the flyback inductor, when the synchronous transistor is in the on state, as shown in Fig. 4.7

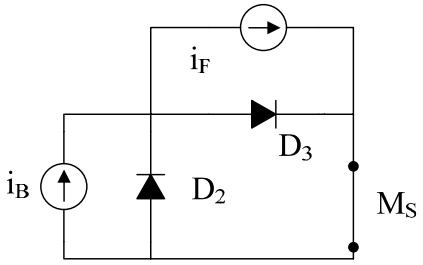

Fig. 4.7. Equivalent circuit during the synchronous transistor M_S on-time.

It can be demonstrated that the diodes D_2 and D_3 role is to balance the current mismatch between buck- and flyback-inductors. This is, as long as the buck-inductor current is higher than that of the flyback inductor, diode D_3 will be forward-biased and D_2 reverse-biased, and vice versa, as long as the current through the flyback inductor is higher, D_2 will be forward-biased and D_3, reverse-biased [4.6].

The following sections will cover the study of the IBF converter for Full DCM and DCM/CCM operation. The relations between currents are gathered in Table IV.I for all the stages of each operation mode.

4.2.1. Full DCM Operation Mode

In this mode, both the buck and flyback inductors are operated in DCM. However, two situations could be distinguished: flyback inductor current higher than that of buck converter, or vice versa. The definition of voltages and currents is that indicated in Fig. 4.6.

4.2.1.1. Full DCM Operation, $i_F > i_B$:

The following stages, which are depicted in Fig. 4.8, could be highlighted:

- Stage I. Transistor in on-state: $0 < t \leq dT$

In this stage, the transistor is in the on-state and the inductors are charged by drawing current from the power supply. Provided that $i_F > i_B$, the current through the bus capacitor, i_{CB} is negative due to the current flows assumed, so the capacitor is providing enough current to balance the difference between the two inductor currents. This current flow forces diodes D_1 and D_3 to be reverse-biased, forward-biasing diode D_2. This implies that the bus capacitor is discharged through the flyback inductor, the synchronous transistor, and diode D_2.

Moreover, it can also be verified that the synchronous transistor only manages the higher of the two currents: the flyback current in this case.

- Stage II. Transistor in off-state: $dT < t \leq min(d_B, d_F)T$

In this stage, the transistor is turned off and the inductors are discharged and transfer the energy stored to the bus capacitor, the output capacitor, and the load. Stage II covers the time elapse for which one of the inductors reaches the DCM after the transistor has been turned off.

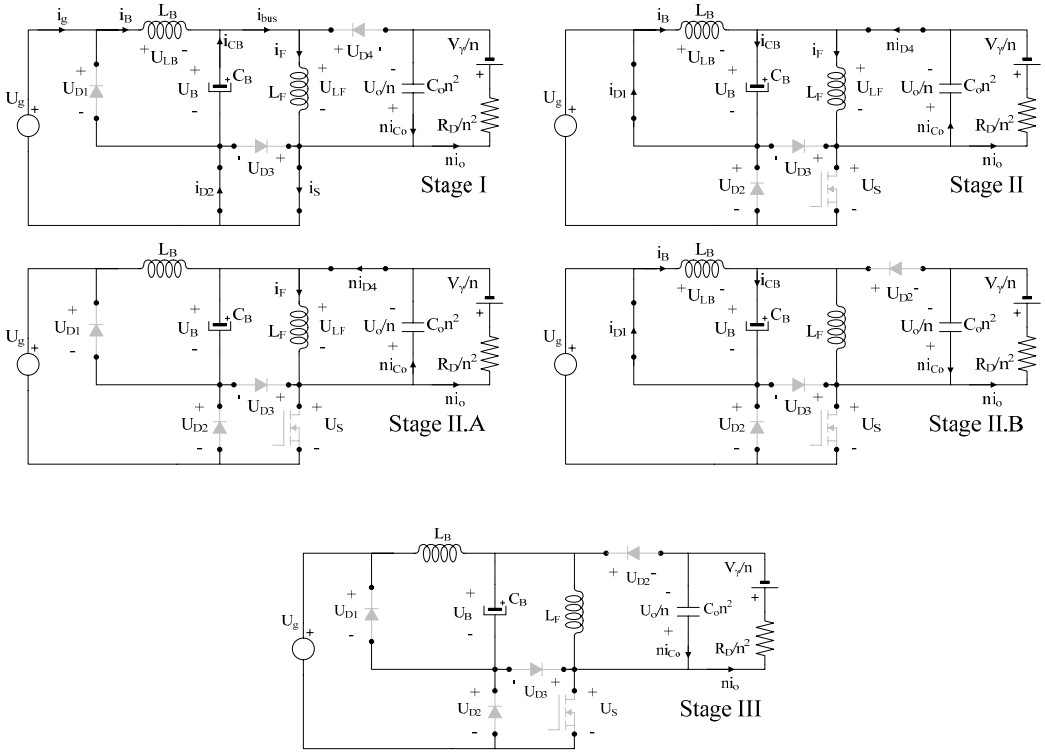

Fig. 4.8. Full DCM operation stages for $i_F > i_B$.

The current through the output capacitor will be positive – this is, entering the capacitor, as long as the discharge flyback-inductor current is higher than the output current. Once the flyback inductor current has reached the output current from above, the output capacitor will provide the difference between both currents and therefore, the output capacitor current will become negative as in Stage I. As the discharge time of the buck inductor and the discharging time of the flyback inductor, d_BT and d_FT, respectively, are equal only for a particular case, two sub-stages will be considered: Stage II.A and Sage II.B

- Stage II.A. Transistor in off-state, $dB < d_F$: $d_BT < t \leq d_FT$

In this stage, the buck-inductor current reaches zero before the flyback-inductor current. As in the previous stage, once the flyback-inductor current reaches the output current from above, the output-capacitor current will be negative.

- Stage II.B. Transistor in off-state, $d_B > d_F$: $dFT < t \leq d_BT$

In this stage, the flyback-inductor current reaches zero before the buck-inductor current. The bus-capacitor current is positive, i.e. entering the capacitor, whereas the output capacitor is negative, supplying the LED load.

- Stage III. Zero current in both inductors: $max(d_B, d_F)T < t \leq T$

In this stage, both inductor currents have already reached zero and there is no current flowing in the converter but from the output capacitor supplying the LED load.

The main waveforms are shown in Fig. 4.9 a). In this figure, a generic situation is considered: it is assumed that the discharging time of the buck inductor is shorter than that of the flyback. This is stated by the use of a dashed line for the flyback-inductor discharging current. The different operation stages are also highlighted.

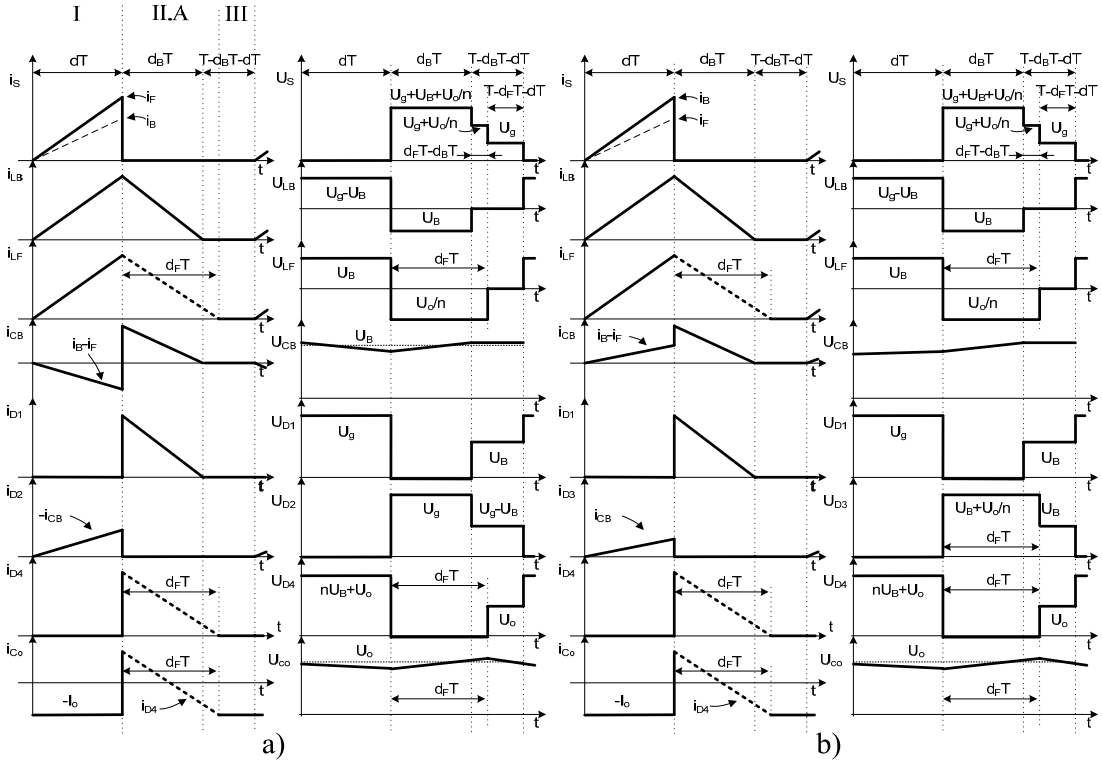

Fig. 4.9. Full-DCM-operation main current and voltage waveforms for a) $i_F > i_B$, b) $i_B > i_F$.

4.2.1.2. Full DCM Operation, $i_B > i_F$:

In this operation mode the voltages and currents criteria are kept as in the previous case. The operation stages are the same as in the previous case, except for Stage I and Stage II, which are depicted in Fig. 4.10.

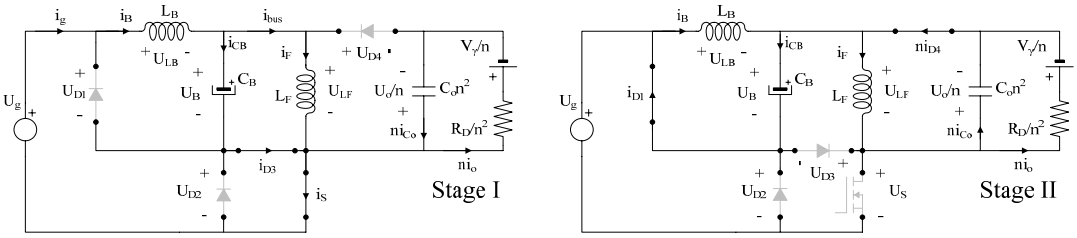

Fig. 4.10. Full DCM operation stages for $i_B > i_F$.

The operation stages are characterised as follows:

- Stage I. Transistor in on-state: $0 < t \leq dT$

As in the previous case, the transistor is in the on-state and the inductors are charged by drawing current from the power supply. Provided that now $i_B > i_F$, the current through the bus capacitor, i_{CB} is positive, so the bus capacitor is being charged. As diodes D_1 and D_2 are reverse-biased, diode D_3 has to manage the imbalance between the buck and the flyback current, being therefore forward-biased.

It should be noted that the bus capacitor current is positive due to the current flows assumed. Again, it can be verified that the synchronous transistor only manages the higher of the two currents, the buck inductor in this case.

- Stage II. Transistor in off-state, discharging inductors: $dT < t \leq min(d_B, d_F)T$

As commented in the previous case, in this stage the transistor is in the off state and the inductors are discharged and transfer the energy stored to the bus capacitor, the output capacitor, and the load. Again, it will be considered that either the buck or the flyback inductor will reach zero current while the other current is still greater than zero.

As in the previous case, the current through the output capacitor will be positive – this is, entering the capacitor, as long as the discharge flyback-inductor current is higher than the output current. Once the flyback inductor current has reached the output current from above, the output capacitor will provide the difference between both currents and therefore, the output capacitor current will become negative as in Stage I.

Moreover, it should be noted that the current through the bulk capacitor is still positive, as in Stage I. This means that this operation mode is not feasible in steady state under DC supply, since the charge balance in the bulk capacitor is not null, and therefore, the average current in steady state would not be zero and energy would be being stored, which contradicts the principle of zero current across capacitors in steady state. Nevertheless, it has to be remarked that this operation mode is feasible in transient periods and in certain steady-state periods under AC supply for given designs.

Again, two sub-stages will be considered: Stage II.A and Sage II.B, depending on the discharging times of the inductors.

- Stage II.A. $d_B < d_F$: $d_BT < t \leq d_FT$

In this stage, the buck-inductor current reaches zero before the flyback-inductor current. The relations between the currents are identical to those of the previous case. As in the previous stage, once the flyback-inductor current reaches the output current from above, the output-capacitor current will be negative.

- Stage II.B. $d_B > d_F$: $d_FT < t \leq d_BT$

As in the previous analysis, the flyback-inductor current reaches zero before the buck-inductor current, the bus-capacitor current being positive and the output capacitor negative.

- Stage III. Zero current in both inductors: $max(d_B, d_F)T < t \leq T$

As in the previous case, both inductor currents have already reached zero and there is no current flowing in the converter but from the output capacitor supplying the LED load.

The main waveforms are shown in Fig. 4.9 b). In this figure, a generic situation is considered: it is assumed that the discharging time of the buck inductor is shorter than that of the buck-boost converter. Moreover, it has to be noted than in this operation mode, the diode D_2 is never forward-biased, but D_3 is.

4.2.2. DCM/CCM Operation Mode

In this operation mode, the buck inductor still works in DCM in order to perform PFC, whilst the flyback inductor works in CCM. As the buck-inductor current starts from zero at each switching cycle, but the flyback inductor current does not, the relation between both currents will be either a higher flyback current for the entire switching period or only for a given time.

Therefore, two situations could be distinguished: either a flyback-inductor current higher than that of buck converter, or vice versa. The voltages and currents definition is the same as in Fig. 4.6 whereas the currents relation is the same as in (4.1). The currents relations are gathered in Table IV.I.

4.2.2.1. DCM/CCM Operation, $i_F > i_B$ for the entire switching period.

This operation mode would be a particular case where the flyback current is higher than that of the buck inductor for the entire switching period. As opposed to the Full DCM operation mode, two stages could be distinguished, which are sketched in Fig. 4.11:

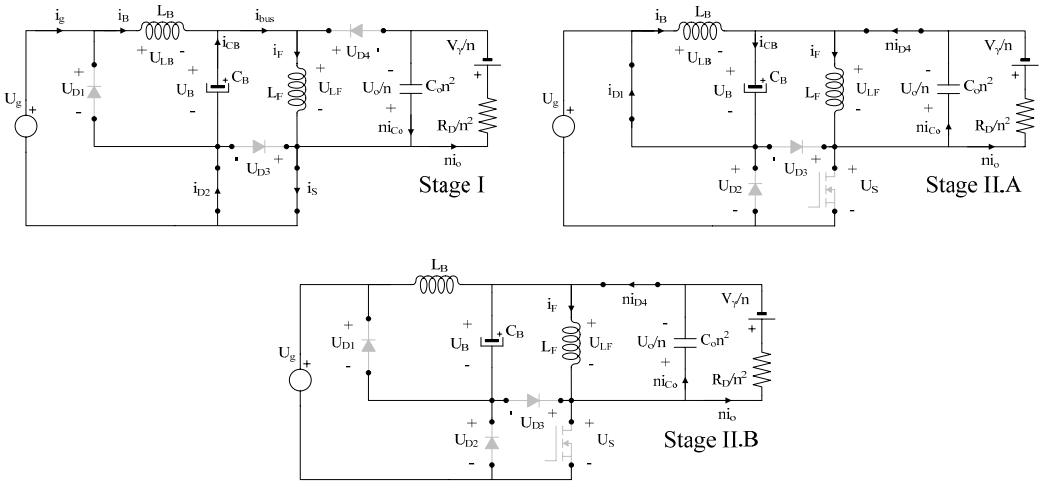

Fig. 4.11. DCM/CCM operation stages.

- Stage I. Transistor in on-state: $0 < t \leq dT$:

This stage is equivalent to that of the operation in Full DCM: this is, the transistor is in the on state and the inductors are charged by drawing current from the power supply. In addition, since the buck inductor is working in DCM and the flyback inductor in CCM, the current through the flyback inductor at the starting point will be non-zero. Provided that $i_F > i_B$ for the entire switching period, the current through the bus capacitor, i_{CB} is negative during the transistor on-time, while the capacitor is providing enough current to balance the difference between the two inductor currents. These current relations force diodes D_1 and D_3 to be reverse-biased, forward-biasing diode D_2. The currents are expressed as in (4.2) and (4.3).

- Stage II. Transistor in off state: $dT < t \leq (1\text{-}d)T$:

In this stage, the transistor is in the off state. However, as the buck converter is operating in DCM whereas the flyback converter is in CCM, two substages may be distinguished:

- Stage II.A. Transistor in off-state, buck inductor discharging: $dT < t \leq d_BT$:

In this stage, the inductors are discharged, transferring the energy stored to the bus capacitor, the output capacitor, and the load. As the buck inductor is operated in DCM, this inductor will become de-energised before the transistor is switched again, while the flyback inductor still stores energy.

It should be noted that, although the average current through the output diode is higher than the output current in buck-boost-based converters in CCM, the high-frequency output current ripple will be determined by the flyback inductor during this stage. This implies that depending

on the inductance value, the current through the output capacitor will be positive – this is, entering the capacitor, for the entire stage as long as the output-current ripple is small. Otherwise, the current through the flyback inductor may reach lower current levels than the output current so the output capacitor is led to supplying current to the LED load.

- Stage II.B. Buck inductor fully discharged: $d_BT < t \leq T$:

In this stage, the buck inductor is fully discharged, but the flyback inductor is not. The flyback inductor is still supplying energy to the output capacitor and the load. However, depending on the inductance value, and therefore, on the output-current ripple, the current across diode D_4 might be low enough to make the output capacitor provide energy to the LED load. The main voltage and current waveforms are sketched in Fig. 4.12 a).

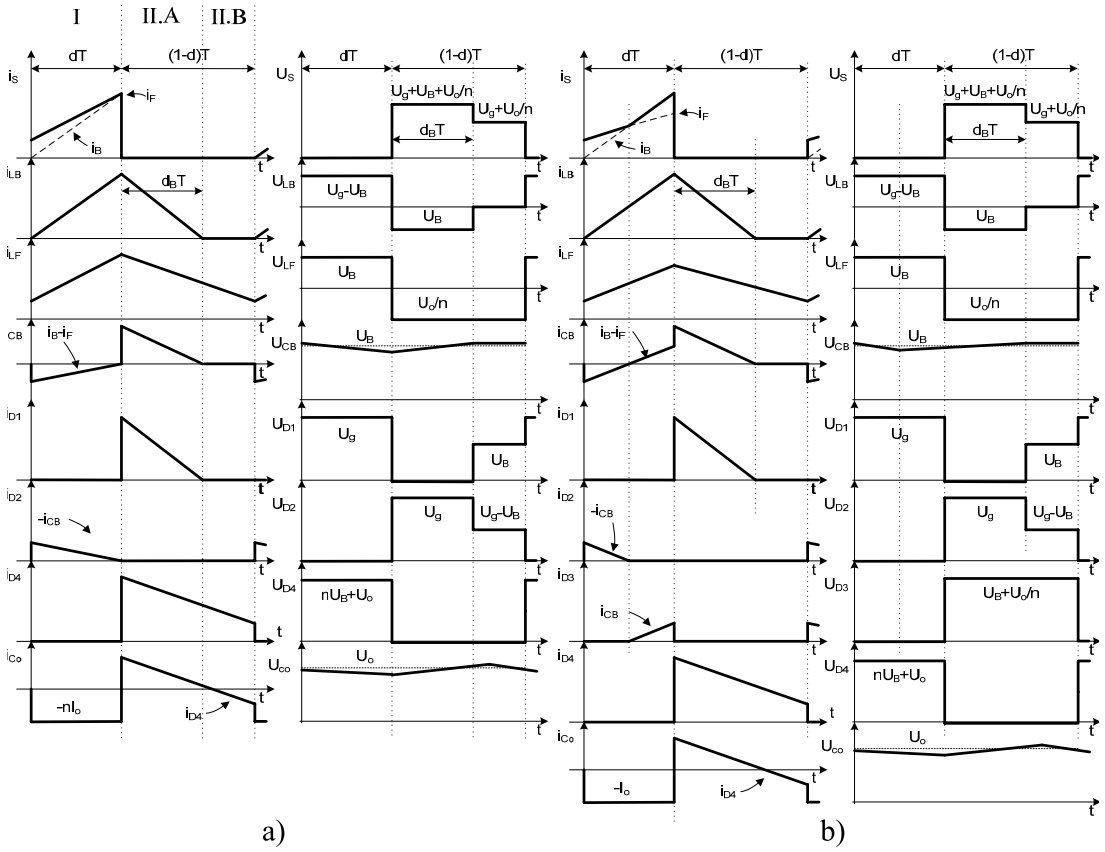

Fig. 4.12. DCM/CCM-operation main current and voltage waveforms for a) $i_F > i_B$, b) $i_B > i_F$.

4.2.2.2. DCM/CCM Operation, general case.

The general case is referred to those DCM/CCM operation modes, either in steady-state or under transient conditions, where the current through the flyback inductor may drop below that of the buck inductor. This is achieved in steady-state when the buck maximum current is higher than that of the flyback inductor, since the initial current is higher in the latter, provided that the flyback converter is operated in CCM. The voltages and currents definitions considered are those gathered in (4.1) and depicted in Fig. 4.6. The following stages, which are the same as in the previous case, depicted in Fig. 4.11, are:

TABLE IV.I
CURRENT RELATIONS OF THE IBF CONVERTER IN FULL DCM AND DCM/CCM

<table>
<tr><th rowspan="2">Stage</th><th colspan="2">Full DCM Operation</th><th colspan="2">DCM/CCM Operation</th></tr>
<tr><th>$i_F > i_B$</th><th>$i_B > i_F$</th><th>$i_F > i_B$</th><th>$i_B > i_F$</th></tr>
<tr><td rowspan="2">Stage I</td><td colspan="2">$i_g = i_B$
$i_F = i_{bus}$
$i_{CB} = i_B - i_F$
$i_o = -i_{Co}$</td><td colspan="2">$i_g = i_B$
$i_{CB} = i_B - i_F$
$i_F = i_{bus}$
$i_o = -i_{Co}$
$i_{D2} = -i_{CB}$</td></tr>
<tr><td>$i_{D2} = -i_{CB}$
$i_S = i_F$</td><td>$i_{D3} = i_{CB}$
$i_S = i_F + i_{CB}$
$i_S = i_B$</td><td>$i_S = i_F$</td><td>$i_{bus} = i_B - i_{CB}$
$i_{D2} = i_F - i_B$
$i_{D3} = i_{CB}$
$i_{D3} = i_B - i_F$
$i_S = i_F + i_{D3}$</td></tr>
<tr><td>Stage II</td><td>$i_{D1} = i_B$
$i_F = ni_{D4}$
$i_B = i_{CB}$</td><td>$i_{CB} = i_{D1}$
$i_F = ni_{D4}$
$i_{Co} + i_o = i_{D4}$</td><td colspan="2">-</td></tr>
<tr><td>Stage II.A</td><td colspan="2">$i_F = ni_{D4}$
$i_{Co} + i_o = i_{D4}$</td><td>$i_{D1} = i_B$
$i_F = ni_{D4}$
$i_B = i_{CB}$</td><td>$i_{CB} = i_{D1}$
$i_F = ni_{D4}$
$i_{Co} + i_o = i_{D4}$</td></tr>
<tr><td>Stage II.B</td><td>$i_B = i_{D1} = i_{CB}$</td><td>$i_{Co} = -i_o$</td><td colspan="2">$i_{Co} + i_o = i_{D4}$</td></tr>
<tr><td>Stage III</td><td colspan="2">$i_{Co} = -i_o$</td><td colspan="2">-</td></tr>
</table>

- Stage I. Transistor in on-state: $0 < t \leq dT$:

This stage is equivalent to that of the operation in Full DCM, namely, the transistor is in the on state and the inductors are charged by drawing current from the power supply.

Since the buck inductor is working in DCM and the flyback inductor in CCM, the current through the flyback inductor at the starting point will be non-zero. Provided that in the general case the buck-inductor peak current will be higher than that of the flyback, both diodes D_2 and D_3 will be forward-biased at some time while the synchronous transistor is in the on-state. The function of both diodes, as in the previous cases, is to manage the current mismatch between both inductors: as long as the flyback current is higher than the buck current, diode D_2 will be forward-biased and the bus capacitor will supply the rest of the current, whereas as long as the buck inductor is higher, diode D_3 will be forward-biased and the bus capacitor will be charged with the difference between the flyback current and the buck current.

It has to be noted that in this case, the current through the synchronous transistor will change within the on-time, being equal to the flyback current as long as the flyback current is higher, and being equal to the buck inductor as long as it is higher than the flyback inductor.

- Stage II. Transistor in off-state: $dT < t \leq (1\text{-}d)T$:

Again, as the buck converter is operating in DCM whereas the flyback converter is in CCM, two substages may be distinguished.

- Stage II.A. Buck inductor discharging: $dT < t \leq d_BT$:

In this stage, the transistor is in the off-state and the inductors transfer the energy stored to the bus capacitor, the output capacitor, and the load. As the buck inductor is operated in DCM, this inductor will become de-energised before the transistor is switched again, while the flyback inductor still stores energy. The currents are related as in the previous operation mode. The considerations about the high-frequency output ripple and the polarity of the current across the output capacitor are the same as in the previous case, where the flyback current is higher than the buck current for DCM/CCM operation.

- Stage II.B. Buck inductor fully discharged: $d_BT < t \leq T$:

As in the previous case, the buck inductor is fully discharged, but the flyback inductor is still supplying energy to both the output capacitor and the load.

4.2.3. Static analysis of the IBFC

The static analysis of the IBF converter will be developed in order to determine its conversion ratio for both the Full DCM and the DCM/CCM operation modes.

4.2.3.1. Full DCM mode

In order to analyse the converter statically and to determine the conversion ratio, the voltages and currents values averaged over a switching cycle are to be determined. The analysis will be developed for a generic relation between the flyback- and buck-inductor peak currents. First, by applying the volts-seconds balance to the inductors, the buck- and flyback-inductor discharging times, d_B and d_F, respectively, are calculated as:

$$d_B = d\frac{(U_g - U_B)}{U_B} \qquad d_F = nd\frac{U_B}{U_o} \tag{4.2}$$

In order to calculate the charge balance in the bulk capacitor, the average current across the capacitor is zero in steady state. This means that the average current through the buck inductor is the same as the average bus current, which is the same as the current through the synchronous transistor:

$$I_B = I_{bus} = I_S \tag{4.3}$$

The buck-inductor current average for a switching cycle can be calculated as:

$$I_B = \frac{(U_g - U_B)}{m}\frac{d^2T}{2L_B} \tag{4.4}$$

where $m = U_B/U_g$ is the buck PFC conversion ratio.

The averaged current through the synchronous transistor, in the case $i_F > i_B$, can be calculated as:

$$I_S = U_B \frac{d^2 T}{2L_F} \tag{4.5}$$

Otherwise, if $i_B > i_F$, the transistor current is that of the buck converter:

$$I_S = \left(U_g - U_B\right) \frac{d^2 T}{2L_B} \tag{4.6}$$

By equalling (4.4) and (4.5), and rearranging, the supply-to-bus voltage conversion ratio can be obtained as:

$$\frac{U_B}{U_g} = \frac{2}{1 + \sqrt{1 + 4\alpha_L}} \tag{4.7}$$

where $\alpha_L = L_B/L_F$ is the buck-to-flyback inductor ratio. This relation has already been introduced in [4.6], [4.7]. The importance of this expression is that in steady state, the bus voltage depends only on the input voltage and the inductor ratio [4.4], [4.6].

The buck and flyback equivalent resistances at the operation point can be determined as:

$$R_B = \frac{2L_B}{d^2 T} \qquad\qquad R_F = \frac{2L_F}{d^2 T} \tag{4.8}$$

Since the input current, i_g, is the same as the buck inductor, it can easily be concluded that the IBFC input port behaves a buck converter with input equivalent resistance R_B.

With regard to the output current, the conversion ratio will be calculated assuming a lossless converter. Attending to the bus-to-output conversion ratio, and considering the LED lamp parameters V_γ and R_D, threshold voltage and dynamic resistance, respectively:

$$U_B I_{bus} = V_\gamma I_o + R_D I_o^2 \tag{4.9}$$

Expanding (4.9) and solving for the output current:

$$I_o = -\frac{V_\gamma}{2R_D} + \sqrt{\left(\frac{V_\gamma}{2R_D}\right)^2 + \frac{{U_B}^2}{R_D} \frac{d^2 T}{2L_F}} \tag{4.10}$$

The first negative addend is obtained from the LED linear model and means that the output current will be positive only once the second addend reaches that value.

In addition, the average electrical stress on the semiconductors can be calculated by averaging currents and voltages for a switching cycle. The results obtained are gathered in Table IV.II.

With regard to the operation conditions for each Full DCM operation mode, the condition for $i_F > i_B$ will be obtained. As both inductors are in discontinuous mode, this implies that the buck-inductor current is higher than the flyback-inductor at any time within the switching period. Thus, this can be calculated by their peak value:

$$\frac{U_B}{L_F} dT > \frac{U_g - U_B}{L_B} dT \tag{4.11}$$

TABLE IV.II
ELECTRICAL STRESSES IN THE IBFC IN FULL DCM AVERAGED FOR A SWITCHING CYCLE

Device	**Full DCM Operation**			
	I		***V***	
	$i_F > i_B$	$i_B > i_F$	$i_F > i_B$	$i_B > i_F$
D_1	$\frac{(U_g - U_B)^2}{U_B}\frac{d^2T}{2L_B}$		U_B	
D_2	$((\alpha_L + 1)U_B - U_g)\frac{d^2T}{2L_B}$	0	$U_g - U_B$	
D_3	0	$(U_g - (\alpha_L + 1)U_B)\frac{d^2T}{2L_B}$	U_B	
D_4^*	$n\frac{U_B^2}{U_o}\frac{d^2T}{2L_F}$		$\frac{U_o}{n}$	
M_S	$U_B\frac{d^2T}{2L_F}$	$(U_g - U_B)\frac{d^2T}{2L_B}$	U_g	
L_B	$\frac{(U_g - U_B)}{m}\frac{d^2T}{2L_B}$		0	
L_F^*	$U_B\frac{d^2T}{2L_F} + n\frac{U_B^2}{U_o}\frac{d^2T}{2L_F}$		0	

**: referred to the primary side of the transformer*

Therefore, this operation mode is assured always if the IBFC parameters meet the following condition:

$$\alpha_L > \frac{1}{m} - 1 \tag{4.12}$$

Moreover, even during a transient period or AC line supply, this is fulfilled if the instantaneous input voltage, u_g, meets the following condition:

$$u_g < (\alpha_L + 1)U_B \tag{4.13}$$

Otherwise, the buck-inductor current will be higher than that of the flyback inductor.

Finally, the maximum duty cycle, d, for which the IBFC operates in Full DCM can be calculated for both inductors from (4.2). Thus, for the buck converter:

$$d < \frac{U_B}{U_g} = m \tag{4.14}$$

Analogously, for the flyback converter:

$$d < \frac{1}{1 + n\,{U_B}/{U_o}} \tag{4.15}$$

In case (4.14) is not met, the buck converter will not perform PFC as a voltage-follower, deprecating its performance unless other control strategies are implemented [4.10]-[4.13]. On the contrary, if (4.15) is not met, the IBFC will reach the DCM/CCM operation mode, explained in the next section.

4.2.3.2. DCM/CCM operation mode

Analogously to the Full DCM operation mode, the volt-seconds balance in the inductors will be calculated in order to determine the converter conversion ratio. Regarding the buck inductor, the discharging time has been calculated in (4.2). Since the flyback inductor is operated in CCM, the volt-second balance directly yields the bus-to-output conversion ratio. Thus, after considering the LED load and solving for the output current:

$$I_o = -\frac{V_\gamma}{R_D} + \frac{U_B}{R_D} n \frac{d}{1-d} \tag{4.16}$$

As can be seen from (4.16), and as opposed to the case of Full DCM operation, in DCM/CCM the bus voltage does depend on other parameters than the inductance ratio, such as the duty cycle, the turns ratio, and the load. In order to determine the bus voltage variation as a function of the output power, the bus-capacitor current must be studied. In order to fulfil the steady-state condition, the average current across the bus capacitor must be zero. Therefore, the average current across the buck inductor and the bus current, i.e. the flyback input current, must be equal. Given that the current through the flyback inductor is continuous, it can be calculated as a regular buck-boost converter from the bus power balance:

$$U_B I_{bus} = \frac{U_o}{n} n I_o \tag{4.17}$$

By rearranging, substituting the voltage ratio, solving for I_S, equalling the buck inductor current, and solving for the bus voltage the following expression is achieved:

$$U_B = U_g - \frac{P_o}{U_g} \frac{2L_B}{d^2 T} \tag{4.18}$$

Inspection of (4.18) shows that the bus voltage depends on several parameters such as the supply voltage, the output power, and the buck-converter equivalent resistor, which in turn depends on the duty cycle, as can be seen in (4.8). Moreover, it can be seen that for a given power, an appropriate choice of duty cycle allows an optimal bus voltage to be selected. It has to be noted that this operation mode introduces more freedom in the design, as the duty cycle can be obtained for a given bus voltage, or vice versa, with the turns ratio as an extra degree of freedom.

In addition, the electrical stress on the semiconductors can be calculated. Thus, by averaging currents and voltages for a switching cycle, the results obtained are gathered in Table IV.III.

TABLE IV.III
ELECTRICAL STRESSES IN THE IBFC IN DCM/CCM AVERAGED FOR A SWITCHING CYCLE

Device	DCM/CCM Operation			
	I		V	
	$i_F > i_B$	$i_B > i_F$	$i_F > i_B$	$i_B > i_F$
D_1	$\frac{(U_g - U_B)^2}{U_B}\frac{d^2T}{2L_B}$		U_B	
D_2	$\left(\frac{nI_o}{1-d} - \frac{1}{2}\Delta I_{LF}\right)d + \frac{U_B(\alpha+1) - U_g}{\alpha 2L_F}d^2T$	$< I_o\frac{nd}{1-d}$	$U_g - U_B$	
D_3	0	$< (U_g - U_B)\frac{d^2T}{2L_B}$	$\left(U_B + \frac{U_o}{n}\right)(1-d)$	
D_4^*	nI_o		$\left(U_B + {}^{U_o}/_{n}\right)d$	
M_S	$I_o\frac{nd}{1-d}$	$< I_o\frac{nd}{1-d} + (U_g - U_B)\frac{d^2T}{2L_B}$	U_g	
L_B	$\frac{(U_g - U_B)}{m}\frac{d^2T}{2L_B}$		0	
L_F^*	$I_o\frac{n}{1-d}$		0	

*: *referred to the primary side of the transformer*

It has to be remarked that the DCM/CCM general case is more complex than the DCM/CCM operation mode for $i_F > i_B$, as the current through the synchronous transistor will be either that of the flyback or the buck converter, depending on which is higher at any moment, D_2 and D_3 managing the imbalance between both currents. Therefore, the average current through the synchronous transistor and diodes D_2 and D_3 can be bounded by the sum of the buck and flyback currents, by the buck current and by the flyback current, respectively.

4.3. Considerations on the operation mode: ¿Full DCM or DCM/CCM?

By the time of setting the most suitable operation mode, several considerations are to be taken. The first stage must be operated in DCM in order to perform PFC as a voltage-follower, thus limiting the harmonic content under any input voltage and output power conditions. Moreover, with regard to the second stage, the operation mode choice has to be taken according to the benefits of each operation mode in certain aspects, namely efficiency, bus voltage control, and output current ripple.

With reference to the efficiency, the operation of the second stage in CCM implies a lower rms current through the synchronous transistor, reducing the losses. However, since zero-current switching (ZCS) in the diodes is lost, the importance of the reverse recovery rises, inducing a decrease on the efficiency. This could be overcome by the use of synchronous

rectification, although the final cost would be increased. Since the rms values across the transistor are kept at a low level at low-to-medium output power applications, the operation of the second stage in DCM would be a feasible choice.

Regarding the bus voltage control, it can be seen from (4.7) and (4.18) that in the case of operation in DCM, the bus voltage depends only on the input voltage and the inductance ratio. On the contrary, in the case of CCM operation, the bus voltage depends on the line voltage, the output power and the buck equivalent resistance, undergoing an increase on the bus voltage for lower power levels. This last issue has been reported for an Integrated Double Buck-Boost converter in [4.14]. Two considerations may be done: on the one hand, an increase on the bus voltage induces higher peak voltage stress on the transistor, which increases the switching losses, likely compensating for the increase on efficiency that lower currents imply. On the other hand, and as has been stated in Chapter 3 regarding the performance of the buck PFP, an increasing bus voltage will induce an increase on the dead angle, leading to a higher harmonic content and eventually, the non-compliance of the Class C regulations.

In addition, CCM operation of buck-boost and flyback converters introduces an RHP zero that makes the controller design more demanding.

Finally, the output-current ripple will be determined by the low-frequency voltage gain of the second stage, which will amplify –or attenuate, the bus voltage ripple that will produce an output-current ripple due to the dynamic resistance of the LED load.

The bus voltage will feature a DC level, U_B, and a given ripple at twice the line frequency, $\hat{u}_B$, as disclosed in Chapter 3. This bus voltage can therefore be expressed as follows:

$$u_B(t) = U_B + \hat{u}_B(t) \tag{4.19}$$

As previously stated, the second stage, operating either in DCM or CCM will supply the LEDs from the bus voltage. Assuming that the cut-off frequency of the second stage is much above twice the line frequency, which is a usual practice in order to minimise the size of the reactive components, the low-frequency ripple is transferred to the output by the DC gain of the second stage. Therefore, the bus-to-voltage amplitude ratio, which will be called the ripple-gain factor, v, [4.14], [4.15] could be obtained after taking the derivative of (4.10) and (4.16) for the second stage DCM and CCM operation, respectively. Thus, by taking the partial derivative of (4.10) with respect to the bus voltage:

$$v_{DCM} = \frac{\partial I_o}{\partial U_B} = \frac{2U_B}{R_F\left(2R_D I_o + V_\gamma\right)} \tag{4.20}$$

Regarding the CCM ripple-gain factor, the partial derivative of (4.16) yields:

$$v_{CCM} = \frac{\partial I_o}{\partial U_B} = \frac{n}{R_D}\frac{d}{1-d} \tag{4.21}$$

By careful inspection of (4.20) and (4.21), it can be said that in order to reduce the LED output-current ripple, the following situation would be of benefit: a low bus-voltage ripple; a second stage featuring a low gain-ripple factor; an LED lamp featuring a high dynamic-resistance.

According to the ripple-gain factor, it can be stated that in DCM operation mode, the higher the buck equivalent resistor, the lower the ripple-gain factor, which implies a low duty cycle and/or high buck inductance: On the contrary, in CCM operation mode, the ripple-gain factor

depends on the turns ratio and the duty cycle, not accounting for the dynamic resistance, in such way that duty cycles below 0.5 will induce a gain lower than 1, provided that the turns ratio is 1 or lower.

The following illustrative example will be proposed: given a flyback converter, either in DCM or CCM operation mode, cascaded to a 100 V DC bus with a 5% voltage ripple supplying the Cree XLamp XR-E proposed in the illustrative example in Chapter 2, which features V_γ = 169.85 V and R_D = 49 Ω at 350 mA output current. Both converters work at full load with 0.4 duty cycle in order to assure low conduction losses and a wide load regulation, with 100 kHz switching frequency. By introducing the mentioned parameters in (4.10) and (4.16), a 123 µH flyback inductor is obtained in the DCM case whereas a 2.81 turns ratio is calculated for the CCM case. The bus-voltage to output-current characteristics as a function of the duty cycle and as a function of the bus voltage under constant duty cycle (4.10) and (4.16) are depicted in Fig. 4.13.

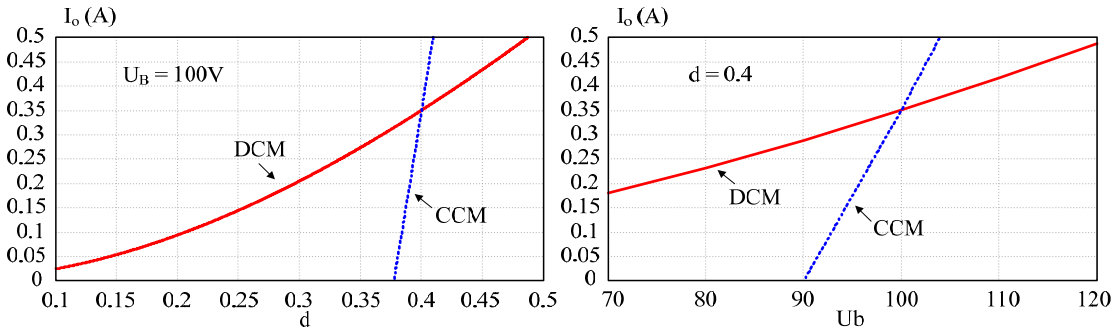

Fig. 4.13. Bus-voltage to output-current characteristic for a flyback in DCM (red solid line) and CCM (blue dashed line) as a function of the duty cycle (left) and bus voltage (right) supplying an LED lamp from a 100 V DC bus.

As can be seen from Fig. 4.13, the higher gain of the CCM operation mode is displayed as a steeper bus-voltage to output-current characteristic, resulting in a higher gain-ripple ratio. Fig. 4.14 shows the output current obtained by using the parameters mentioned above in (4.10) and (4.16) considering a 100 Hz, 10 V AC peak-to-peak ripple superimposed to the bus 100 V DC voltage.

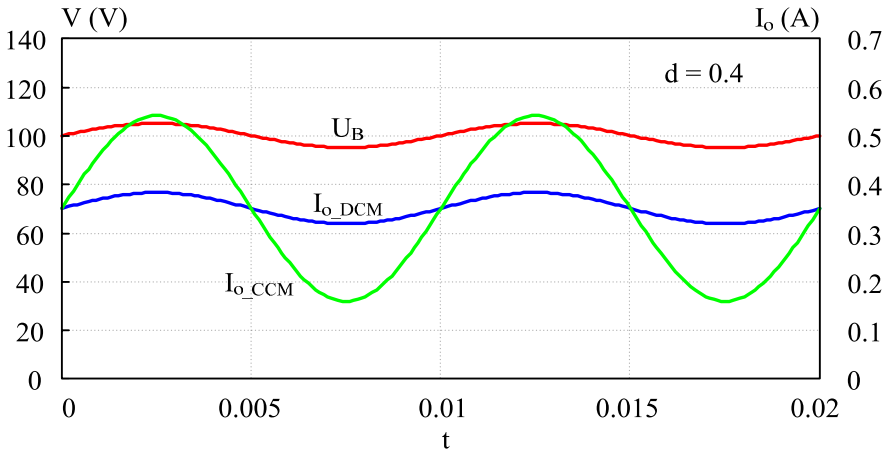

Fig. 4.14. Output current of the DCM and the CCM flyback converters running from a 100 V DC bus with a 5% voltage ripple.

As can be seen from Fig. 4.14, due to the higher gain of the CCM operation mode, the output-current AC ripple is much higher, leading to higher and more bulky bus capacitors, likely rising the need for electrolytic devices, which lower the life-span of the electronic converter. A practical comparison can be obtained from [4.14] and [4.15], where the same LED lamp was supplied by a Full DCM Integrated Double-Buck-Boost Converter (IDBBC) featuring a 12 μF bus capacitor and a 3 μF output capacitor whereas the DCM/CCM IDBBC needed a 80 μF bus capacitor and 40 μF output capacitor for the same output-current ripple performance.

4.4. The DCM-IBF converter as a high power factor off-line LED driver.

The IBF converter operating in DCM (DCM-IBFC) and supplied from an AC source behaves as previously studied in Chapter 3 – the buck PFP, and as described in Section 4.2 – the IBF converter. Therefore, the DCM-IBFC will draw current from the AC line only when the instantaneous input voltage is higher than the bus voltage, leading to a dead angle, α. It was demonstrated in Chapter 3 that Class C requirements are satisfied for dead angles shorter than 25º. Since the IBFC is operated in Full DCM, it will feature a bus voltage that is independent of the duty cycle, output power, switching frequency, etc. Indeed, it will only depend on the buck-to-flyback inductor ratio, α_L. Moreover, under AC input voltage, the IBFC will behave as a DCM flyback converter supplied from the DC bus. Thus, three equivalent circuits could be distinguished according to the instantaneous line voltage and the synchronous transistor state. These circuits are illustrated in Fig. 4.15 for a half-line period.

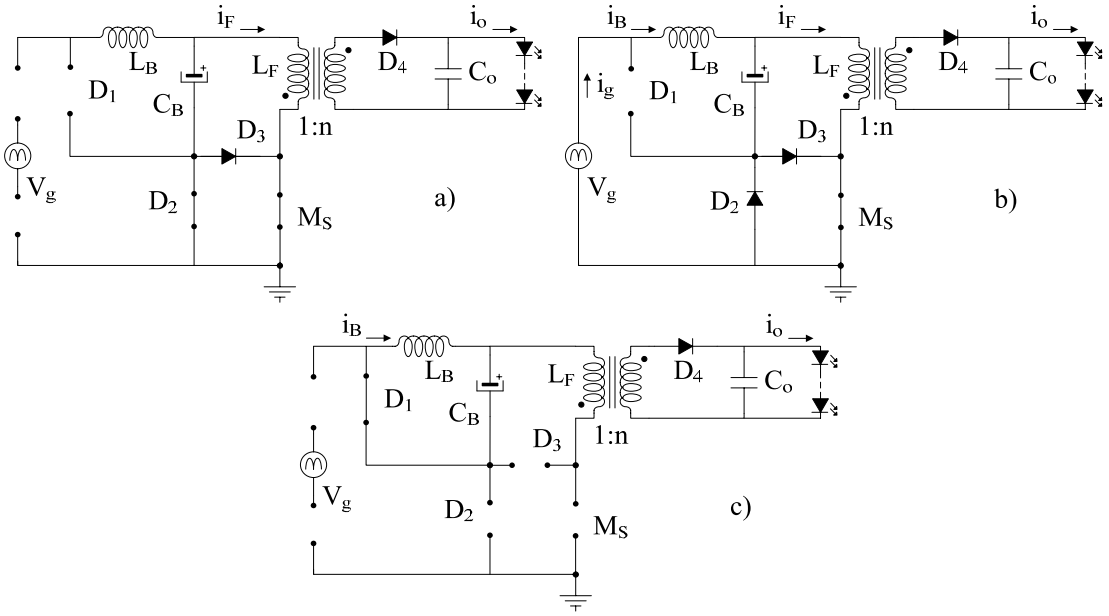

Fig. 4.15. Equivalent circuits of the IBFC according to the instantaneous line voltage and the transistor state. a) $u_g < U_B$ and M_S on; b) $u_g > U_B$ and M_S on; $u_g > U_B$ and M_S off.

During the intervals when the instantaneous line voltage, u_g, is lower than the bus voltage, the rectifier-bridge diodes are reverse-biased and the converter operates in flyback mode taking energy from the bus capacitor through the synchronous transistor, M_S, and diodes D_2 and D_4, the buck inductor being de-energised, diode D_1 reverse-biased, and diode D_3 short-circuited or reverse-biased, depending on the transistor state. This is illustrated in Fig. 4.15 a). On the contrary, when the instantaneous line voltage is higher than the bus voltage, two equivalent circuits can be highlighted, which are shown in Fig. 4.15 b) and Fig. 4.15 c). Both inductors are energised while the transistor is in the on-state, as shown in Fig. 4.15 b), and diodes D_1 and D_4

are reverse-biased. Regarding diodes D_2 and D_3, they will be forward-biased or short-circuited according to the difference between the buck- and the flyback-inductor currents, as has already been analysed in Section 4.2.1. Finally, when the synchronous transistor is in the off-state, diodes D_1 and D_4 will become forward-biased whereas D_2 and D_3 will be reverse-biased, as shown in Fig. 4.15 c).

The behaviour of the IBFC is equivalent to that of a buck PFP cascaded with a flyback converter. As previously stated, the buck converter will draw current from the line supply only while the line voltage is higher than the bus voltage. In addition, since the flyback converter is operated in DCM too, it will behave as a resistor, R_F, as shown in (4.8). Therefore the input stage of the IBFC can be analysed by the equivalent circuit shown in Fig. 4.16.

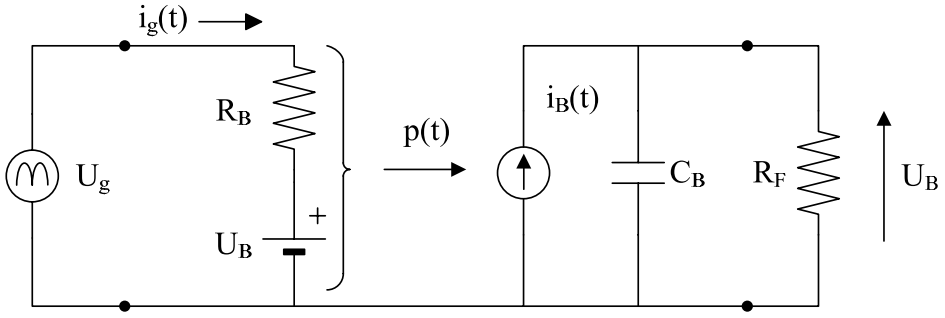

Fig. 4.16. Equivalent circuit of the IBFC input stage.

The first step to analyse the topology behaviour is the calculation of the ratio between the bus voltage and the line voltage, m. This relation is given by the dead angle of the buck converter, α, and, complementarily, to a conduction angle θ, defined as $\theta = \pi - 2\alpha$. Thus:

$$m = sin\left(\frac{\pi - \theta}{2}\right) = \frac{V_B}{V_g} \tag{4.22}$$

It must be noted that the maximum duty cycle equals the ratio m for operation in the boundary between DCM and CCM. Moreover, it has to be remarked that the maximum voltage conversion ratio is limited by the maximum dead angle, corresponding to approximately 25º, as demonstrated in Chapter 3. This dead angle yields a maximum conversion ratio $m = 0.4226$.

In a second step the inductance ratio, α_L, must be determined. This ratio is related to the voltage ratio, m, as stated in the following expression:

$$m - \frac{1}{2m\alpha_L}\left(1 - \frac{2}{\pi}\sin^{-1}(m)\right) + \frac{1}{\pi\alpha_L}\sqrt{1 - m^2} = 0 \tag{4.23}$$

which is obtained from the normalised bus current disclosed in Chapter 3, and has already been comprehensively derived in [4.6]. As can be noticed from (4.23), the voltage ratio depends only on the inductance ratio α_L, which confirms for AC operation the same results obtained for DC operation. This expression can be plotted as shown in Fig. 4.17, from which the inductance ratio can be obtained for a given voltage ratio.

Once the dead angle is set for complying with Class C requirements and accounting for a trade-off between bus voltage and ripple, as described in Chapter 3, the bus voltage ripple can be obtained for a given bus capacitor under any operation output power.

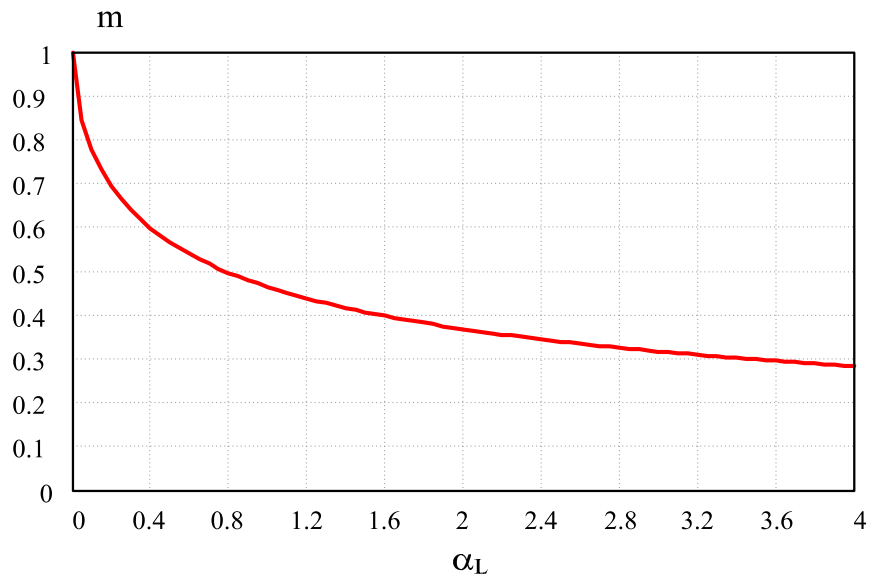

Fig. 4.17. Voltage ratio, *m*, as a function of inductance ratio, α_L.

In order to size the converter components, the maximum duty cycle has firstly to be obtained. Since both converters share the same switch, they will operate with the same duty cycle, so the maximum duty cycle will be either that of the buck or that of the flyback, whichever is lower. Thus, the buck maximum duty cycle is $d_{Buck\_max} = m$, since that is the voltage ratio for which the CCM condition is met.

Regarding the flyback maximum duty cycle, it can be obtained as a function of m from (4.15):

$$d_{Flyback\_max} = \frac{U_o}{U_o + nmU_g} \tag{4.24}$$

As can be seen, the first limiting factor when setting the duty cycle comes from the buck DCM operation, which is selected by the appropriate dead angle for fulfilling the Class C requirements. Then, the flyback turns ratio should be chosen as close as possible to the maximum duty cycle so the turns ratio is kept at the lowest level, which reduces the discharging time, as can be seen from (4.2). This assures the shortest dead times possible in the flyback inductor, while guaranteeing ZCS in the output diode, and the lowest output current peak values, which in turn allows for the efficiency enhancement and the furthest output capacitor reduction. This way, the optimal turns ratio can be obtained as:

$$n_{opt} = \frac{U_o(1 - d_{max})}{mU_g d_{max}} \tag{4.25}$$

The output power can be expressed as:

$$P_o = \frac{U_B^2}{R_F} = U_B^2 \frac{d^2}{2L_F f_s} \tag{4.26}$$

where f_s is the switching frequency, *1/T*. This way, both the flyback inductor necessary and the duty cycle swing for the load range can be obtained. Regarding the flyback inductor, accounting for the converter efficiency, η_F, and considering the LED lamp parameters:

$$L_F = \eta_F \frac{U_B^2 d^2}{2\left(V_\gamma I_o + R_D I_o^2\right) f_s} \tag{4.27}$$

Afterwards, the buck inductance can be obtained from the flyback inductance by the needed inductance ratio.

In order to determine the output current, the flyback stage of the IBFC operating from the AC line is actually supplied by the bus DC voltage, so the output current can be calculated as concluded in Section 4.2.3.1. Therefore, in the AC-DC IBFC, the output current is also given by (4.10). However, and since the bus voltage will depend only on the inductance ratio and the input voltage, expression (4.10) can be re-arranged in order to deduce the output current as a function of the line voltage. Hence:

$$I_o = -\frac{V_\gamma}{2R_D} + \sqrt{\left(\frac{V_\gamma}{2R_D}\right)^2 + \frac{m^2 {U_g}^2}{R_D}\frac{d^2 T}{2L_F}} \tag{4.28}$$

Expression (4.28) gives the output current as a function of the lamp parameters: forward voltage and resistance. Thus, it can be used to evaluate the changes of the operating point for variations in the lamp parameters due to the effect of temperature and aging.

Finally, by re-arranging (4.28), the duty cycle as a function of the lamp parameters can be obtained:

$$d = \frac{\sqrt{K_F I_O \left(I_O R_D + V_\gamma\right)}}{mU_g} \tag{4.29}$$

where mU_g can be substituted by U_B, and $K_F = 2L_F/T$.

This expression can be used to evaluate the duty cycle swing for a given lamp junction-temperature range due to the LED parameters change, as evaluated in Chapter 2.

4.5. Design example

In order to test the possibilities of the proposed converter, a universal input (90-265 V_{rms}) AC-DC converter has been designed to supply a total output power of 72 W, with a rated lamp current of 350 mA. This design has already been published in [4.16], where more detailed information is included.

4.5.1. LED lamp

The nominal power requirement for most LED streetlights ranges from 60 W to 150 W [4.17]. The load finally chosen is made of 10 DragonTape run at 350 mA. These devices consist of six LW W5SG Golden Dragon LEDs in series attached to a flexible self-adhesive tape that achieve a luminous efficiency of 21 lm/W at 350 mA [4.18]. This gives a total of 60 LEDs emitting 1500 lm at 72 W.

In order to design the power converter properly, the LED load has to be modelled. A first-approach LED model was obtained by measuring the forward voltage for several current values in steps of 50 mA approximately. Those current levels were applied to the load only during few seconds so that heating effects on the threshold voltage were made negligible. After that, the devices were allowed to cool down again. The empirical results extracted from the test are

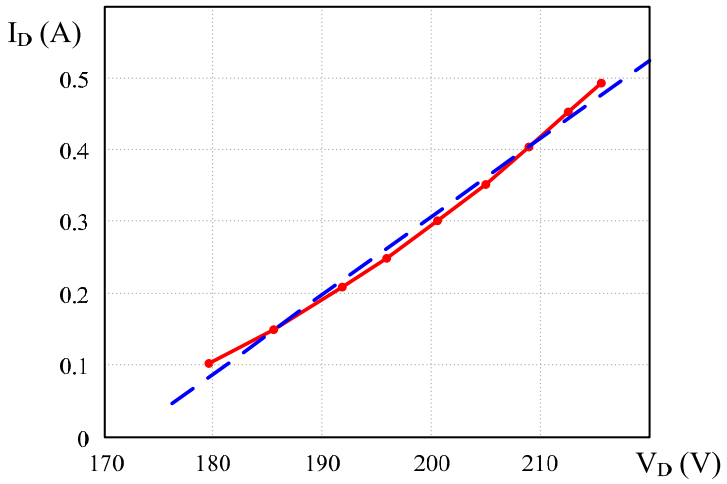

Fig. 4.18. Forward current I_D and forward voltage V_D values obtained from the LED lamp built and tested in the lab (dotted line) and least-square-fitted linear model (dashed line).

shown in Fig. 4.18, together with the linear model interpolated by the least squares method. Further information is provided in [4.16].

4.5.2. Converter design

In order to minimise the passive components, a 100 kHz switching frequency was selected.

The conduction angle for the buck converter was set at 130º, so that the European requirements for Class C devices can be fulfilled. Thus, the voltage ratio is limited to $m = 0.423$, which also equals the maximum allowed duty cycle to assure DCM operation. Additionally, this voltage ratio leads to bus voltages ranging from 53 V up to 158 V, the bus nominal voltage being 124 V. The bus capacitor was designed for a maximum 10% voltage ripple at 90 V_{rms} input voltage, leading to a 1.3% bus-voltage ripple under the nominal operation conditions. The flyback inductor was built using the interleaving technique in order to minimise the leakage inductance. A value as low as 0.75 µH was obtained for the leakage inductance, which represents less than 4% of the magnetizing inductance. In order to minimise the copper losses, litz wires were used. The selected strands and diameters were 25x0.2 mm in the primary and 15x0.2 mm in the secondary. The semiconductor devices were selected according to their voltage and current stresses, being shown in Table IV.IV.

TABLE IV.IV
COMPONENTS OF THE LABORATORY PROTOTYPE

Component	Value
L_B	L=26.1 µH EFD25 N87; N=32
L_F	L=19.3 µH ETD29 F44; n=4; N1=10; N2=40
M_1	SPW17N80C2
D_1	STTH512
D_6	MUR860
D_7	MUR860
D_8	MUR840
C_B	570 µF/250 V
C_o	1.5 µF/250 V

Fig. 4.19 shows the duty cycle as a function of the bus voltage for a fixed junction temperature of 25 ºC.

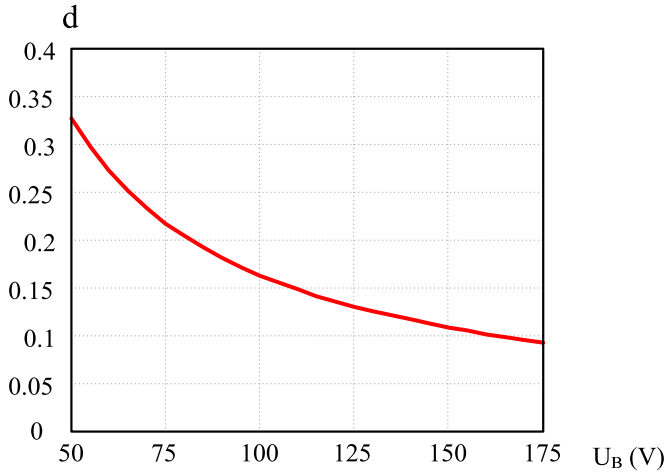

Fig. 4.19. Duty cycle, d, for an output current of 350 mA as a function of bulk capacitor voltage, U_B.

Also, the duty cycle is affected by changes in lamp parameters due to temperature variations and aging. From the manufacturer data, a k = -4 mV/ºC temperature coefficient is obtained [4.18]. Thus, using equation (4.29), the range of duty cycle can be depicted as shown in Fig. 4.20 for an output current of 350 mA and a junction temperature ranging from -40 ºC to 125 ºC.

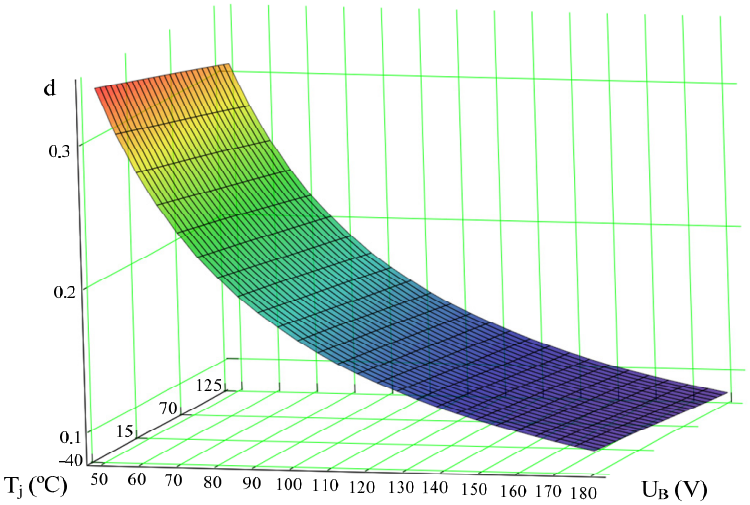

Fig. 4.20. Duty cycle, d, for an output current of 350 mA as a function of bulk capacitor voltage, U_B, and junction temperature, T_j.

As can be seen, an increase of the temperature produces a decrease of the duty cycle, thus assuring DCM operation for the entire operation range.

4.5.3. Converter modelling

The averaging technique can easily be employed to model the output stage of the proposed converter. The IBFC flyback will be modelled considering that the bus voltage is constant due to the large bus capacitor that is used. Therefore, the dynamic model of the IBFC can be reduced to only the DCM flyback dynamic model, so the same circuit that has been studied in

the illustrative example included in Chapter 2 can be used for determining the averaged values of current and voltages. Then, by applying the Kirchoff's Current Law (KCL) to that equivalent circuit:

$$\langle i_C \rangle(t) + \langle i_O \rangle(t) = \langle i_{DC} \rangle(t) \tag{4.30}$$

where the symbol ⟨ ⟩ is used to denote averaged values of the different variables.

Using the average output current, which is the Full DCM diode D_4 current shown in Table IV.2 in (4.30), the following expression can be obtained:

$$C_O \frac{d}{dt}\langle u_O \rangle + \frac{\langle u_O \rangle - V_\gamma}{R_D} = \frac{\langle u_B \rangle^2 \langle d \rangle^2}{2L_F f_s \langle u_O \rangle} \tag{4.31}$$

Since the variable of interest from the control point of view is the output current, it is of interest to relate output voltage and current using the load behavior as follows:

$$\langle u_O \rangle = V_\gamma + R_D \langle i_O \rangle \tag{4.32}$$

Substituting (4.32) in (4.31) yields:

$$R_D C_O \frac{d}{dt}\langle i_O \rangle + \langle i_O \rangle = \frac{\langle u_B \rangle^2 \langle d \rangle^2}{2L_F f_s \left(V_\gamma + R_D \langle i_O \rangle\right)} \tag{4.33}$$

Perturbing and linearising (4.33) for the transfer function of interest – output current versus duty cycle, and applying the Laplace transform gives:

$$sR_D C_O i_O(s) + i_O(s) = \frac{2U_B^2 D}{L_F f_s U_O} d(s) - \frac{U_B^2 D^2 R_D}{L_F f_s U_O^2} i_O(s) \tag{4.34}$$

By re-arranging (4.34) and solving for the duty cycle, the following expression is finally obtained for the output-current to duty-cycle transfer function:

$$G(s) = \frac{i_O(s)}{d(s)} = \frac{2\frac{I_O}{dC_O R_D}}{s + \frac{U_O + I_O R_D}{U_O R_D C_O}} = \frac{G_{d0}}{1 + s\omega_{dp}} \tag{4.35}$$

where:

$$G_{d0} = \frac{2I_O U_O}{d(U_O + I_O R_D)} \qquad \omega_{dp} = \frac{U_O + I_O R_D}{U_O R_D C_O} \tag{4.36}$$

Since the design parameters are I_o = 0.35 A; U_o = 200.605 V; d = 0.119; C_o = 1.5 µF; and R_D = 87.151 Ω, the following values are obtained: G_{d0} = 5.11 A, ω_{dp} = 8.81 krad/s (1.4 kHz).

It shall be noted that the series equivalent resistance (ESR) of the output capacitor has been neglected in this model since the output capacitor needed for this converter is very small (1.5 µF). This can be done because a non-electrolytic capacitor can then be used, which provides very low ESR resistance. The zero generated by the ESR would be far beyond the frequencies of interest.

4.5.3.1. Controller design

Dimming is of great interest in many applications. In this prototype, the regulation loop was designed accounting for holding eventual dimming PWM operation. Moreover, a first-order behaviour was pursued in order to avoid electrical stress in the LED load caused by overshooting. The current-control fixed-frequency regulator was designed using the SISOtool toolbox from MATLAB. Expression (4.37) gives the transfer function of the modified PI regulator employed in the prototype.

$$C(s) = C_R \cdot \frac{s + s_z}{s \cdot (s + s_p)} \tag{4.37}$$

where:

$$C_{CO} = \frac{g_m}{C_2} \qquad s_{cz} = \frac{1}{RC_1} \qquad s_p = \frac{1}{R\,\dfrac{C_1 C_2}{C_1 + C_2}} \tag{4.38}$$

The regulator zero was located to compensate the effect of the pole in the converter open-loop transfer function and an additional pole was used to provide sufficient bandwidth and stability to the closed-loop operation. The regulator was implemented using the OTA included in LM3524 IC, as shown in Fig. 4.21.

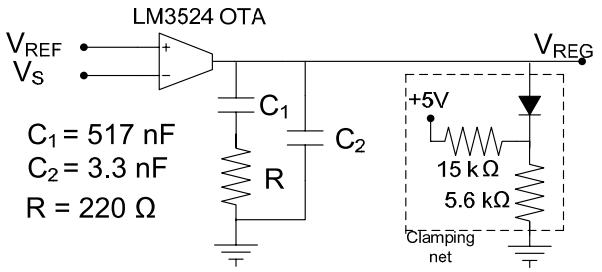

Fig. 4.21. Control loop circuit using the OTA included in the LM3524 IC and soft-start clamping net.

It shall be noted that high currents through the rectifier diodes, inductors, the MOSFET itself or even the LED load could be reached during the start up period. This overcurrent might also be caused by an underdamped response of the converter at the lowest line voltages or under operation conditions different to the designed point which would cause the highest duty cycles. Therefore, the duty cycle is limited before reaching excessive values by a clamping net in order to avoid the risk of electrical failure during the start-up period. A voltage divider and a diode are added, so that the controller output is clamped to a maximum value, thus limiting the duty cycle.

In order to sense the output current, a 1 Ω resistor was placed in series with the lamp. This value was chosen as a trade-off between low power dissipation and good Signal-to-Noise Ratio SNR. Additionally, a voltage amplifier with a third order low-pass response was implemented using an LM358 operational amplifier (OA). A 10 kHz cut-off frequency was selected for the filter so that a high noise rejection can be obtained while the open-loop dynamics of the converter remains practically unaffected. Since the ramp wave generated by the LM3524 ranges from 0.6 V to 3.2 V, and taking into account that the OTA common mode voltage must be higher than 1.5 V, the reference value was set to 3.0 V for the rated LED lamp current of 350 mA. For this reference value, the DC gain of the third order filter was adjusted to 8.8.

Fig. 4.22 shows the final open loop Bode diagram, considering the current sensor and the controller. The Bode diagram for closed loop is depicted in Fig. 4.23.

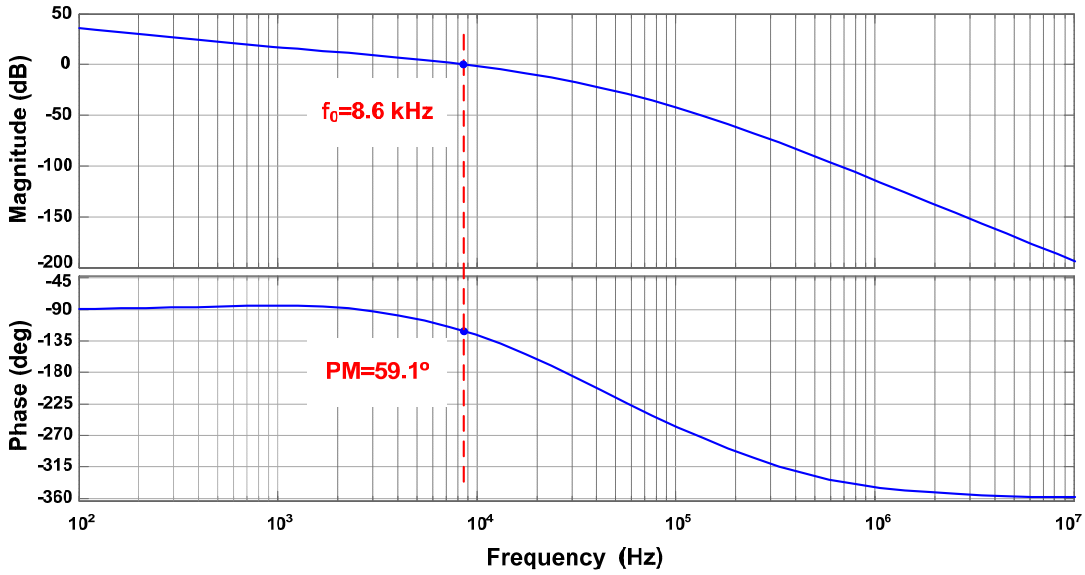

Fig. 4.22. Full-DCM IBFC open-loop Bode diagram.

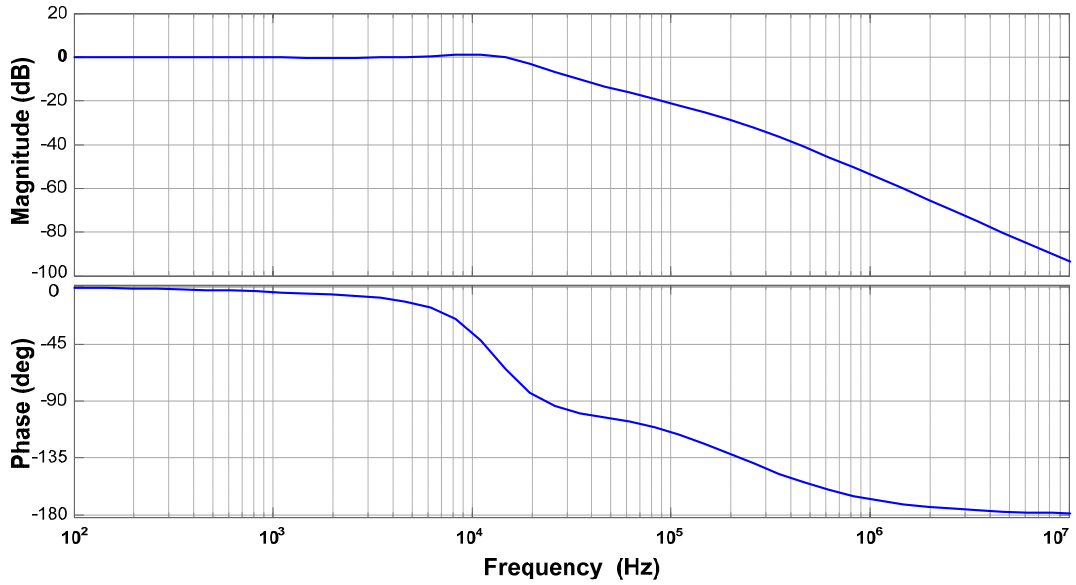

Fig. 4.23. Full-DCM IBFC closed-loop Bode diagram.

As can be seen from Fig. 4.22 and Fig. 4.23, a good trade-off between stability and fast response was achieved as the phase margin was set to approximately 59º, with a barely underdamped response. Provided that the bus-voltage ripple is negligible under nominal operation, it can be assumed that such a fast control loop will not introduce 2nd harmonic distortion in the input current due to the twice line-frequency ripple that results from the processing of energy at 50 Hz.

4.5.4. Experimental Results

The electric diagram of the complete prototype is shown in Fig. 4.24. An EMI filter was included at the input with the following values: C_i = 100 nF, L_1 = 2.34 mH, L_2 = 2.34 mH and C_o = 220 nF. The prototype was tested under four input voltages: the lowest (90 V_{rms}), the highest (265 V_{rms}), at intermediate input voltage (150 V_{rms}) and the European nominal input voltage (230 V_{rms}). The experimental results obtained are summarized in Table IV.V where U_g is the input voltage, I_o is the output current, U_o is the output voltage, P_o is the output power, P_1 is the input power, PF is the power factor, η is the converter efficiency, and THD_1 is the input current total harmonic distortion.

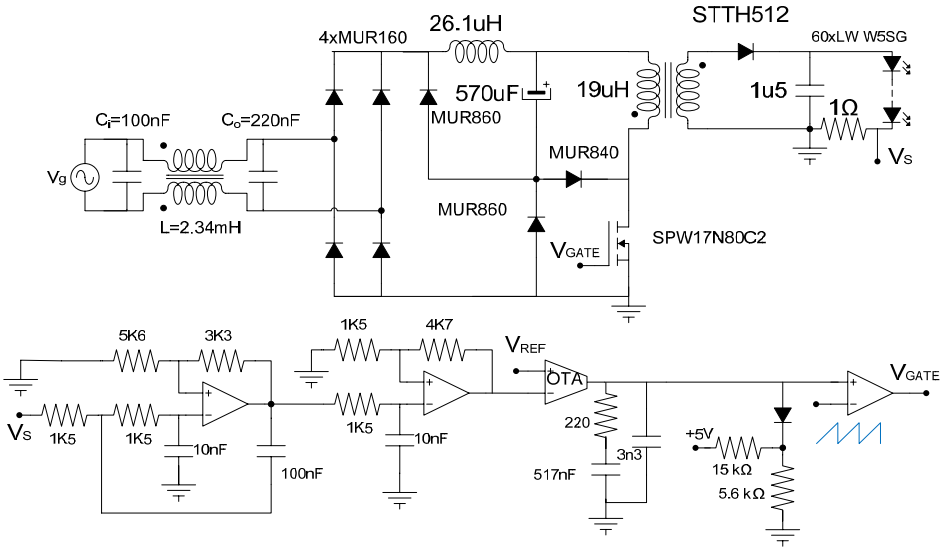

Fig. 4.24. Entire electric diagram of the developed prototype.

Fig. 4.25 shows the line voltage and current for different line voltage levels. The measured conduction angle is similar to that obtained from the theoretical design and simulations and the converter operates in DCM for the entire line voltage range.

The harmonics contained in the input current are depicted in Fig. 4.26 for the nominal operation point, along with the mask for complying with IEC Class C regulations.

TABLE IV.V
EXPERIMENTAL RESULTS AT T_B=35ºC

U_g (V_{rms})	90	150	230	265
I_o (A)	0.351	0.353	0.353	0.354
U_o (V)	202.6	202.2	203.9	202.4
P_o (W)	71.2	71.5	72.1	71.7
P_1 (W)	91.1	89.6	92.6	93.8
PF	0.948	0.950	0.957	0.953
η (%)	78.2	79.8	78.2	76.5
THD_1 (%)	32.5	31.0	27.5	29.3

Fig. 4.27 shows the detailed waveforms of the MOSFET drain-source voltage and current stresses for two different operating points. The highest peak voltage value reaches less than 650 V. The highest peak current value is less than 800 mA, and the rms value for input current is always lower than 300 mA.

Fig. 4.28 illustrates line and bus voltage. The DC level and ripple voltage are similar to the values expected from the theoretical analysis. The maximum ripple is approximately 10%.

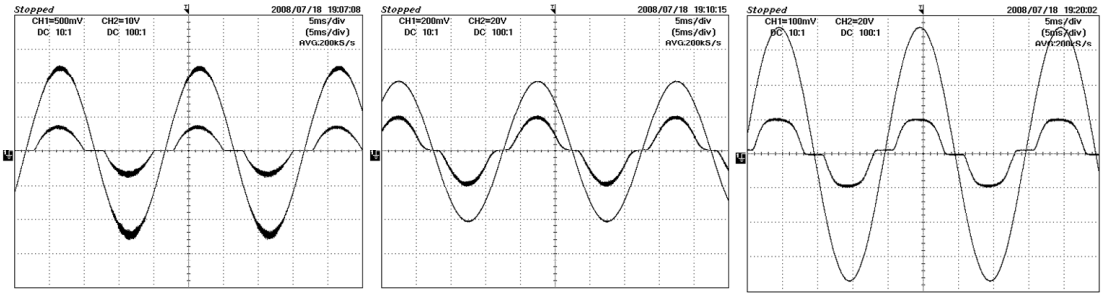

Fig. 4.25. Line current and voltage at different line voltages. Left: 90 V_{rms}, 50 V/div, 2.5 A/div; centre: 150 V_{rms}, 100 V/div, 1 A/div; right: 265 V_{rms}, 100 V/div, 0.5 A/div. Horizontal scales: 5 ms/div.

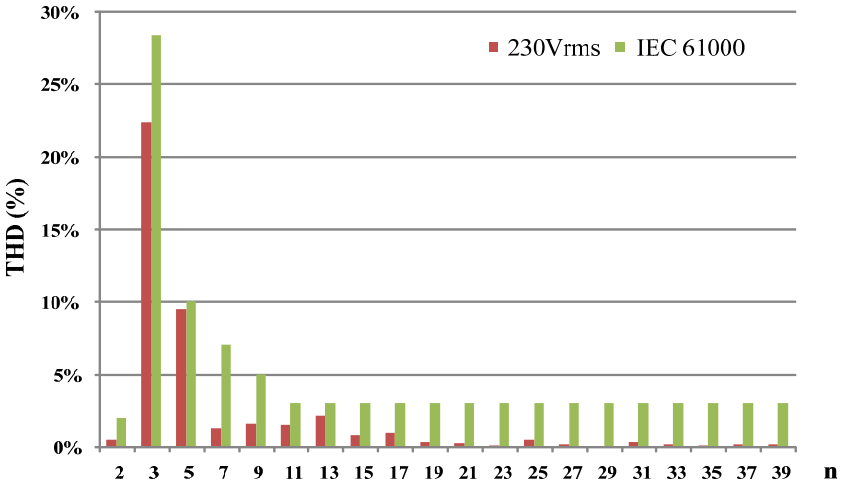

Fig. 4.26. Harmonic content of the input current, showing the results obtained and the limits stated in the IEC 61000-3-2 Class C Regulations.

Fig. 4.29 depicts the efficiency as a function of the input voltage. A maximum around 80% is obtained at 150 V_{rms} input voltage, whereas the minimum is always above 75%. These are reasonable figures of merit taking into account that the converter has been designed for operation under universal input-voltage range.

4.6. Summary and conclusions

In this Chapter, a two-stage topology proposed for performing PFC and supplying LED lamps in the range of 50 – 100 W from the AC mains supply has been introduced. However, due to the versatility and satisfactory trade-off between cost, size and performance that IPCs feature, an IPC based on the two-stage architecture based on a cascaded buck-flyback converter, the IBFC, has been proposed for this work in order to reduce the BoM and the cost of the converter. Thus, the integration technique has firstly been introduced, depicting the integration process of the buck-flyback converter intended for LED lighting.

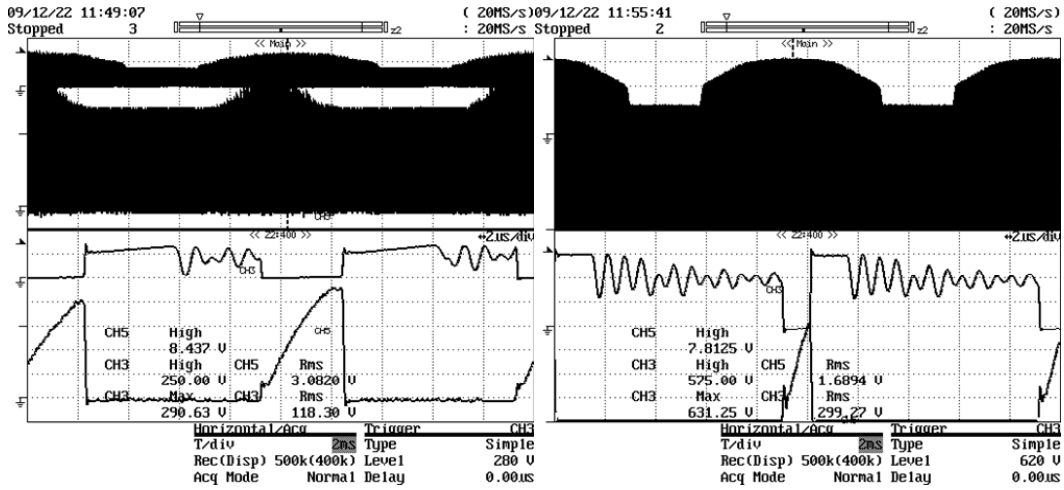

Fig. 4.27. Waveforms of MOSFET drain-source voltage (higher) and MOSFET current (lower). Left: minimum input voltage: 90 V_{rms}. Right: maximum input voltage: 265 V_{rms}. Vertical scale: 200 V/div, 0.2 A/div. Horizontal scale: 2 ms/div.: Bottom: zoom of the signals above. Horizontal scale: 2 µs/div.

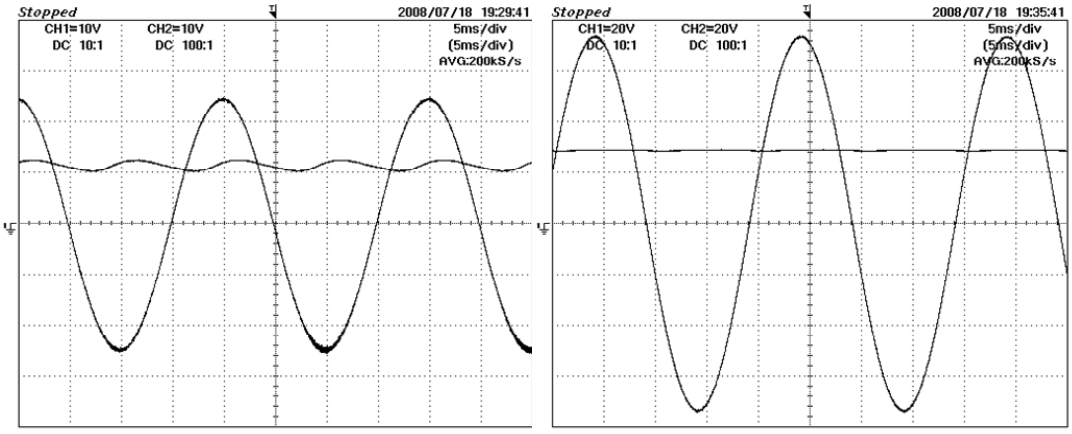

Fig. 4.28. Line voltage and bulk capacitor voltage. Left: 90 V_{rms} input, 50 V/div for both traces. Right: 265 V_{rms} input, 100 V/div for both traces. Horiz. scale: 5 ms/div.

Afterwards, a deep and comprehensive study about the static operation of the IBFC has been developed, analysing the two operation modes taken into account: Full DCM and DCM/CCM modes. Then, both operation modes were compared in order to determine which one is more advantageous for supplying an LED lamp from the AC mains. Thus, the ripple-gain factor has been analysed for both operation modes, concluding that the lower gain of the DCM operation mode leads to a higher output-current ripple attenuation. In addition, the Full DCM mode is characterised by a bus voltage that depends only on the inductance ratio and the line voltage, as opposed to the DCM/CCM mode, where it depends on several parameters, including the output power and the LED load characteristics. Hence, it can be concluded that the Full DCM operation is preferable to the DCM/CCM as the output-current ripple will be lower for the same output power, lamp parameters and bus capacitor. This also allows for the avoidance of electrolytic capacitors, which endanger the life-span of the converter.

The operation of the Full-DCM IBFC has then been analysed for supplying an LED load from the AC mains, highlighting the most important parameters calculation. After that, a design example has been proposed in order to check the feasibility of the IBFC for running a street lighting-like 70 W LED load as a low-cost PFC solution under universal input-voltage range.

In this example, a 70 W LED lamp has been built and modelled, also modelling the converter and designing a modified PI controller. The efforts were focused on the converter stability, dynamic response, and capability for eventually performing PWM dimming.

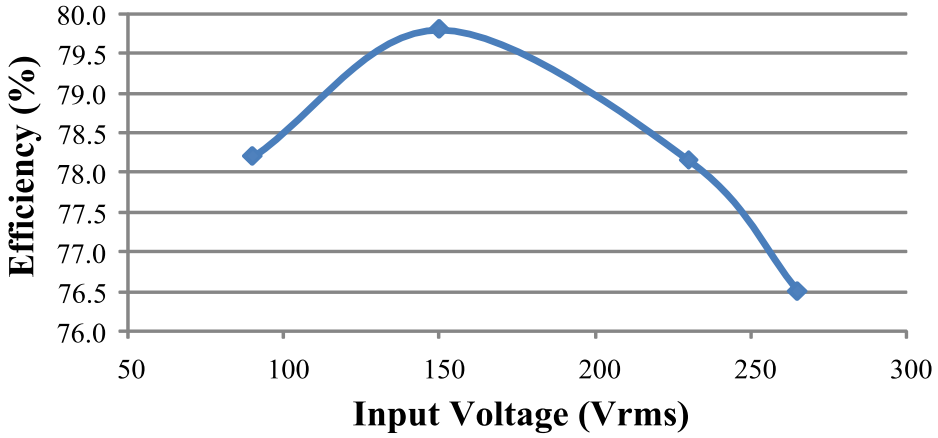

Fig. 4.29. Efficiency as a function of the input line voltage.

The experimental results showed a good low-frequency harmonic reduction, complying with IEC 61000-3-2:2005 Class C, the efficiency ranging between 75% and 80%. This is considered adequate, taking into account that the converter was designed to operate under universal input range and it is obtained through the integration on an OV-cell.

The lower cost of this solution relies on the elimination of one of the transistors of the two-stage equivalent architecture together with an extra control loop. Moreover, the operation in DCM also allows for the use of simpler control circuits, further reducing the cost. Moreover, since the lowest bus voltage achievable with the application example drops to around 60 V while still operating in DCM, this converter could easily be modified in order to operate from an UPS unit, since only few modifications would be needed besides the connection of the UPS unit to the converter DC bus.

As a conclusion, it can be considered that the Full-DCM IBFC proposed in this Chapter results in a versatile LED driver, suitable for many lighting applications.

4.7. References

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Chapter 5

Modelling of the Integrated Buck-Flyback Converter

In this chapter, the modelling of the IBFC is arisen in order to study its large-signal behaviour and small-signal dynamics. Closed-loop operation introduces control of a desired variable in order to prevent deviations from the established reference regardless of the input voltage, perturbations, or changes in the operation point, among many others. Moreover, LED drivers usually operate in closed-loop in order to achieve a proper regulation of the current through the LED due to their characteristics as a power load and their dependency on operation temperature.

For the sake of simplicity, the IBFC will be dynamically studied employing its equivalent cascaded buck-flyback converter. Thus, two large-signal approaches will be considered: i) the Loss-Free Resistor (LFR) approach, which considers the converter as a two-port device. In this approach, the input port is modelled as a resistor and the output port as a current source; ii) the averaged model described in [5.15]. This model considers each switch, either diodes or transistors, as current sources, and will be applied in order to obtain an alternative large-signal model. Both large-signal models will be tested by PSIM simulations and the results will be compared to the simulation results of the actual IBFC converter for off-line operation.

After the large-signal models are tested, the small-signal model will be obtained from the averaged circuit. Moreover, the whole converter will be studied and modelled in order to verify the interaction between the buck PFP and the flyback LED driver, obtaining the complete set of small-signal transfer functions for determining the input and output currents. Once the small-signal analysis is done, it will be applied to the IBFC described in Chapter 4, obtaining some theoretical transfer functions of interest, and comparing to the PSIM simulation results

5.1. Introduction

Electronic lighting has lately gained a prominent role in the past years due to the advantages of electronic ballasts over their magnetic and passive counterparts. This issue has been notorious in the case of gas discharge lamps, where the introduction of electronic ballasts allowed for the incorporation of advanced features, such as light control – namely dimming. With regard to solid-state lighting, switched-mode (SM) electronic drivers are widely used due to the LEDs characteristics as power loads. This way, high power factor (HPF) AC-DC converters are employed, which operate in closed loop in order to regulate the output current, in several applications, such as street, outdoor, indoor or automotive lighting, among many others. Therefore, it is essential to model the power stage properly both at large- and small-signal in order to provide the designer with simple, but complete models to be employed in the design, simulation and optimisation of a lighting fixture.

Several modelling methodologies have been proposed in the literature for different conduction modes, as well as for control strategies, such as free-wheeling current, fixed-frequency, current programming, etc. [5.1]-[5.13], most of them using the state-space averaging technique, averaged switches, DC transformer circuits, or extracting and averaging the differential equations that describe the converter operation.

This chapter tackles the modelling of the AC-DC HPF-DCM IBFC converter by using two different approaches: (i) by one side, the loss-free resistor (LFR) model [5.14] will be deduced for large-signal fast simulations, and (ii) employing an averaging process consisting in the substitution of the switches in the circuit by their equivalent: either a current or a voltage source as presented in [5.15] for modelling DC-DC converters. The latter also allows the designer to obtain large-signal averaged equivalent circuits to perform fast simulations, whereas linearisation of the large-signal model yields the small-signal model that can be employed to determine any small-signal converter response and therefore allows for a proper design of the feedback loop.

First, the large-signal models using the LFR approximation will be calculated for the buck PFP and the cascaded buck-boost or flyback converter. As in Chapter 4, the analysis given here will be applicable to either a buck-boost or a flyback converter. The results obtained from the large-signal equivalent circuit will be compared with simulation results of the IBFC in PSIM in order to check the accuracy of the proposed large-signal model.

Second, the large-signal models of both the buck PFP and the cascaded flyback converter will be linearised in order to obtain the small-signal IBFC equivalent circuit that can be used to determine the dynamic response of the converter. The modelling methodology will be applied to the cascaded buck-flyback converter, provided that it is equivalent to that of the IBFC, featuring a fixed-frequency, constant duty cycle quasi-static operation.

Finally, the large- and small-signal equivalent circuits will be compared to the IBFC results through PSIM and MATLAB simulations.

5.2. IBFC low-frequency, large-signal averaged model: loss-free resistor

As previously disclosed in Chapters 3 and 4, the preferred IBFC operation mode is Full DCM due to its advantages, namely lower ripple-transfer gain, higher control easiness due to the situation of the RHP zero at frequencies beyond the switching frequency, and inherent behaviour as voltage follower. Thus, the LFR arises as an extremely simple way to study the large-signal behaviour of each converter separately and the cascaded two-stage topology in

order to compare the obtained results with the integrated-topology simulations. Due to the inherent voltage-follower behaviour of the DCM buck and flyback converters, the LFR model is very handy to use. This model considers the converter input as a resistor, drawing a current that is proportional and in phase to the line supply. In addition, it is assumed that the input power is completely transferred to the output, so $P_o = P_i$, what is referred to as *POPI concept*, [5.14], the load being supplied by a power source. Hence, an ideal resistor is considered with regard to the input port. As previously disclosed in Chapter 4, the equivalent input resistor of buck and flyback converters, R_B and R_F, respectively, is:

$$R_B = \frac{2L_B}{d^2 T_s} \qquad R_F = \frac{2L_F}{d^2 T_s} \tag{5.1}$$

where L_B and L_F are the buck and flyback inductors, respectively, d is the converter duty cycle, and T_s is the switching time. However, it has to be taken into account that the input current in the buck converter is also affected by the bus voltage, the buck equivalent resistance being defined from the input to the bus voltages. With regard to the output ports, the inductor and the output diode currents could be modelled as a current source, provided that both converters operate in DCM. The buck and flyback output currents, i_B and i_F, respectively, corresponding to the buck inductor and the flyback output diode currents are reminded:

$$i_B = \frac{u_g(u_g - u_B)}{u_B}\frac{d^2 T_s}{2L_B} \qquad i_F = \frac{{u_B}^2}{u_o}\frac{d^2 T_s}{2L_F} \tag{5.2}$$

where u_g, u_B, and u_o are the input (line) voltage, the buck output (bus) voltage, and the flyback output voltage, respectively, and i_F is referred to the primary side of the flyback converter. Expression (5.2) makes use of d, u_g, u_B, and u_o instead of D, U_g, U_B, and U_o as these parameters are expected to be time-variant.

The LFR model of the buck and flyback converter is sketched in Fig. 5.1, accounting for the capacitor equivalent series resistor (ESR). Input and output voltages in Fig. 5.1 are considered as if the converters where cascaded. Thus, the input voltage of the buck converter is the line voltage, whereas that of the flyback converter is the bus voltage, which in turn is the output voltage of the buck converter. As the LFR model considers an output power source, this can easily be achieved by setting the output current as the input power divided by the output voltage. Indeed, the large-signal models in Fig. 5.1 lead to the determination of the steady-state conversion ratio. Thus, the input power of the buck converter, p_B, can be calculated as:

$$p_B = u_g i_g = u_g(u_g - u_B)\frac{1}{R_B} \tag{5.3}$$

where i_g is the buck input current. With regard to the flyback converter power, p_F, this would lead to:

$$p_F = u_B i_B = \frac{u_B^2}{R_F} \tag{5.4}$$

Assuming $P_o = P_i$, the output current can be expressed as the output power divided by the output voltage. Thus, for the buck converter:

$$i_B = \frac{p_g}{u_B} = u_g\frac{(u_g - u_B)}{u_B}\frac{1}{R_B} \tag{5.5}$$

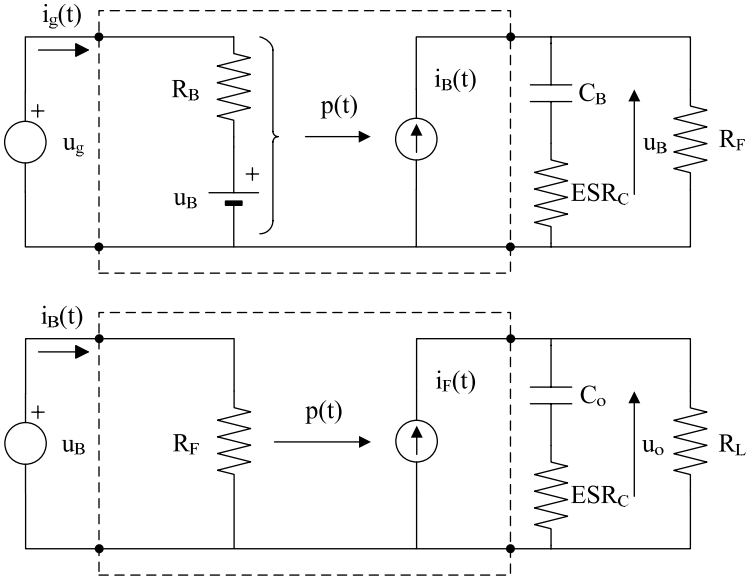

Fig. 5.1. LFR averaged model of the buck (top) and flyback (bottom) converter.

whereas for the flyback converter, as referred to the primary side:

$$ni_F = \frac{p_F}{u_o/_n} = n\frac{u_B^2}{u_o}\frac{1}{R_F} \longrightarrow i_F = \frac{u_B^2}{u_o}\frac{1}{R_F} \tag{5.6}$$

which agree with (5.2) and with the results obtained in Chapter 4.

Since only the averaged variables are considered, and the dynamic effects of the inductors are disregarded and assimilated to the input-port resistance and output-port power source, this model is valid only for steady-state and low-frequency operation, yet very powerful in order to determine the voltage and current ripples in PFC converters. In addition, the accuracy regarding the bus-voltage ripple is also improved by considering the capacitor ESR. This model would also allow for the calculation of the small-signal analysis through differentiation and linearisation of the output current source and by applying it to the RC net composed by the output capacitor and the load. This yields to the simplified dynamic model obtained in Section 4.5.3 in Chapter 4. However, the accuracy is only assured for low-frequency perturbations. Nevertheless, these reduced-order models are very interesting in order to perform fast simulations in simulation software such as PSIM or Simulink when the performance as a PFC is checked. Fig. 5.2 shows the averaged electrical model of ideal buck and flyback converters,

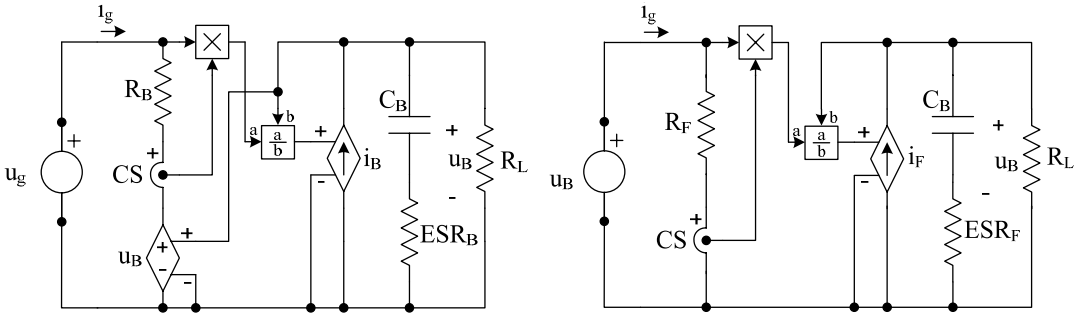

Fig. 5.2. LFR averaged model of the buck converter (left) and flyback (right) converters for simulation in PSIM.

which can also be used to perform the simulation of the cascaded converter performing PFC and supplying the LED load. The buck and flyback ideal converters are modelled by the resistance R_B and R_F, respectively, at the input. The input current is sensed using the current sensor *CS*, and then multiplied by the input voltage in order to obtain the instantaneous input power, p_g. This power is divided by the instantaneous output voltage, so that the instantaneous output current, i_B and i_F, respectively, is obtained. It has to be noted that in the case of the buck converter, the input current depends on the output (bus) voltage. This is modelled by a voltage-controlled voltage source equal to the instantaneous output (bus) voltage, connected in series with the input resistance. This current is finally generated by using a voltage-controlled current source. Note that resistance R_L can represent either a load, such as the LED lamp, or the equivalent input resistance of the second stage. In addition, the corresponding equivalent series resistance (ESR) of the buck and flyback capacitors, ESR_B and ESR_F respectively, is also included.

This large-signal model straightforwardly allows for the calculation of the output voltage and current if the buck output voltage (bus voltage) is considered small enough so that the bus voltage can be approximated by its mean value when calculating the output current. However, when this condition is not fulfilled, the precision of the obtained bus voltage ripple will decrease. However, the averaged circuits presented in Fig. 5.2 are valid for high output-voltage ripples and can be used to investigate these cases by computer simulation. Simulations performed by using these circuits will be several orders of magnitude faster than simulating the actual switched PFC converters. These circuits can also be combined in order to simulate the complete IBFC. The cascaded LFR large-signal model of the IBFC as introduced in Chapter 4 is shown in Fig. 5.3, where the resistive load is replaced by the actual LED load. The large-signal model parameters can be calculated from (5.1), (5.5) and (5.6) after substituting the values provided in Chapter 4.

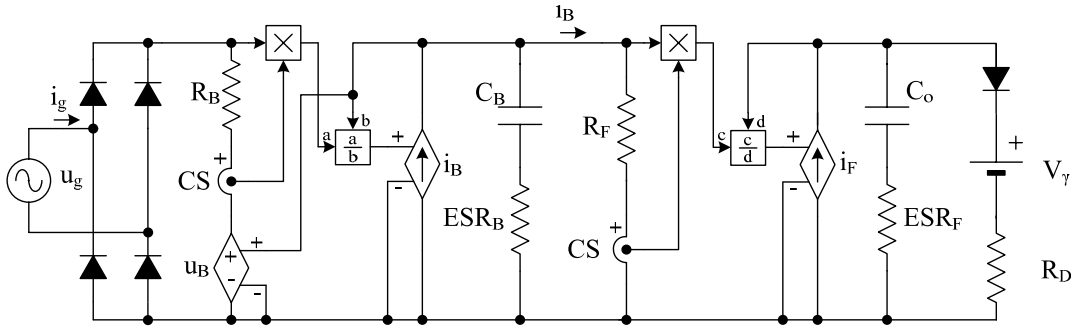

Fig. 5.3. LFR averaged model of the cascaded buck-flyback converter for simulation in PSIM.

With the values provided in Chapter 4, the buck and flyback input equivalent resistors would be approximately 368.62 Ω and 272.58 Ω, respectively. The IBFC and its large-signal model were simulated in PSIM. The results for output current, input current, and bus voltage are shown in Fig. 5.4. The capacitor ESRs are disregarded for the sake of simplicity, as the purpose of this simulation is only to validate the averaged model

As can be seen from Fig. 5.4, the large-signal model is highly accurate provided that the actual converter keeps the DCM condition. Otherwise, the reliability of the model is lost, as can be seen for the first few cycles, where the converter enters the CCM and the model cannot predict the average input current and shows a higher error for the bus voltage. With regard to the error seen during the first cycle, it would be caused by the converter CCM initial operation. In addition, this LFR model is applicable to the IBFC converter although derived from the

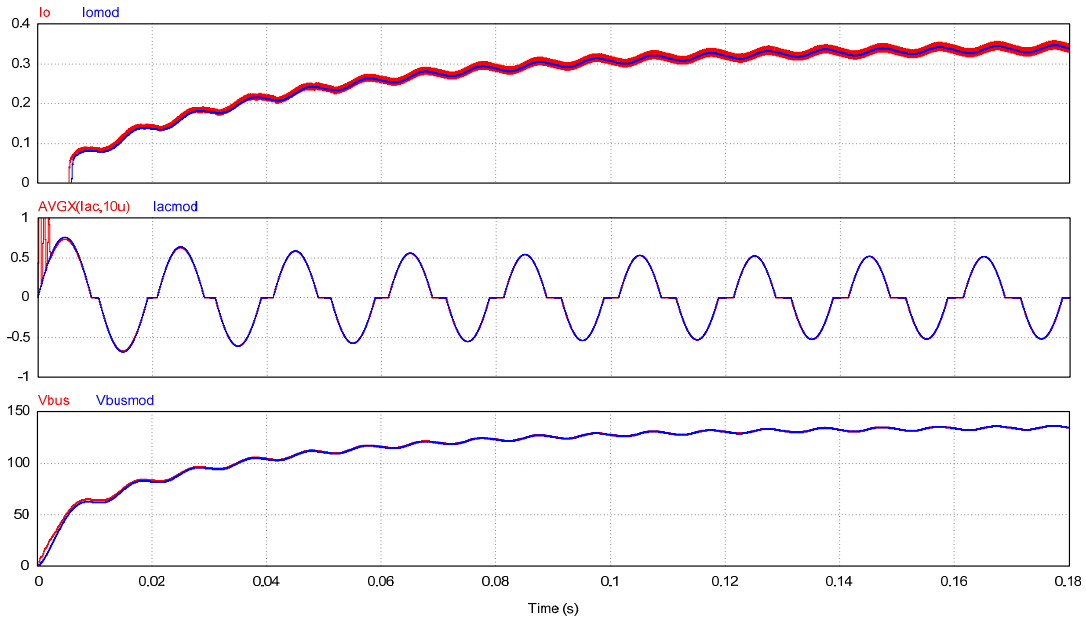

Fig. 5.4. PSIM simulation results for output current (top trace), average input current (middle trace) and bus voltage (bottom trace) for the cascaded buck-flyback converter LFR averaged model (blue lines) and the IBFC (red lines).

cascaded buck-flyback converter, as their behaviours are equivalent, provided that the input port for both topologies is that of the buck converter and the output port is that of the flyback converter.

Since the application of this large-signal model is straightforward and very useful for determining the PFC behaviour, it will be used for evaluating the performance of the IBFC as an HPF LED driver in the optimisation section of the IBFC that will be included in Chapter 7. Nevertheless, more comprehensive models are required in order to gain a deeper insight on the dynamic behaviour of the converter and to design a closed-loop controller, as will be presented in subsequent sections.

5.3. IBFC averaged model

The modelling process described in this Section is based on the procedure presented in [5.15] for modelling DC-DC converters. All the modelling process is based on equivalent circuits that are very easy to obtain from the basic converter operation. In addition, the inclusion of parasitic resistances, such as the capacitor ESR or the on-resistance of MOSFETs, R_{DSon}, results in a trivial task. A large-signal averaged equivalent circuit that can be used to perform fast simulations is thus obtained this way. The circuit is then linearised to achieve a small-signal equivalent circuit that can be employed to determine any small-signal response of the converter. The modelling methodology will be derived for the buck and flyback converters separately, prior to combining their transfer function in order to get the dynamic behaviour of the cascaded converter. In addition, this procedure can be applied both to averaging at the switching frequency or at the twice the line frequency. In the first case, the model is strictly valid up to half the switching frequency, although the high-frequency zero caused by the inductor dynamics and neglected in this averaged model introduces a phase lag, so the model could cause a loss of accuracy from around one third of the switching frequency [5.16]. In the second case, only the DC values are considered, which is useful in order to predict the behaviour of slow converters such as HPF IPCs and to design a proper feedback loop for performing PFC [5.17].

5.3.1. Large-signal averaged model

This procedure is based on the averaging of the currents and voltages across the diodes and transistors of the converter. Some simplifications will be made, as in [5.15], [5.18]. Thus, the transistor and diode output capacitances will be neglected, the transistor on-resistance will be considered constant, and the diode will be simplified by the threshold voltage. Finally, passive components will be considered linear, time-invariant and frequency-independent, accounting only for the parasitic resistances. The switching frequency is much higher than the line frequency; therefore, a quasi-static study can be developed. The large-signal averaged model of the buck and flyback converters is shown in Fig. 5.5.

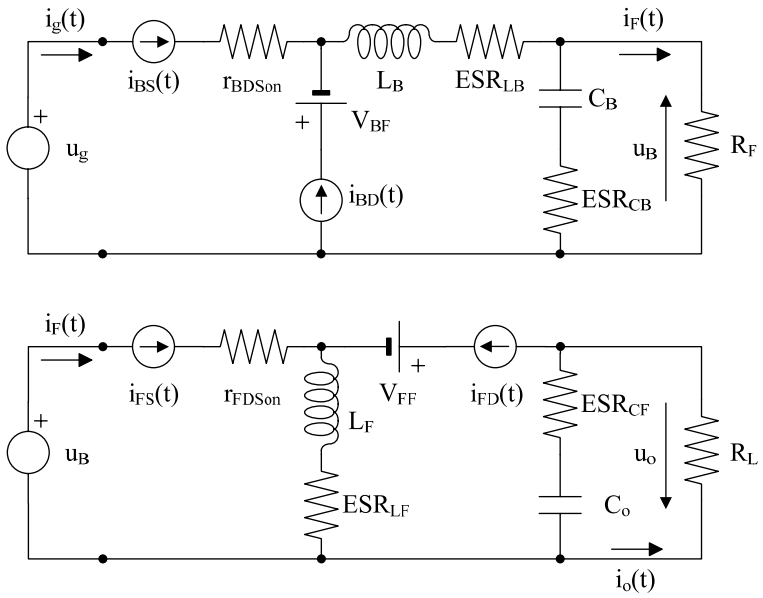

Fig. 5.5. Large-signal averaged model of the buck (top) and flyback (bottom) converters by the method described in [5.15].

Fig. 5.5 shows the averaged models for the buck and flyback transistor currents, $i_{BS}(t)$ and $i_{FS}(t)$, and diode currents, $i_{BD}(t)$ and $i_{FD}(t)$, respectively. Parasitic effects are also considered, accounting for the buck and flyback transistor on resistances, r_{BDSon} and r_{FDSon}; inductor series resistances, ESR_{LB} and ESR_{LF}; and capacitor series resistance, ESR_{CB} and ESR_{CF}, respectively. However, the IBFC has undergone a topological transformation by the substitution of one transistor with two diodes, although its operation is equivalent to a buck-flyback cascaded converter. Hence, in order the cascaded buck-flyback large-signal model to be equivalent to the IBFC operation, the transistor on-resistance losses shall be neglected, the inductor and capacitor series resistances remaining. Thus, the cascaded buck-flyback equivalent model is depicted in Fig. 5.6.

The current supplied by the current sources in the models shown in Fig. 5.5 and Fig. 5.6 are those corresponding to regular buck and flyback converters, namely:

$$
\begin{aligned}
i_{BS}(t) &= \big(u_g(t) - u_B(t)\big)\frac{1}{R_B} \\
i_{BD}(t) &= \frac{\big(u_g(t) - u_B(t)\big)^2}{u_B(t)}\frac{1}{R_B} \\
i_{FS}(t) &= \frac{u_B(t)}{R_F} \\
i_{FD}(t) &= \frac{u_B(t)^2}{u_o}\frac{1}{R_B}
\end{aligned}
\tag{5.7}
$$

Fig. 5.7 shows the cascaded buck-flyback converter large-signal model for simulation in PSIM.

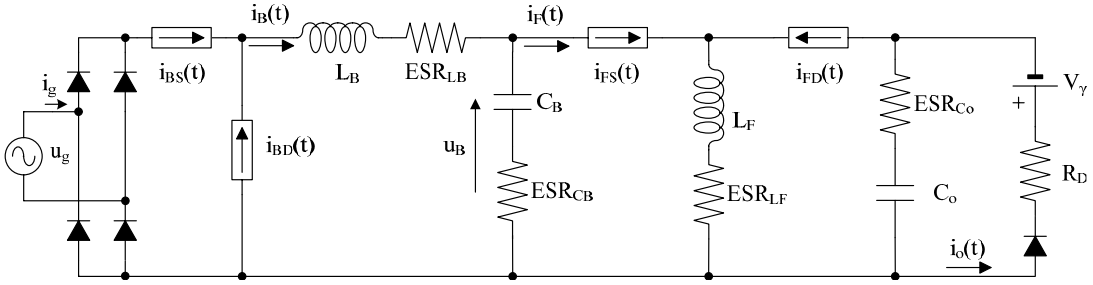

Fig. 5.6. Large-signal averaged model of the cascaded buck-flyback converter equivalent to the IBFC by the method described in [5.15].

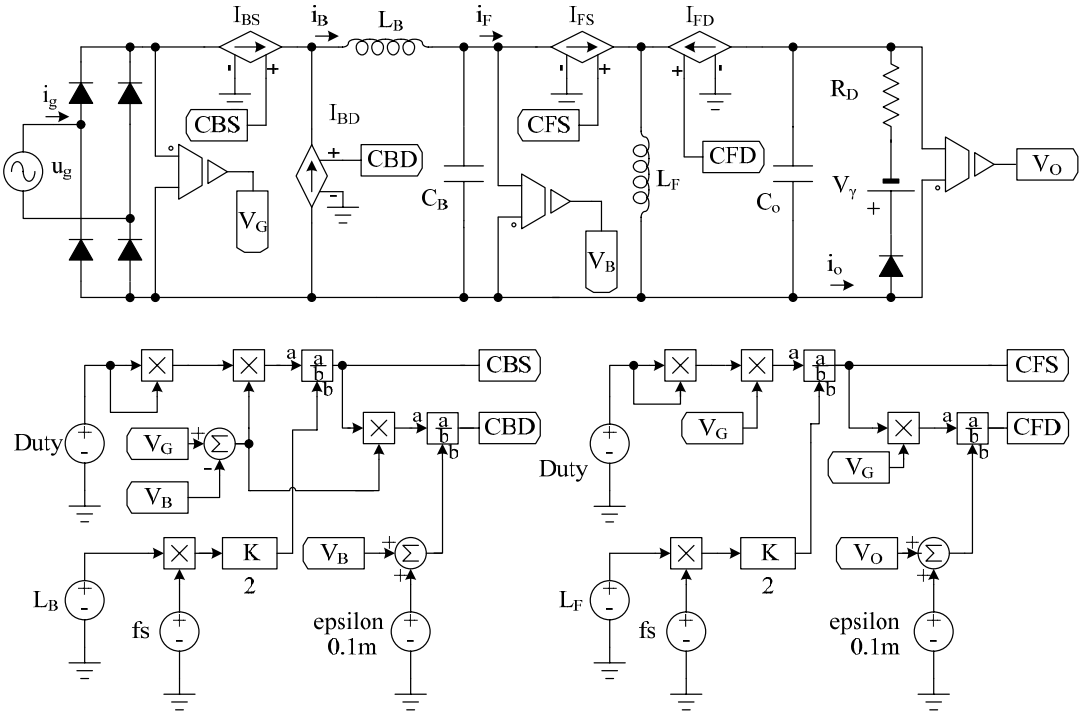

Fig. 5.7. Large-signal averaged model of the cascaded buck-flyback converter by the method described in [5.15] for simulation in PSIM.

As with the LFR large-signal model, the cascaded buck-flyback converter was simulated in PSIM using the values provided for the application example in Chapter 4, with a 570 µF and 1.5

μF bus and output capacitors, respectively, and a 26.1 μH and 19.3 μH buck and flyback inductors, respectively. The IBFC and its large-signal model were simulated together, the results for output current, input current, and bus voltage being shown in Fig. 5.8.

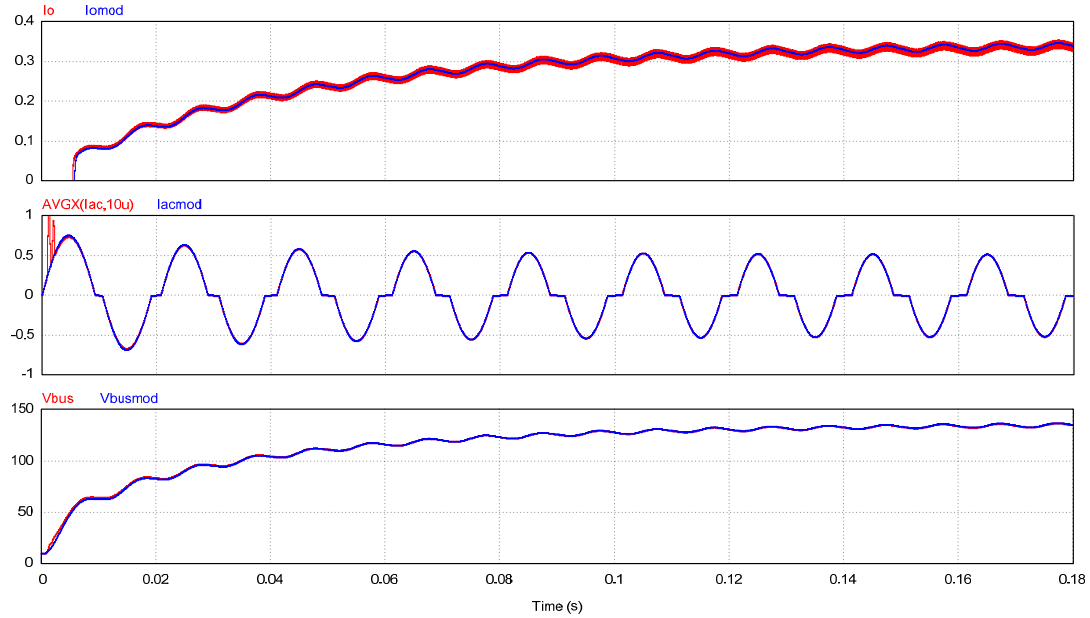

Fig. 5.8. PSIM simulation results for output current (top trace), average input current (centre trace) and bus voltage (bottom trace) for the cascaded buck-flyback converter averaged model by the method described in [5.15] (blue lines), and the IBFC (red lines).

As can be seen from Fig. 5.8, this large-signal model is highly accurate too, provided that the actual converter keeps the DCM condition, as in the previous case. With regard to the error seen in the input current under steady-state conditions, it is kept under the error achieved with the LFR-based large-signal model. Nevertheless, a small output-current steady-state error can be seen, which might be caused by truncation errors in the converter values. An epsilon voltage was added to the bus and output voltage in order to prevent from divisions by zero.

In addition, this large-signal model straightforwardly gives the complete small-signal model by derivation and linearisation of the current sources at a given operation point, which will be dealt with in subsequent sections. Moreover, this linearisation also gives a full-order model accurate at high frequencies up to half the switching frequency, according to the Nyquist-Shannon sampling theorem.

5.3.2. IBFC small-signal model

In this section, the small-signal model of the cascaded buck-flyback equivalent converter averaged at the switching frequency will be obtained, assuming quasi-static operation. The small-signal model is based on the averaging of the currents across the converter diodes and transistors and its subsequent perturbation and linearisation so that they can be represented in the Laplace variable domain. A conventional small-signal analysis will be developed, considering the currents averaged at a switching cycle. This analysis will be helpful in order to study the effects of low-to-mid frequencies perturbations on the converter performance. Since the high-frequency poles introduced by the inductors dynamics are generally placed at frequencies beyond the switching frequency, reduced-order models will be enough in order to study the converter dynamics, as only the phase will be noticeable affected at high frequencies [5.18].

The small-signal model can be obtained from the large-signal model achieved in Section 5.3.1. It shall be noted that, as previously stated, the small-signal model is valid for frequencies up to half the switching frequency due to the Nyquist-Shannon sampling theorem. Moreover, the classical approach to averaged small-signal models usually neglects the inductor dynamics, which has been shifted to high frequencies due to the DCM operation. It has been proven that the accuracy of reduced-order models is fair for the gain at frequencies up to one third of the switching frequency, introducing a higher error in the phase [5.18]. Nevertheless, provided that HPF converters feature slow dynamics, these reduced-order models can be considered accurate enough in order to design a feedback loop.

As previously stated, the small-signal model can easily be obtained from linearisation of the large-signal current sources $i_{BS}(t)$, $i_{BD}(t)$, $i_{FS}(t)$, and $i_{FD}(t)$ with respect to the variation of several parameters at a steady-state operation point, averaged for a switching cycle. Thus, the IBFC small-signal model will be derived from the equivalent cascaded buck-flyback converter:

$$\begin{aligned}
\hat{\imath}_{BS} &= \left.\frac{\partial\langle i_{BS}\rangle}{\partial u_g}\right]_{SS}\hat{u}_g + \left.\frac{\partial\langle i_{BS}\rangle}{\partial u_B}\right]_{SS}\hat{u}_B + \left.\frac{\partial\langle i_{BS}\rangle}{\partial d}\right]_{SS}\hat{d} \\
\hat{\imath}_{BD} &= \left.\frac{\partial\langle i_{BD}\rangle}{\partial u_g}\right]_{SS}\hat{u}_g + \left.\frac{\partial\langle i_{BD}\rangle}{\partial u_B}\right]_{SS}\hat{u}_B + \left.\frac{\partial\langle i_{BD}\rangle}{\partial d}\right]_{SS}\hat{d} \\
\hat{\imath}_{FS} &= \left.\frac{\partial\langle i_{FS}\rangle}{\partial u_g}\right]_{SS}\hat{u}_B + \left.\frac{\partial\langle i_{FS}\rangle}{\partial d}\right]_{SS}\hat{d} \\
\hat{\imath}_{FD} &= \left.\frac{\partial\langle i_{FD}\rangle}{\partial u_g}\right]_{SS}\hat{u}_B + \left.\frac{\partial\langle i_{FD}\rangle}{\partial d}\right]_{SS}\hat{d} + \left.\frac{\partial\langle i_{FD}\rangle}{\partial u_o}\right]_{SS}\hat{u}_o
\end{aligned} \tag{5.8}$$

where the symbol "‹ ›" represents the variable averaged over a switching cycle and the symbol "^" represents the variation of a variable. Renaming the derivatives of the averaged current sources and transferring to the Laplace domain:

$$\begin{aligned}
i_{BS}(s) &= k_{BSG}U_g(s) + k_{BSB}U_B(s) + k_{BSD}d(s) \\
i_{BD}(s) &= k_{BDG}U_g(s) + k_{BDB}U_B(s) + k_{BDD}d(s) \\
i_{FS}(s) &= k_{FSB}U_B(s) + k_{FSD}d(s) \\
i_{FD}(s) &= k_{FDB}U_B(s) + k_{FDD}d(s) + k_{FDO}U_o(s) \\
U_o(s) &= R_D I_o(s)
\end{aligned} \tag{5.9}$$

where the coefficients *k* are:

$$k_{BSG} = \frac{D^2 T_s}{2L_B} = \frac{1}{R_B} \qquad k_{FSB} = \frac{D^2 T_s}{2L_F} = \frac{1}{R_F}$$

$$k_{BSB} = -\frac{D^2 T_s}{2L_B} = -\frac{1}{R_B} \qquad k_{FSD} = U_B \frac{DT_s}{L_F}$$

$$k_{BSD} = \left(U_g - U_B\right)\frac{DT_s}{L_B} \qquad k_{FDB} = \frac{2U_B \frac{1}{R_F}}{R_D I_o + V_\gamma}$$

$$k_{BDG} = \frac{U_g - U_B}{U_B}\frac{D^2 T_s}{L_B} \qquad k_{FDD} = \frac{2\frac{U_B^2}{D}\frac{1}{R_F}}{R_D I_o + V_\gamma} \qquad (5.10)$$

$$k_{BDB} = -\frac{U_g^2 - U_B^2}{U_B^2}\frac{1}{R_B} \qquad k_{FDO} = -\frac{\frac{U_B^2}{R_F}}{\left(R_D I_o + V_\gamma\right)^2}$$

$$k_{BDD} = \frac{\left(U_g - U_B\right)^2}{U_B}\frac{DT_s}{L_B}$$

The next step is to obtain the small-signal equivalent circuit, which is achieved by substituting the large-signal current sources from Fig. 5.6 by its equivalent small-signal components. This is depicted in Fig. 5.9.

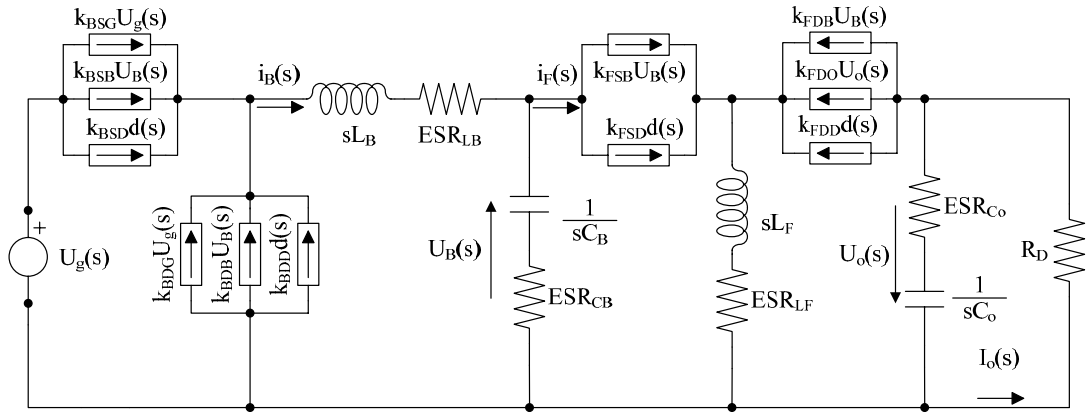

Fig. 5.9. Small-signal averaged model of the cascaded buck-flyback converter equivalent to the IBFC by the method described in [5.15].

Starting from this small-signal equivalent circuit, the different converter transfer functions can be obtained. It has to be stated that, as the converters are cascaded and integrated, operating with the same duty cycle, their dynamics cannot be studied separately due to their mutual interactions [5.2], [5.3] if the dynamic behaviour of one of the converters is not negligible. The transfer functions are calculated as follows:

- **Bus voltage to output current, $G_{oB}(s)$:**

This transfer function, which gives information about the input-ripple rejection, is calculated as:

$$G_{oB}(s) = \frac{I_o(s)}{U_B(s)} \qquad (5.11)$$

It is obtained by disconnecting all the current sources that depend on other parameters than the output current and the bus voltage.

The small-signal equivalent circuit of Fig. 5.9 is reduced to that shown in Fig. 5.10.

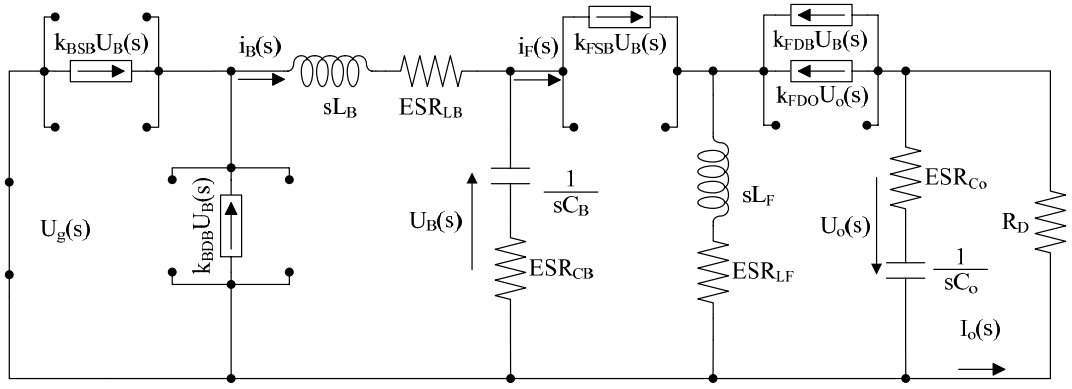

Fig. 5.10. Small-signal averaged model in order to determine the flyback audiosusceptibility.

It has to be noted that the current sources k_{BSB}, k_{BDB}, and k_{FSB} just affect the currents through the inductors and the bus capacitor, only k_{FDB} and k_{FDO} affecting the output current. Thus, the flyback input-ripple rejection transfer function reduces to:

$$G_{oB}(s) = \frac{I_o(s)}{U_B(s)} = \frac{k_{FDB}}{1 - k_{FDO}R_D} \cdot \frac{1 + sC_oESR_{Co}}{1 + sC_o\left(\frac{R_D(1 - k_{FDO}ESR_{Co}) + ESR_{Co}}{1 - k_{FDO}R_D}\right)} \tag{5.12}$$

- **Input voltage to bus voltage, $G_{Bg}(s)$.**

This input-ripple rejection transfer function, in this case, the bus audiosusceptibility, is calculated analogously to the flyback bus-voltage to output-current transfer function:

$$G_{Bg}(s) = \frac{U_B(s)}{U_g(s)} \tag{5.13}$$

The small-signal equivalent circuit of Fig. 5.9 is reduced to that shown in Fig. 5.11.

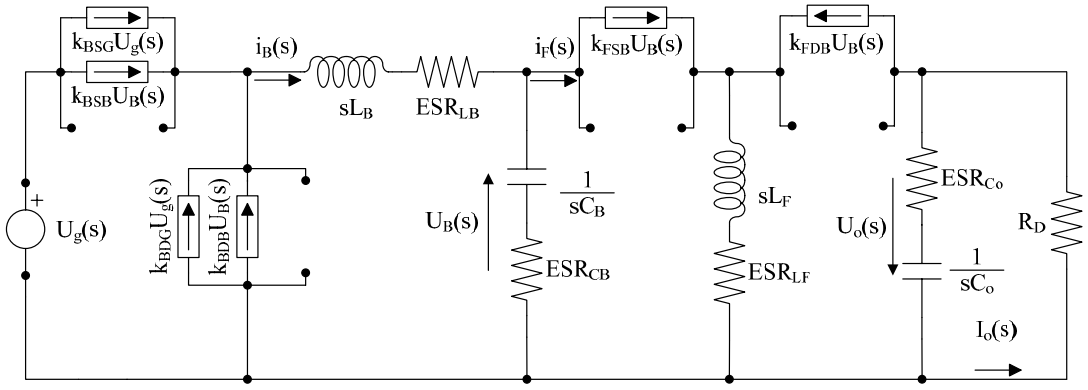

Fig. 5.11. Small-signal averaged model in order to determine the bus audiosusceptibility.

As in the previous transfer function, the current sources affecting the bus voltage are only k_{BSG}, k_{BSB}, k_{BDG}, k_{BDB}, and k_{FSB}, whereas k_{FDB} affects only the output current. The bus audiosusceptibility reduces to:

$$G_{Bg}(s) = \frac{U_B(s)}{U_g(s)} = k_{BG} \cdot \frac{1 + sC_B ESR_{CB}}{-1 + sp_{BB}} \tag{5.14}$$

where:

$$\begin{aligned} k_{BG} &= \frac{k_{BSG} + k_{BDG}}{k_{BSB} + k_{BDB} - k_{FSB}} \\ p_{BB} &= C_B \left(\frac{1 - ESR_{CB}(k_{BSB} + k_{BDB} - k_{FSB})}{k_{BSB} + k_{BDB} - k_{FSB}} \right) \end{aligned} \tag{5.15}$$

- **Control to bus voltage, $G_{Bd}(s)$.**

This transfer function gives information about the variation on bus voltage with respect to variations in duty cycle. It is calculated as:

$$G_{Bd}(s) = \frac{U_B(s)}{d(s)} \tag{5.16}$$

The small-signal equivalent circuit of Fig. 5.9 is reduced to that shown in Fig. 5.12.

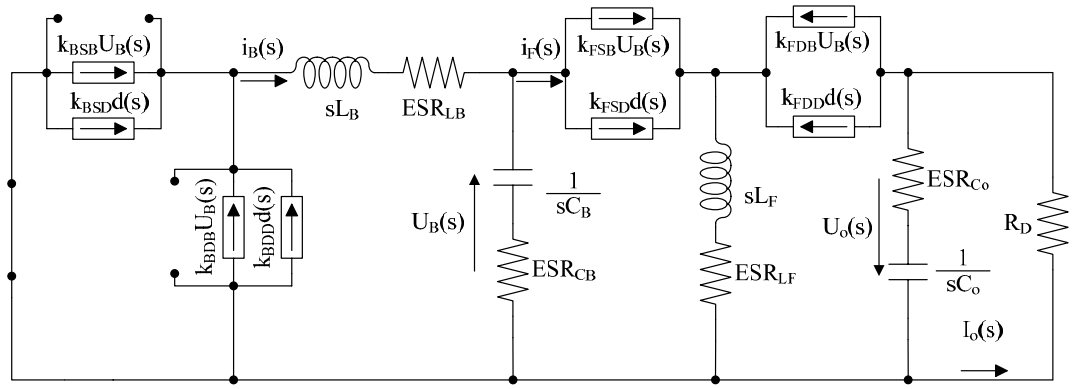

Fig. 5.12. Small-signal averaged model in order to determine the control to bus voltage transfer function.

As in the previous cases, the current sources of interest for determining $G_{Bd}(s)$ are only k_{BSB}, k_{BSD}, k_{BDB}, k_{BDD}, k_{FSB}, and k_{FSD}, whereas k_{FDB} and k_{FDD} affect only the output current. Therefore:

$$G_{Bd}(s) = \frac{U_B(s)}{d(s)} = k_{BD} \cdot \frac{1 + sC_B ESR_{CB}}{sp_{BB} - 1} \tag{5.17}$$

Analogously to the $G_{Bg}(s)$ transfer function, the following relation is found:

$$k_{BD} = \frac{k_{BSD} + k_{BDD} - k_{FSD}}{k_{BSB} + k_{BDB} - k_{FSB}} \tag{5.18}$$

- **Input voltage to output current, $G_{og}(s)$.**

This transfer function gives information about the variation on output current with respect to variations in input voltage. In other words, it is the line input-ripple rejection transfer function of the converter. It is calculated as:

$$G_{og}(s) = \frac{I_o(s)}{U_g(s)} \tag{5.19}$$

Nevertheless, the output current is not directly affected by the input voltage, as can be seen in Fig. 5.9, but on the bus voltage, which in turn depends on the input voltage, as already calculated. Therefore, and provided that superposition applies to linearised variables, the input-ripple rejection function will be calculated as:

$$G_{og}(s) = \frac{I_o(s)}{U_g(s)} = \frac{I_o(s)}{U_B(s)} \frac{U_B(s)}{U_g(s)} \tag{5.20}$$

The reduced small-signal equivalent circuit is the same as in Fig. 5.11.

The corresponding transfer functions have already been calculated. Thus, (5.20) yields:

$$G_{og}(s) = \frac{k_{FDB} k_{BG}}{1 - k_{FDO} R_D} \frac{(1 + sC_o ESR_{Co})(1 + sC_B ESR_{CB})}{\left(1 + sC_o \left(\frac{R_D(1 - k_{FDO} ESR_{Co}) + ESR_{Co}}{1 - k_{FDO} R_D}\right)\right)(sp_{BB} - 1)} \tag{5.21}$$

- **Control to output current, $G_{od}(s)$.**

This transfer function studies the effects that variations on the duty cycle imply on the output current, i.e. $\partial I_o/\partial d$. However, the output current is also affected by the bus voltage, which is in turn affected by the duty cycle. These interactions between both converters are, as previously stated, to be taken into account if both converters feature a fast enough dynamics that makes their dynamic behaviour non negligible. Nevertheless, the variations produced by the bus voltage sensitivity to the duty cycle will be considered as a perturbation. Thus, the control to output current can be simply defined as:

$$G_{od}(s) = \left.\frac{I_o(s)}{d(s)}\right]_{\hat{u}_B = 0} \tag{5.22}$$

The reduced small-signal equivalent circuit of Fig. 5.9 is reduced to that shown in Fig. 5.13.

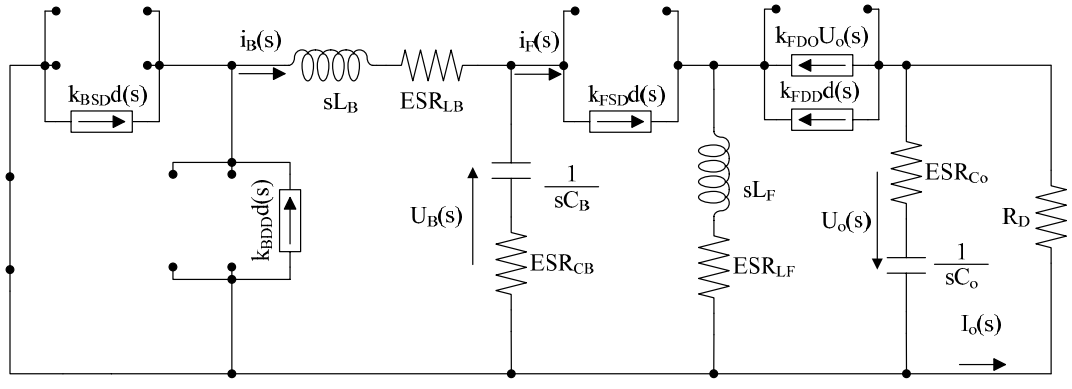

Fig. 5.13. Small-signal averaged model in order to determine the control to output current transfer function.

In order to determine $I_o(s)/d(s)$, the only current sources of interest are k_{FDO} and k_{FDD}. As in a regular flyback converter supplied from a DC source, this leads to the following transfer function:

$$\frac{I_o(s)}{d(s)} = \frac{k_{FDD}}{1 - k_{FDO}R_D} \cdot \frac{1 + sz_o}{1 + sp_{DO}} \tag{5.23}$$

where:

$$z_o = C_o ESR_{Co}$$
$$p_{DO} = C_o \left(\frac{R_D(1 - k_{FDO} ESR_{Co}) + ESR_{Co}}{1 - k_{FDO}R_D} \right) \tag{5.24}$$

- **Control to input current, $G_{id}(s)$.**

This transfer function studies the effects that variations on the duty cycle imply on the input current, i.e. $\partial I_i/\partial d$. This transfer function could introduce interesting information in order to design a feedback loop with a minimal – or a given, distortion of the input current. Therefore, as superposition applies since these are linearised variables, both transfer functions can be determined as:

$$G_{id}(s) = \frac{I_i(s)}{d(s)} \tag{5.25}$$

The small-signal equivalent circuit of Fig. 5.9 is reduced to that shown in Fig. 5.14.

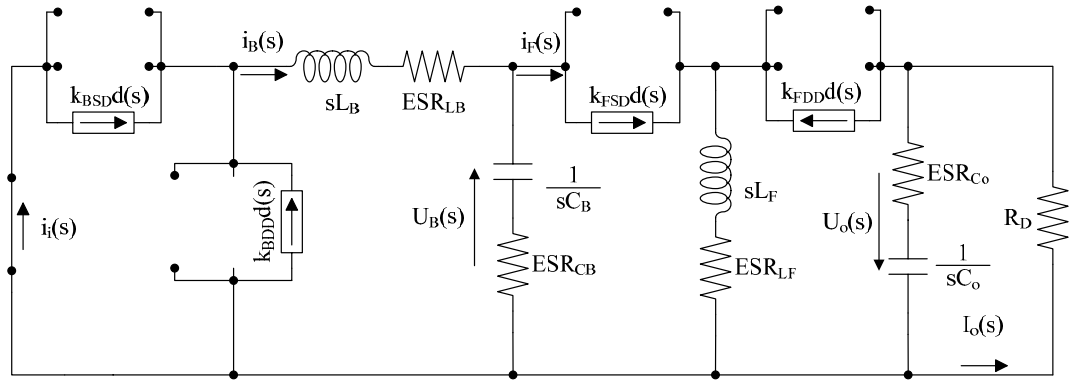

Fig. 5.14. Small-signal averaged model in order to determine the control to input current transfer function.

As in the previous cases, the current sources of interest for determining $G_{id}(s)$ are only k_{BSD}, and k_{BDD}, whereas k_{FSD} and k_{FDD} affect only the output current. In addition, the transfer function $I_i(s)/d(s)$ at $\hat{u}_B = 0$ precisely is the current source k_{BSD}. Hence, (5.25) reduces to:

$$G_{id}(s) = k_{BSD} \tag{5.26}$$

- **Bus voltage to input current, $G_{iB}(s)$.**

As stated before, the input current is affected not only by the duty cycle, but also by the bus voltage, which is in turn affected by the duty cycle. Therefore, the effects on the input current caused by perturbations on the bus voltage will be studied in order to determine the interaction between both converters. This transfer function can be calculated as:

$$G_{iB}(s) = \frac{I_i(s)}{U_B(s)} \tag{5.27}$$

In this case, the current sources of interest for determining $G_{iB}(s)$ are only k_{BSB}, and k_{BDB}, whereas k_{FSB} and k_{FDB} affect only the output current. In addition, the transfer functions $I_i(s)/U_B(s)$ precisely is the current source k_{BSB}. Hence:

$$G_{iB}(s) = \frac{I_i(s)}{U_B(s)} = k_{BSB} \tag{5.28}$$

As a consequence, the input current is affected not only by the duty cycle, but also by the bus voltage, which is in turn affected by the duty cycle

- **Input impedance, $Z_i(s)$.**

This transfer function gives information about the ratio between input voltage at a given frequency and the corresponding harmonic current. It is an interesting parameter in order to optimise the design of an input or EMI filter [5.19]. By employing the same definition for the buck converter PFP input impedance as that considered in Chapter 4:

$$Z_i(s) = \frac{U_g(s)}{I_i(s)} = \frac{U_g(s)}{k_{BSG}U_g(s) + k_{BSB}U_B(s)} \tag{5.29}$$

The reduced small-signal equivalent circuit of Fig. 5.9 is reduced to that shown in Fig. 5.15.

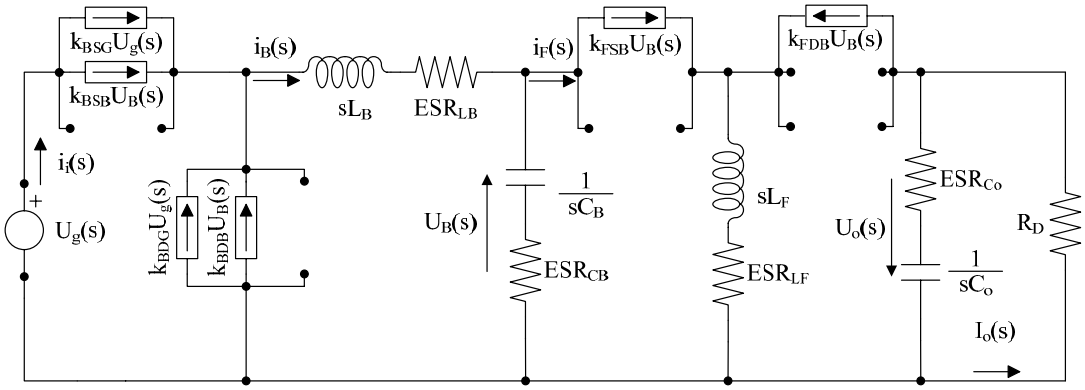

Fig. 5.15. Small-signal averaged model in order to determine the input impedance transfer function.

Since the bus voltage also depends on the input voltage through the $G_{Bg}(s)$ transfer function, (5.29) can be re-written as:

$$Z_i(s) = \frac{1}{k_{BSG} + k_{BSB}G_{Bg}(s)} \tag{5.30}$$

However, provided that $k_{BSB} = -k_{BSG}$, and $k_{BSG} = 1/R_B$, (5.30) yields:

$$Z_i(s) = R_B \frac{s(p_{BB} + k_{BG}z_B) - (1 + k_{BG})}{sp_{BB} - 1} \tag{5.31}$$

which shows that the input impedance is constant under DC operation, its value depending on the buck equivalent resistance and the input-voltage to bus-voltage transfer function static gain, and features a pole and a zero that depend on the capacitance of the bus capacitor.

- **Input admittance, $Y_i(s)$.**

It could also be interesting to study the effects that small-signal input voltage perturbations have on the input current. Thus, the input admittance is defined as:

$$Y_i(s) = \frac{I_i(s)}{U_g(s)} = \frac{k_{BSG}U_g(s) + k_{BSB}U_B(s)}{U_g(s)} \tag{5.32}$$

which actually is $1/Z_i(s)$. The small-signal equivalent circuit is the same that for the input impedance in Fig. 5.15. By developing (5.32) as proceeded with the input impedance:

$$Y_i(s) = k_{BSG}\frac{s(p_{BB} + k_{BG}z_B) - (1 + k_{BG})}{sp_{BB} - 1} \tag{5.33}$$

As can be seen from (5.33), the input admittance introduces a pole and a zero, which implies that different current harmonics are differently damped, being a likely source of input current distortion.

- **Output admittance, $Y_o(s)$.**

The output impedance generally is an interesting transfer function, since it provides useful information about the shift on output voltage that a sudden load step, this is, a current step, can induce. So much so the source of unexpected instabilities in closed-loop can be found by examination of the output impedance transfer function [5.20]. However, the function of interest in a current-controlled load might be the effects on output current that shifts in output voltage may induce. Therefore, the output admittance will be studied instead of the output impedance. The output admittance can be defined as:

$$Y_o(s) = \frac{I_o(s)}{U_o(s)} \tag{5.34}$$

The reduced small-signal equivalent circuit of Fig. 5.9 is reduced to that shown in Fig. 5.16.

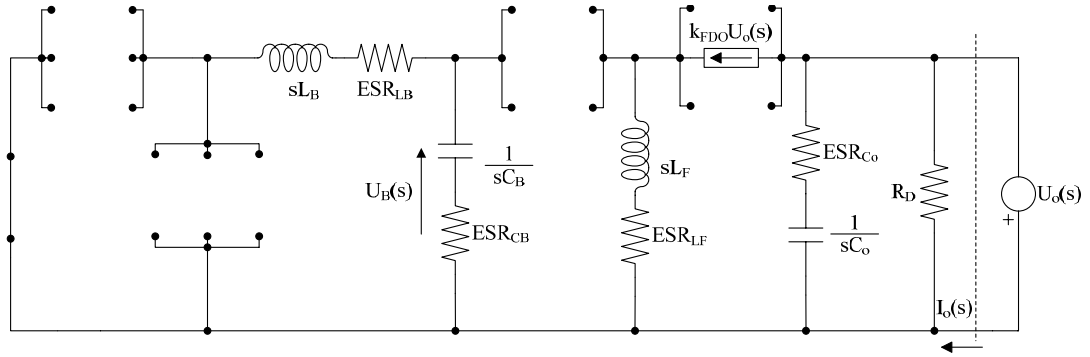

Fig. 5.16. Small-signal averaged model in order to determine the output admittance transfer function.

The output admittance can be calculated by studying the effects that the voltage source $u_o(s)$ connected in parallel to the load induces on the output current. Thus, the output current can be expressed as:

$$I_o(s) = \frac{U_o(s)}{R_D} + \frac{U_o(s)}{\frac{1 + sC_oESR_{Co}}{1 + sC_o}} - k_{FDO}U_o(s) \tag{5.35}$$

By re-arranging (5.35), the output admittance is finally achieved:

$$Y_o(s) = \frac{1-k_{FDO}}{R_D} \cdot \frac{1 + sC_o(R_D + ESR_{Co} - ESR_{Co}R_Dk_{FDO})}{1 + sC_oESR_{Co}} \tag{5.36}$$

In case of needing the output impedance transfer function in order to determine the response of the IBFC converter under a load step, as a connection of an extra LED string would be, the output impedance is easily yielded by calculating $1/Y_o(s)$.

Therefore, with the transfer functions calculated above, both the output and input currents of the IBFC could be determined with the block diagram shown in Fig. 5.17

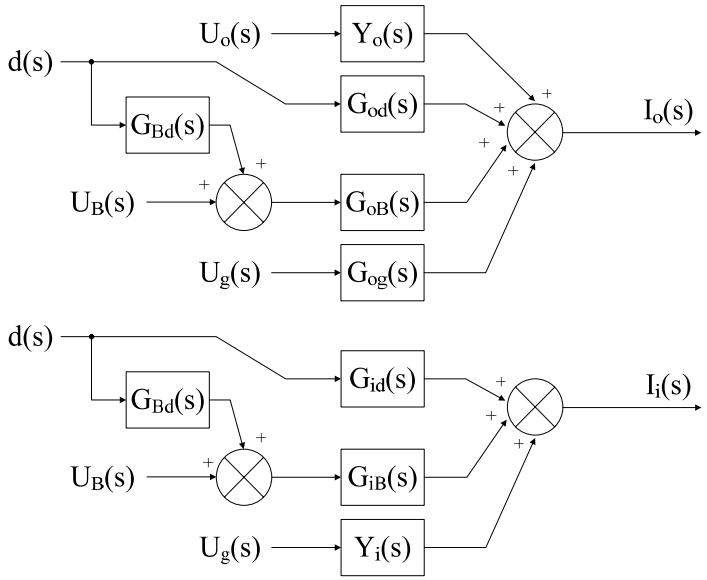

Fig. 5.17. Block diagram of the IBFC converter including all the transfer functions involved.

5.3.3. Application example

This section will show the control-to-output function considering the interactions between the buck and the flyback converters, i.e. $G_o(s)=G_{od}(s)+G_{oB}(s)G_{Bd}(s)$, IBFC line input-ripple rejection function, flyback input-ripple rejection function, and input impedance transfer functions calculated above applied to the IBFC shown in Chapter 4. The components used in the calculations are shown in Table V.I.

TABLE V.I
COMPONENTS OF THE SMALL-SIGNAL MODEL

U_g (V)	242.5	C_B (µF)	570	L_B (µH)	26.1
U_B (V)	137.5	ESR_{CB} (Ω)	0	L_F (µH)	19.3
d	0.119	C_o (µF)	1.5	V_γ (V)	170.1
I_o (A)	0.350	ESR_{Co} (Ω)	0	R_D (Ω)	87.2

The input voltage was set to 242.5 V provided that this is the DC input voltage that induces a 137.5 V bus voltage by using (4.7) in Chapter 4, which in turn leads to a 350 mA output current at 0.119 duty cycle. Such an input voltage is used due to the open-loop operation aimed on achieving the nominal bus voltage and output current. With these parameters, the coefficients of the small-signal model are gathered in Table V.II.

TABLE V.II
COEFFICIENTS OF THE SMALL-SIGNAL MODEL

k_{BSG} (Ω^{-1})	$2.713 \cdot 10^{-3}$	k_{BSB} (Ω^{-1})	$-2.713 \cdot 10^{-3}$	k_{BSD} (A)	4.795
k_{BDG} (Ω^{-1})	$4.155 \cdot 10^{-3}$	k_{BDB} (Ω^{-1})	$-5.746 \cdot 10^{-3}$	k_{BDD} (A)	3.672
k_{FSB} (Ω^{-1})	$3.669 \cdot 10^{-3}$	k_{FSD} (A)	8.467	k_{FDO} (Ω^{-1})	$-1.766 \cdot 10^{-3}$
k_{FDB} (Ω^{-1})	$5.090 \cdot 10^{-3}$	k_{FDD} (A)	5.874		

Nevertheless, the small-signal models already calculated allow a piece-wise small-signal model to be obtained for the AC input voltage [5.19]. Fig. 5.18 depicts the theoretical Bode diagrams for the output transfer functions stated above, namely, $G_o(s)$, $G_{og}(s)$ and $G_{oB}(s)$. With regard to the input admittance, this transfer function is depicted in Fig. 5.19.

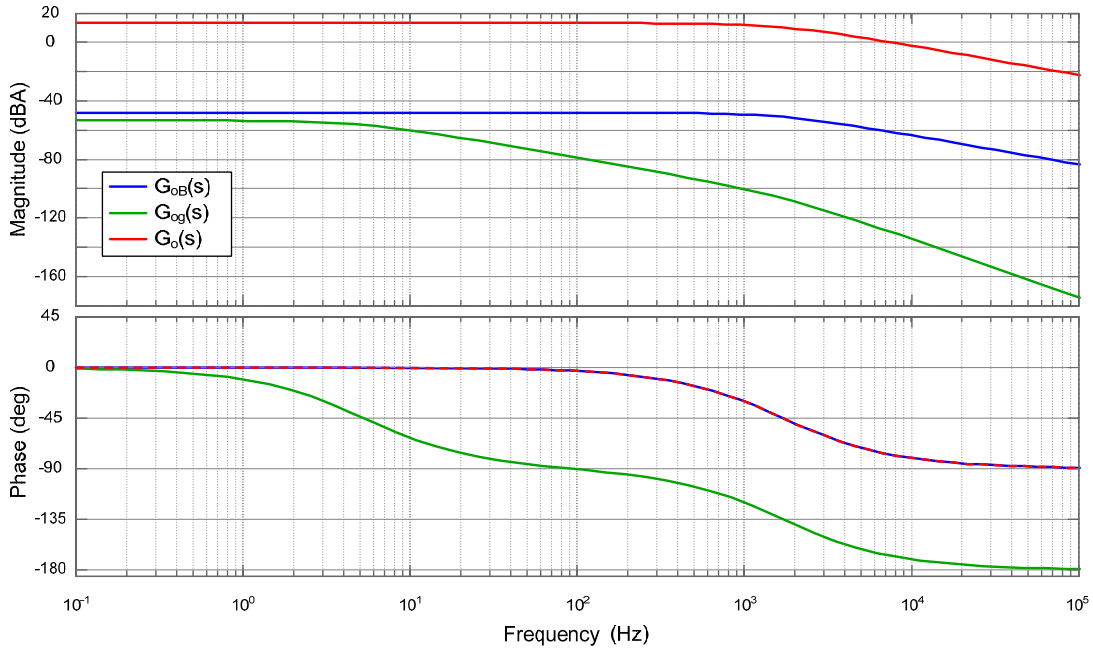

Fig. 5.18. Bus voltage to output current, line audiosusceptibility, and control to output current of the IBFC with the components and operation point stated in Table V.I.

As can be seen from Fig. 5.18, a high bus-to-output noise-rejection capability is achieved, provided that the $G_{oB}(s)$ transfer function attenuation is around -50 dB, thus confirming the low ripple-gain factor derived in Chapter 4 for the DCM flyback LED driver. In addition, it can be seen the high-frequency pole introduced at around 1.5 kHz by the output capacitor, C_o. With regard to the line audiosusceptibility, a high line-ripple rejection is confirmed, with a low-frequency attenuation around -50 dB, which is further improved from the bus-capacitor pole frequency, located at approximately 280 Hz. Moreover, as this transfer function results from the combination of the $G_{Bg}(s)$ and $G_{oB}(s)$ transfer functions, the line audiosusceptibility function also features the high-frequency pole introduced by the output capacitor, further improving the line-noise rejection at high frequencies. The control to output transfer function, $G_o(s)$, also features the output high-frequency pole, with a high low-frequency gain corresponding to the current amplification required for the duty cycle nominal point.

As can be seen from Fig. 5.19, the input admittance shows a particular behaviour. On the one hand, a DC gain corresponding to the input impedance, but affected by a low-frequency

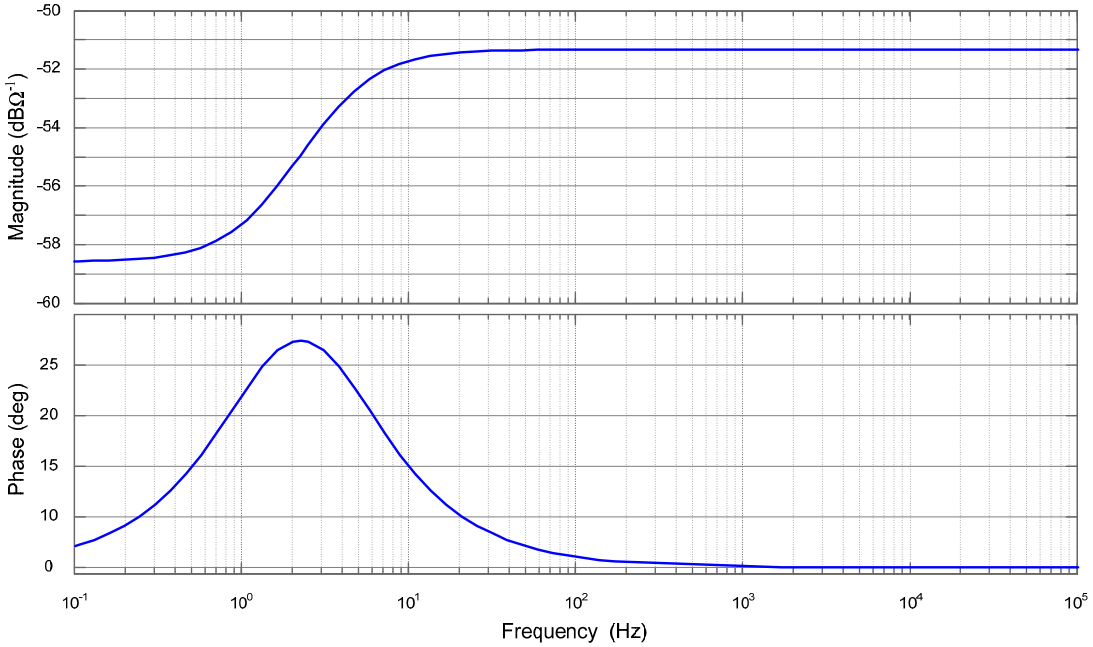

Fig. 5.19. Input admittance of the IBFC with the components and operation point stated in Table V.I.

zero and a one decade higher pole introduced by the bus capacitor, increasing the input admittance gain. It can also be seen in the phase plot, where a low-frequency phase-lead effect is induced by the bus capacitor and the interaction with the flyback converter.

This theoretical Bode diagrams where tested by PSIM simulations of the actual IBFC for the $G_o(s)$, $G_{bg}(s)$ and the $Y_i(s)$ transfer functions, the results being depicted in Fig. 5.20. The IBFC converter was simulated under DC nominal operation with sinusoidal perturbation superimposed to the variables of interest at different frequencies. In addition, the control-to-output function, $G_o(s)$, and the input admittance, $Y_i(s)$ were experimentally measured. As can be seen from the figure, a very good agreement between the theoretically predicted and simulated Bode diagrams and the experimentally measured transfer functions has been obtained. The experimental tests show that for the nominal DC operation values, as preview by the theoretical results, there is no interaction between the buck converter and the flyback converter regarding the control to output transfer function, being their dynamics through $G_{Bd}(s)$ decoupled. This can be demonstrated by further rearrangement and simplification of the current gain k_{BD} introduced in (5.18) and solving for $k_{BD} = 0$. This leads to the IBFC DC operation conversion ratio derived in expression (4.7) in Chapter 4. However, it has to be taken into account that this result is valid only for DC supply. Moreover, the line ripple-rejection transfer function has been confirmed from the theoretical calculations by simulations. Finally, the input admittance has experimentally been verified to be affected by the zero and pole introduced by the bus capacitor, leading to higher currents at higher frequencies, which will be a likely source of input current distortion, even if the duty cycle is kept constant.

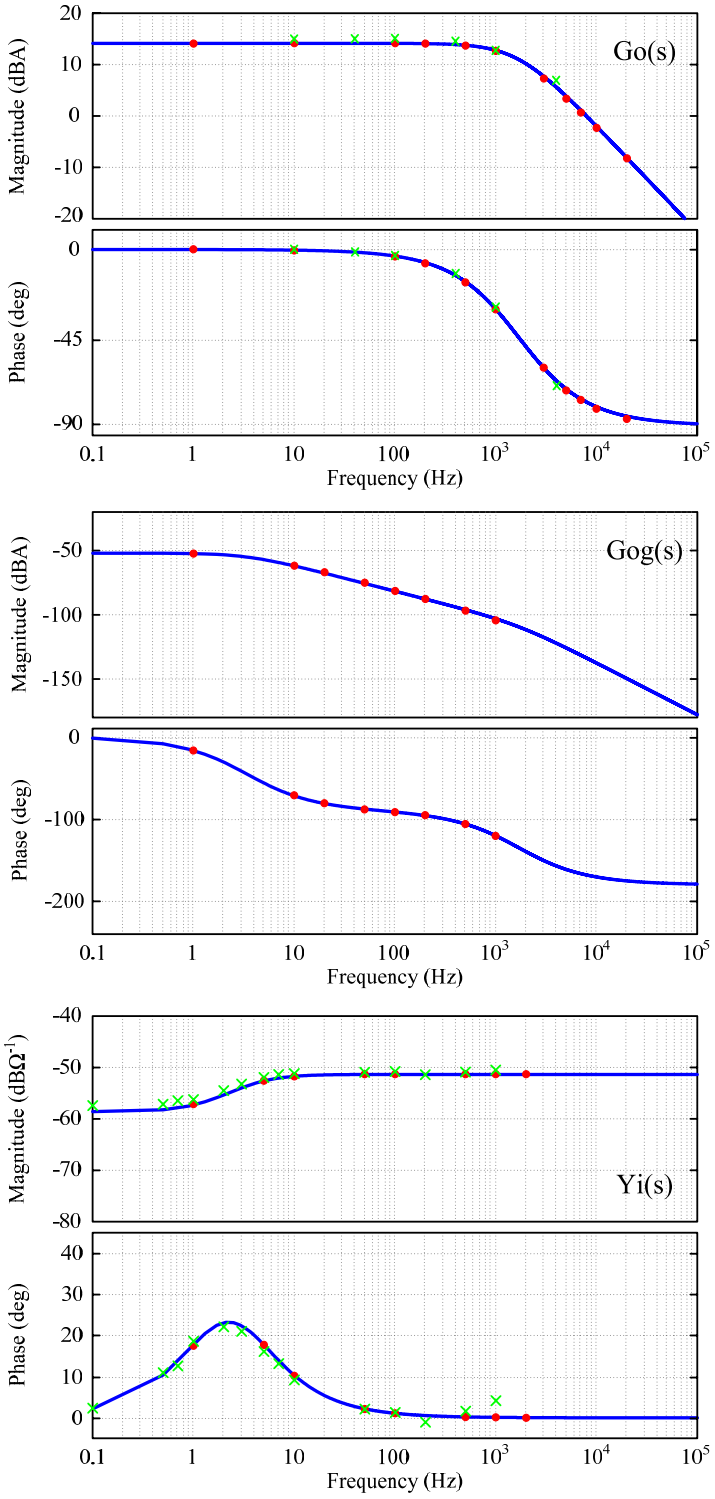

Fig. 5.20. Theoretical predictions (blue solid line), simulated results (red dots) and experimental measures (green crosses) of the Bode diagrams for the control-to-output transfer function, $G_o(s)$, (top); line audiosusceptibility, $G_{og}(s)$, (middle); and input admittance, $Y_i(s)$, (bottom). The magnitude is depicted in the upper trace whereas the phase is depicted in the lower trace.

5.4. Conclusions

In this chapter, the modelling of the IBFC has been developed. The modelling procedure have been performed considering a cascaded buck-flyback converter for the sake of simplicity, provided that its behaviour and operation are equivalent to those of the IBFC even though the topological transformation. Indeed, the additional diodes allow the currents to be balanced as if it were a conventional two-stage cascaded converter.

With regard to the models, two approaches were taken, aimed on solving different issues, either large-signal design and simulation, or small-signal analysis and design. Firstly, the large-signal LFR approach was considered. Thus, the entire IBFC converter was modelled as a cascaded connection of the buck PFP and the flyback LED driver, the former supplying the latter. Provided that the inductors dynamics is neglected, this approach allows for a simple and fast design that yields accurate results in the range from line frequency to low-medium frequency. The results obtained from the simulation of the large-signal model and the IBFC confirm the suitability of the LFR approach.

Secondly, the large-signal model has also been obtained from the method described in [5.15], where the converter transistors and diodes are handled as current sources. Thus, and provided that DCM operation is maintained, by averaging their currents at a switching cycle a large-signal model valid for frequencies up to around one-third to half the switching frequency is obtained due to the high-frequency phase shift introduced by the inductor dynamics [5.16]. It has to be remarked that this model considers that the average voltage across the inductors is zero, so unexpected effects on the phase for frequencies below the switching frequency are likely, depending on the location of the poles introduced by the inductors [5.16]. Nevertheless, this model is accurate in the mid-frequency range. The simulation results obtained from the comparison to the IBFC converter showed its accuracy.

After the large-signal model was derived, the linearisation of the current sources at an operation point was performed, in order to obtain the small-signal model. This procedure also included the buck converter, aiming on studying the interactions between the buck and flyback dynamics. Thus, a complete set of transfer functions that comprehensively describes the converter small-signal behaviour has been derived. Furthermore, the small-signal model has been applied to the IBFC converter described in Chapter 4 in order to obtain the control to output transfer function, line audiosusceptibility, flyback audiosusceptibility, and input admittance, and the theoretical transfer functions have been compared to those obtained from PSIM simulation of the IBFC, achieving high accuracy. In addition, it has been stated that the dynamics of the buck and the flyback converter regarding duty cycle perturbation is decoupled for a DC nominal operation point. Furthermore, it has been checked that the input admittance is affected by the bus voltage ripple, being a likely source of current harmonic distortion for off-line operation.

5.5. References

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Chapter 6

Dimming of Light-Emitting Diodes

In this chapter, the dimming capability applied to the IBFC developed in previous chapters is comprehensively studied and discussed. Thus, a brief introduction to the most significant concepts in dimming operation is provided. Therefore, both analogue and PWM dimming methods are studied for its addition to the IBFC LED driver in order to extend its application from street lighting to general indoor/outdoor lighting. The main dimming techniques, namely analogue and PWM dimming, are introduced. In this way, since PWM dimming is considered to offer the best dimming performance, the three main PWM dimming schemes are revised and compared. Analogue dimming is also considered, being the simplest and most cost-effective dimming technique. Analogue dimming is the first test carried out, prior to studying the challenges that PWM schemes present. Afterwards, the suitable PWM dimming schemes will be tested in the laboratory and the experimental results will be discussed. This PWM dimming schemes are enable and series dimming.

Afterwards, a suitable PWM dimming control scheme for low slew-rate or slow-dynamics LED drivers will be developed. This way, a new approach to series dimming technique is proposed: the high frequency series PWM dimming, which overcomes all the problems that standard PWM series dimming features. A deeper insight in this technique is given using the approximation by the control sensitivity function

6.1. Introduction

The previous chapters presented the study of LEDs as a power load and its dependence on temperature, the requirements for complying with IEC61000-3-2 Class C regulations power levels beyond 25 W, the performance of the different voltage-follower PFPs, and the application of the integrated buck-flyback converter for driving a 70 W LED assembly intended for street lighting applications. Moreover, dimming capability, or luminous output control, has already been mentioned as a topic to account for. Dimming operation, dimmed operation, or simply, dimming, is an interesting feature of high-performance LED drivers for power savings in sustainable lighting or building automation; or in ambient intelligence, where different scenes are pursued. In consequence, a strong research work is currently being developed in this field in backlighting systems, [6.1]-[6.4]; or general lighting such as in [6.5], where an adaptive voltage control is applied for active-equalisation and PWM dimming of low-power LED lamps. In [6.6], several paralleled LED strings are driven and equalised by means of either series pulse-width modulation (PWM) or by switching off certain strings. In [6.7], TRIAC-dimmer compatible drivers are studied and analysed. In reference [6.8], the authors propose a PWM dimming technique that is implemented in parallel to the load in a pure current-source buck converter. In [6.9], series PWM dimming is employed in a hysteretic boost converter. Other research efforts are focused on determining the behaviour of the analogue versus PWM dimming in terms of linearity, luminous flux control, and CCT and chromaticity coordinates shift [6.10]-[6.13], efficiency [6.14], [6.15], and long-term reliability [6.16], [6.17]. Other studies are focused on reducing both the radiated and conducted EMI of PWM dimming, such as in [6.18] and [6.22], where the PWM dimming is modulated by stochastic pulse density.

As can be found in literature, the most remarkable advantages of analogue over PWM dimming are a higher efficiency due to the droop effect, which forces the saturation of the luminous flux at high currents, and its higher simplicity and low cost due to its straightforward implementation just by varying the output current reference. On the contrary, PWM dimming offers a higher dimming ratio and a more linear regulation.

With regard to the chromaticity shift, two effects are to be accounted for: on the one hand, higher forward currents will imply a shift on the peak emission toward shorter wavelengths, i.e. toward blue, which also induces lower emission from the phosphor due to the deviation of the blue emission with respect to the phosphor best-absorbing wavelength. On the other hand, the increase in junction temperature will induce a shift in the peak emission toward larger wavelengths, this is, toward red, the phosphor absorbing a higher amount of blue light and thus, emitting a higher amount of yellow light. Higher chromaticity-coordinates stability in analogue dimming has been reported in [6.12], whereas PWM dimming has been proven to be more stable in [6.11]. However, the former performs analogue dimming from 100 mA to 1000 mA, PWM dimming driven under a 1000 mA peak-value current, whereas the latter sets the dimming at 350 mA peak current. Therefore, it can be concluded that these results are influenced by the driving current and the LED employed in the tests, not allowing for a generalisation.

In this work, both dimming techniques will be taken into account, since analogue dimming is sufficiently flexible at a low cost in street-lighting applications, where neither a high dimming ratio nor a tight control are required, and PWM dimming offers a better performance in commercial and general indoor lighting, provided that the dimming range is higher. Since the implementation of analogue dimming is straightforwardly achievable by adjusting the output current reference and this technique has already been introduced in Chapter 1, only PWM dimming will be comprehensively discussed.

6.2. Pulse-Width Modulated dimming

As disclosed in Chapter 1, pulse-width modulated dimming is based on supplying the LED load with a square-wave current, where the peak value is kept constant and the average value is modulated by the duty cycle. Fig. 6.1 shows the PWM-dimming operation principles introduced in Chapter 1, where the dimming period, T_{DIM}, the lit-on time, t_{ON}, the peak current value, I_D and the average value, I_{AVG} are highlighted, However, some definitions are to be presented. First, the dimming duty cycle, d_D, which sets the time for which the LED lamp is lit on over the dimming signal period:

$$d_D = \frac{t_{ON}}{T_{DIM}} \tag{6.1}$$

where the dimming period is the inverse of the dimming frequency: $T_{DIM} = 1/f_D$.

Another interesting parameter is the dimming ratio, or contrast ratio, *CR*, which establishes the maximum luminous flux attenuation achievable by the dimming scheme [6.11]-[6.21]:

$$CR = \frac{d_{D\_max}}{d_{D\_min}} : 1 \tag{6.2}$$

where d_{D_max} and d_{D_min} are the maximum and minimum dimming duty cycle that the dimming scheme can achieve, accounting for the delay times, and rising and falling edges. If the perfect square-wave output current is assumed, the *CR* can be diretly defined as:

$$CR = \frac{1}{d_{D\_min}} : 1 \tag{6.3}$$

Dimming ratios as high as 1000:1 have been reported in the literature [6.9].

According to the current waveform shown in Fig. 6.1, the average current can easily be obtained as:

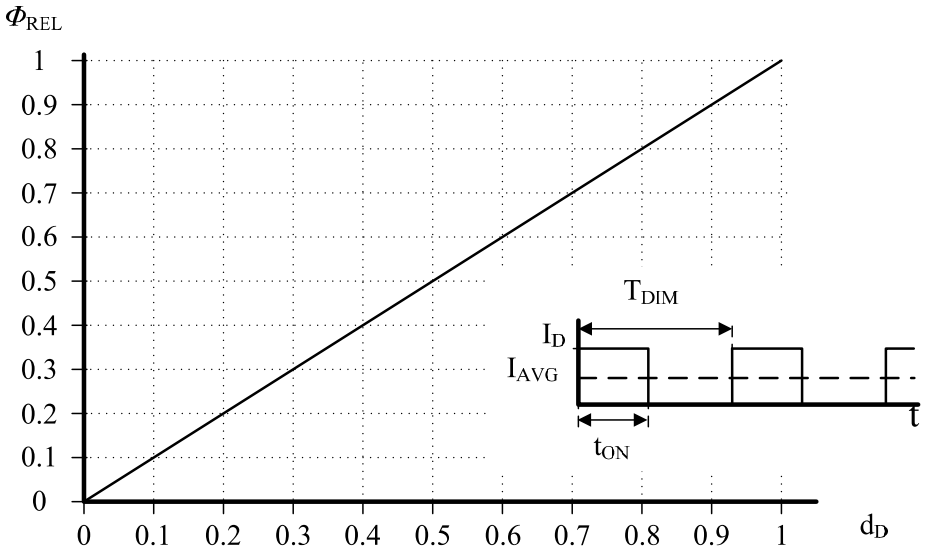

Fig. 6.1. Relative luminous flux as a function of the lit-on time of the Pulse-Width Modulation technique. The pulse train current is shown in the graph inset, where the dimming period, the lit-on time, the peak current value, and the average value are highlighted.

$$I_{AVG} = \frac{1}{T_{DIM}} \int_0^{d_D T_{DIM}} I_D dt = d_D I_D \tag{6.4}$$

Assuming constant junction temperature, the luminous flux, ϕ_D, will then be proportional to the maximum luminous flux, ϕ_K, corresponding to the current peak value, and the dimming duty cycle. Hence:

$$\phi_D = d_D \phi_K \tag{6.5}$$

However, since the dimming duty cycle affects the average power supplied to the LED, the junction temperature will also depend on that parameter, so the luminous flux will be affected, not performing linearly, although the linearity achieved is higher than that of the analogue technique [6.10], [6.15], [6.22], [6.23]. Several proposals have been made in order to overcome this issue. Thus, a flux estimator has been proposed in [6.10], achieving a high linearity. Also, more sophisticated dimming schemes have been developed, such as the bilevel dimming technique [6.15], where current-pulse train features a minimum current value, or more evolved techniques derived from the bilevel, as multivel and/or sequential PWM dimming patterns [6.23], [6.24].

With regard to the maximum dimming frequency and *CR* in order to achieve the most linear possible dimming linearity regarding the effects of junction temperature, the following affecting effects can be highgligthed: lag between the dimming signal and the converter response, and the converter slew-rate, both in the rising and falling edge. This is sketched in Fig. 6.2, where t_D is the converter lag, and t_{SU} and t_{SD} are the slope of the rising and falling edge, respectively.

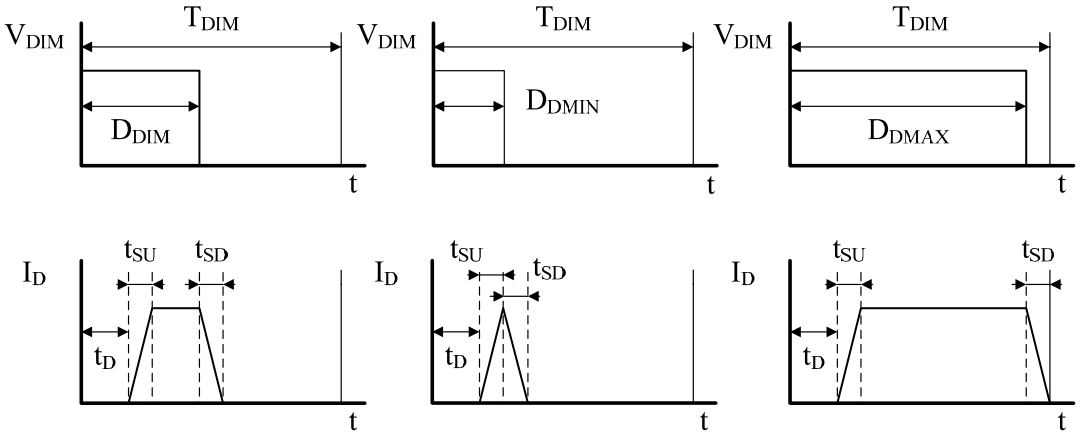

Fig. 6.2. Practical limitations for dimming frequency and dimming ratio. Left: converter lag, rising and falling edges affected by the converter slew-rate. Centre: minimum dimming duty cycle produced by rising and falling edge slopes. Right: maximum dimming duty cycle produced by converter lag and rising and falling edge slopes.

Thus, the maximum and minimum duty cycle can be calculated as:

$$d_{D\_min} = \frac{t_D + t_{SU}}{T_{DIM}} \qquad d_{D\_max} = \frac{T_{DIM} - t_{SD}}{T_{DIM}} \tag{6.6}$$

This yields the maximum *CR* achievable by the PWM dimming scheme after substituting (6.6) in (6.2):

$$CR_{max} = \frac{T_{DIM} - t_{SD}}{t_D + t_{SU}} : 1 \tag{6.7}$$

Since t_D and t_{SU} depend on the converter and the dimming control, and t_D depends more on the control scheme [6.20], [6.21], it can be seen that, for a given converter, the lower the dimming frequency, the higher the dimming ratio. In order to enhance the dimming performance, the following actions can be developed:

- Lowering the dimming frequency.
- Properly choosing and designing the converter topology and control scheme in order to enhance the slew-rate.
- Properly choosing the dimming scheme in order to reduce the rising and falling edge slopes.

Depending on the dimming scheme employed, the lag time and the rising and falling edges will differ. The basic PWM dimming techniques that are available in the literature are shown as follows [6.20], [6.21].

6.2.1. Enable dimming

This scheme is the simplest and most cost-effective PWM dimming scheme. It consists of alternately switching the converter on and off at high frequencies, thus dimming the lamp light. This is achieved by applying a logic-level PWM signal to the Enable/Disable or Shutdown pin featured by most of the drivers designed for general switched-mode power supplies (SMPS) applications, or to a specific dimming pin in LED drivers. Fig. 6.3 sketches this technique.

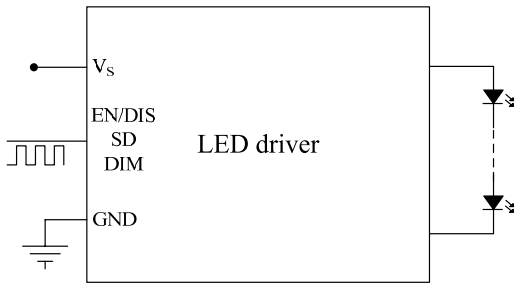

Fig. 6.3. PWM enable dimming scheme.

This technique is compatible with any topology and control loop [6.19]-[6.21]. However, the main drawback of this technique lies in the high dependence on the converter slew-rate, due to the fact that the delay and rise times will compromise the dimming frequency and will enlarge the time that LEDs spend between zero current level and DC current, where the chromatic characteristics of LEDs are not guaranteed. This matter is of vital importance in the case of power factor pre-regulators (PFP), whose slow dynamic response –usually around few tens of Hz and with a slow turn-on transient– would compromise the performance of this technique [6.20], [6.21]. Moreover, due to the low *CR* achievable by this technique, the dimming frequency should be around few hundreds of Hz, which could cause the injection of low-frequency conducted EMI into the AC supply.

6.2.2. Series dimming

When enable dimming is impractical due to the low dimming frequency required, or the low *CR* attainable, a series-dimming scheme can be implemented by placing a transistor in series to the LED load. This way, by varying the duty cycle of the PWM dimming signal applied to the dimming transistor, the LED load is open-circuited during the time needed for a given *CR*. This dimming scheme is depicted in Fig. 6.4.

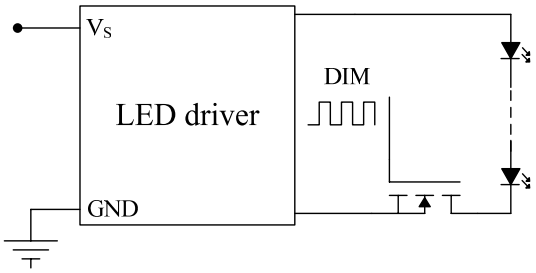

Fig. 6.4. PWM series dimming scheme.

General purpose SMPS usually feature voltage-mode PWM control or preferably current-mode programming (CMP), being the output voltage one of the parameters to be measured. The load can be switched on and off by means of a series transistor commanded by a PWM signal and the output voltage remains constant around the nominal value due to the energy stored in the output capacitor. In this case, linear post-regulators are to be used in order to supply the LED lamp adequately, but efficiency drops unless other control techniques are used, such as adaptive voltage control loops [6.25]. Nevertheless, LEDs are current controlled devices, so the feedback parameter is no longer the output voltage, but the LED forward current instead. When a current-controlled load is open-circuited, an extremely hard load transient takes place and the feedback loop is disconnected, leading the error-amplifier output signal to oscillation in some control schemes [6.20], [6.21], which rises the need for more specific control loops. Some strategies found in the literature are:

- Disconnection of the control loop while the lamp is open-circuited, although a larger rising edge is attributed [6.21].
- Feedback error-signal clamping so the oscillation is limited [6.20].
- Bus-voltage adaptive control techniques with post-regulators optimised for low power consumption [6.25].
- Peak-current or hysteretic control loops with feedback of output voltage and current in order to modify the output-current reference [6.9].

This dimming technique features high *CR* with dimming frequencies in the range of several hundreds of Hz or few kHz, with sharper rising and falling edges depending on the chosen strategy.

6.2.3. Parallel or shunt dimming

As LEDs are current-controlled devices, current-sourcing converters shall be used. This means that the LED forward current cannot be interrupted abruptly; otherwise overvoltage and oscillation problems would appear.

In this dimming technique, a transistor is placed in parallel to the load. Then, it is alternately switched on and off commanded by a PWM signal, shunting the LED load [6.8], [6.20], [6.21]. This is sketched in Fig. 6.5.

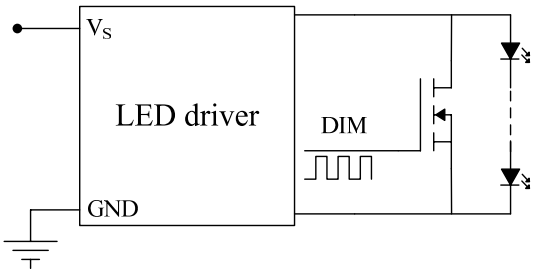

Fig. 6.5. PWM shunt dimming scheme.

This scheme allows the fastest dimming and highest dimming ratio possible, as all the delay and converter turn-on times are diminished, as well as the rising and falling edges. However, as the converter is kept working, the efficiency is slightly reduced due to the losses that take place in the dimming transistor during the lamp lit-off time.

This scheme is better suited to free-wheeling control loops, such as hysteretic control in HPF BCM converters, which might produce more injected EMI, making a more bulky EMI filter necessary. Another issue is that it is not an adequate solution when the converter requires the use of an output capacitor, such as boost or buck-boost topologies. In this case, the output capacitor will be short-circuited, generating a very high current spike through the switch. In addition, in the case of CCM boost- and buck-boost-based converters, an output short-circuit causes stability problems due to the RHP zero [6.20]. These issues make the shunt dimming technique unfeasible or at least hard to implement with boost and buck-boost topologies [6.20], [6.21]. An alternative where the inductor is short-circuited is presented in [6.26]

6.3. Dimming the IBFC LED driver

The dimming techniques exposed above were studied for its application to the IBFC controlled by a fixed-frequency constant-current control loop shown in Chapter 4. As long as analogue dimming is the simplest and cheapest technique used to vary the luminous flux output, the first test was to check the performance of this technique applied to the IBF converter. As analogue dimming is based on changing the output current DC value, the implementation of this technique is straightforward: by applying a variable DC voltage to the output current reference of the IBFC design example presented in Chapter 4. As the intended application of the IBFC was street lighting, a two-level analogue dimming could be enough [6.27]-[6.32]. In addition, Energy Star requirements state at least two levels, not including nominal output flux, ranging from 35% to 100% of the total output [6.33]. The output current was varied from a 20% of the nominal DC current, i.e. 70 mA, to a 100% of the nominal DC current, which is 350 mA, in 10% steps at 150 V_{rms} line voltage, in order to test the dimming performance under an intermediate supply. The obtained results were satisfactory, with a slight decrease of *PF* and efficiency at high dimming ratios, whereas the THD_I was kept constant. The experimental results are shown in Section 6.6. It has to be noted that the converter was not formerly optimised for dimming, so this line voltage selection is aimed on providing enough dimming ratio.

With the aim of extending its application from street lighting to general indoor/outdoor lighting, analogue dimming might be insufficient in order to develop a fully-featuring LED

driver. In this way, the PWM dimming technique has to be considered in order to overcome the disadvantages featured by analogue dimming.

Provided that PWM enable dimming is the simplest PWM dimming scheme, this was the first to be tested. These tests were carried out using the IBFC developed and tested in Chapter 4. The enable/disable dimming action was carried out by means of an external 125 Hz PWM signal applied to the output current reference. The experimental results measured at 230 V_{rms} input voltage are illustrated in Fig. 6.6.

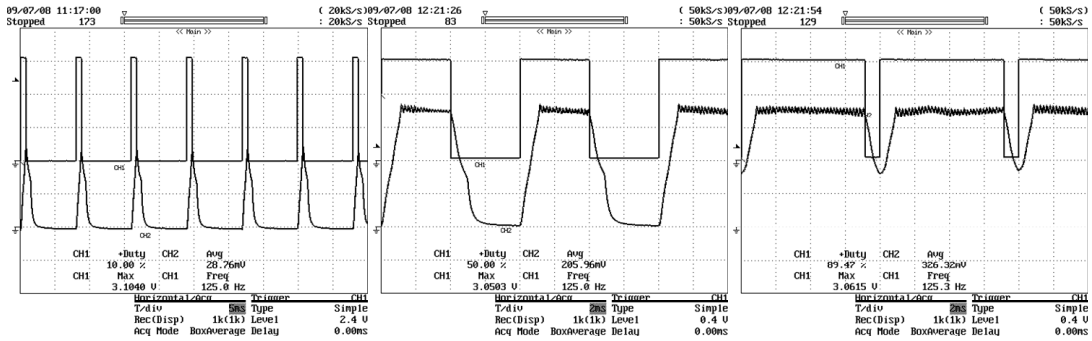

Fig. 6.6. PWM enable dimming test using a 125 Hz PWM signal reference. Channel 1 (top trace): Reference signal. Channel 2 (bottom trace): Output current. Left: 10% dimming duty ratio. Horizontal scale: 5 ms/div. Center: 50% dimming duty ratio. Horizontal scale: 2 ms/div. Right: 90% dimming duty ratio. Horizontal scale: 2 ms/div. Vertical scale: 1 V/div, 100 mA/div.

As can be seen, the obtained rise and fall times in the output current are approximately 1 ms. With these times, dimming ratios between 20 – 80% are easily achieved, leading to a 4:1 CR. This dimming ratio is adequate for most street, commercial and general lighting applications. It was also observed that at low dimming levels the linearity in output luminous flux is lost since the peak current does not reach the nominal value. For higher duty ratios the current waveform approximates to the DC level, which could cause a small displacement of the light colour coordinates and lack of linearity, yet acceptable for street lighting applications. On the other hand, no flicker was noticed even at the lowest dimming ratio, i.e. 10%. Fig. 6.7 shows the input power, output power and converter efficiency. It is remarkable that the converter behaves reasonably linear in terms of efficiency versus dimming ratio in the range between 20% and 80%.

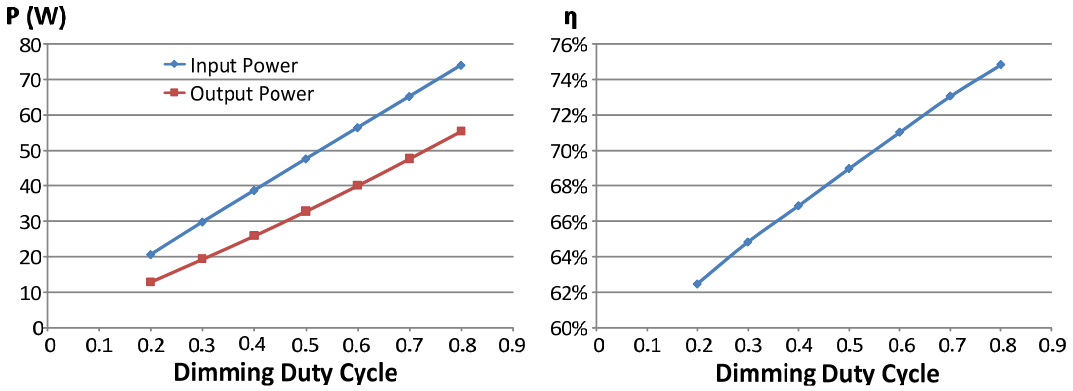

Fig. 6.7. PWM enable dimming test at 125 Hz. Left: Input power and output power vs. dimming ratio. Right: efficiency vs. dimming duty cycle. Input voltage: 230 V_{rms}.

It is also important to remark that one of the drawbacks of the enable-based dimming is the high THD_I obtained in the input current, which can reach more than 70% for minimum dimming levels. This is gathered in Table VI.1, where the values for the dimming duty ratio, d_D, output average current, $I_{o<AVG>}$, average output power, $P_{o<AVG>}$, efficiency, η, power factor, PF, and input-current total harmonic distortion, THD_I, are also included.

TABLE VI.I

EXPERIMENTAL RESULTS OBTAINED FROM THE DIMMING TEST AT 125 HZ

d_D (%)	$I_{o<AVG>}$ (mA)	$P_{o<AVG>}$ (W)	η (%)	PF	THD_I (%)
20	78.6	12.9	62.5	0.638	72.7
30	114.1	19.4	64.8	0.757	62.4
40	148.2	25.9	66.9	0.838	52.4
50	182.5	32.9	69.0	0.890	44.3
60	216.7	40.1	71.0	0.913	39.7
70	251.0	47.7	73.1	0.923	37.6
80	285.0	55.5	74.8	0.932	35.3
100	353.0	71.5	79.8	0.950	31.0

Due to the low CR achieved by the enable dimming test at 125 Hz, some modifications were made on the IBFC developed in Chapter 4 in order to improve the slew-rate of the converter, reducing the rising and falling edges as much as possible. This way, a higher gain 10 kHz cut-off frequency current sensor was used, whilst the output capacitor was reduced down to 1 µF in order to achieve the fastest dynamic response while keeping the high-frequency output-current ripple at a reasonable level, around 15%. In addition, the controller was also modified to the new configuration by placing the zero with a slight phase displacement regarding the converter low-frequency pole. Nevertheless, an adequate 2.7 kHz cross-over frequency and 63º phase margin were achieved. The loop-gain transfer function is shown in Fig. 6.8.

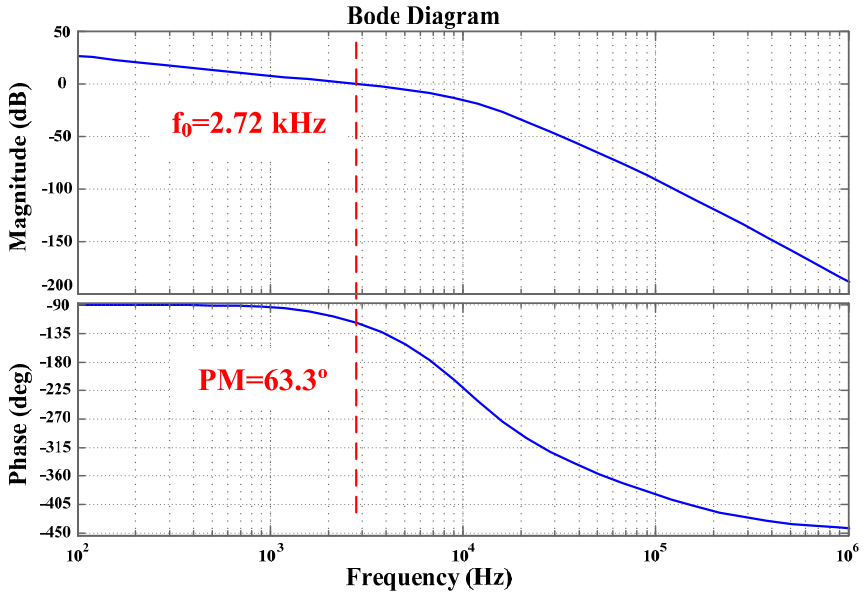

Fig. 6.8. Loop-gain transfer function Bode plot of the IBFC.

In addition, Fig. 6.9 shows the closed-loop transfer-function Bode diagram of the whole system, based on the same simplified model from Chapter 5.

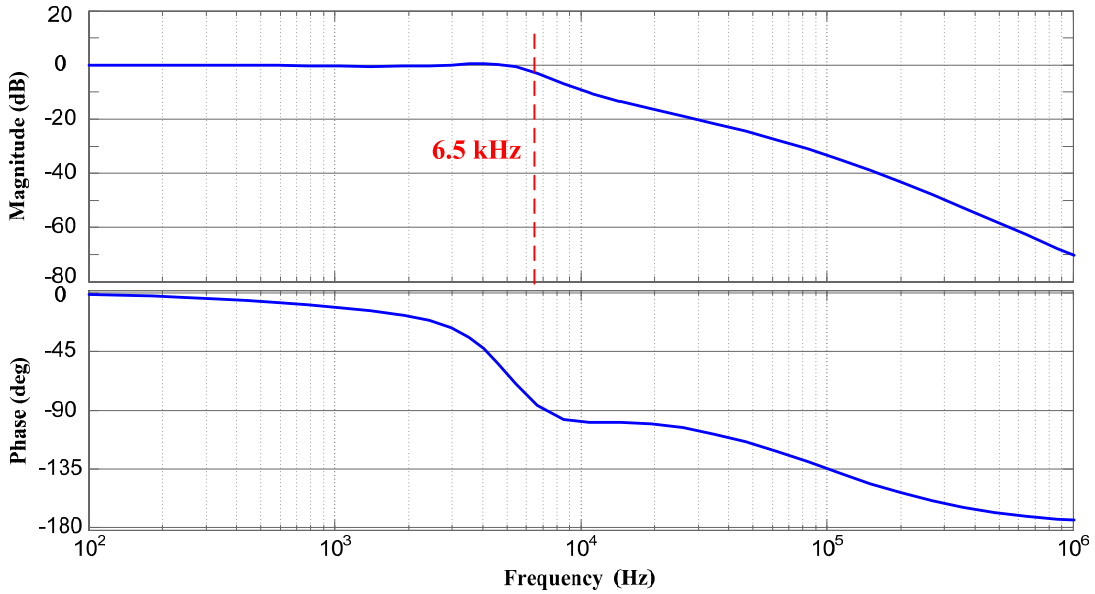

Fig. 6.9. Closed-loop transfer function Bode plot of the IBFC.

The first test was performed at 200 Hz, after the improvements were made in the converter, and as this is the minimum frequency recommended by some authors [6.21], with a dimming duty cycle ranging from 20 % to 80 %. However, although higher than in the previous test, the closed-loop converter slew-rate resulted too low for performing PWM enable dimming at 200 Hz satisfactorily. These results are shown in Fig. 6.10.

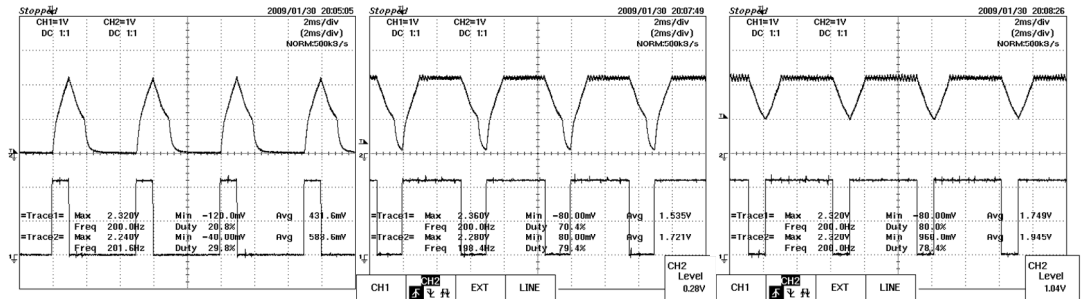

Fig. 6.10. PWM enable dimming test performed at 200 Hz. Left: 20% dimming duty cycle (5:1 dimming ratio). Centre: 70% dimming duty cycle (1.43:1 dimming ratio). Right: 80% duty cycle dimming (1.25:1 dimming ratio). Upper trace: output current. Vert. scale: 150 mA/div. Lower trace: PWM dimming signal. Vert. scale: 1 V/div. Horiz. scale: 2 ms/div.

As can be seen from Fig. 6.10, a short lag, t_D, is present, although the limiting parameters are the rising and falling time, t_{SU} and t_{SD}, respectively, around 0.5 ms for the former and 1 ms for the latter. This way, 20% is the minimum dimming duty cycle in order the output current to reach the peak value

After that, a 100 Hz test was carried out in order to check the converter dynamic limits and its behaviour when being dimmed at such a low frequency. The results obtained are shown in Fig. 6.11.

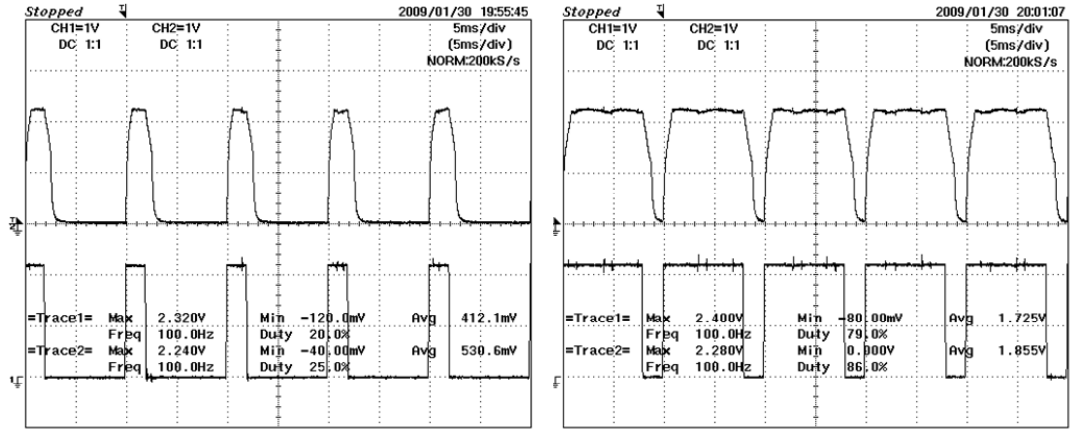

Fig. 6.11. PWM enable dimming test performed at 100 Hz. Left: 20% dimming duty cycle (5:1 dimming ratio). Right: 80% duty cycle dimming (1.25:1 dimming ratio). Upper trace: output current. Vert. scale: 150 mA/div. Lower trace: PWM dimming signal. Vert. scale: 1 V/div. Horiz. scale: 5 ms/div.

As can be seen, the converter is at best capable of achieving only low dimming ratios, whereas the line current is highly distorted. Indeed, a 70% THD_I was measured as long as the PF was decreased down to 0.59 for a 5:1 dimming ratio.

According to the results obtained from the PWM enable dimming test, the unfeasibility of PWM enable dimming applied to the IBFC featuring an average-current, fixed-frequency control is stated due to the low dimming frequency needed for a satisfactory dimming ratio, which increases the harmonic content of the input current, worsening the power factor due to the strong modulation imposed by the PWM dimming at low frequencies. In addition, the THD_I also depends on the synchronisation of the dimming signal with the line voltage, since the converter might be drawing current like a TRIAC dimmer, if a proper synchronisation is obtained, or, on the contrary, a more distorted current is achieved. This is shown in Fig. 6.12, together with the THD_I achieved in each test, which is highlighted in the figure.

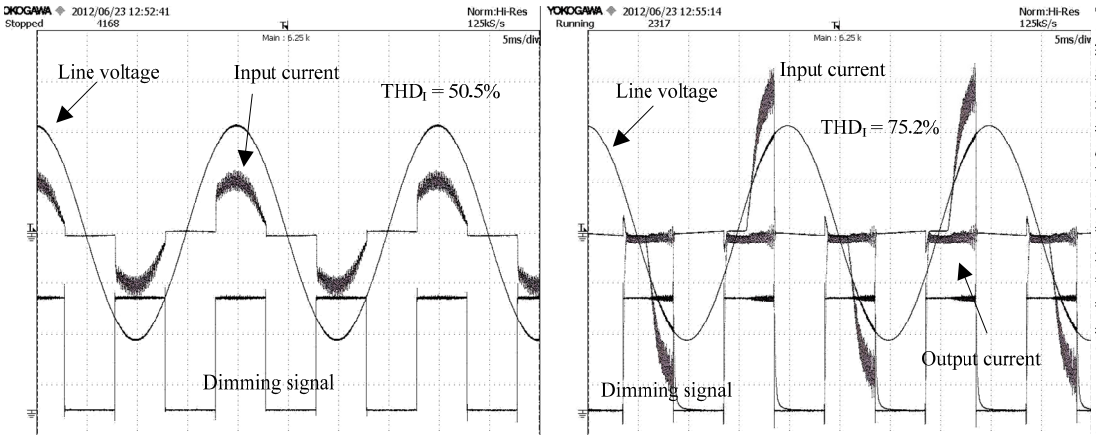

Fig. 6.12. 100 Hz PWM enable dimming test at 2:1 dimming ratio. Left: proper synchronisation with line voltage. Right: bad synchronisation with line voltage. The achieved THD_I is stated. Vertical scale: line voltage, 100 V/div; input current, 500 mA/div; output current, 100 mA/div; dimming signal, 1 V/div. Horizontal scale: 5 ms/div.

6.4. Enhanced PWM enable dimming

It was noticed during the enable dimming tests that a dimming-frequency limiting factor was the dynamic response of the controller. This way, after the reference signal is set to zero, the controller signal still needs a time lapse to reach the zero level and therefore, to stop the energy processing. This issue was solved by a modification on the control circuitry, by placing an AND gate whose inputs are the gate signal coming from the PWM modulator, and the PWM dimming signal. An SPW17N80C2 CoolMos from Infineon was used in these tests. This is depicted in Fig. 6.13.

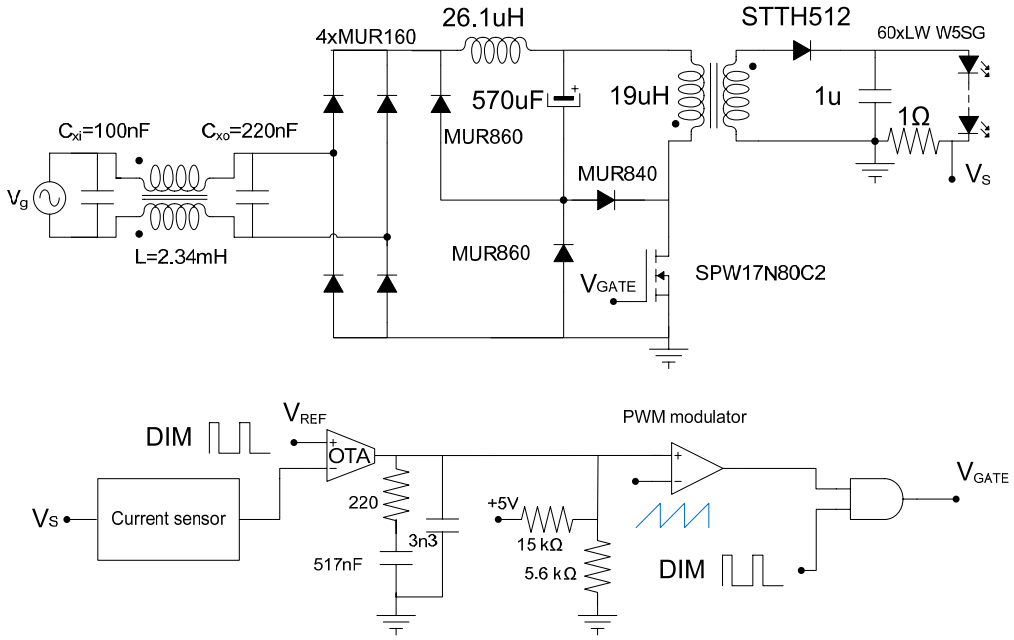

Fig. 6.13. Enhanced PWM enable dimming schematics.

This new configuration achieved a higher dimming frequency due to the improved control of the transistor gating signal, also extending the dimming ratio to 10:1 at frequencies up to 300 Hz. Fig. 6.14 shows the experimental results for PWM enable dimming performed at 200 Hz. Three operation point are shown: 10%, 50% and 90% dimming duty cycle.

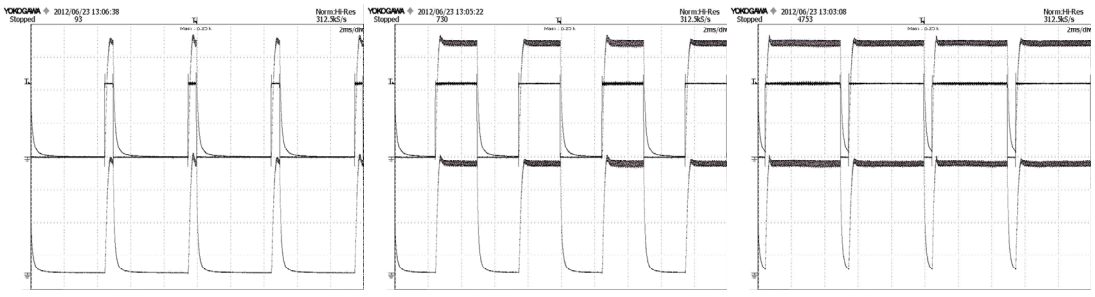

Fig. 6.14. Enhanced PWM enable dimming test at 200 Hz. Left: 10:1 dimming ratio (10% dimming duty cycle); centre: 2:1 dimming ratio (50% dimming duty cycle); right: 1.11:1 dimming ratio (90% dimming duty cycle). Upper trace: output power, 20 W/div. Centre trace: dimming signal, 1 V/div. Bottom trace: output current, 100 mA/div. Horizontal scale: 2 ms/div

As can be seen from Fig. 6.14, the rising and falling edges are steeper in this enhanced PWM enable dimming scheme, with a high linearity between output current and dimming duty

cycle for a 10:1 dimming ratio. However, as in the previous enable dimming test, the THD_I was highly affected by the dimming duty cycle, reaching values around 94% for the 10:1 dimming ratio. As can be seen, the only way to reduce the impact of PWM enable dimming on the THD_I relies on increasing the dimming frequency so it is out of the IEC 61000-3-2 Class C scope, i.e. above the 40th harmonic, which is 2 kHz for a 50 Hz-based line. However, only a fairly satisfactory dimming performance from 20% to 80% dimming duty cycle was achieved at dimming frequencies as high as 500 Hz.

The dimming performance at 500 Hz as well as the input current for 10%, 50% and 90% dimming duty cycles are depicted in Fig. 6.15.

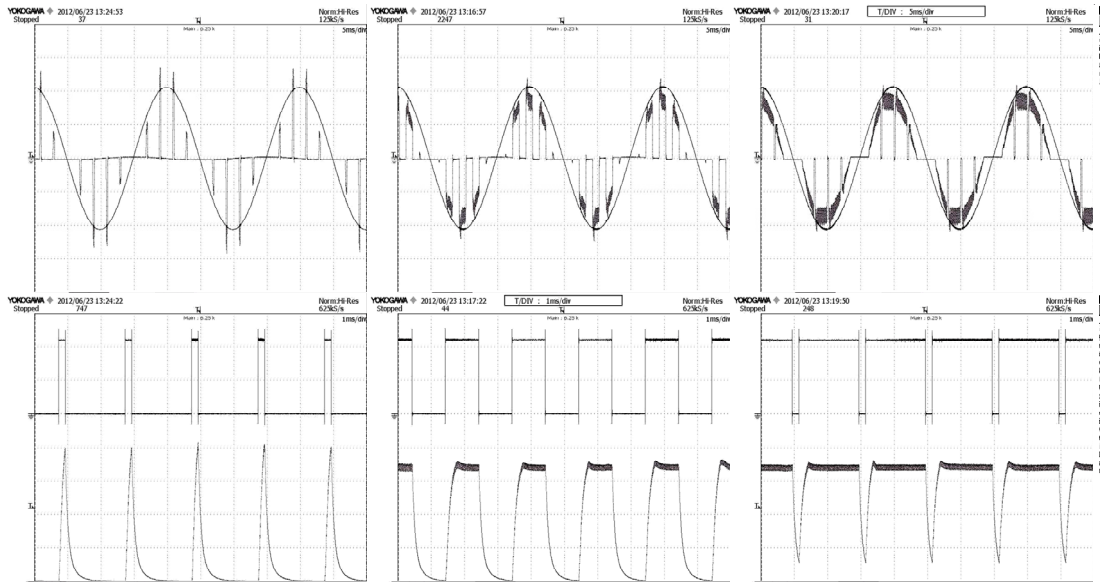

Fig. 6.15. Enhanced PWM enable dimming test at 500 Hz. Left: 10:1 dimming ratio (10% dimming duty cycle); centre: 2:1 dimming ratio (50% dimming duty cycle); right: 1.11:1 dimming ratio (90% dimming duty cycle). Top: line voltage and input current. Vertical scale: 100 V/div, 500 mA/div. Horizontal scale: 5 ms/div. Bottom: PWM dimming signal (upper trace), 1 V/div; output current (lower trace), 100 mA/div. Horizontal scale: 1 ms/div.

As can be seen from Fig. 6.15, although the rising and falling times are highly improved compared to the former PWM enable dimming scheme, the enhancement is enough only to reach a maximum dimming frequency below 500 Hz for a high dimming ratio. In this case, good linearity is assured only for dimming duty cycles ranging 20% - 80%. Moreover, the input current is highly distorted by the PWM modulation frequency, which is kept within the audible range and the Class C requirements scope. Therefore, a higher-frequency dimming techinque is to be studied.

6.5. PWM series dimming: issues and study of the sensitivity function

After proving that PWM enable dimming is unfeasible, even the enhanced scheme, and discarding the PWM shunt dimming technique since being incompatible with an output capacitor, the PWM series dimming technique is taken into consideration for the PWM dimming capability research.

A generic PWM-mode controlled converter featuring PWM series dimming can be modelled as shown in Fig. 6.16, where the series dimming action is approximated as a perturbation, *p(s)*, applied to the controlled output, *y'(s)*.

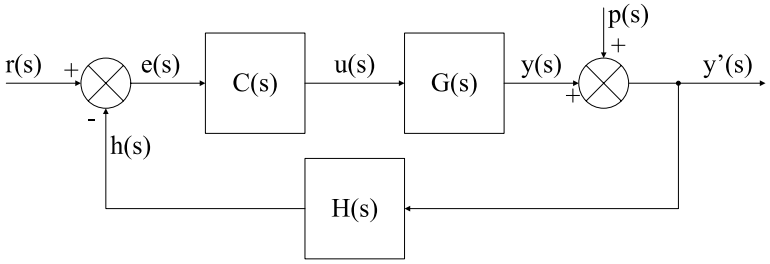

Fig. 6.16. Closed-loop block diagram of the IBFC featuring PWM series dimming, considering the series dimming transistor as an output perturbation.

Where *C(s)* is the controller; *G(s)* is the converter; *H(s)* is the feedback filter; *r(s)* is the output current signal; *e(s)* is the error signal; *h(s)* is the feedback signal; *u(s)* is the control signal; *y(s)* is the output signal in no dimming operation; *p(s)* is the dimming signal and *y'(s)* is the output current perturbed by the dimming transistor, this is, the pulsed output current signal when the converter is being dimmed.

As stated in Section 6.2.2, the PWM series dimming technique may lead a fixed-frequency constant-current-controlled converter to oscillation due to the high unload transient that an open-circuit at the output implies [6.20], [6.21]. This behaviour can easily be understood from the control sensitivity function, $S_u(s)$, which provides information about the controller capability for rejecting output perturbations:

$$S_u(s) = \frac{H(s)C(s)}{1 + C(s)G(s)H(s)} \tag{6.8}$$

The $S_u(s)$ function is defined from the closed-loop output to the controller signal. This means, from *p(s)* to *u(s)*, as shown in Fig. 6.17.

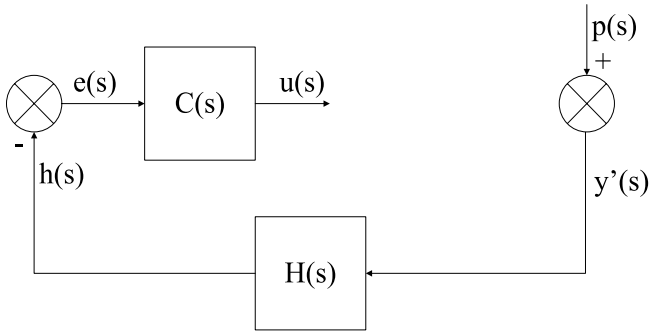

Fig. 6.17. Block diagram for the study of the control sensitivity function, $S_u(s)$.

The control sensitivity function can be applied to the simplified dynamic model of the IBFC in order to study the effects of a load transient on the control signal. This is depicted in Fig. 6.18.

As can be noticed, low-frequency output perturbations will be slightly attenuated and in phase opposition to the control signal. Furthermore, in this case there is a range of frequencies around 6 kHz which will actually be amplified. This means that the control signal will indeed be a square wave ranging from zero to the error-signal clipping-voltage value. Hence, as PWM dimming signals in the low-frequency range will cause harmonics in this frequency region, the output perturbations will be amplified, leading the converter to oscillation or even to a high in-

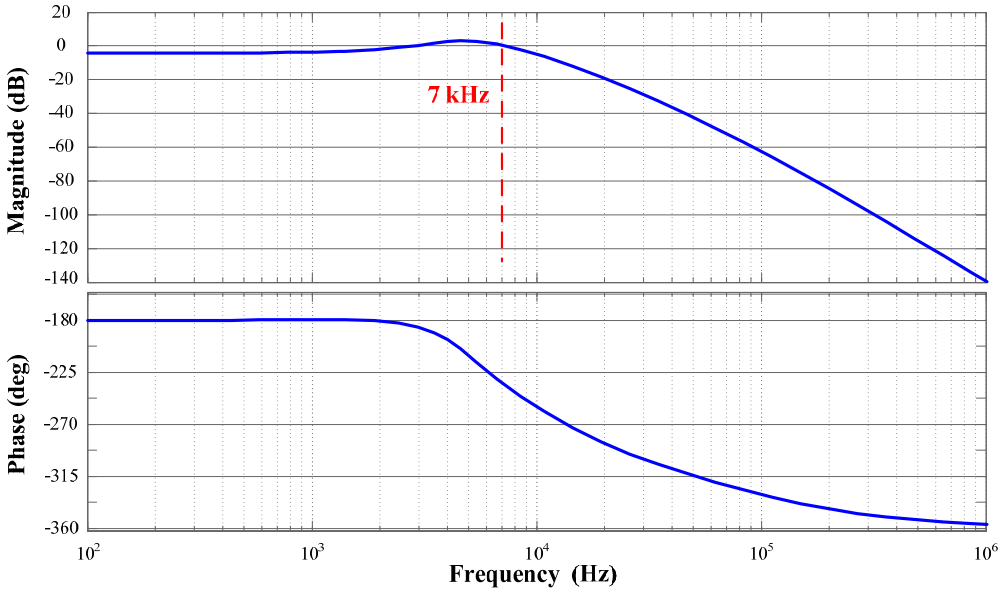

Fig. 6.18. Control sensitivity function, $S_u(s)$, of the simplified dynamic model of the IBFC.

rush current. It should be noted that most usual dimming frequencies are located in the range from few hundreds of Hz to few kHz. Therefore, if a low-frequency PWM series dimming is to be implemented, complementary strategies should be taken into account, such as those listed in Section 6.2.2, of which the simplest one consists of disconnecting the control loop while the lamp is lit off. Clamping the feedback signal is also simple to implement. However, this only limits the control signal oscillation. In addition, since the converter is expected to operate under universal input voltage, the oscillation would not be limited under certain line voltages.

Moreover, the output perturbations in the high-frequency range will be filtered and highly phase-shifted. In this case, frequencies above 7 kHz will be highly attenuated, with a 60 dB/dec slope. This means that the controller will not be capable of acting on the AC component of the output current, but on the DC value instead.

6.5.1. PWM series dimming with disconnection of the control loop

Since a harsh output perturbation at low frequencies such as a series dimming action would make the converter to oscillate, a low-frequency PWM series dimming scheme should introduce a control-loop disconnection feature to prevent the control signal to from oscillation. This technique has already been introduced in [6.9]. Thus, starting from the schematics shown in Fig. 6.13, an IRF840 series dimming transistor is introduced. This schematics is shown in Fig. 6.19.

Based on the same control loop as the enhanced PWM enable dimming scheme, the addition of the series transistor allows for steeper rising and falling edges, which will lead to higher dimming ratios and frequency. Indeed, the dimming ratio could be extended to 20:1, i.e. to a 5% dimming duty cycle with no output-current oscillation and only a slight decrease on the peak current. In addition, the synchronous transistor used in these tests was an STW12NK80Z from ST. A first test was carried at 1 kHz, which is a usuall dimming frequency. The experimental results for the output current are shown in Fig. 6.20 for 10% and 90% dimming duty cycle.

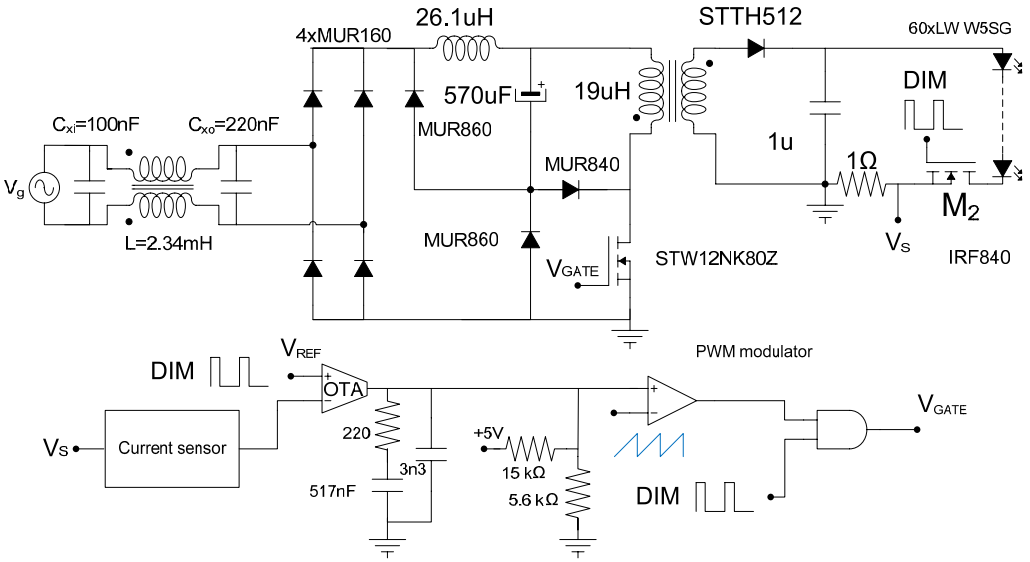

Fig. 6.19. PWM series dimming schematics.

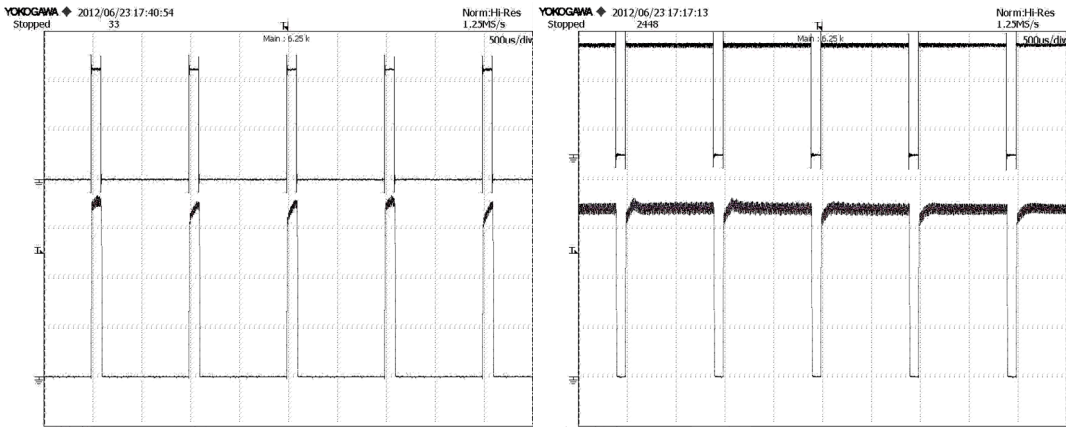

Fig. 6.20. PWM series dimming test at 1 kHz. Left: 10:1 dimming ratio (10% dimming duty cycle). Right: 1.11:1 dimming ratio (90% dimming duty cycle). Upper trace: PWM dimming signal, 1 V/div. Lower trace: output current, 100 mA/div. Horizontal scale: 500 μs/div.

As can be seen from the results obtained in Fig. 6.20, the rising and falling edges are practically instantaneous for a 1 kHz dimming frequency, achieving a high linearity between average output current and dimming duty cycle, which will also assure a high linearity between dimming duty cycle and luminous output, at the expense of the non-linearity introduced by the dependence of junction temperature on the average power and in turn, the dependence of luminous depreciation on junction temperature.

In addition, the 1 kHz dimming frequency represents the 20th harmonic in a 50 Hz line. As a consequence of performing the input current modulation at an even harmonic, the resulting energy in the discrete Fourier transform (DFT) will be cancelled at the PWM fundamental harmonic and its energy will be spread across adjacent harmonics, resulting in lower harmonic peaks. This could help the input current individual harmonics to be kept below the IEC 61000-3-2 Class C mask. Nevertheless, the 19th and 21st harmonics are above the mask for even a 90% dimming duty cycle. Fig. 6.21 shows the input current for a 10%, 50% and 90% dimming duty

cycle, whereas Fig. 6.22 shows the input current harmonic content for the 50% dimming duty cycle.

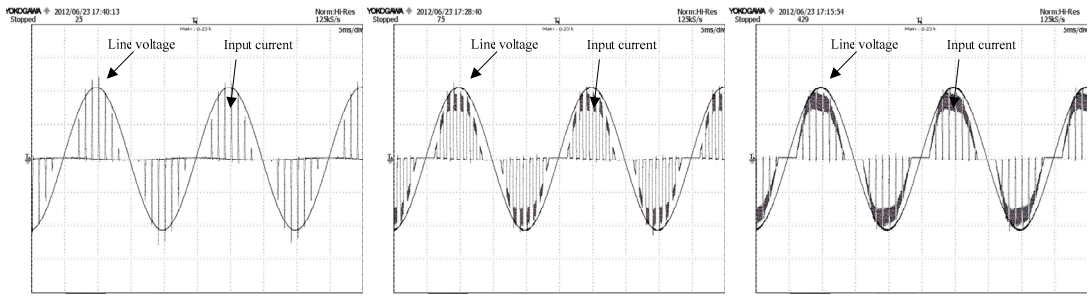

Fig. 6.21. PWM series dimming test at 1 kHz: line voltage and input current. Left: 10% dimming duty cycle. Centre: 50% dimming duty cycle. Right: 90% dimming duty cycle. Vertical scale, 100 V/div, 500 mA/div. Horizontal scale: 5 ms/div.

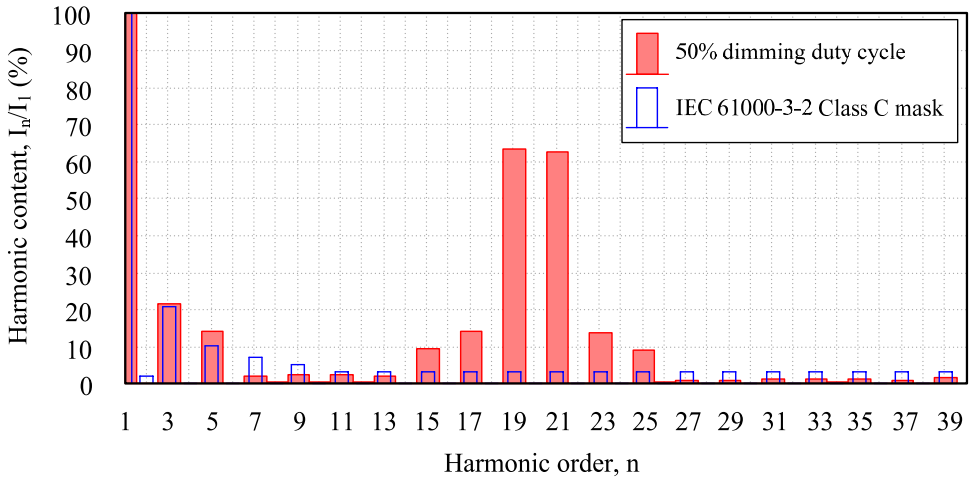

Fig. 6.22. Input-current harmonic content for the PWM series dimming scheme performed at 1 kHz and with 50% dimming duty cycle.

As can be seen from Fig. 6.22, the strong modulation induced by the burst operation in this PWM series dimming scheme highly increases the THD_I, and reduces the *PF*. This issue could be solved by proper sizing of the EMI filter. However, for such low dimming frequencies, the EMI filter needed would be bulky, making this technique disadvantageous. Another solution would be to increase the dimming frequency beyond the Class C scope. Hence, performing PWM series dimming at 2 kHz would still introduce some harmonic content in the 37th and 39th harmonics in 50 Hz based lines. Therefore, dimming frequencies beyond 2.5 kHz, which are also beyond the 40th harmonic in 60 Hz lines, should be employed. The PWM series dimming technique was also tested at 3 kHz and 5 kHz, the experimental results for the output current for 10% and 90% dimming duty cycles being displayed in Fig. 6.23.

As can be seen from Fig. 6.23, a 10:1 dimming ratio is not achievable, since the output current hardly reaches 250 mA peak value. In addition, a small low-frequency oscillation was detected at both test frequencies. Nevertheless, there is no harmonic distortion in the input current after performing the DFT for the first 40 harmonics. However, it has to be noted that the *PF* is degraded due to the input-current burst consumption. This issue could be solved with the addition of a low-pass filter specifically designed for the dimming frequency, which would lead

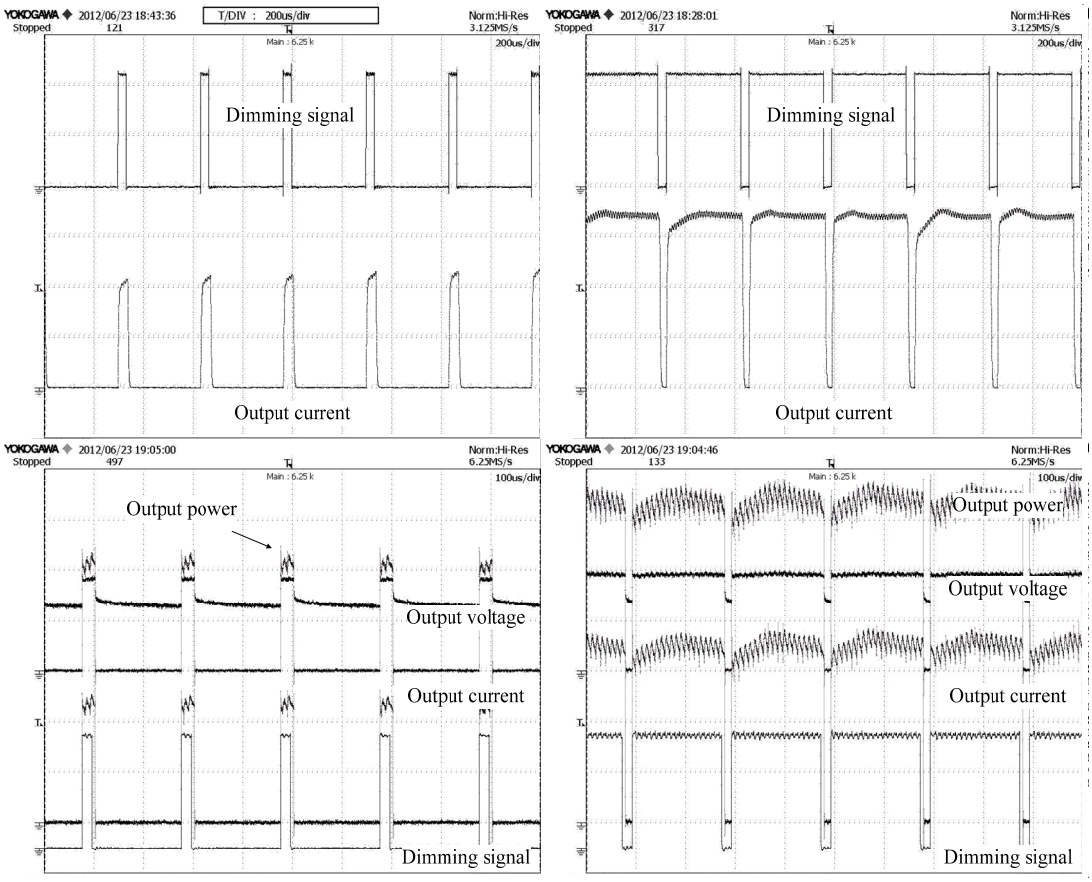

Fig. 6.23. PWM series dimming test. Top: test at 3 kHz. Bottom: test at 5 kHz. Left: 10% dimming duty cycle. Right: 90% dimming duty cycle. Vertical scale: dimming signal, 1 V/div; output current, 100 mA/div; output voltage, 100 V/div; output power, 20 W/div. Horizontal scale: 3 kHz test, 200 μs/div; 5 kHz test, 100 μs/div.

to a bulkier EMI filter. This issue would be solved by pushing the dimming frequency beyond 20 kHz in order to use a small EMI filter and to avoid acoustic noise. This way, PWM dimming at 20 kHz, 50 kHz and 100 kHz was tested. However, even at 20 kHz a 90% dimming duty cycle is not achievable due to the time response of the dimmig circuit, leading to continuous current instead of a pulse-width modulated output current. Moreover, a strong low-frequency oscillation appears for the three dimming frequencies tested due to the dimming-circuit time response. This phenomena are illustrated in Fig. 6.24. Therefore, it can be concluded that PWM series dimming is not a practical dimming method for IPCs, since the dimming modulation is directly transmitted to the input current, degrading *PF* and THD_I at low dimming frequencies, and degrading *PF* too and leading the converter to oscillation at high dimming frequencies.

Further experimental results will be provided and discussed in Section 6.6.

6.5.2. PWM series dimming: The High-Frequency Technique

The high-frequency filtering effect reported in Section 6.4 and shown in Fig. 6.18 is quite interesting for low slew-rate or slow-dynamics converters, such as integrated single-stage topologies or especially one-stage PFP, as the crossover frequency is located at frequencies lower than a decade below the switching frequency in the former case or below twice the line frequency in the latter case. Then, dimming frequencies above the audible range but lower than

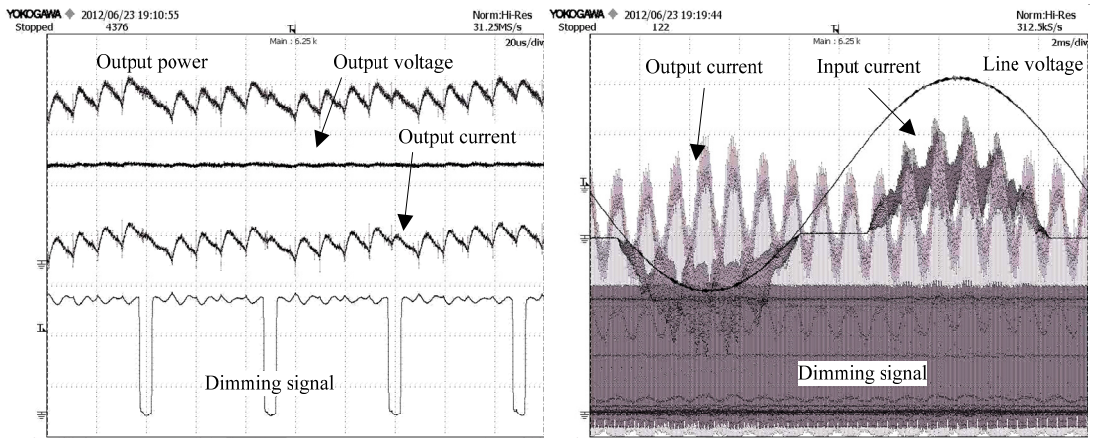

Fig. 6.24. PWM series dimming test at 20 kHz. Left: 90% dimming duty cycle. Vertical scale: dimming signal, 1 V/div; output current, 100 mA/div; output voltage, 100 V/div; output power, 20 W/div. Horizontal scale: 20 μs/div. Right: 50% dimming duty cycle. Vertical scale: line voltage, 100 V/div; input current, 500 mA/div; dimming signal, 1 V/div; output current, 100 mA/div. Horizontal scale: 2 ms/div.

the switching frequency can be selected, implementing the high-frequency series (HFS) dimming technique.

Thanks to this filtering action, it is easy to see that as the dimming ratio is increased, this is, the dimming duty cycle is reduced, the output current mean value, I_{AVG}, perceived by the controller is decreased, as follows:

$$I_{AVG} = \frac{1}{T_{DIM}} \int_0^{d_D T_{DIM}} I_{PK} dt = d_D I_{PK} \tag{6.9}$$

where I_{pk} is the peak value of the output current, i.e. the DC current level. It has to be noted that at such high frequencies, the output voltage can be considered constant owing to the output capacitor. In addition, since the converter is controlled by an average-current, fixed-frequency loop, it implies that the output power is kept constant during the PWM dimming operation. As a consequence of this, under PWM dimming operation, the average output current, and the reference signal become unbalanced. Therefore, the controller will increase the control signal in order to match both signals:

$$V_H = V_R = H_0 d_D I_{PK} \tag{6.10}$$

where V_H is the feedback signal; V_R is the reference signal; and H_0 is the feedback sensor DC gain, in terms of V/A. From (6.10), it is easy to see that the increase in the output-current peak value, I_{pk}, is proportional to the inverse of the dimming duty cycle. This way, if the output current reference, *r(s)* in Fig. 6.16, is properly modified, the output current peak value will be kept constant. The proposed control block diagram used to modify the output-current peak level according to the proposed strategy is shown in Fig. 6.25.

The feedback signal, V_H, this is, the DC level provided by the sensing filter, is proportional to the dimming duty-cycle, d_D, and the output-current peak value, I_{pk}. Therefore, these signals are to be varied accordingly in order to obtain a dimming duty-cycle dependant reference that keeps the output-current peak value constant. This is achieved by multiplying the output current reference, V_{RP}, by the dimming duty cycle, d_{avg}, so that a new output current reference, V_R, is generated. Afterwards, this new reference is compared to the feedback signal, V_H, in order to

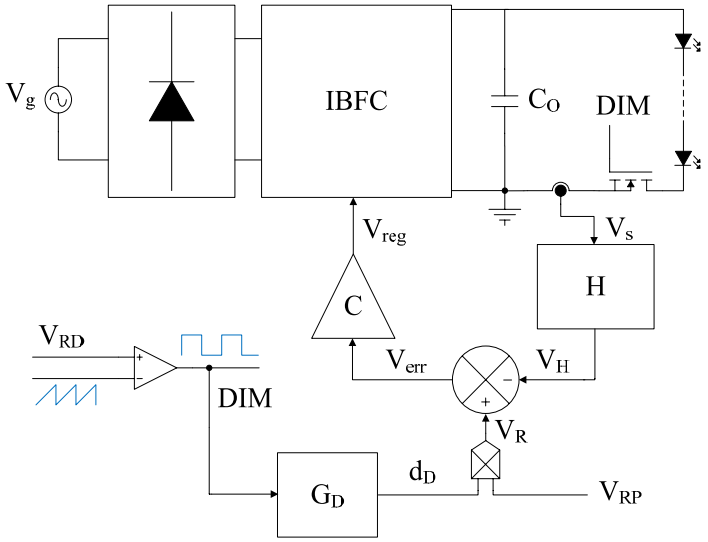

Fig. 6.25. Block diagram of the HFS dimming scheme.

obtain the error signal, V_{err}, which will be processed by the controller, block C, to generate the control signal, V_{reg}. The PWM dimming signal, DIM, is filtered by the block G_D in order to obtain the value for the dimming duty cycle, d_D, which will be multiplied by the output current reference, the signal V_{RP}.

There is a simplification for this scheme that avoids the use of the multiplier, as shown in Fig. 6.26.

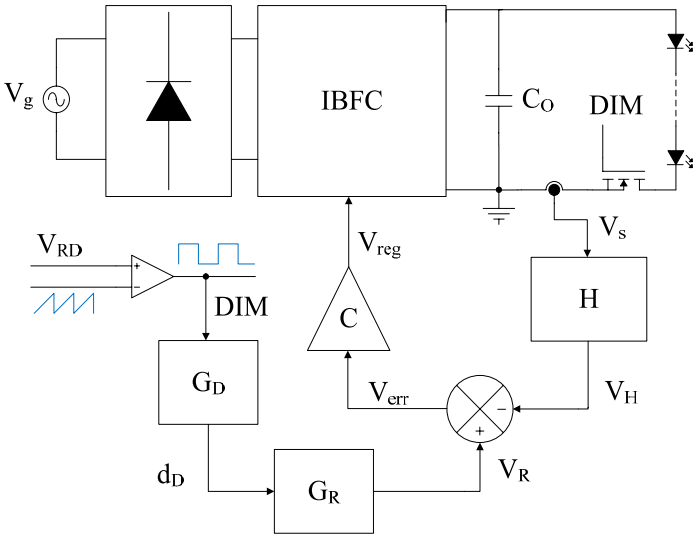

Fig. 6.26. Block diagram of the simplified HFS dimming scheme.

The new output current reference, V_R, is generated by means of a gain block, G_R. In this solution, a fixed output-current peak value is featured. Thus, the only system input variable is the dimming ratio reference, V_{RD}, which modifies the output-current average value, analogueously to the scheme presented in Fig. 6.25.

A prototype was built and tested at the laboratory. Generally, EMI concerns are supposed to rise as dimming frequency is increased. However, dimming frequencies above 20 or 25 kHz are considered to be advantageous since audible emissions are eliminated [6.34]. This way, the

dimming frequency was set to 100 kHz, the same as the switching frequency, for the sake of simplicity. Besides, this allows both switches to be operated synchronously, avoiding the generation of additional EMI harmonics. The control scheme implemented in the laboratory tests is depicted in Fig. 6.27.

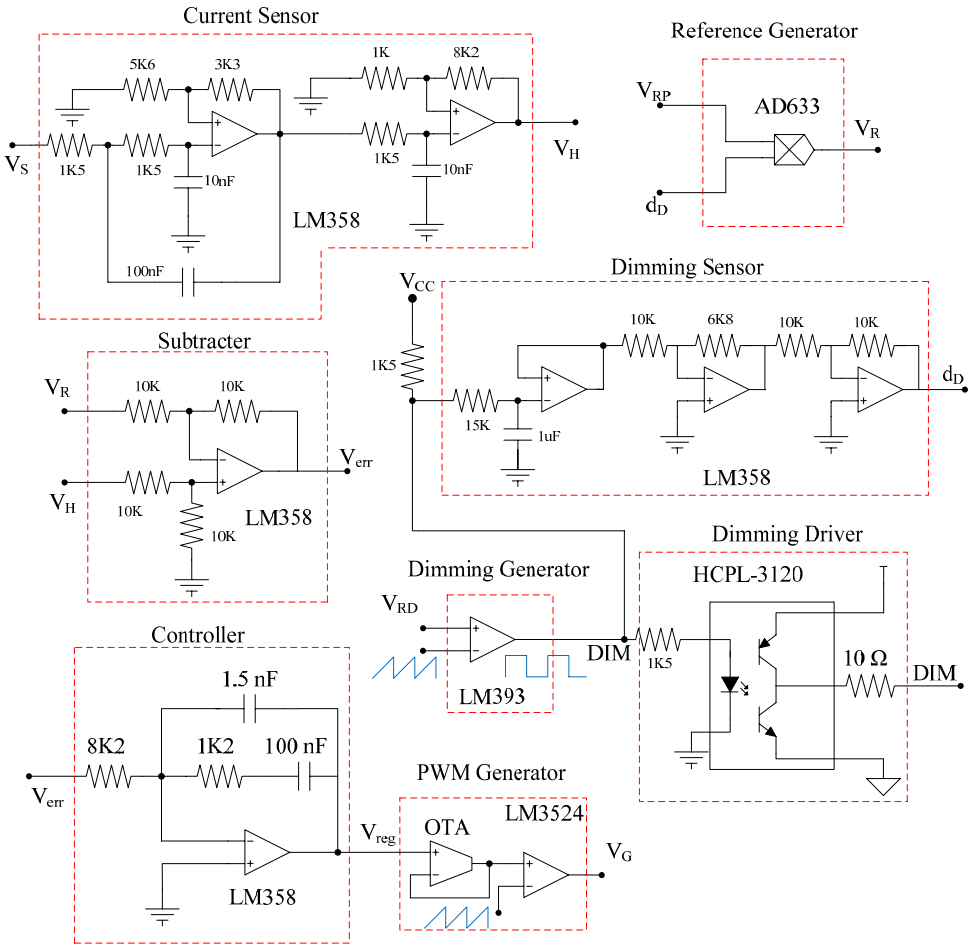

Fig. 6.27. Dimming-technique control-circuit scheme. Blocks current sensor, reference generator, subtracter, dimming sensor, dimming generator, dimming driver, controller, and PWM generator are highlighted.

The 100 kHz signal generated by the LM3524 IC is a 0.6 to 3.8 V saw-tooth wave. This signal is compared to the dimming reference, V_{RD}, by means of an LM393 comparator in order to generate the PWM dimming signal. This block is labeled as *Dimming Generator* in Fig. 6.27. This PWM dimming signal is then applied to an IRF840 MOSFET transistor through the *Dimming Driver*.

The average PWM dimming value, d_D, is extracted by means of a first-order low-pass filter, labeled as *Dimming Sensor* in the figure, implemented with an LM358 IC. Its cut-off frequency was set to 10 Hz to remove the high frequency ripple completely. After that, the signal is normalized to a 0 – 10 V range.

The new output current reference is generated by multiplying the dimming duty-cycle value, d_D, and the output current reference, V_{RP}. For this purpose, an AD633 analogue multiplier is used, labeled as *Reference Generator* in Fig. 6.27. Afterwards, this signal is compared to the feedback signal, i.e. the *Current Sensor* signal, in the *Subtracter* block shown in Fig. 6.27 in order to obtain the error signal, V_{err}, which will be processed by the *Controller* to generate the

control signal, V_{reg}. The *Subtracter* block is implemented by an LM358 IC in a differential amplifier configuration.

As the new gain configuration for the *Current Sensor* block could imply the output current reference, V_{RP}, to go out of the OTA common-mode input voltage, a new proportional-integral (PI) compensator was implemented using the LM358 IC, labelled as *Controller* in Fig. 6.27. Its root locus is maintained from the former version discussed in Section 6.3. However, the LM3524 IC was kept for working as a PWM generator. Finally, a decoupled *Dimming Driver* was built using an HCPL-3120 optocoupler with an isolated voltage supply.

Since the root locus is maintained, the closed-loop and loop-gain transfer functions are the same as in Fig. 6.8 and Fig. 6.9 in Section 6.3. The topology used in the tests is presented in Fig. 6.28. An overcurrent snubber was implemented, as shown in Fig. 6.28, where L_S is the snubber inductor, R_L is its series resistance and D_L is the free-wheeling diode. This snubber circuit is used in order to prevent from permanent damage in the light emitters caused by peak-current stresses at the output-current rising edges due to the output-capacitor instantaneous discharge through the LED load.

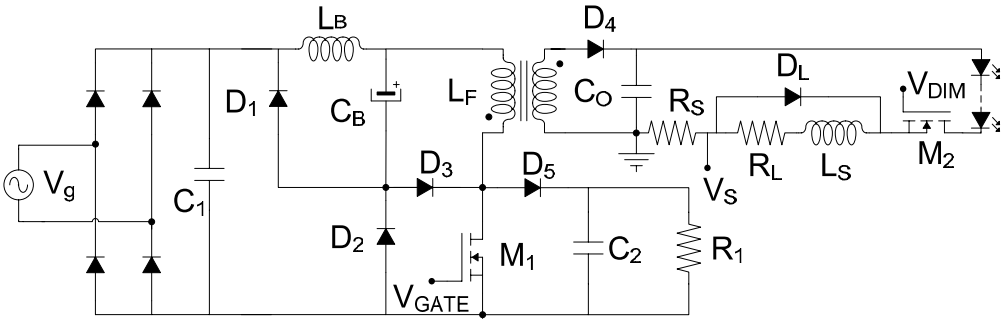

Fig. 6.28. HPF IBFC topology with overcurrent snubber employed for supplying the LED load and performing PWM HFS dimming and PFC.

The converter was tested in closed-loop at 150 V_{rms} input voltage as in the analogue dimming and PWM series cases in order to check its dimmability and comparable PFC performance along the entire dimming range.

The dimming results are shown in Fig. 6.29, where four different operation points are depicted: 350 mA DC output current and 100%, 70%, 50%, and 10% dimming duty cycle, i.e. 10:1 dimming ratio. The overcurrent snubber was proven to cancel the overcurrent stress for a highly wide dimming range, while showing fast rising and falling edges. This means that the former dimming capability has not been affected. As can be inferred from this test, at least a 10:1 dimming ratio capability has been achieved, which is satisfactory for most general applications.

With regard to the input-current harmonic content, Fig. 6.30 shows how the input current is hardly distorted, even for the 10:1 dimming ratio, the highest checked. The harmonic content was measured for the same operation points shown in Fig. 6.29.

6.6. Experimental results: comparison and discussion

The input-current harmonic content, power factor and efficiency of the tested dimming techniques are compared in this section. For the sake of simplicity, only the most significant techniques are considered for the comparison, namely analogue dimming under 150 V_{rms}, 125 Hz PWM Enable dimming under 230 V_{rms}, 500 Hz PWM enhanced-enable dimming under 150

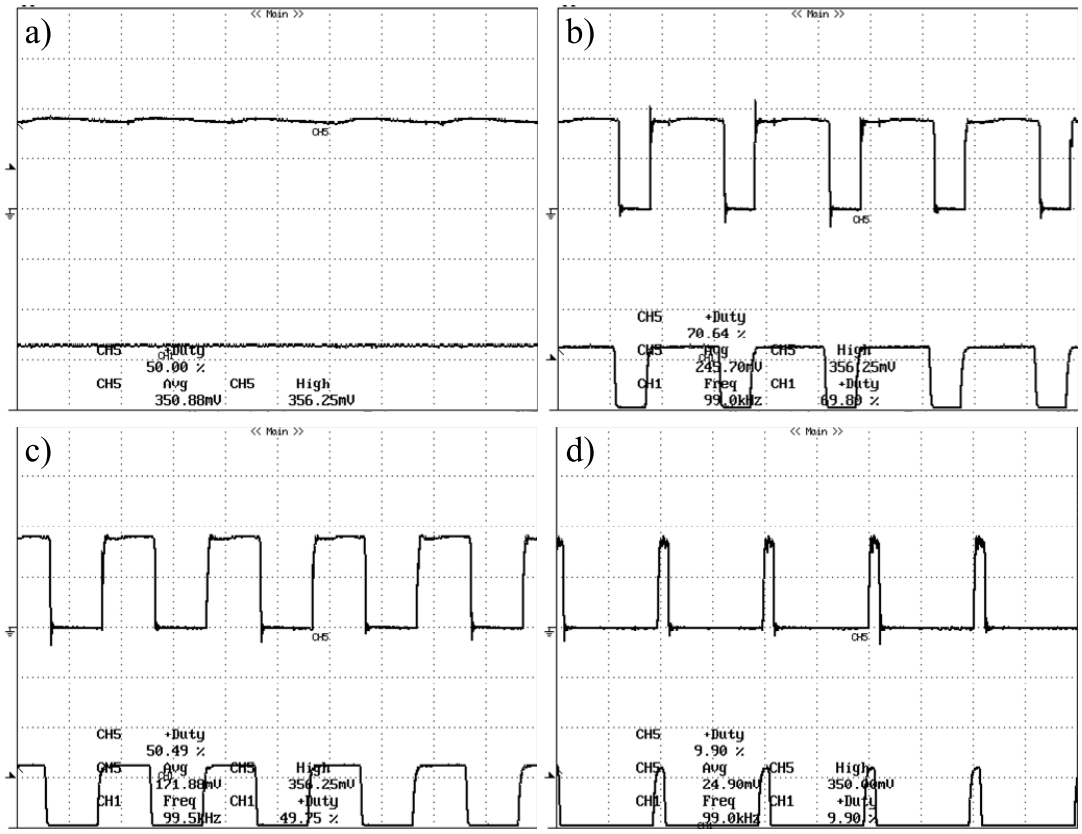

Fig. 6.29. Output current (upper trace) and PWM dimming signal (lower trace) under 150 V_{rms} input line for four operation points: a) DC output current; b) 70% dimming duty cycle; c) 50% dimming duty cycle; d) 10% dimming duty cycle. Vert. scale: output current, 200 mA/div; dimming signal, 5 V/div. Horiz. scale: 5 µs/div.

V_{rms}, 1 kHz PWM series dimming under 150 V_{rms} and PWM HFS dimming under 150 V_{rms}. Fig. 6.31 shows the results of the THD_I obtained versus the output power dimming, whereas Fig. 6.32 shows the results for power factor and Fig. 6.33 illustrates the results for efficency. It should be noted that in the case of PWM dimming technique in Fig. 6.31, Fig. 6.32 and Fig. 6.33, the results are expressed as a function of dimming duty cycle. In the case of analogue dimming, the percentage refers to the relative output current, as normalised to 350 mA.

As can be seen from Fig. 6.31, when developing PWM enable dimming the harmonic content is highly increased, surpassing 90% as the diming ratio rises. This is also applicable to PWM series dimming, and may be attributed to the burst input-current consumption at low frequencies. However, 125 Hz PWM enable dimming achieved better results in terms of THD_I at high dimming ratios, with a 20% lower total harmonic distortion at high dimming ratios. In addition, it can be seen that the rise in THD_I is lower for high dimming duty cycles, but it sharply increases when the dimming duty cycle goes below 50%. This fact could likely be caused by the synchronisation of the dimming signal with the line voltage, as analysed in Section 6.3. It is also remarkable that the THD_I behaviour of the 1 kHz series and the 500 Hz enable techniques showed the same results. However, there is no noticeable change in THD_I when performing either HFS or analogue dimming.

As can be seen from Fig. 6.32, the same results have been obtained for the measured input power factor. This way, those dimming techniques where the input current is drawn in burst mode featured a strong degrade in power factor as long as the dimming duty cycle was reduced.

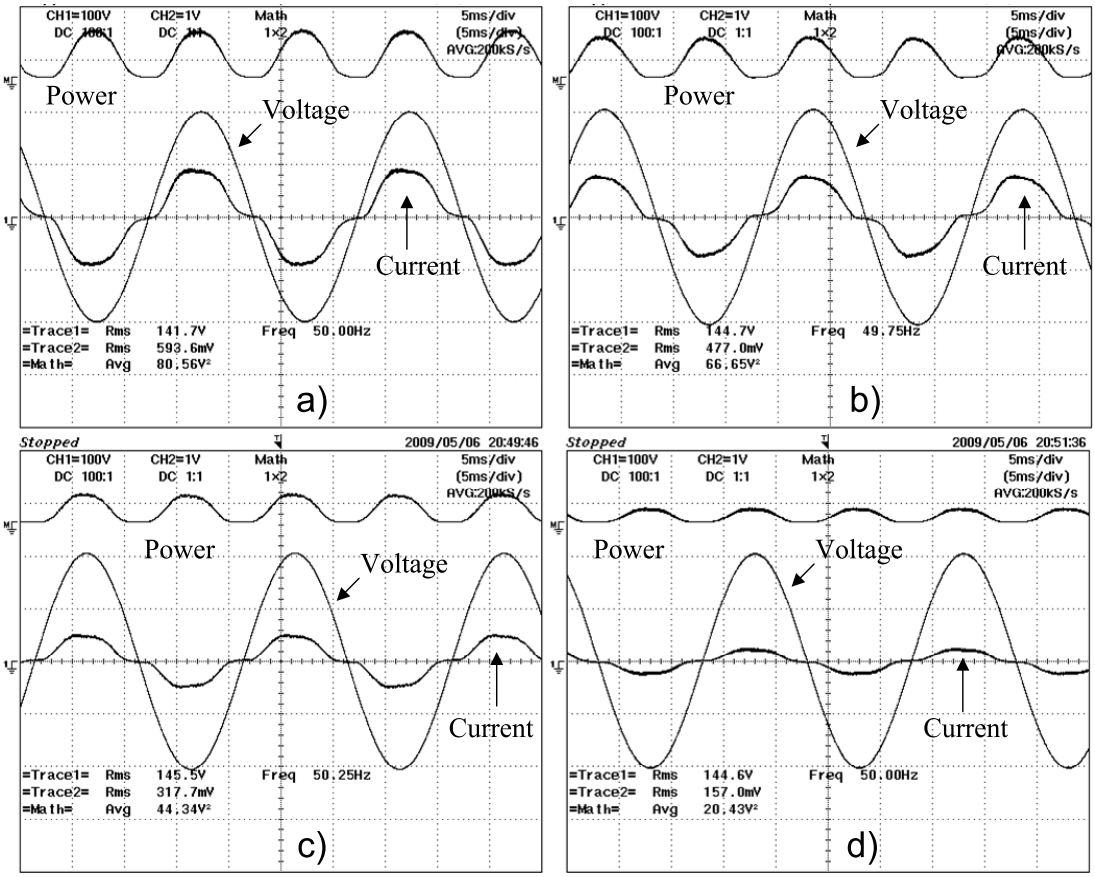

Fig. 6.30. Input voltage, current, and power for four different dimming ratios under 150 V_{rms} input. a) DC output current; b) 70% dimming duty cycle; c) 50% dimming duty cycle; d) 10% dimming duty cycle. Vert. scale: input voltage, 100 V/div; input current, 1 A/div; input power, 100 W/div. Horizontal scale: 5 ms/div.

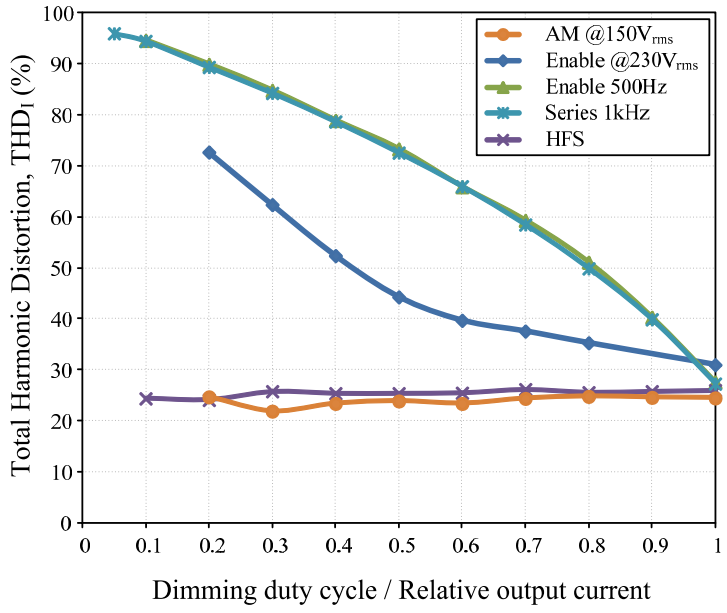

Fig. 6.31. Input current Total Harmonic Distortion (THD_I) results obtained from the laboratory tests of analogue dimming at 150 V_{rms}, 100 Hz enable dimming at 230 V_{rms}, 500 Hz enhanced enable dimming at 150 V_{rms}, 1 kHz PWM series dimming, and HFS dimming.

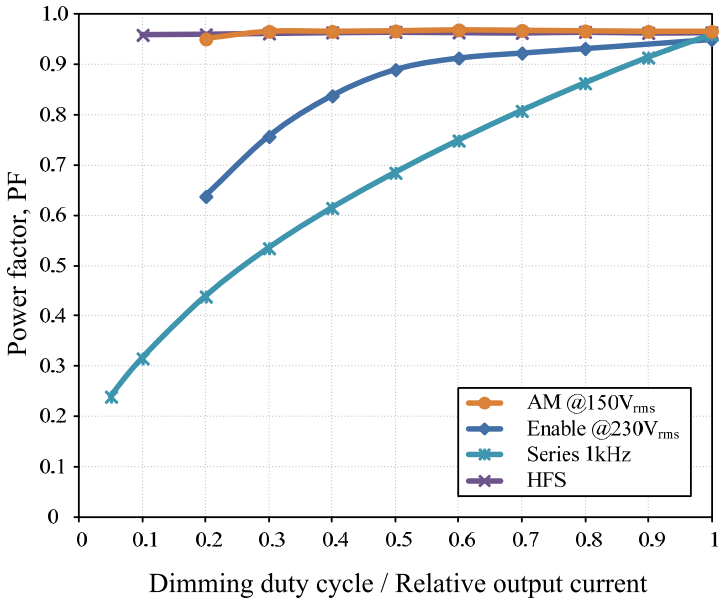

Fig. 6.32. Power factor (*PF*) results obtained from the laboratory tests of analogue dimming at 150 V_{rms}, 100 Hz enable dimming at 230 V_{rms}, 500 Hz enhanced enable dimming at 150 V_{rms}, 1 kHz PWM series dimming, and HFS dimming.

Indeed, the behaviour of the dimming techniques *PF* was analogous to that of the THD_I: in the series scheme, a great drop in *PF*, wheras in the enable scheme, the *PF* was slightly lowered at high dimming duty cycles but underwent a high fall below 0.5 dimming duty cycle. This is reasonable, since *PF* and THD_I are strongly related, as stated in (3.5) in Chapter 3. With regard to analogue dimming, the *PF* is somewhat lower than that of HFS dimming, although both techniques feature the best *PF* maintenance, with a flat curve for the entire dimming range.

Finally, Fig. 6.33 depicts the measured efficiency for all the tested techniques. As can be seen, PWM enable dimming techniques offer the worst efficiency maintenance at high dimming ratios, i.e. light load, since the efficiency is progressively decreased as long as the dimming duty cycle is reduced. On the contrary, analogue and PWM series technique offer a fairly flat efficiency curve for the entire dimming range, although a decrease is hinted at the highest dimming ratios. This may be caused in the former by the compensation of the switching losses by a decrease on the conduction losses due to lower rms currents across the synchronous transistor. In the latter, it could be attributed to the disconnection of the control loop, and thus, the entire converter in that way that the energy remains stored at the bulk and output capacitors, not needed for extra energy consumption once the converter is turned on again. With regard to the HFS technique, it shows a decrease in efficiency as in the case of the enable scheme, although the HFS technique might be considered a hybrid between analogue and PWM dimming techniques. In this case, this behaviour could be caused by the switching losses that appear in the dimming transistor, which might not be compensated by the reduced rms currents any longer. Anyway, HFS dimming technique still shows a slight advantage over the 125 Hz enable scheme. In addition, the higher efficiency shown by the 500 Hz enhanced enable scheme is due to the use of an SPW17NC802 CoolMos device, which achieves the best efficiency of all the tested transistors. Therefore, only the behaviour should be directly compared.

Finally, it can be concluded that the HFS dimming technique performs at least as an enable scheme in terms of relative efficiency.

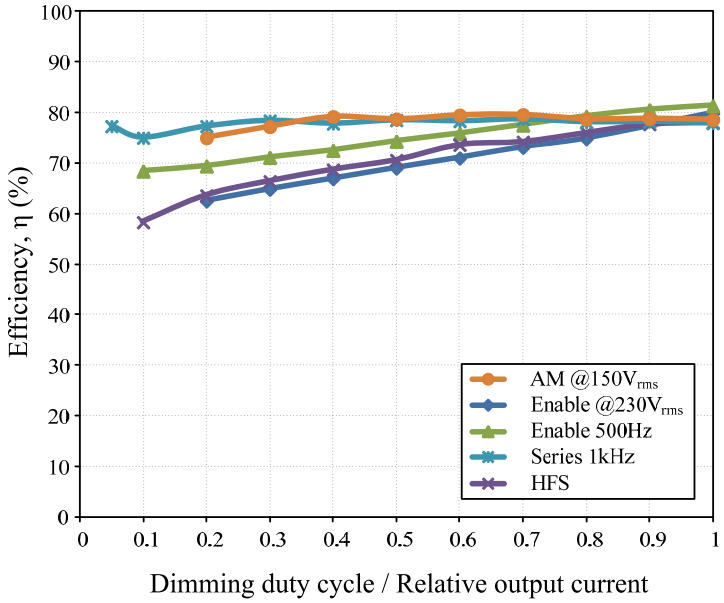

Fig. 6.33. Efficiency results obtained from the laboratory tests of analogue dimming at 150 V_{rms}, 100 Hz enable dimming at 230 V_{rms}, 500 Hz enhanced enable dimming at 150 V_{rms}, 1 kHz PWM series dimming, and HFS dimming.

6.7. Conclusions

This chapter covers the dimming operation of an IPC such as the IBFC developed in Chapter 4. First, the main dimming techniques are introduced and explained, namely analogue and PWM dimming. Since analogue dimming is straightforward implementable, the chapter is mainly focused on PWM dimming. Hence, the three main schemes are comprehensively discussed, also defining the most important magnitudes to account for, such as dimming ratio, rising and falling edges, etc. In addition, the main drawbacks of the three basic PWM dimming schemes are highlighted. Moreover, advanced dimming techniques such as the bi-level dimming scheme have also been mentioned.

Then, PWM dimming capabilities have been studied for its addition to the IBFC LED driver in order to extend its applications from street lighting to general indoor/outdoor lighting. Thus, a suitable PWM dimming control scheme for low slew-rate or slow-dynamics LED drivers, such as the IBFC, has been researched. This way, since PWM dimming is considered to offer the best dimming performance, the three main PWM dimming schemes, namely enable, series and parallel, were revised and compared. Analogue dimming was also considered, as it is the simplest and most cost-effective dimming technique.

With regard to the experimental results, analogue dimming was the first technique tested, achieving good results in terms of input current harmonic distortion and power factor, with no effect of dimming on those parameters. Moreover, efficiency was also maintained with only a slight decrease at the highest dimming ratios.

Since some applications might require PWM dimming schemes in order to achieve a more precise and linear control, or higher dimming ratios are needed, 125 Hz PWM enable dimming was the first PWM scheme test carried out. The dimming action was made by turning the converter on and off by means of a logic signal applied to the output-current reference. However, poor results were achieved in terms of efficiency, THD_I, PF and dimming ratio, being capable only of achieving a 4:1 dimming ratio. In order to improve the performance of this

scheme, the output capacitor was reduced and the loop gain was adjusted by an increased current-sensor gain. Nevertheless, the experimental results were practically the same.

Afterwards, the main reason for such a bad performance was identified and a new PWM enable dimming scheme, the so-called enhanced enable dimming, was obtained by adding an AND gate to the dimming control circuit, in the way that this AND gate is applied to the converter synchronous transistor after solving the AND operation on the dimming and the LM3524 PWM modulator signals. This allowed the dimming frequency to be pushed further, although satisfactory performance was obtained only up to 500 Hz in order to reach at least a 10:1 dimming ratio. Anyway, the results obtained for THD_I, PF and efficiency showed the same behaviour as in the previous enable dimming tests. Therefore, if a low THD_I at any dimming level is pursued, this technique may not be feasible.

Since enable dimming features high THD_I, PWM series dimming was covered, and the challenges that this technique presents were dealt with. In order to analyse the likely issues that the implementation of this technique would introduce, the control sensitivity function of the IBFC developed in Chapter 4 was studied, concluding that a PWM dimming action at low frequencies would lead the converter to oscillate, whereas high frequency perturbations would be filtered by this function. Thus, the first approach chosen for implementing a PWM series technique at low frequencies consisted of the series scheme with disconnection of the control loop, as proposed in [6.9]. Starting from the control loop developed for the enhanced enable scheme, a dimming transistor was connected in series with the LED load in such a way that the dimming signal switches the dimming transistor, the current reference and the synchronous transistor simultaneously. This assures a stable control-loop error signal and hence, oscillations due to the low-frequency perturbation are avoided. The first tests were performed at 1 kHz, which is a common dimming frequency. Nevertheless, although the dimming ratio achieved was 20:1 and the efficiency was kept constant for the entire dimming range, the strong modulation imposed in the input current due to the 1 kHz PWM dimming signal induced a great increase in THD_I and decrease on PF, such as in the enable scheme dimming. Therefore, dimming frequencies out of the scope of the Class C requirements were chosen in subsequent tests. However, even though the THD_I was unaltered considering the first 40 harmonics, the PF was reduced due to the pulsed input current. In addition, only 5:1 dimming ratio was achievable from 3 kHz onwards. Aimed on improving the PF, the dimming frequency was pushed even further, to frequencies easily filtered by the EMI filter without increasing its size. Additionally, dimming frequencies above 20 kHz could be desirable in order to avoid the generation of acoustic noise, what was noticed in all the dimming tests performed at low frequency. Thus, 20 kHz, 50 kHz and 100 kHz dimming frequencies were tested, achieving poor results in terms of dimming ratio. Moreover, a dimming-ratio dependent low frequency oscillation appeared, which could likely be caused by the limitations of the control-loop disconnection circuit.

Afterwards, a new approach to the series dimming technique was proposed: the high frequency series (HFS) PWM dimming, which overcomes all the problems that standard PWM series dimming featured. Since a high attenuation is expected from the control sensitivity function at high frequencies, the dimming frequency was set to 100 kHz and a new dimming control was proposed. This way, the average-current control is kept and the control loop is not disconnected, but an output-current reference conditioning circuit is introduced in order to keep the output-current peak value constant. This way, the synchronous transistor duty cycle is varied accordingly to the desired dimming level, overcoming the issues noticed in previous tests. Two control systems were proposed: i) a control that allows the user to set both the dimming ratio and the peak current, and ii) a simplified control that only allows the user to set the desired

dimming ratio at a fixed peak current. The results obtained during the laboratory tests showed that at least a 10:1 dimming ratio is achievable, which is quite satisfactory for general lighting applications such as residential lighting.

In the case of implementing this dimming control scheme in multi-string LED-lamp drivers, no negative effects are expected since the whole lamp is dimmed at high frequency, so any perturbation is filtered by the Control Sensitivity function. In any case, the overcurrent snubber might have to be re-sized, as the parallel connection of LED parasitic capacitances implies an increase in the whole lamp parasitic capacitance.

The only drawback of this solution is the efficiency decrease produced when the dimming ratio is increased. However, this efficiency drop is similar to that taking place when applying the PWM enable dimming technique. Furthermore, the apparently low efficiency achieved by this converter is due to its optimisation for the universal input range (90 to 265 V_{rms}) which introduces new efficiency concerns when working out of the nominal operation point. Therefore, further optimisation studies should be carried in order to improve the light-load operation. Chapter 7 will discuss some aspects for this purpose. Nevertheless, although the achieved efficiency is by far lower than that achieved by passive solutions [6.35] or one-stage converters [6.25], the converter performance is at least comparable to that achieved by many other solutions such as voltage-fed linear current regulators [6.25]; single-stage LED driver proposals, such as the LED driver presented in [6.36]; and it is also close to the efficiency performance featured by common solutions at comparable power levels, as in the case of a boost-flyback two-stage LED driver [6.37].

Moreover, it has to be noted that the HFS PWM dimming technique is straightforward applicable to low slew-rate or slow-dynamics converters such as fixed-frequency constant-current single-stage integrated converters or one-stage power factor pre-regulators, especially well suited for applications where PWM dimming is required and the THD_I cannot be degraded at dimmed operation.

In conclusion, a highly-reliable PWM dimming technique has been proposed for its application to slow-dynamics converters such as Integrated Single-Stage or PFP converters, achieving good results in terms of dimmability and input-current harmonic content, with the only disadvantage of a slightly lower efficiency if compared to analogue dimming, but with all the advantages that PWM schemes introduce. Derived from the innovation and benefits of this PWM dimming technique a Spanish patent has been granted [6.38].

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Chapter 7

Optimisation of the IBFC. Final Proposals and Implemented Prototype

In this chapter, the IBFC is optimised in several aspects. Firstly, the IBFC operation is studied in order to enhance the efficiency. In addition, three lamp configurations will be considered, including paralleled LED strings. Self-equalisation of LED strings will be studied in order to achieve a low cost solution. Secondly, the low-frequency flicker index is obtained in order to set an appropriate output-current ripple and determine its corresponding bus-voltage ripple. Then, the bus capacitor can be calculated. In addition, and provided that the bus-voltage ripple affects the input current, this effect will be studied in order to determine the optimal dead angle. The main purpose of these studies is to reduce the required bus capacitance to values that are available in MKP devices.

A completely functional laboratory prototype has been built, featuring a digital control that will accommodate different lamp configurations, partially compensating the output current ripple while still complying with Class C requirements. Also, both analogue and HFS-PWM dimming techniques will be implemented, achieving a highly flexible, reliable LED driver for 60 - 70 W general indoor/outdoor applications.

7.1. Introduction

This chapter will deal with the technical considerations needed for developing a low cost, efficient, highly reliable, fully-functional LED driver. This prototype is intended for supplying a 60 W LED lamp suitable for mid-power applications such as Street lighting, indoor commercial lighting or outdoor general lighting. The efforts will be focused on reducing the DC-link capacitor in order to use MKP-based devices, and the operation of the IBFC will be studied in order to enhance the efficiency.

Firstly, the current and voltage waveforms of the semiconductors will be studied. Then, the LED load will be studied in order to identify possible optimisations. Furthermore, different configurations of a 60 W LED load will be considered: one string of 60-series LEDs at 350 mA driving current, one string of 30-series LEDs at 700 mA driving current, or two paralleled strings of 30 LEDs at 350 mA driving current each.

In order to substitute the DC-link electrolytic capacitors with their MKP counterparts, the output current ripple requirements will firstly be maximised. Then, according to each lamp configuration and the characteristics of each lamp, the maximum forward-voltage ripple will be calculated for setting the maximum bus-voltage ripple. However, the input current is affected by a significant ripple present in the bus voltage, as it will be demonstrated in this Chapter. Consequently, the bus-voltage ripple will be pushed upwards to the practical limits imposed by both the maximum output-current ripple admissible and the maximum input-current distortion allowable by the IEC 61000-3-2 Class C regulations in order to reduce the required capacitance and allow for the use of MKP-based devices. In addition, the controller can introduce a certain amount of distortion in the line current. Thus, its design will be focused on improving the bus-voltage ripple while maintaining the line-current distortion below the Class C requirements with a minimised bus capacitor. Furthermore, the HFS PWM dimming technique proposed in Chapter 6 will also be implemented. Finally, comprehensive experimental results will be provided in order to confirm the satisfactory performance of the proposed solution.

The final prototype will be intended for Street lighting applications, outdoor general lighting or indoor commercial applications, so the 60 W LED lamps built and studied in previous Chapters feature an adequate power level. As outdoor use is expected, the converter will be designed to operate under a wide range of ambient temperatures. Therefore the LED lamps operation will be considered from -10 ºC, corresponding to steady-state operation at temperatures below -20 ºC, to 100 ºC, which is considered the maximum junction temperature allowable in order to assure high luminous efficiency and long-term reliability. In addition, the converter will be designed in order to supply the four LED lamps built and tested in Chapter 2 without any diminishing in performance.

7.2. Study on the efficiency optimisation of the IBFC.

Efficient designs are a strong requirement for today's LED drivers in order to reach the high efficiency that these light sources are capable of. Therefore, and derived from the fair efficiency results obtained from the IBFC tests included in Chapter 4, the losses that take place in the converter will be briefly and qualitatively overviewed in the subsequent sections, distinguishing between switching and conduction losses. Both losses depend on the electrical stress present in the semiconductor devices, this is, currents and voltages across. These waveforms, corresponding to the synchronous transistor and diodes D_1, D_2, D_3 and D_4, shown in Fig. 7.1, are depicted in Fig. 7.2. The forward current of both diodes D_2 and D_3 is considered. Although the leakage inductance of the flyback primary winding introduces significant losses, the overshoot

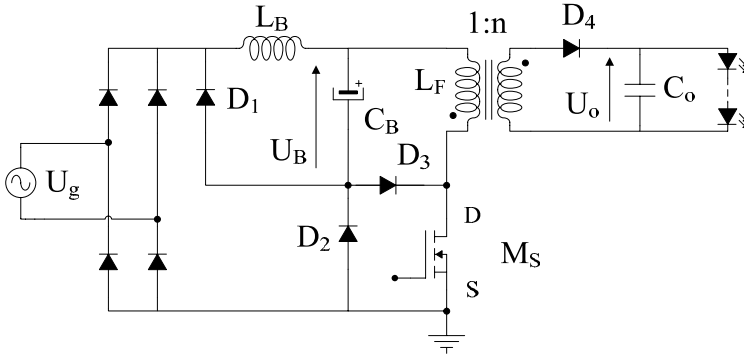

Fig. 7.1. Integrated buck-flyback converter.

produced is disregarded for the sake of simplicity. Further considerations regarding the leakage inductance will be discussed in subsequent sections in order to design an appropriate snubber.

7.2.1. Switching losses.

Switching losses are produced during the turn-on and turn-off of the different semiconductor devices present in the LED driver. Thus, the energy dissipated depends on the semiconductor electrical stress during these transitions, and the total power dissipated is proportional to the switching frequency:

$$P_{sw} = \left(W_{on} + W_{off}\right) f_s \tag{7.1}$$

where P_{sw} is the power lost due to switching process, W_{on} is the energy needed in order to turn the semiconductor on, W_{off} is the energy needed to turn the semiconductor off, and f_s is the switching frequency. As can clearly be seen from (7.1), the higher the switching frequency, the higher the switching losses. Regarding the energy lost during the on-off transitions, the voltage and current waveforms are to be studied.

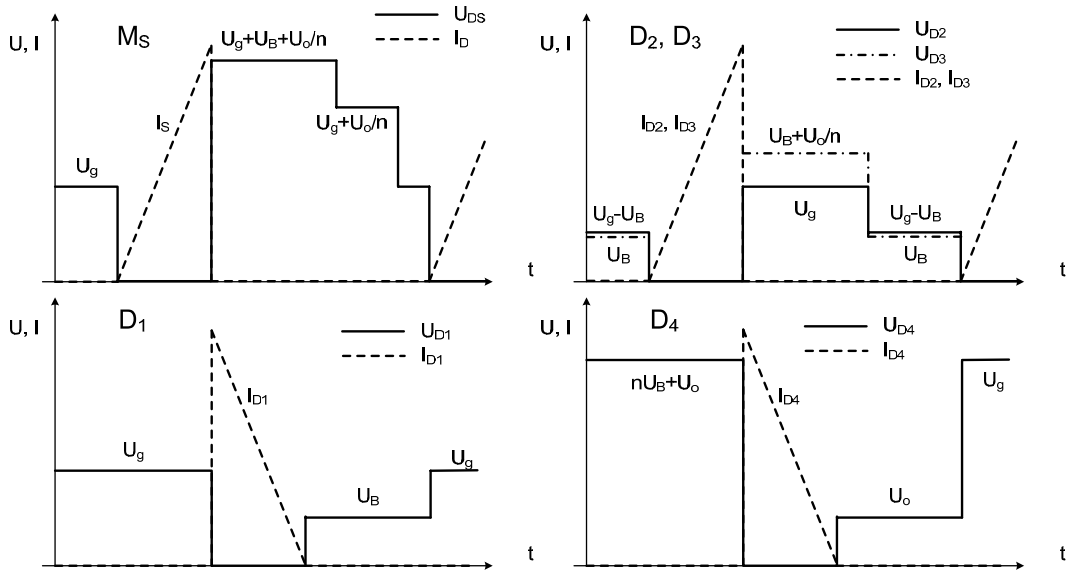

Fig. 7.2. Sketch of the current and voltage simplified waveforms of the synchronous transistor, diode D_1, diode D_2 and D_3, and diode D_4 in the IBFC.

As can be seen from Fig. 7.2, the DCM operation entails zero-current switching (ZCS) in certain transitions depending on the device. This way, the turn-on of the synchronous transistor and diodes D_2 and D_3 take place at zero current. Thus, turn-on losses are made negligible. In the case of the transistor, only the output capacitance, C_{oss}, induces losses during the turn-on. Moreover, the current across diodes D_1 and D_4 reaches zero at the switching instant, making the turn-off losses negligible. Therefore, soft-switching is naturally achieved in these transitions through ZCS, enhancing efficiency.

On the contrary, hard-switching takes place in the rest of the transition periods, namely, turn-off of the synchronous transistor and diodes D_2 and D_3, and turn-on of diodes D_1 and D_4. These transitions will be discussed separately:

- Turn-on of diodes D_1 and D_4: this transition occurs with the diode reverse-biased and a forward current step with high current slope, di_F/dt. Under these conditions, a forward voltage overshoot is present as the forward current is increased, leading to higher losses [7.1]. In the case of diode D_1, these losses could only be lowered by reducing the peak forward current, as the forward voltage at the turn-on is the line peak voltage. This is only achievable by increasing the duty cycle in order to keep delivering the same power to the load. With regard to diode D_4, the same situation is present. Nonetheless, in this case, the reverse voltage at the turn-on can be modified according to Fig. 7.2, the turn-on losses could be reduced, besides reducing the peak current value, by reducing the bus voltage, decreasing the turns ratio, or reducing the lamp forward voltage. In addition, a proper choice of semiconductors can overcome this issue. Thus, ultra-fast switching diodes are to be used, which make the turn-on losses negligible [7.1].
- Turn-off of diodes D_2 and D_3: this transition occurs with a significant forward current and a sudden reverse-biasing. Under these conditions, the reverse recovery of the diode arises. These losses could mainly be lowered by lowering the forward peak current, which induces lower di_F/dt across the *p-n* junction, by increasing the duty cycle. In addition, reducing the reverse voltage that is applied at the turn-off also helps to reduce the reverse-recovery losses. Regarding the reverse voltage, it could be optimised only in the case of diode D_3 by increasing the turns ratio, reducing the lamp forward voltage, or reducing the bus voltage. In addition, ultra-fast switching diodes with soft recovery are needed in order to minimise the reverse-recovery losses. Fortunately, as introduced in Chapter 4, only D_2 or D_3 are carrying forward current at the same time, depending on the values of line and bus voltage. This also helps to keep the reverse-recovery losses at a low level.
- Turn-off of the synchronous transistor: in this situation the transistor is abruptly led to blocking state. However, it still carries the full current while the drain-to-source voltage reaches the rail level as shown in Fig. 7.2. Moreover, the current finally reaches zero only when diodes D_1 and D_4 become forward-biased. In the meanwhile, the coexistence of drain-to-source voltage and drain current yields to energy dissipation. These losses could be lowered by: i) reducing the peak current value by increasing the duty cycle for the same average current, and/or, ii) reducing the drain-to-source voltage, which is affected by the line peak voltage, the bus voltage, the turns ratio and the lamp forward voltage. With regard to the drain-to-source voltage, only the bus voltage, the turns ratio, and the lamp forward voltage can be modified.

7.2.2. Conduction losses

Conduction losses are produced by the flow of current through the different devices present in a circuit, whether they feature a resistive parasitic effect or a voltage drop. These power losses are calculated from the rms value of the current flowing through a resistive element, whereas the average value is used if the element features a forward voltage drop. Thus, in a diode, the conduction losses, P_{Don}, will be determined by:

$$P_{Don} = V_\gamma I_{Davg} + R_s I_{Drms}^2 \tag{7.2}$$

where V_γ and R_D are the threshold voltage and the series resistance respectively, as discussed in Chapter 2, I_{Davg} is the forward average current, and I_{Drms} is the diode forward rms current. However, it can be assumed that ultra-fast switching diodes feature a negligible series resistance.

Regarding the conduction losses in the resistive elements, such as the MOSFET drain-to-source on-resistance the losses are determined as:

$$P_{Son} = R_{DSon} I_{Srms}^2 \tag{7.3}$$

where R_{DSon} is the MOSFET on-resistance and I_{Srms} is the drain current rms value.

It can be seen from (7.2) and (7.3) that conduction losses feature a quadratic relation with the squared current and the parasitic resistances on one hand, and a linear relation between conduction losses and average current due to the forward voltage drop in diodes on the other. These losses can be especially significant in DCM converters, since for a given current average value, their rms values are much higher than in the CCM counterparts. Therefore, it is important that the conduction losses are minimised. This is achieved by reducing both the average value and the rms current. Therefore, two main solutions are present:

- Increasing the bus voltage in order to reduce the buck and flyback inductors current for the same bus power.
- Increasing the lamp forward voltage in order to reduce the forward current for the same power level. This decreases the average and rms current through the diode D_4 and the flyback secondary winding resistance.
- Increasing the flyback turns ratio will reduce the peak current value and, therefore, the rms value of the flyback secondary winding and diode D_4, thus reducing the conduction losses.

7.2.3. Final considerations regarding the efficiency

As can be seen from the previous sections, the MOSFET switching losses are lowered by reducing the bus and the lamp forward voltages, and by increasing the turns ratio. With regard to the diodes, the reduction on bus and lamp forward voltages and the increase on the turns ratio also help reducing the reverse recovery. However, reducing the bus voltage implies higher currents, which increase the di_F/dt in the diodes with hard switching. Lower bus voltages also yield to higher bus capacitors due to the increase in specific current, as discussed in Chapter 3.

Regarding the flyback and lamp configuration, the lower the forward voltage, the lower the voltage reflected to the primary side. However, the practical limits for the turns ratio are imposed by the CCM operation of the flyback converter. In addition, any turns ratio higher than 1 reduces the lamp forward voltage reflected to the primary side. Nevertheless, a higher turns

ratio lowers the primary-side reflected lamp forward voltage, although increases the bus voltage reflected in the flyback secondary side, which in turn increases the electrical stress on diode D_4. However, the bus voltage is kept under 137 V in order to comply with Class C harmonic content requirements, as seen in Chapter 3 and 4, so it can be seen that only a high turns ratio would induce higher electrical stresses in diode D_4 than in the MOSFET, which would lead to the need for higher reverse-voltage diodes, with lower figures of merit, eventually degrading the performance of the converter.

With regard to the conduction losses, it can easily be seen that lower bus voltages will induce higher currents through diodes D_1, D_2/D_3, and the MOSFET, lowering the efficiency. Therefore, higher bus voltages are needed in order to optimise the conduction losses, although the bus voltage is limited by the maximum value admissible in order to comply with Class C requirements of harmonic content, as discussed in Chapter 3. Related to the lamp forward voltage, higher values will induce lower currents through diode D_4. However, there is a practical limit imposed by the reverse voltage induced in diode D_4, which could lead to the need for high-voltage devices with worse figures of merit. Regarding the turns ratio, it can easily be seen that the higher the turns ratio, the lower rms value through the flyback secondary winding and therefore, through diode D_4, reducing the conduction losses in the flyback winding. However, there is a maximum value for the turns ratio imposed by the flyback operation in DCM. The counterpart is an increase in the bus voltage reflected on the secondary winding, which may induce high electrical stresses on diode D_4.

Taking into account all the aforementioned considerations, a trade-off between switching losses and conduction losses shall be achieved. Since the IBFC integration process is performed in an OV-cell [7.2], the transistor is subjected to high voltage stresses that increase the switching losses, and due to the DCM operation, high rms currents are expected. Therefore, the focus will be more on these effects, paying less attention to switching and conduction losses on other components. Thus, and intending to reduce the conduction losses in the transistor, the buck inductor and the primary flyback winding, the bus voltage will preferably be the maximum value for complying with the regulations. In addition, and aimed on reducing the transistor switching losses, a lower-voltage lamp of the same power as in Chapter 4 will be considered. The turns ratio will also be optimised in order to minimise the reflected voltage in both flyback windings while trying to reduce the rms currents in the secondary side. Moreover, interleaving technique will be considered in the construction of the flyback inductor so that a low leakage flux is produced, leading to a low leakage inductance. Provided that a cost-efficient LED driver is pursued, a simple, low-cost RCD snubber will be considered, disregarding active-clamp techniques due to their higher complexity and cost.

Hitherto, only the factors affecting the electrical stresses have been taken into consideration. Regarding the semiconductor devices, the following choice of components would improve the efficiency:

- Silicon or Silicon-Carbide ultra-fast switching or Schottky diodes with soft recovery, in order to make the forward recovery negligible and minimise the reverse recovering power dissipation by limiting the reverse-recovering time and the di_F/dt.
- Power MOSFETs with reduced output capacitance, C_{oss}, in order to reduce the energy stored in the device and reduce the transition time, thus improving efficiency.
- Low on-resistance MOSFETs and low forward-voltage diodes in order to minimise the conduction losses. This point is quite important, since the conduction losses depend on

the rms value of the current across the components, this value being high in DCM converters.

7.3. Study on the LED lamp configuration: parallel connection of strings

Parallel connection of several strings of series-connected LEDs is a useful way to reduce the entire forward voltage of the lamp ensemble. However, and due to the dispersion of characteristics that even binned LEDs feature, as introduced in Chapter 1 and discussed in Chapter 2, there can be a high forward voltage mismatches between paralleled strings of LEDs. As LEDs are voltage-source like devices with low series resistance, such a forward voltage mismatch can lead to high forward current mismatches, being the main disadvantage of the parallel connection of LEDs.

Several techniques have been proposed in order to eliminate or, at least, reduce the forward current mismatch between paralleled strings. These techniques could be divided into two categories: i) active techniques, and ii) passive techniques.

With regard to active techniques, they consist in placing an LED driver, either a switched or a linear regulator, in series to each LED string. However, the extra driver per LED string increases the cost, size and complexity of the entire system. Yet, the LED driver allows the LED lamp to be easily dimmed. In addition, the efficiency is worsened if linear drivers are chosen. Examples of such system can be found in [7.3] and [7.4], where a linear transconductance amplifier is used to drive the LED and perform dimming operation, and [7.5], where a PFP stage drives several paralleled LED strings each with its own linear regulator. The efficiency is enhanced in the latter case by means of a bus-voltage adaptive control loop.

On the other hand, passive techniques make use of passive devices in order to reduce the current mismatch between paralleled branches. Thus, the most extended technique consisted in placing series resistors to each LED string in order to make the forward current less sensitive to variations in the forward voltage. However, this solution was usually designed for the worst case, leading to significant losses in the equalising resistors. A fairly good current matching was achieved by introducing p-1 coupled inductors per LED string, where p is the number of strings. This solution can be found in [7.6] for supplying the LED load with DC current, and [7.7], where the LED load is supplied with a square wave that also features dimming operation. However, this solution is highly bulky and more expensive if there are a large number of strings. Finally, a resistor-based equalising circuit was presented in [7.8], where the resistors are optimised by a statistical study of the forward voltage deviation of both binned and unbinned LEDs from a manufacturer. This solution achieves a 30% better efficiency owing to equalising resistors one hundred times lower than their counterparts in the classical worst-case design.

Provided that the IBFC design pursues to be cost-efficient, the study on paralleled LED strings will be aimed on passive solutions in order to avoid extra regulators. Therefore, the coupled-inductors solution is also discarded. In addition, as also a high efficiency is a main target, the technique proposed in [7.8] will be taken as a basis. Moreover, in order to avoid the utilisation of series-connected resistors, which increase cost and conduction losses, the LED series parasitic resistance will be study as the equalising resistor. Thus, self-equalisation of the LED lamps will be studied. As the forward voltage will be common for all the strings, the following equality can be obtained from the linear approximation for two parallel strings i and k with the lower forward voltage and dynamic resistance, and the highest values for those parameters:

$$V_{\gamma i}(T_j) + R_{Di}(T_j)I_{Di} = V_{\gamma k}(T_j) + R_{Dk}(T_j)I_{Dk} \tag{7.4}$$

where V_γ is the threshold voltage and R_D is the dynamic resistance of the linear model. This connection is depicted in Fig. 7.3.

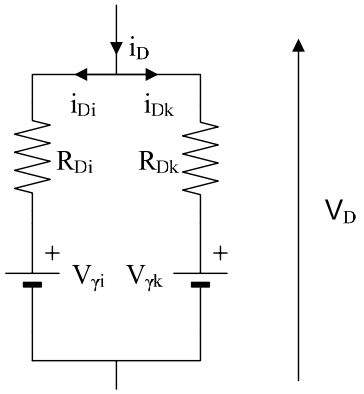

Fig. 7.3. Parallel connection of two LED strings.

This way, this connection will yield the maximum forward voltage deviation admissible corresponding to a given forward current deviation. Thus, by rearranging (7.4):

$$V_{\gamma i}(T_j) - V_{\gamma k}(T_j) = R_{Dk}(T_j)I_{Dk} - R_{Di}(T_j)I_{Di} \tag{7.5}$$

Since there are no statistical data about the dynamic resistance variation and its probability density function, the typical value will be considered under the same forward current, using the fitting polynomials obtained in Chapter 2 and gathered in Chapter 2 and the Appendix. Then, the difference in voltage between both strings can be expressed as the typical value multiplied by the forward voltage deviation obtained for a given sample size, ε, and so is the forward current deviation, ψ. Nevertheless, it has to be taken into account that both the forward voltage and the dynamic resistance are temperature-dependent. Moreover, considering that there is no dynamic resistance deviation across the string, the threshold voltage variation will be the same as the forward voltage variation for a given number of LEDs in series:

$$\varepsilon V_D(T_j) = R_D(T_j)\psi I_D \tag{7.6}$$

Rearranging:

$$\psi = \frac{\varepsilon V_D(T_j)}{R_D(T_j)I_D} \tag{7.7}$$

This is sketched in Fig. 7.4, where the effect that the forward voltage variation in two paralleled devices induces in the forward current of each one can be seen.

It has to be noted that this assumption can only be made considering that the junction temperature of the LEDs in the lamp is very similar. Nevertheless, the experimental results obtained in Chapter 2 showed that the board temperature is rather homogeneous, so the junction temperature is expected not to feature a large variation across the lamp.

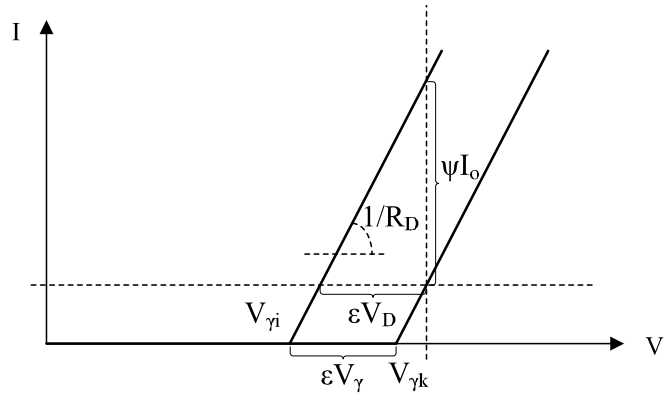

Fig. 7.4. *I-V* curve of two paralleled LEDs and effect that the forward voltage variation induces on the forward current of each string.

As can be seen from Fig. 7.4, the forward current variation can be kept under a given value by limiting the forward voltage variation, εV_D. Thus, the maximum forward voltage variation can be calculated for a minimum sample size, which corresponds to the minimum number of series-connected LEDs. This calculation is obtained as in Chapter 2, considering a 95% confidence level:

$$\varepsilon = \frac{1.96\sigma}{\mu\sqrt{N}} \tag{7.8}$$

Thus, by using the fitting polynomials obtained in Chapter 2 for the forward voltage and dynamic resistance as a function of temperature, considering the -10 ºC to 100 ºC range, and applying it to (7.7), the voltage deviation will be determined for a given current deviation, namely 5% and 10%. The minimum series-connected LEDs with a 95% confidence level for a given forward current variation, ψ, are gathered in Table VII.I for 350 mA and 700 mA at the worst-case condition imposed by junction temperature.

TABLE VII.I
MINIMUM SAMPLE SIZE FOR A GIVEN FORWARD CURRENT DEVIATION

LED	**N**	
	ψ =0.05	***ψ =0.1***
Golden Dragon Plus 350 mA	1009	253
Golden Dragon Plus 700 mA	541	136
Luxeon K2 350 mA	39	10
Luxeon K2 700 mA	24	6
Z-Power P4 350 mA	97	24
Z-Power P4 700 mA	44	11
XLamp XR-E 350 mA	1017	255
XLamp XR-E 700 mA	448	112

Building a 60 W LED lamp would lead to a forward current deviation greater than 0.05, as can be seen from Table VII.I. The best case, that corresponding to the Luxeon K2 –a binned device, would need 39 series-LEDs run at 350 mA in order to match the 0.05 forward voltage deviation, eventually leading to an approximately 80 W LED lamp. Moreover, it has to be taken into account that a practical minimum sample size has to be established in order to apply the Central Limit Theorem (CLT). This minimum value is typically set to 30. Therefore, a lamp

composed by two parallel strings of 15 series LEDs run at 700 mA will be discarded, as the CLT is not applicable. Therefore, the forward voltage deviation will be calculated for a lamp composed of two paralleled strings of 30 LEDs each, run at 350 mA. These results are gathered in Table VII.II.

TABLE VII.II
FORWARD CURRENT DEVIATION FOR 30 SERIES LEDS AT 350 MA: THEORETICAL

LED	ψ (%)
Golden Dragon Plus	29.0
Luxeon K2	5.6
Z-Power P4	9.0
XLamp XR-E	29.1

As can be seen from the results gathered in Table VII.II, only the Luxeon K2 and the Z-Power P4 would perform satisfactorily in order to achieve a forward current deviation lower than a 10%.

The four lamps characterised in Chapter 2 were rearranged as a two parallel strings of 30 LEDs each and supplied at 700 mA in the laboratory in order to confirm the results exposed above. The test was conducted at ambient temperature. The results corresponding to the lamp forward voltage, V_D, each string current, I_{D1} and I_{D2}, the total current, I_o, and the forward current deviation are shown in Table VII.III. The estimated junction temperature is also included. Nevertheless, it has to be noted that these temperature values are approximate and illustrative due to the current mismatch between strings.

TABLE VII.III
FORWARD CURRENT DEVIATION FOR 30 SERIES LEDS AT 350 MA: EXPERIMENTAL RESULTS

LED	V_D (V)	T_{j_est} (ºC)	I_{D1} (mA)	I_{D2} (mA)	I_o (mA)	ψ (%)
Golden Dragon Plus	92.74	68.9	341.5	362.7	704.2	3.0
Luxeon K2	97.63	63.2	354.5	345.1	699.6	1.3
Z-Power P4	91.35	53.9	338.0	361.9	699.9	3.4
XLamp XR-E	91.44	39.7	327.2	372.6	699.8	6.5

As can be seen from Table VII.III, all the LEDs except for the XLamp XR-E met a maximum forward current deviation of 5% for two-strings of 30 series LEDs. However, it has to be noted that even though the Golden Dragon Plus meets the 5% deviation, several Golden Dragon Plus lamps should be tested, as this LED is unbinned and therefore its standard deviation is large. However, it can be assumed that at least, the Luxeon K2 LED is suitable for self-equalisation in the conditions aforementioned. Thus, parallel LED strings will be considered in the final design.

7.4. Design of the LED lamp

Finally, three 70 W lamp configurations will be studied in order to optimise the efficiency of the converter, namely, 60 series LEDs at 350 mA (from here onwards 1x60), 30 series LEDs at 700 mA (from here onwards 1x30), and two strings of 30 series LEDs at 350 mA each string (from here onwards, 2x30).

As previously stated, the LED lamps will be designed for a -10 ºC to 100 ºC nominal operating temperature range, since outdoors operation is expected. Therefore, the forward voltage shift induced by thermal effects will have to be taken into account, including the margins that the LED characteristics deviation will require. Thus, with the forward voltage deviation obtained from (7.8), the mean value and the standard deviation for a given bin calculated in Chapter 2, and the sample size, the following forward-voltage limit values can be calculated for a given number of series LEDs as previously introduced in Chapter 2:

$$\begin{aligned} V_{Dmax} &= NV_{Dtyp}(T_j) + N\varepsilon V_{Dtyp}(T_j) \\ V_{Dmin} &= NV_{Dtyp}(T_j) + N\varepsilon V_{Dtyp}(T_j) \end{aligned} \tag{7.9}$$

where V_{Dmax} and V_{Dmin} are the forward voltage maximum and minimum value, respectively, V_{Dtyp} is the typical value for a given junction temperature, T_j, as calculated from the fitting polynomials obtained in Chapter 2, N is the sample size or number of LEDs connected in series, and ε is the forward voltage deviation.

Thus, the forward voltage limit values, as well as the dynamic resistance limit values for the three lamp configuration considered are calculated and gathered in Table VII.IV. Since further studies on the statistical distribution of the dynamic resistance would be needed, only the typical values are provided. The dynamic resistance values for the 2x30 configuration (2 parallel strings of 30 LEDs at 350 mA each) included in the table are those corresponding to the parallel dynamic resistance.

TABLE VII.IV
FORWARD VOLTAGE AND DYNAMIC RESISTANCE LIMIT VALUES FOR THE DIFFERENT LAMP CONFIGURATIONS

Lamp configuration		***Golden Dragon Plus***	***Luxeon K2***	***Z-Power P4***	***XLamp XR-E***
1x60 (1x350 mA)	V_{Dmax} **(V)**	201.6	214.2	202.3	201.3
	V_{Dmin} **(V)**	177.9	186.4	173.7	169.3
	R_{Dmax} **(Ω)**	44.4	55.5	45.2	36.6
	R_{Dmin} **(Ω)**	43.7	63.7	63.4	57.8
1x30 (1x700 mA)	V_{Dmax} **(V)**	108.6	117.4	111.2	110.6
	V_{Dmin} **(V)**	94.8	102.0	93.6	89.8
	R_{Dmax} **(Ω)**	16.3	22.1	24.1	21.8
	R_{Dmin} **(Ω)**	16.0	20.6	18.2	14.7
2x30 (2x350 mA)	V_{Dmax} **(V)**	101.5	107.3	101.4	101.3
	V_{Dmin} **(V)**	88.4	93.1	86.6	84.1
	R_{Dmax} **(Ω)**	11.1	13.9	11.3	9.2
	R_{Dmin} **(Ω)**	10.9	15.9	15.8	14.5

With the values included in Table VII.IV, the converter can be calculated for optimal operation in the -10 ºC to 100 ºC junction temperature range considered. The design of the converter will be described in subsequent sections.

7.5. Optimisation of the bus capacitor

One of the most remarkable features of LEDs is their extremely long life span, around several tens of thousands of hours. However, this feature implies a challenge when designing off-line LED power supplies. Generally, high-capacitance electrolytic capacitors are required to store the energy processed at twice the line frequency. However, these devices feature a much lower life span than that of LEDs [7.9], [7.10]. Therefore, the avoidance of electrolytic capacitors is an important topic of research. In [7.11], the operation with an increased voltage ripple across the storage capacitor together with a method to inject a third harmonic current is proposed. In [7.12], a bidirectional buck-boost converter is placed across the bus capacitor to compensate the energy transfer during each charging/discharging interval. In [7.13], a two-stage solution is proposed, based on a current-fed inverter with a rectified and filtered output that supplies the LED lamp. However, the energy is stored in a filter inductor instead of a capacitor, thus requiring huge inductance values. In [7.14], a ripple reduction circuit is added to the converter so that several strategies can be applied. Other solutions make use of two-stage converters with hysteretic control in order to stand large bus-voltage ripples [7.15], [7.16]. However, these strategies can become complex to be implemented besides featuring higher cost, low reliability, bulky inductors, poor efficiency, or unsuitability for low-medium power range and expensiveness

The optimisation technique that will be employed is that proposed in [7.17]. Thus, the minimum capacitance will be calculated in order to meet a given output current ripple.

7.5.1. Determination of the maximum bus-voltage ripple

As previously introduced in Chapter 4, the bus-voltage ripple is related to the output-current ripple through the ripple-gain factor, *v*:

$$v = \frac{\partial I_o}{\partial U_B} = \frac{2U_B}{R_F\left(2R_D(T_j)I_o + V_\gamma(T_j)\right)} \tag{7.10}$$

where I_o is the output current, U_B is the bus voltage, R_F is the flyback equivalent resistor, and R_D and V_γ are the LED dynamic resistance and threshold voltage, respectively. As can be seen from (7.10), the ripple-gain factor depends on the lamp itself, and on the operation point of the converter, i.e. bus voltage, output current, etc. The maximum bus-voltage ripple can be obtained from the expression for the output current in steady-state:

$$I_o = -\frac{V_\gamma(T_j)}{2R_D(T_j)} + \sqrt{\left(\frac{V_\gamma(T_j)}{2R_D(T_j)}\right)^2 + \frac{{U_B}^2}{R_F R_D(T_j)}} \tag{7.11}$$

By rearranging (7.11) and solving for U_B, the following result is achieved:

$${U_B}^2 = R_F\left(R_D(T_j){I_o}^2 + I_o V_\gamma(T_j)\right) \tag{7.12}$$

where the maximum and minimum bus voltages will correspond to the maximum and minimum output current values, provided that the flyback equivalent resistance and the lamp parameters remain constant. Thus, by subtracting the maximum and the minimum values:

$$\Delta\left({U_B}^2\right) = R_F\left(R_D(T_j)\Delta\left({I_o}^2\right) + \Delta I_o V_\gamma(T_j)\right) \tag{7.13}$$

It can be demonstrated that developing the terms $\Delta(U_B^2)$ and $\Delta(I_o^2)$ leads to:

$$\Delta\left({U_B}^2\right) = 2U_B\Delta U_B$$
$$\Delta\left({I_o}^2\right) = 2I_o\Delta I_o \tag{7.14}$$

Therefore, by substituting (7.14) in (7.13) and normalising in order to achieve the unitary bus-voltage ripple relation, δU_B, with the unitary output-current ripple, δ:

$$\delta U_B = \frac{R_F\left(R_D(T_j)2\delta I_o^2 + \delta I_o V_\gamma(T_j)\right)}{4U_B^2} \tag{7.15}$$

Therefore, once an acceptable low-frequency output-current ripple limit is determined, the maximum bus-voltage ripple is easily obtained and therefore, the required bus capacitor. In order to set an adequate low-frequency output-current ripple, the non-visible low-frequency ripple caused by the processing of energy at twice the line frequency has to be taken into account, since it might be a source of physiological hazards [7.18]. The flicker of a light source can be measured in several ways, being the *Low Frequency Flicker Index* (*LFFI*) and the *Low Frequency Percent Flicker* (*LFPF*) the most representative and useful when dealing with low-frequency non-visible flicker [7.19]:

$$LFFI = \frac{\int_t^{t+T} max\{X_{trunc}(\lambda) - X_{avg}, 0\}d\lambda}{\int_t^{t+T} X_{trunc}(\lambda)\, d\lambda}$$
$$LFPF = \frac{max\{X_{trunc}(t)\} - min\{X_{trunc}(t)\}}{max\{X_{trunc}(t)\} + min\{X_{trunc}(t)\}} \times 100 \tag{7.16}$$

where X_{trunc} is the Fourier Series decomposition of the light source luminous output truncated to the harmonics of interest, and X_{avg} is the light source average luminous output.

In order to consider a worst-case practical limit, ideal linearity between LED forward current and luminous output will be considered. Moreover, thermal effects will be disregarded, although large ripples would likely induce thermal modulation on the junction temperature, as could be demonstrated in Chapter 2. This will yield and absolute maximum value for the *LFFI* and *LFPF*. In addition, just the first harmonic, at twice the line frequency, could be considered in HPF IPCs. Thus, the relative luminous output, namely luminous intensity, I_v, could be expressed as:

$$I_v = I_{v\_avg} + I_{v\_avg}\delta I_v cos\left(2\frac{2\pi}{T}t\right) \tag{7.17}$$

where $I_{v\text{-}avg}$ is the average luminous intensity, δI_v is the luminous intensity ripple, and T is the line period. Thus, the *LFFI* and the *LFPF* of the luminous intensity described in (7.17) are depicted in Fig. 7.5 as a function of the current ripple.

As can be seen from Fig. 7.5, even with current ripples greater than 30%, the *LFFI* is kept below 0.1. As a comparison, 60 W A19 incandescent bulbs feature 0.02 *LFFI* and 6.6% *LFPF*, 35 W halogen MR16 lamps feature 0.01 *LFFI* and 3.8% *LFPF* whereas magnetic ballast-supplied T12 fluorescent tubes feature 0.07 *LFFI* and 28.4% *LFPF*. Therefore, a 20% ripple (40% peak-to-peak ripple) could be assumed, since it yields a 0.063 *LFFI* and a 20% *LFPF*, improving the results obtained by a T12 fluorescent lamp. Moreover, it has to be noted that this values would be yielded by an ideally linear device, although the droop effect and the thermal modulation imposed by large current-ripples with a proper heatsink design would eventually lead to much lower *LFFI* and *LFPF* [7.20], [7.21]. In addition, output-current ripples in the

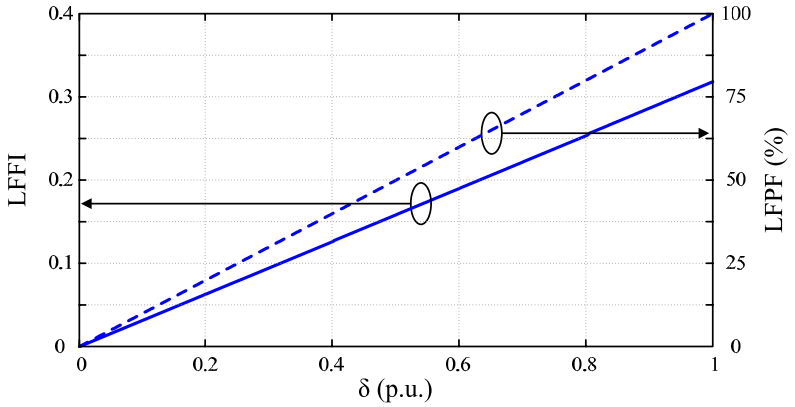

Fig. 7.5. *LFFI* (solid line) and *LFPF* (dashed line) of an LED lamp forward current accounting for the low-frequency harmonics produced by the processing of energy at the line frequency.

range of 15% (approximately 30% peak-to-peak ripple) have been used without significant visible effects [7.17]. With regard to efficiency considerations, there is no expected drop on the LED luminous flux due to ripples in the range of 30%. An efficiency loss of less than 10% has been reported for a 60 Hz full-wave rectified current [7.22].

7.5.2. Effects of the bus capacitance on the input-current distortion

Unlike DCM buck-boost-based PFPs, where the input current is naturally sinusoidal, the harmonic content of the input current of a DCM buck-based PFP depends on the conduction angle, which in turn depends on the bus voltage, as studied in Chapter 3. Indeed, as seen in Chapter 3, the input current averaged over a switching period, I_g, can be expressed as:

$$I_g = \frac{U_g - U_B}{R_B} \tag{7.18}$$

where U_g s the input voltage, U_B is the bus voltage, and R_B is the buck-converter equivalent resistance. However, if the buck converter is supplied from the AC mains, the input current can be expressed as:

$$i_g(t) = \begin{cases} \dfrac{V_g \sin(\omega_L t) - U_B}{R_B} & if\ \left|V_g \sin(\omega_L t)\right| > U_B \\ 0 & Otherwise \end{cases} \tag{7.19}$$

where V_g is the AC line peak amplitude. As can easily be seen, further calculations of (7.19) will lead the results obtained in Chapter 3 for the harmonics map as a function of the dead angle, which determines the bus voltage, assuming that the bus voltage is constant throughout the line period.

However, close examination of (7.19) shows that the input current is also affected by the bus voltage, so a significant bus-voltage ripple will introduce additional distortion in the line current. Therefore, the study conducted in Chapter 3 will be continued in this Section, but considering the bus voltage as a variable. The LFR large-signal model described in Chapter 4 will be used in order to determine the differential equation to be solved. The duty cycle and therefore, the buck and flyback equivalent resistances will be considered constant. The IBFC LFR large-signal model is depicted in Fig. 7.6 with the currents and voltages of interest. The capacitors ESR will be disregarded for the sake of simplicity.

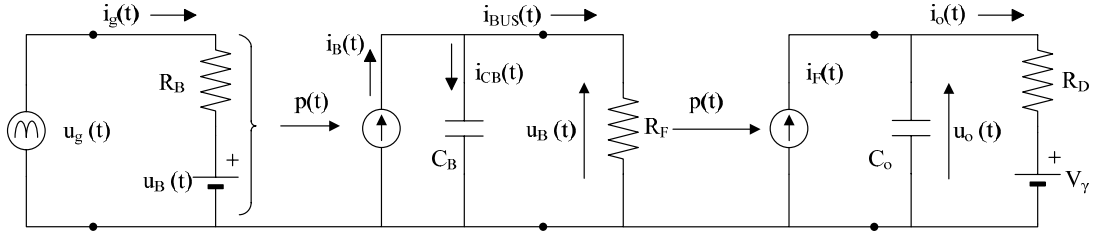

Fig. 7.6. LFR averaged model of the IBFC.

The analysis of the bus voltage will be done in order to obtain the differential equations that the converter features. Thus, from Fig. 7.6:

$$i_B(t) = i_{CB}(t) + i_{BUS}(t) \tag{7.20}$$

By rearranging (7.20), substituting, developing terms, and accounting for the buck inductor conduction range:

$$\frac{du_B(t)}{dt} = \begin{cases} \dfrac{V_g^2 sin^2(\omega_L t) - |V_g \sin(\omega_L t)| u_B(t)}{u_B(t) C_B R_B} - \alpha_L \dfrac{u_B(t)}{C_B R_B} & if\ |V_g \sin(\omega_L t)| > u_B(t) \\ -\alpha_L \dfrac{u_B(t)}{C_B R_B} & Otherwise \end{cases} \tag{7.21}$$

where V_g is the AC-line peak amplitude and α_L is the IBFC inductors ratio, as described in Chapter 4, the relation between the converter inductors being $\alpha_L = R_B/R_F$, where R_F is the flyback equivalent resistance. As the bus voltage is variable, the input current defined in (7.19) shall be redefined:

$$i_g(t) = \begin{cases} \dfrac{V_g \sin(\omega_L t) - u_B(t)}{R_B} & if\ V_g \sin(\omega_L t) > u_B(t) \\ -\dfrac{|V_g \sin(\omega_L t)| - u_B(t)}{R_B} & if\ V_g \sin(\omega_L t) < -u_B(t) \\ 0 & Otherwise \end{cases} \tag{7.22}$$

In order to perform a generalised analysis, the same procedure as in Chapter 3 will be followed. Thus, the normalised and specific magnitudes will be obtained. Since the converter will be designed for a specific dead angle considering the bus voltage constant and the duty cycle is also considered constant, the expression for the equivalent resistor is kept:

$$R_B = \frac{V_g^2}{2P_g}\left(1 - \frac{2\alpha + sin\,2\alpha}{\pi}\right) \tag{7.23}$$

where P_g is the power drawn from the AC line and α is the design dead angle. By substituting (7.23) in (7.21), the analysis of the unitary bus voltage, $\overline{u_B}$, can be done:

$$\frac{d\overline{u_B}}{dt} = \begin{cases} \dfrac{2\overline{P_n}}{C_B\left(1 - \dfrac{2\alpha + sin\,2\alpha}{\pi}\right)}\left(\dfrac{sin^2(\omega_L t) - |\sin(\omega_L t)|\overline{u_B}}{\overline{u_B}} - \alpha_L \overline{u_B}\right) & if\ |\sin(\omega_L t)| > \overline{u_B} \\ -\alpha_L \dfrac{2\overline{P_n}}{C_B} \dfrac{\overline{u_B}}{\left(1 - \dfrac{2\alpha + sin\,2\alpha}{\pi}\right)} & Otherwise \end{cases} \tag{7.24}$$

where $\overline{P_n}$ is the specific bus power, $\overline{P_n} = P_g/V_g^2$, measured in W/V^2. Moreover, the bus capacitor can be redefined in order to make its analysis independent of the processed power.

Thus, by defining a new specific capacitor, $\overline{C_n}$, such that $\overline{C_n} = C_B/2P_n$, measured in *1/rad·s*$^{-1}$, (7.24) can be rewritten as:

$$\frac{d\overline{u_B}}{dt} = \begin{cases} \dfrac{1}{\overline{C_n}\left(1-\dfrac{2\alpha+sin\,2\alpha}{\pi}\right)}\left(\dfrac{sin^2(\omega_L t)-|\sin(\omega_L t)|\overline{u_B}}{\overline{u_B}}-\alpha_L\overline{u_B}\right) & if\ |\sin(\omega_L t)|>\overline{u_B} \\ -\alpha_L\dfrac{1}{\overline{C_n}}\dfrac{\overline{u_B}}{\left(1-\dfrac{2\alpha+sin\,2\alpha}{\pi}\right)} & Otherwise \end{cases} \tag{7.25}$$

The same procedure can be followed with the input current in order to obtain the unitary input current, $\overline{i_g}$, where $\overline{i_g} = I_g/V_g$, measured in A/V. Therefore, by substituting the buck equivalent resistor as a function of the dead angle provided in (7.23) and the specific bus power in (7.26), the following unitary expression is achieved for the input current:

$$\overline{i_g} = \begin{cases} \dfrac{2\overline{P_n}}{\left(1-\dfrac{2\alpha+sin\,2\alpha}{\pi}\right)}(sin(\omega_L t)-\overline{u_B}) & if\ \ sin(\omega_L t)>\overline{u_B} \\ -\dfrac{2\overline{P_n}}{\left(1-\dfrac{2\alpha+sin\,2\alpha}{\pi}\right)}(|sin(\omega_L t)|-\overline{u_B}) & if\ \ sin(\omega_L t)<-\overline{u_B} \\ 0 & Otherwise \end{cases} \tag{7.26}$$

Once the specific bus power is known, equations (7.25) and (7.26) will provide all the information regarding bus voltage average value and low-frequency ripple, and the low-frequency components of the input current. Thus, by performing the Fast Fourier Transform (FFT) on (7.26) for a given bus capacitor and dead angle, the line current THD_I and PF can be calculated. Fig. 7.7 shows the bus-voltage waveforms for several values of the specific capacitor considering a dead angle of 25º and a specific power value of $6.6\cdot10^{-4}$ W/V^2, which corresponds to a 70 W output power at the European line voltage.

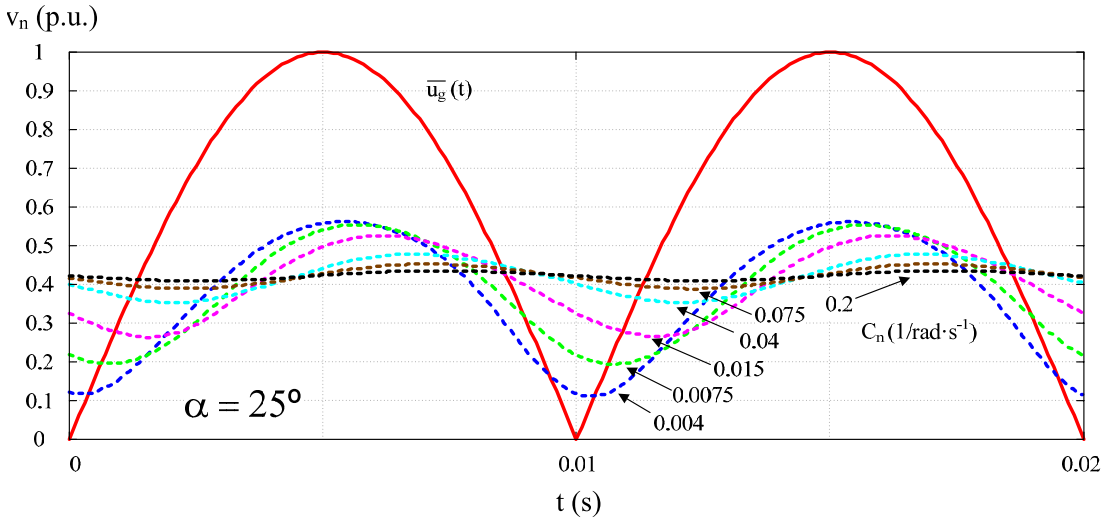

Fig. 7.7. Unitary bus-voltage waveforms for several values of specific capacitor at a dead angle of 25º and a specific power of $6.6\cdot10^{-4}$ W/V^2.

As can be noticed in Fig. 7.7, two related effects can be realised: on one hand, the average value is lowered as the bus capacitor is lowered, and in the other, this induces an increased conduction angle. Regarding the bus-voltage average value, Fig. 7.8 shows the normalised average value and the unitary ripple as a function of the bus capacitor for a 25º dead angle and a

$6.6 \cdot 10^{-4}$ W/V^2 specific power. The theoretical average bus voltage corresponding to a negligible bus ripple, as defined and calculated in Chapter 3, is also depicted.

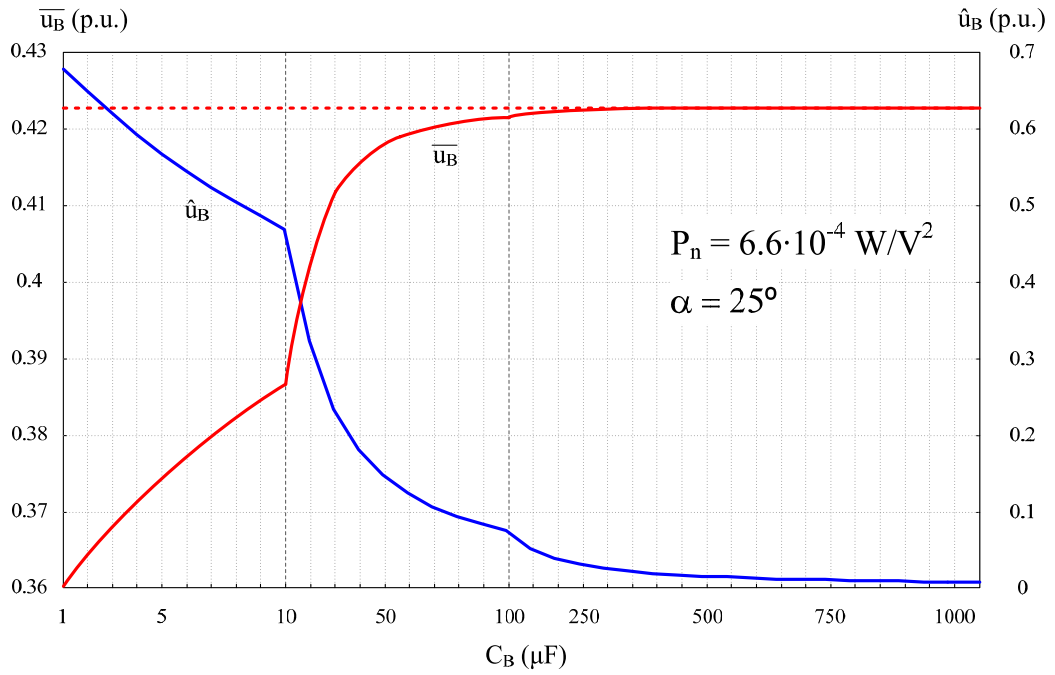

Fig. 7.8. Normalised bus-voltage average value and unitary bus-voltage ripple as a function of bus capacitor for a 25º dead angle and a $6.6 \cdot 10^{-4}$ W/V^2 specific power. The theoretical bus-voltage average value corresponding to negligible ripple is also illustrated (dashed line).

As can be seen from Fig. 7.8, bus-voltage ripples up to 0.1 hardly affect the bus-voltage average value, being its drop slightly greater than a 1% for a 0.1 ripple value. However, as long as the bus capacitor is reduced, the bus-voltage ripple is increased and the bus-voltage average value decreases at a higher rate.

With regard to the increased conduction angle, it would likely improve the PFC performance. However, this increased conduction angle is produced as a consequence of a significant ripple in the bus voltage, which in turn will further affect the input current. Therefore, a study on the input current is to be done. Fig. 7.9 shows the input-current waveforms for the same values as in the bus voltage, i.e. the dead angle considered is 25º, considering the same specific capacitor values. The theoretical waveform corresponding to a pure DC bus voltage is also depicted, its specific capacitor labelled as ∞.

As can be seen from Fig. 7.9, the effect of a significant ripple consists in an increased distortion present in the input current and a higher conduction angle. Moreover, effect of the bus-voltage ripple can be seen, which results in a phase-advanced input current with respect to the line voltage. This increases the displacement factor introduced in Chapter 3. This effect has already been described in [7.23]. This work contributes with the analysis of bus-voltage ripple in terms of THD_I and PF. Thus, by performing the FFT on the bus voltage and input current as a function of the specific bus capacitor, a harmonics map can be obtained similar to that provided in Chapter 3, but specifying the harmonics as a function of the bus capacitor. This harmonics map will be calculated considering a theoretical dead angle of 25º and a specific vale of $6.6 \cdot 10^{-4}$ W/V^2, as in the previous case. Therefore, the harmonics map will be expressed as a function of the bus capacitance, in μF, corresponding to that specific power. This map is shown in Fig. 7.10.

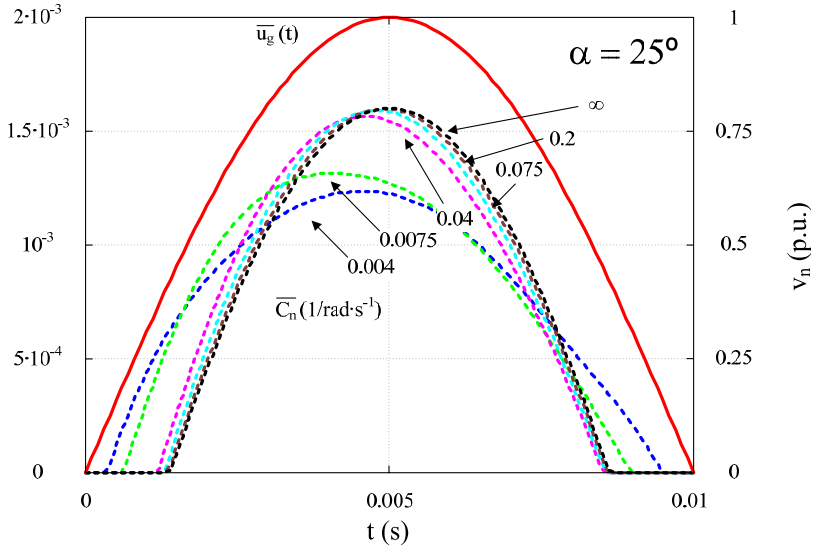

Fig. 7.9. Unitary input-current waveforms for several values of specific capacitor at a dead angle of 25º and a specific power of $6.6 \cdot 10^{-4}$ W/V^2.

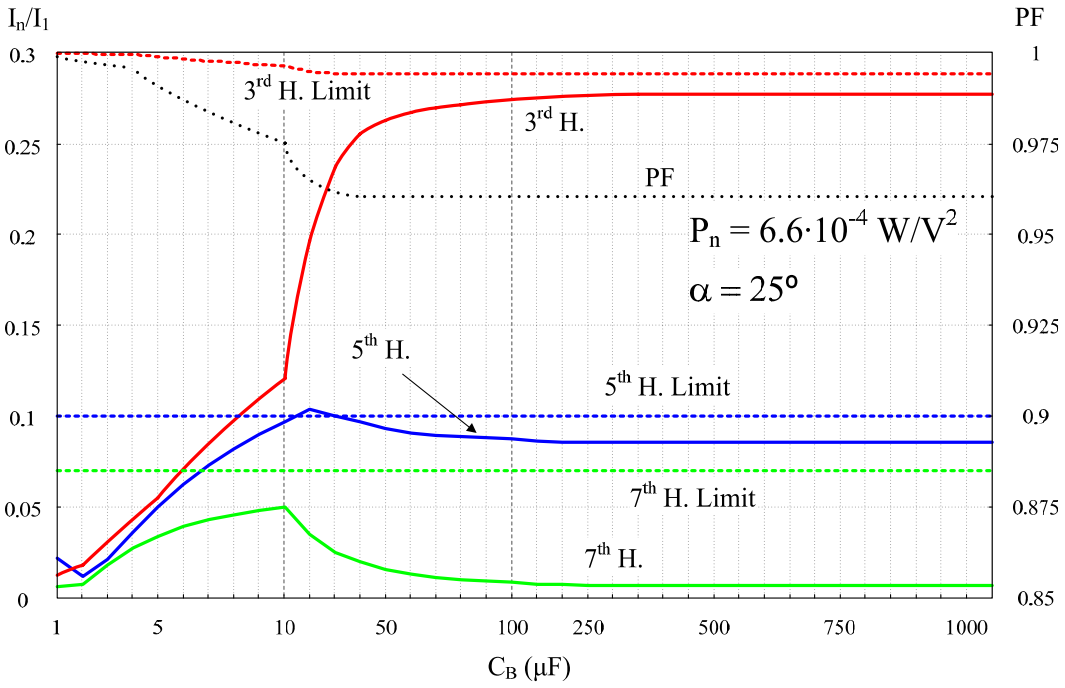

Fig. 7.10. Normalised harmonics map up to 7th harmonic and power factor (*PF*) as a function of the bus capacitor for a 25º dead angle and a $6.6 \cdot 10^{-4}$ W/V^2 specific power, illustrating also the Class C limits. Line frequency 50 Hz.

As can be seen from Fig. 7.10, the bus-voltage capacitance affects each input-current harmonic in a different way. Regarding the 3rd harmonic, allowing for a higher bus-voltage ripple, this is, reducing the bus capacitor, leads to a reduction of this harmonic, which is much steeper for bus-voltage ripple values beyond 0.2. Nevertheless, the 5th and 7th harmonics undergo a rise in its value when the bus-voltage ripple is increased up to a 0.35, approximately, with a decrease in all the harmonics value for bus-voltage ripples beyond 0.4. Besides, the power factor is also affected. As can be seen, the power factor is improved as long as the bus-

voltage ripple is higher, with a higher rate when the 5th and 7th harmonics start to be reduced. However, the 5th harmonic surpasses the limit imposed by the Class C requirements. Therefore, there is a bus-voltage ripple band going from values slightly higher than 0.2 to values around 0.45 that is to be avoided. Otherwise, the converter would not be IEC 61000-3-2 Class C compliant.

7.5.3. Optimisation and determination of the conduction angle

As has been discussed in the previous Section, the harmonic overall content is reduced when the bus-voltage ripple target is higher. Consequently, a dead angle greater than 25º, which would not meet Class C requirements, could lead to a compliant harmonic content provided the bus-voltage ripple is high enough to assure a low harmonic content while avoiding the use of electrolytic capacitors. Therefore, the harmonics map as a function of the bus capacitor will be also studied for three theoretical dead angles: 10º, 20º, and 30º, for the same specific power, $6.6 \cdot 10^{-4}$. First, the harmonics map up to the 7th and power factor corresponding to a 30º dead angle is shown in Fig. 7.11.

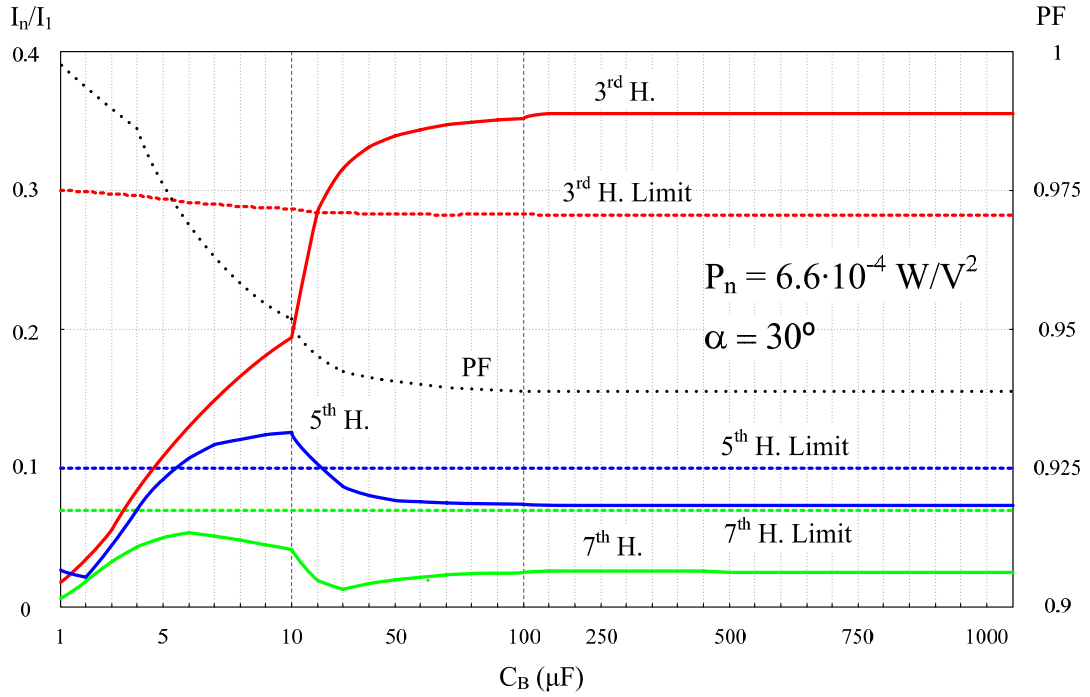

Fig. 7.11. Normalised harmonics map up to 7th harmonic and power factor (*PF*) as a function of the bus capacitor for a 30º dead angle and a $6.6 \cdot 10^{-4}$ W/V^2 specific power, illustrating also the Class C limits. Line frequency 50 Hz.

As can be seen in Fig. 7.11, only extremely low capacitance values would comply with Class C requirements. For large capacitance values, the 3rd harmonic is beyond the limit, whereas the 5th and 7th are compliant. By reducing the capacitance value, the 3rd harmonic starts to decrease due to the higher voltage ripple present in the bus until its value goes below the limit. However the 5th harmonic surpasses the Class C limit at capacitance values slightly higher than those for which the 3rd harmonic meets the limit. Moreover, these three harmonics considered only completely meet the Class C regulations for very low capacitance values, which will induce and extremely bus-voltage ripple. Therefore, the design for dead angles higher than 25º will be discarded.

Since dead angles higher than 25º are not feasible due to the high distortion introduced in the input current unless high bus-voltage ripple levels are allowed, lower bus voltages will be studied. The study will start from the harmonics map introduced in Chapter 3, which is recalled in Fig. 7.12 for better readability. This harmonics map shows relative amplitude of up to the 11th harmonic.

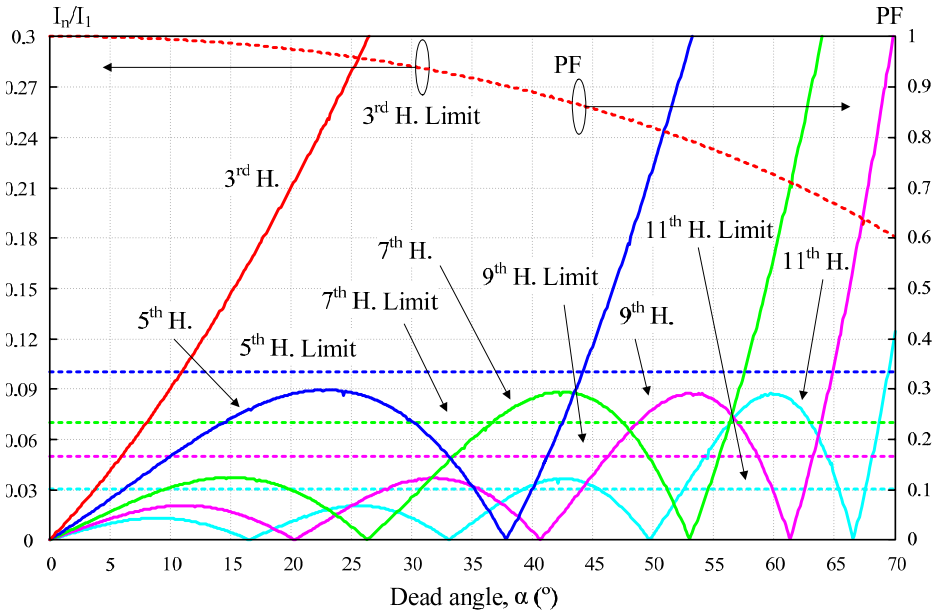

Fig. 7.12. Buck PFC stage: normalised harmonics map up to 11th harmonic and Class C limits. Line frequency 50 Hz.

As can be seen from Fig. 7.12, a 25º dead angle pushes the 3rd harmonic close to its limit. In addition, as can be seen from (7.26), the input current depends on the buck equivalent resistance, and in turn, on duty cycle. This implies that the duty cycle cannot vary within a line period, leading to slow-dynamics converters. Therefore, there is no capability to compensate a higher bus-voltage ripple partially by increasing the loop-control bandwidth in spite of the 3rd harmonics reduction due to smaller DC-bus capacitors. This is caused by the increase in the 5th harmonic that happens for smaller bus capacitances, which will be boosted by the additional distortion caused by the duty cycle variation across a line period. Therefore, smaller dead angles will be studied, namely 20º and 10º. The harmonics map corresponding to a 20º dead angle as a function of the bus capacitance is shown in Fig. 7.13

As can be seen from Fig. 7.13, the 5th and 7th harmonics are somewhat higher than in the case of a 25º dead angle, also confirming the results obtained in Chapter 3 and recalled in Fig. 7.12. Nevertheless, none of these harmonics are increased beyond the limits imposed by Class C regulations for any capacitance value. In addition, the *PF* is significantly improved while the 3rd harmonic is reduced, eventually yielding a wide range of duty cycle variation. Besides, this behaviour is expected to be boosted as the dead angle is reduced. Thus, the harmonics map corresponding to a 10º dead angle is depicted in Fig. 7.14.

As can be seen from Fig. 7.14, for such a low dead angle value, the harmonic content is far below the Class C limits with a consistent reduction in harmonic content as the bus capacitance value is reduced, even leading to a wider duty-cycle variation range if compared to the 20º dead angle situation.

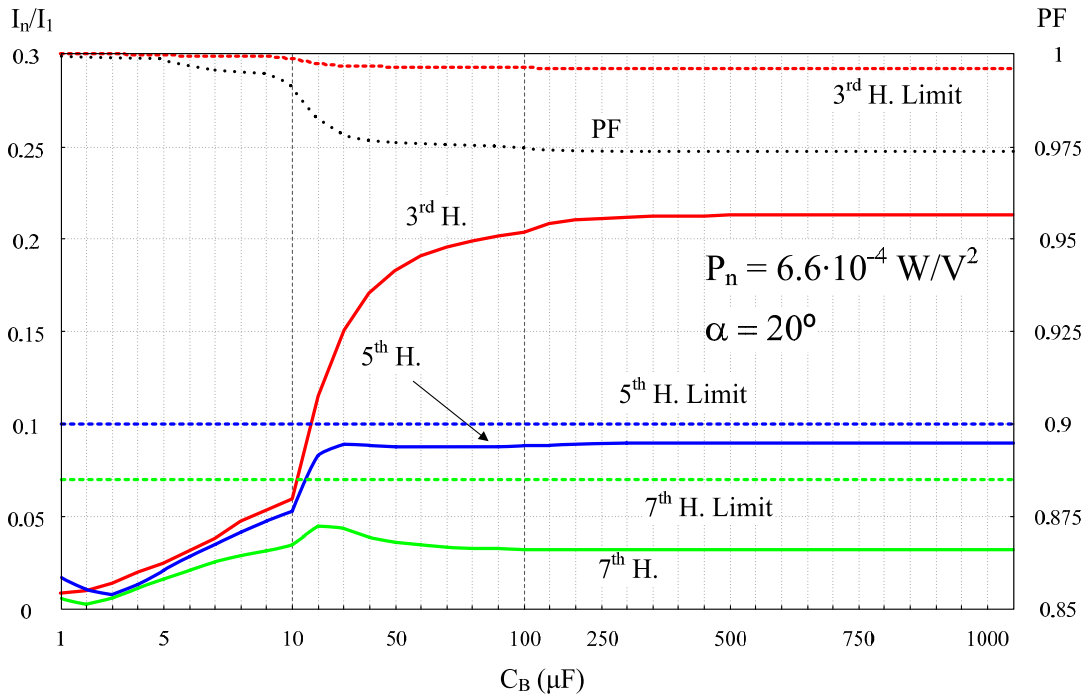

Fig. 7.13. Normalised harmonics map up to 7th harmonic and power factor (*PF*) as a function of the bus capacitor for a 20º dead angle and a $6.6 \cdot 10^{-4}$ W/V^2 specific power, illustrating also the Class C limits. Line frequency 50 Hz.

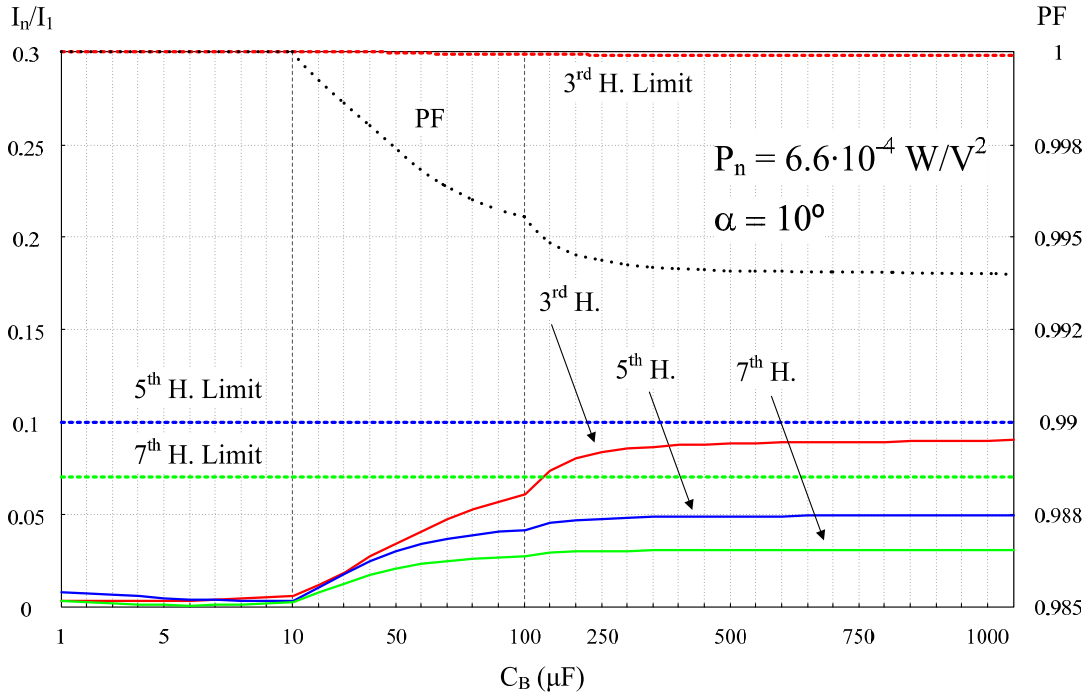

Fig. 7.14. Normalised harmonics map up to 7th harmonic and power factor (*PF*) as a function of the bus capacitor for a 10º dead angle and a $6.6 \cdot 10^{-4}$ W/V^2 specific power, illustrating also the Class C limits. Line frequency 50 Hz.

Nevertheless, it has to be taken into account that lower bus voltages induce higher bus currents and therefore, the bus-voltage ripple will be higher for the same bus capacitor. Thus, a

comparison between different dead angles in terms of bus-voltage ripple is needed. The normalised bus-voltage average value together with the unitary bus-voltage ripple is illustrated in Fig. 7.15 for these dead-angle values, namely 10º and 20º, together with 25º and 30º.

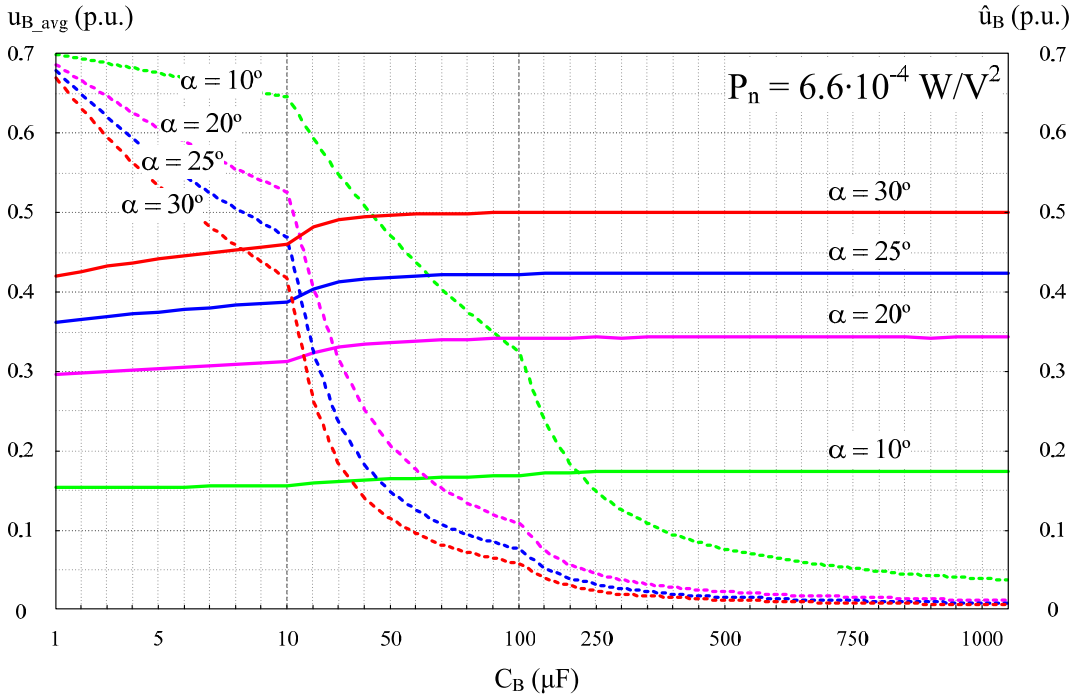

Fig. 7.15. Normalised bus-voltage average value (solid line) and unitary bus-voltage ripple (dashed line) as a function of bus capacitor for different dead angles at a $6.6 \cdot 10^{-4}$ W/V^2 specific power.

As can be seen from Fig. 7.15, the 10º dead angle should be discarded due to the high bus-voltage ripple imposed even for those bus-capacitor values that would imply an electrolytic device. For instance, a 0.1 unitary bus-voltage ripple would need a capacitance value somewhat higher than 350 μF. Moreover and as previously stated, the 30º dead angle should also be discarded due to the large bus-voltage ripple imposed for the bus capacitance values that lead to Class C compliance. With regard to 20º and 25º dead angles, it should be noted that the bus-voltage ripples attained with the same bus capacitor are only a 5% lower in the case of 25º dead angle.

In order to choose an optimal bus voltage, some considerations should be observed. First of all, the efficiency requirements would lead to discard low bus-voltage values, as the bus current would be increased, thus reducing the efficiency. Moreover, a lower bus voltage and therefore, higher bus current would lead to higher capacitance requirements, as has been depicted in Fig. 7.15. Therefore, low bus voltages should be avoided unless they are specifically required, such as in a battery-based DC bus. Moreover, dead angles higher than 25º, which implies high bus voltages, would not meet the Class C requirements unless a high bus-voltage ripple is allowed. An example of this would be a buck PFP with a cascaded stage with high power supply rejection ratio (PSRR), such as a free-wheeling converter [7.15]. With regard to dead angles of 25º or lower, it should be taken into account that, although this dead angle offers the lowest bus capacitor, it pushes the harmonic content up to the Class C limits at the cost of a slow closed-loop. Provided that the duty cycle affects the input current, adding distortion, this means that the duty cycle shall remain constant throughout a line period, which eventually leads to a low closed-loop bandwidth, much lower than 100 Hz. On the contrary, dead angles somewhat lower

than 25º would provide extra margin for complying with Class C requirements at the cost of a larger bus capacitor. However, this extra margin in harmonic content allows the duty cycle to compensate the bus voltage ripple partially, also boosting the converter dynamics and subsequently allowing the use of smaller bus capacitors. Therefore, the preferred dead angle would be in the 20º - 25º range.

7.6. Final design of the proposed converter

The aim of this work is to design a feasible LED driver with PFC that is capable to supply a 60 W LED lamp for several applications while achieving high efficiency and maximum reliability. The intended applications for this IPC are: i) commercial indoor lighting, such as in shopping centres or office buildings; ii) general outdoor lighting, such as in parking lots or stadiums; and iii) street lighting, in either cities or roads/highways. Since outdoor operation is expected, a wide operation temperature range will be considered in the design, as stated in Section 7.4. Thus, the junction temperature range considered will span from -10 ºC to 100 ºC, the nominal junction temperature being 80 ºC. Therefore, the converter will be designed for addressing the large forward voltage variation that is expected. Moreover, the converter will also be designed to operate with different LEDs in different configurations in order to achieve a different trade-off between cost, efficiency, and size. Nevertheless, the 1x60 XLamp XR-E lamp configuration will be considered the nominal design, since this LED features the highest efficiency and lowest thermal resistance. As discussed in Section 7.5.1, a 20% current ripple (this is, a 40% peak-to-peak current ripple) is admissible. This means 140 mA peak-to-peak current ripple for the 350 mA output current and 280 mA peak-to-peak current ripple for the 700 mA output in the 1x30 and 2x30 configurations. The maximum and minimum values of output voltage, V_{Dmax} and V_{Dmin}, and dynamic resistance, R_{Dmax} and R_{Dmin}, for the different lamp configurations, as well as the nominal operation values and the limit values for the nominal lamp are gathered in Table VII.V together with the maximum, minimum and nominal output-voltage ripple values, ΔV_{Dmax}, ΔV_{Dmin}, and ΔV_{Dnom} respectively, for each configuration. In addition, the maximum, minimum and nominal output-power values, P_{max}, P_{min} and P_{nom}, respectively, are included for each configuration.

The output voltage ripple is calculated as $\Delta V_D = R_D \cdot \Delta I_D$, where ΔI_D is the output-current peak-to-peak ripple.

7.6.1. Design procedure

The first step is to determine the operation parameters. The converter will be designed for performing both AM and PWM dimming, intended for reaching at least a 10% of the nominal output power, i.e., a 10:1 dimming ratio. As a high efficiency is a main objective in this design, and considering that there are no tough space constraints, the switching frequency will be set to 50 kHz, which is a usual value [7.17]. Moreover, the converter will be designed to operate at the European line voltage ±20% voltage tolerance. In addition, 85% efficiency will be assumed to size the different components of the IBFC. With regard to the dead angle, an intermediate value between 20º and 25º will be chosen, in order not to increase the bus capacitor significantly, but still having margin for extending the closed-loop bandwidth of a constant duty cycle design. Moreover, as the parameter m sets the limit for the duty cycle, the dead angle chosen shall provide enough duty cycle swing in order to allow dimming operation for the entire expected operation range. Thus, a value $m = 0.4$ was chosen as a satisfactory trade-off between duty cycle swing and corresponding dead angle. Therefore, the dead angle finally chosen is 23.6º. The nominal bus voltage is 130 V for the European line voltage, 230 V_{rms}. Besides, the maximum

and minimum bus voltage values will be 104 V and 156 V considering the line voltage tolerances. These values are obtained from (4.22), which is recalled here for better readability:

$$m = sin\left(\frac{\pi - \theta}{2}\right) = \frac{U_B}{V_g} \tag{7.27}$$

where U_B is the bus voltage, V_g is the line peak voltage, and $2\alpha = \pi\text{-}\theta$, where α is the dead angle and θ is the conduction angle.

TABLE VII.V
LIMIT AND NOMINAL VALUES FOR DIFFERENT LAMP CONFIGURATIONS

Feature	*1x60*	*1x30*	*2x30*	*Nominal*
V_{Dmax} (V)	214.2	117.4	107.3	201.3
V_{Dmin} (V)	169.3	89.8	84.1	169.3
R_{Dmax} (Ω)	63.7	24.1	15.9	57.8
R_{Dmin} (Ω)	36.6	14.7	9.2	36.6
V_{Dnom} (V)	174.6	93.6	87.3	174.6
R_{Dnom} (Ω)	38.6	15.6	9.7	38.6
ΔV_{Dmax} (V)	8.9	6.7	4.5	8.1
ΔV_{Dmin} (V)	5.1	4.1	2.6	5.1
ΔV_{Dnom} (V)	5.4	4.4	2.7	5.4
P_{max} (W)	75.0	82.2	75.1	70.5
P_{min} (W)	59.3	62.9	58.9	59.3
P_{nom} (W)	61.1	65.5	61.1	61.1

7.6.1.1. Design of the buck and flyback inductors

Once the bus voltage is determined, the flyback primary magnetising inductance, L_F, can be calculated from (4.27), which is recalled for the sake of readability. However, it has to account for the maximum power including dimming operation. Therefore, the output power will be modified by the parameter d_D, which expresses the dimming duty cycle, or the relative output power compared to the nominal power, P_{DIM}/P_o:

$$L_F = U_B^2 \frac{d^2}{2d_D \frac{P_o}{\eta} f_s} \tag{7.28}$$

where d is the converter duty cycle, f_s is the switching frequency, and η is the converter assumed efficiency. Since this flyback inductor has to be adequate for all the lamps considered within the entire operation range, it will be calculated for: i) maximum duty cycle, i.e. when the bus voltage is the lowest level and the output power is the maximum, and ii) minimum duty cycle, which occurs with the highest bus voltage and the lowest output power at a 10:1 dimming ratio, this is, $d_D = 0.1$. A minimum duty cycle of 0.1 will be considered in order not to compromise the performance of the converter in terms of reliability and efficiency due to the switching of the transistor in such a short time. The results obtained from (7.28) for the maximum flyback inductor for the two situations considered are shown in Table VII.VI.

TABLE VII.VI
FLYBACK INDUCTOR MAXIMUM VALUES FOR NORMAL AND DIMMING OPERATION

Lamp configuration	U_B (V)	P_o (W)	d	d_D	L_F (µH)
1x60	104	75.0	0.4	1	196.5
	156	5.9	0.1	0.1	349.7
1x30	104	82.0	0.4	1	179.6
	156	6.3	0.1	0.1	329.8
2x30	104	75.1	0.4	1	196.2
	156	5.9	0.1	0.1	352.0

According to the values gathered in Table VII.VI, the flyback inductor finally chosen is 170 µH in order to address both the bus voltage and the output variation ranges.

After the flyback inductor has been sized, the buck inductor, L_B, can be calculated from (4.23), which is recalled here:

$$m - \frac{1}{2m\alpha_L}\left(1 - \frac{2}{\pi}\sin^{-1}(m)\right) + \frac{1}{\pi\alpha_L}\sqrt{1-m^2} = 0 \tag{7.29}$$

where α_L is the inductance ratio, $\alpha_L = L_B/L_F$. By substituting m by the value finally chosen, 0.4, and solving for α_L, a 268.1 µH buck inductor is finally obtained.

Afterwards, the flyback turns ratio can be obtained by expression (4.25). Since the optimal turns ratio is that for which the flyback inductor will enter CCM, the optimal value will be the maximum. This corresponds to the maximum output voltage and minimum bus voltage. Thus, (4.25) can be expressed as:

$$n_{max} = \frac{V_{Dmax}\left(1 - d_{Flyback\_max}\right)}{U_B d_{Flyback\_max}} \tag{7.30}$$

where the maximum duty cycle can be calculated from (4.29). Thus, the maximum turns ratio will be calculated for the different lamp configurations. The values obtained are shown in Table VII.VII.

TABLE VII.VII
FLYBACK INDUCTOR MAXIMUM TURNS RATIO FOR DIFFERENT LAMP CONFIGURATIONS

Lamp configuration	V_{Dmax} (V)	$d_{Flyback\_max}$	n
1x60	214.2	0.372	3.47
1x30	117.4	0.389	1.77
2x30	107.3	0.372	1.74

A turns ratio n = 1.5 will finally be chosen in order to support the operation with the 1x30 and 2x30 configurations while allowing for an easy design of the flyback transformer.

7.6.1.2. Design of the bus capacitor

The converter is designed to operate at 230 V_{rms} input with a ±20% voltage tolerance reliably. However, the European specification for line voltage is 230 V_{rms} ±6%. Consequently, the bus capacitor, which depends on the bus current and therefore on the line voltage, will be designed for a lower tolerance, considering a ±10% line voltage tolerance. This tolerance leads to a maximum and minimum bus voltage of 143 V and 117 V, respectively. These will be the bus voltage values considered in the bus capacitor design. Thus, by rearranging (3.19), the specific bus capacitor is obtained:

$$C_n = \frac{\overline{P_n}}{2\delta U_B \sin^2\alpha}\left[2\alpha + \int_{\alpha}^{\pi-\alpha}\left|\frac{1-\cos 2\theta - 2\sin\alpha\sin\theta}{1-\frac{2\alpha}{\pi}-\frac{\sin 2\alpha}{\pi}} - 1\right| d\theta\right] \tag{7.31}$$

Expanding (7.31), the minimum bus capacitor is finally obtained:

$$C_{min} = \frac{P_o}{2\delta U_B U_B^2}\left[2\alpha + \int_{\alpha}^{\pi-\alpha}\left|\frac{1-\cos 2\theta - 2\sin\alpha\sin\theta}{1-\frac{2\alpha}{\pi}-\frac{\sin 2\alpha}{\pi}} - 1\right| d\theta\right] \tag{7.32}$$

where δU_B can be calculated from (7.15) for each operation point according to line voltage and junction temperature, and P_o can also be calculated as a function of junction temperature and output current by the forward-voltage fitting polynomials calculated in Chapter 2. Fig. 7.16 shows the minimum capacitor required for achieving a 40% peak-to-peak output-current ripple for the XLamp XR-E different configuration as a function of the junction temperature, for maximum, nominal and minimum bus voltages, and as a function of the bus voltage for minimum, nominal and maximum junction temperatures.

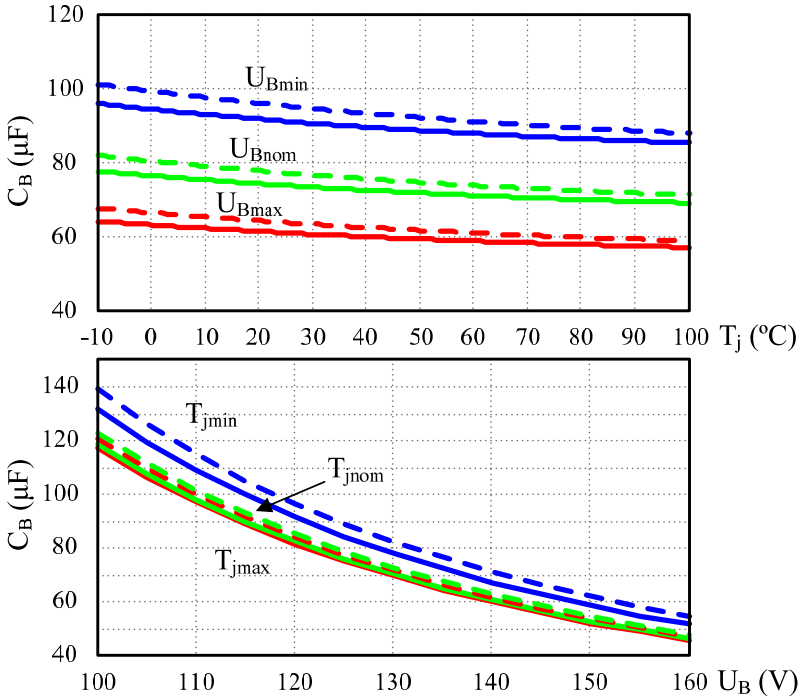

Fig. 7.16. Minimum bus capacitor for a 40% peak-to-peak output-current ripple as a function of junction temperature (upper graph) and bus voltage (lower graph). The three different lamp configurations are considered: 1x60 and 2x30 (solid line) and 1x30 (dashed line).

As can be seen from Fig. 7.16, the bus voltage variations induce more significant ripple variations in the bus voltage than the junction temperature variations. The minimum bus capacitor values for each lamp configuration for the minimum, maximum and nominal junction temperature operation points for the minimum bus voltage the formers, and the nominal bus voltage the latter, are gathered in Table VII.VIII.

TABLE VII.VIII
FLYBACK MINIMUM BUS CAPACITOR FOR DIFFERENT LAMP CONFIGURATIONS

Lamp configuration	***LED***	C_B @ T_{jmin} (μF)	C_B @ T_{jmax} (μF)	C_B @ T_{jnom} (μF)
1x60	Golden Dragon$^+$	95.3	88.0	73.3
	Luxeon K2	98.6	89.5	74.9
	Z-Power P4	92.0	84.9	70.3
	XLamp XR-E	91.2	84.9	70.0
1x30	Golden Dragon$^+$	99.0	91.8	76.3
	Luxeon K2	104.9	95.0	79.5
	Z-Power P4	96.6	88.1	73.2
	XLamp XR-E	95.3	87.4	72.4
2x30	Golden Dragon$^+$	95.3	88.0	73.3
	Luxeon K2	98.6	89.5	74.9
	Z-Power P4	92.0	84.9	70.3
	XLamp XR-E	91.2	84.9	70.0

As can be seen from Table VII.VIII, the minimum capacitor needed at nominal operation for maintaining the required output-current ripple for any lamp configuration is 80 μF, which is available in MKP technology, featuring a life span similar to that of LEDs. However, it has to be remarked that for the minimum bus voltage considered, the needed capacitance raises up to 105 μF for the 1x30 Luxeon K2 configuration. Nevertheless, as the dead angle is lower than 25º, some margin is provided in order to compensate the bus-voltage ripple partially.

However, the effect of the finally chosen bus capacitor has to be studied in terms of input-current harmonic content and bus-voltage and output-current ripple by depicting the line current, bus voltage, output current and output voltage from substituting the prototype values in (7.21) and (7.22) and solving the differential equation, and by substituting the proper values in equation (7.11). Furthermore, the output voltage can easily be calculated from proper rearrangement of (7.11). These waveforms are illustrated in Fig. 7.17 for the 1x60 XLamp XR-E configuration at the nominal operation point. In addition, the phase shift between input current and line voltage is also highlighted.

As can be seen from Fig. 7.17, the multifold effects that the low-frequency bus voltage ripple induces due to the low DC-link storage capacity are easily noticeable. Thus, the significant bus-voltage ripple induces a low output-voltage ripple, but the low dynamic resistance value that LED lamps feature leads to a high output-current ripple. Besides, the input current is phase advanced, introducing a phase shift with the line voltage that will worsen the *PF* and harmonic content. Fig. 7.18 shows the same waveforms for the 1x30 XLamp XR-E configuration.

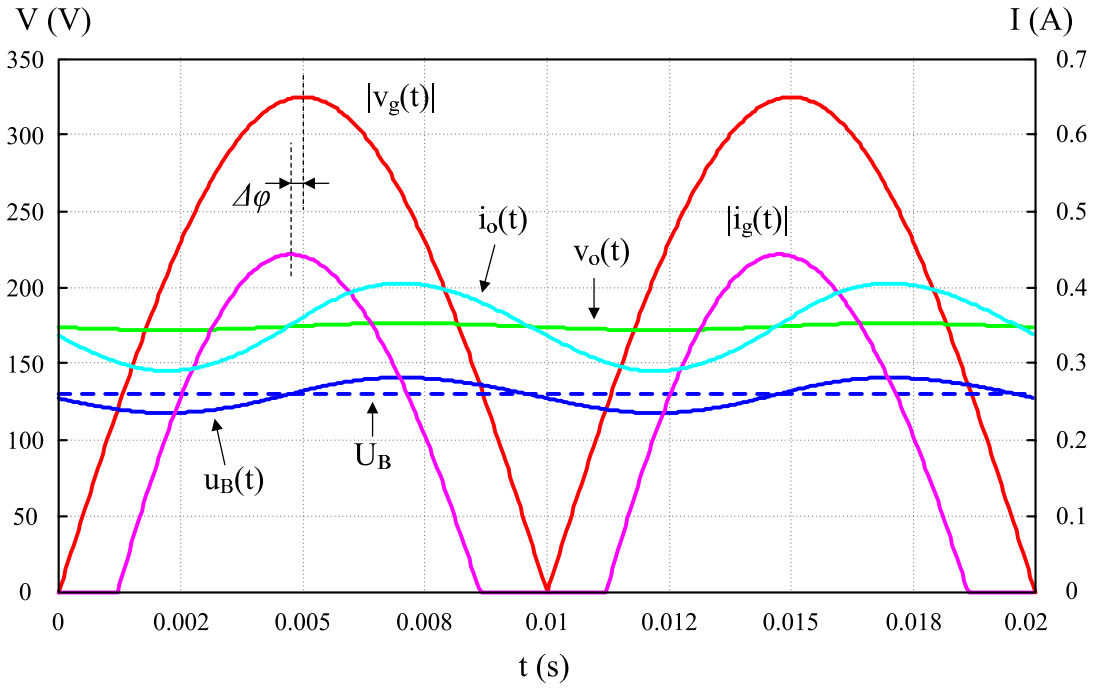

Fig. 7.17. Rectified line voltage, line current absolute value, bus voltage, average bus voltage (dashed line), output current and output voltage for the 1x60 XLamp XR-E lamp configuration under nominal operation conditions. Line frequency: 50 Hz.

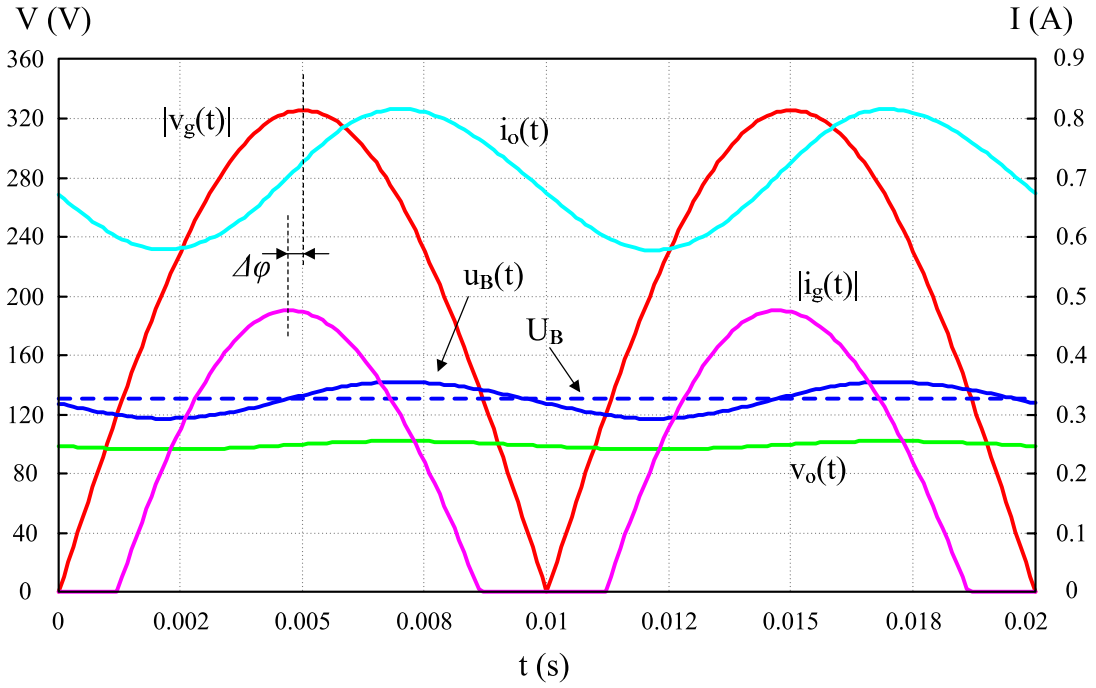

Fig. 7.18. Rectified line voltage, line current absolute value, bus voltage, average bus voltage (dashed line), output current and output voltage for the 1x30 XLamp XR-E lamp configuration under nominal operation conditions. Line frequency: 50 Hz.

The most remarkable difference that can be seen from Fig. 7.18 relies on the higher peak-to-peak output-current ripple caused by the much lower dynamic resistance of the 1x30 configuration.

In order to check whether the converter meets the design requirements with the bus capacitor chosen, Fourier Fast Transform (FFT) analysis can be applied to line current, bus voltage, and output current. Fig. 7.19 shows the harmonic content of the bus voltage and output current, and the harmonic content of line current together with the Class C harmonic limits.

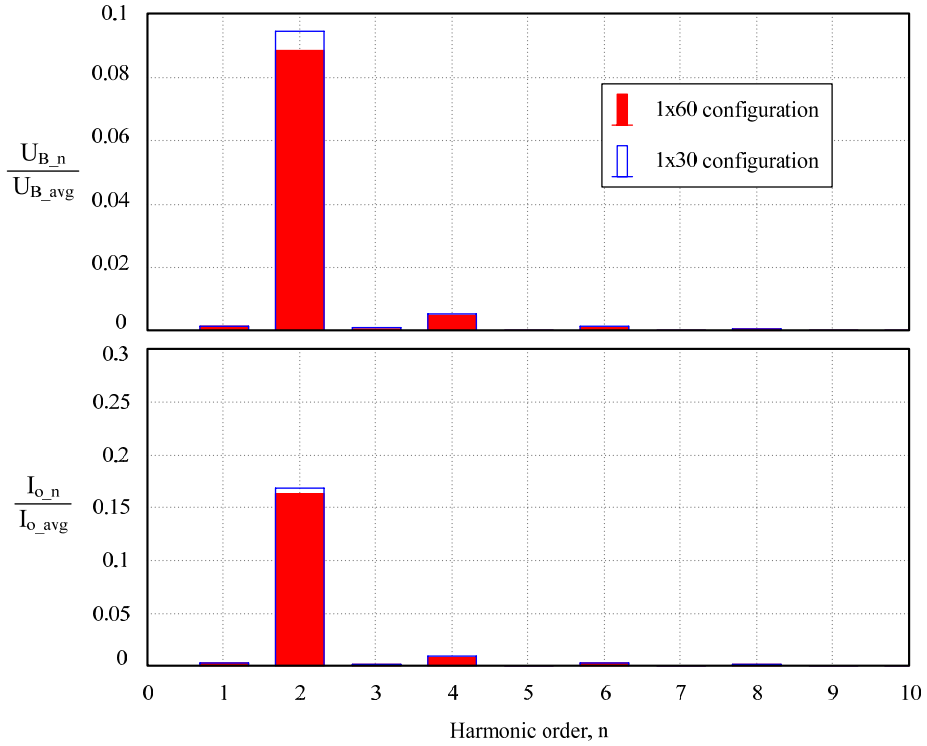

Fig. 7.19. Relative harmonic content of the bus voltage (upper) and output current (lower), disregarding the DC component, for the 1x60 and 1x30 XLamp XR-E configuration. First harmonic frequency: 50 Hz.

As can be seen from Fig. 7.19, two main conclusions can be achieved. First, the 1x30 configuration features higher output-current and bus-voltage ripples as expected. Second, the bus capacitor chosen meets the 20% unitary ripple target for the output current.

With regard to the input-current harmonic content, the FFT will also be applied in order to verify the Class C harmonic limits. This is depicted in Fig. 7.20 for the 1x60 and 1x30 XLamp XR-E configuration.

As can be seen from Fig. 7.20, the lowest-frequency components show similar results, presenting only slight differences in some harmonics. Therefore, the same results are expected for the rest of the lamp configurations, since the harmonic content of the input line depends on the conduction angle and the bus-voltage ripple, which is determined by the bus capacitor and the power drawn from the AC line, being the latter in a narrow range for the four configurations considered. Moreover, it can be seen that there is a wide margin for duty cycle variation in order to meet the Class C limits marginally. Therefore, good output-current ripple compensation is expected for all the lamp configurations.

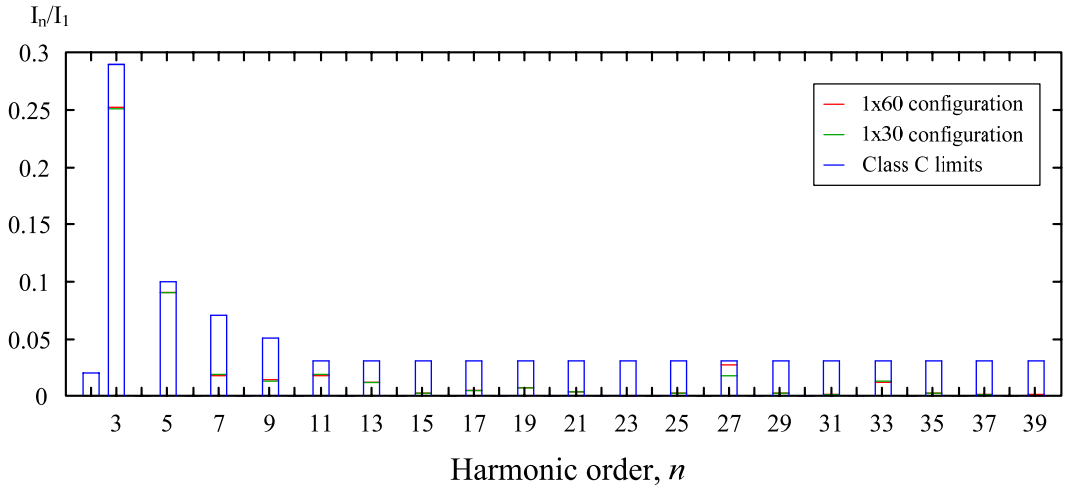

Fig. 7.20. Relative harmonic content of the line current and Class C limits for the 1x60 and 1x30 XLamp XR-E configuration. First harmonic frequency: 50 Hz.

7.6.1.3. Design of the output capacitor

Unlike traditional SMPS, a noticeable high-frequency ripple coming from the switching process does not compromise the performance of an LED driver, since these switching frequencies are much higher even than audible noise limits. In addition, there are no negative effects reported on accelerated ageing and damage of LEDs due to high frequency switching [7.24], [7.25]. Therefore, the output-current ripple will not be tightly limited by the output capacitor, establishing only a practical limit which also provides acceptably fast converter dynamics. Thus, a 5% output-current ripple will be set for the 1x60 XLamp XR-E configuration at the worst operation point, i.e. lowest bus voltage and highest output power. The procedure to determine this output capacitor is the same as in a regular flyback converter:

$$C_{o\_min} = \frac{I_o}{\Delta V_{Dmin}} \frac{d_{max}}{f_s} \tag{7.33}$$

where D_{max} is the duty cycle for the maximum output power and minimum bus voltage, as calculated from (4.29), ΔV_{Dmin} is contained in Table VII and corresponds to the lowest junction temperature, Io is the output current, and f_s is the switching frequency. A 1.5 µF minimum output capacitor is obtained for the lamp configuration state above. However, a 2 µF output capacitor will finally be chosen for a better high-frequency filtering in the 1x30 and 2x30 configurations.

7.6.2. Design of the controller and implementation of the control loop

The control loop will be designed considering two main purposes: first, the control loop will have to provide a fast enough dynamic behaviour that will reject any perturbation on the line voltage or change on the load characteristics in order to supply the LED lamp adequately, including dimmed operation and independently on the lamp configuration; and will also have to reduce the output current ripple partially while keeping the input-current harmonic content within the Class C limits.

Considering that the design of the IBFC allows a significant bus-voltage ripple, the input current will be affected by the duty cycle variation. Thus, the limiting factor for the control loop

will be the fulfilling of Class C requirements. Therefore, a bandwidth around 100 Hz will be needed, which is easily achievable by a simple integration action with the following expression:

$$K(t) = K_{DC} \int_0^t (i_r(\tau) - i_o(\tau))d\tau \tag{7.34}$$

where $K(t)$ is the control signal, i.e. the duty cycle $d(t)$, K_{DC} is the integral gain, $i_r(\tau)$ is the output current reference, and $i_o(\tau)$ is the measured output current. In order to study the input-current harmonic content introduced by the duty-cycle modulation, the following equation system composed by (7.21) and a proper rearrangement of (7.34), expressed in differential form and including (4.10), will be solved:

$$\begin{cases} \dfrac{du_B(t)}{dt} = \begin{cases} \dfrac{d(t)^2 T}{2L_B}\left(\dfrac{V_g^2 sin^2(\omega_L t) - |V_g \sin(\omega_L t)|u_B(t)}{u_B(t)C_B} - \alpha_L \dfrac{u_B(t)}{C_B}\right) & if\ |V_g \sin(\omega_L t)| > u_B(t) \\ -\alpha_L \dfrac{u_B(t)}{C_B}\dfrac{d(t)^2 T}{2L_B} & Otherwise \end{cases} \\ \dfrac{d}{dt}d(t) = K_{DC}\left(i_r(t) + \dfrac{V_\gamma}{2R_D} - \sqrt{\left(\dfrac{V_\gamma}{2R_D}\right)^2 + \dfrac{u_B(t)^2}{R_D}\dfrac{d(t)^2 T}{2L_F}}\right) \end{cases} \tag{7.35}$$

This system of differential equations was solved for the worst case of each lamp configuration considered in the converter design. Thus, the proper K_{DC} gain was calculated for the minimum bus voltage condition, where the bus-voltage ripple is maximum, in order to minimise the output current ripple by pushing the input-current harmonic content up to the maximum. Since the different lamp configurations, namely, 1x60, 1x30, and 2x30, imply different converter transfer functions, three different controllers will have to be implemented in order to implement a high-performance reliable system This can easily be addressed by digital control. Thus, the optimal gains found where K_{DC} = 190 for the 1x60 configuration, and K_{DC} = 80 for the 1x30 and 2x30 configurations. The performance of the converter operating in closed loop with the different K_{DC} values is summarised in Table VII.XIX, where the *PF*, THD_I, 3rd and 5th harmonic relative amplitude, and output-current ripple are gathered for each lamp configuration in the worst-case conditions, this is, for minimum bus voltage and maximum output power considering a ±10% line voltage tolerance, including the nominal condition. The nominal operation for each lamp configuration refers to the XLamp XR-E lamp at 80 ºC junction temperature.

As can be seen from the results gathered in Table VII.XIX, the proposed design meets all the stated requirements. Fig. 7.21 shows the main waveforms of the IBFC: line voltage (rectified), input current (absolute value), bus voltage, output current, and duty cycle. In addition, the maximum and minimum current values for a ±20% voltage ripple are highlighted.

As Fig. 7.21 illustrates, the line current is even more phase-advanced, with a noticeably higher phase-shift compared to the line voltage, which implies a greater harmonic content. However, it can also be easily seen that the bus-voltage and output-current ripples are reduced, improving the output overall behaviour of the LED driver. It can also be seen that the duty cycle features a variation, albeit not leading to a strong control action.

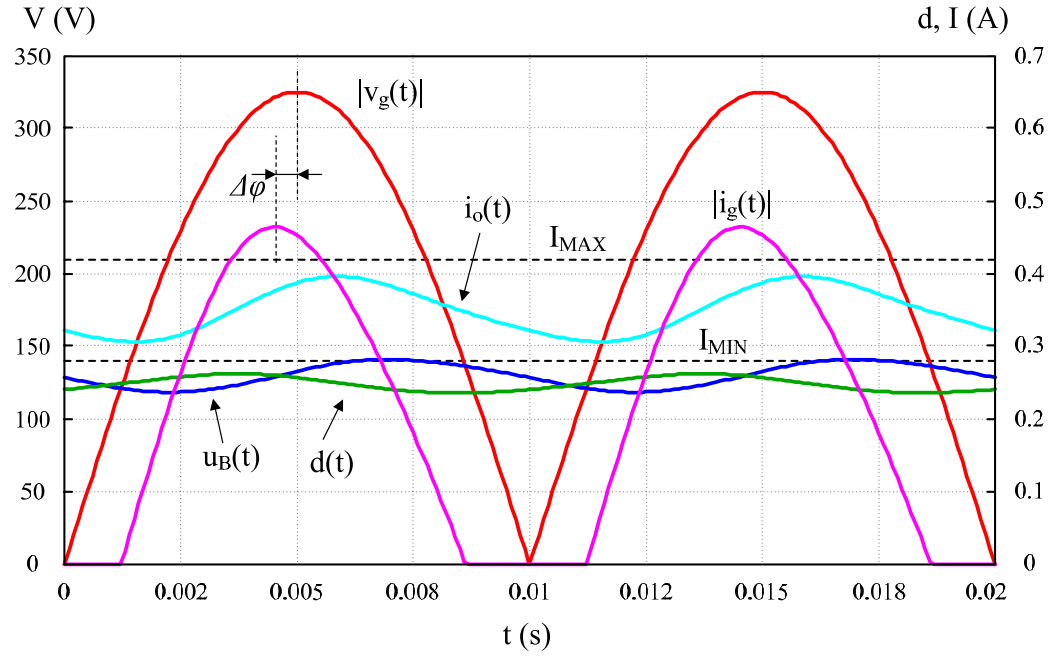

Fig. 7.21. Rectified line voltage, line current absolute value, bus voltage, duty cycle, output current, and maximum and minimum output current limits for the 1x60 XLamp XR-E lamp configuration under closed-loop nominal operation conditions. Line frequency: 50 Hz.

Analogously to Section 7.6.1.3, FFT analysis can be applied to the bus voltage, output current, and duty cycle in order to check the improvements in performance obtained with the control loop proposed, and whether the duty cycle variation is kept within practical values. Thus, Fig. 7.22 shows the harmonic content of bus voltage, output current and duty cycle for the 1x60 XLamp XR-E configuration under nominal operation condition.

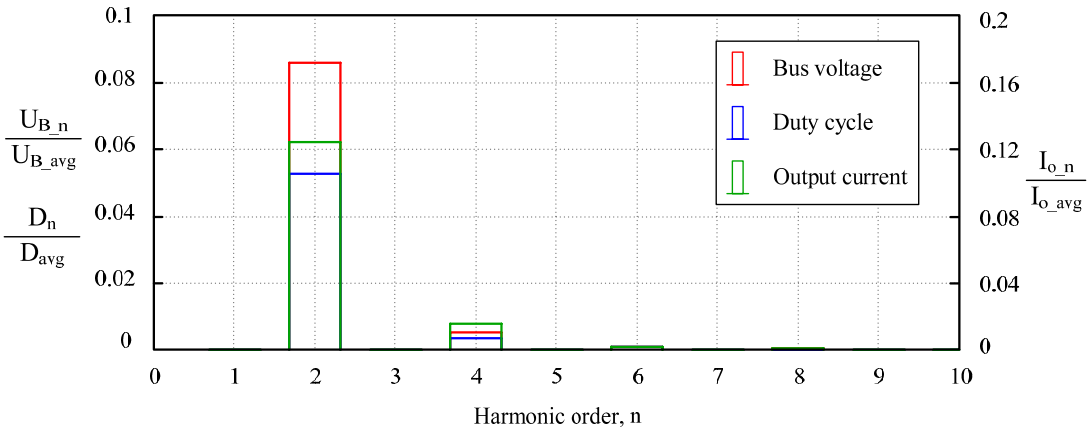

Fig. 7.22. Relative harmonic content of the bus voltage, duty cycle, and output current, disregarding the DC component, for the 1x60 XLamp XR-E configuration under closed-loop nominal operation. First harmonic frequency: 50 Hz.

As can be seen from Fig. 7.22, the bus voltage is slightly reduced, with a greater impact on output-current ripple, which is greatly reduced from somewhat more than 15% down to a 12% with a duty cycle variation roughly around 5%. Finally, Fig. 7.23 shows the input current for the 1x30 XLamp XR-E configuration under nominal operation.

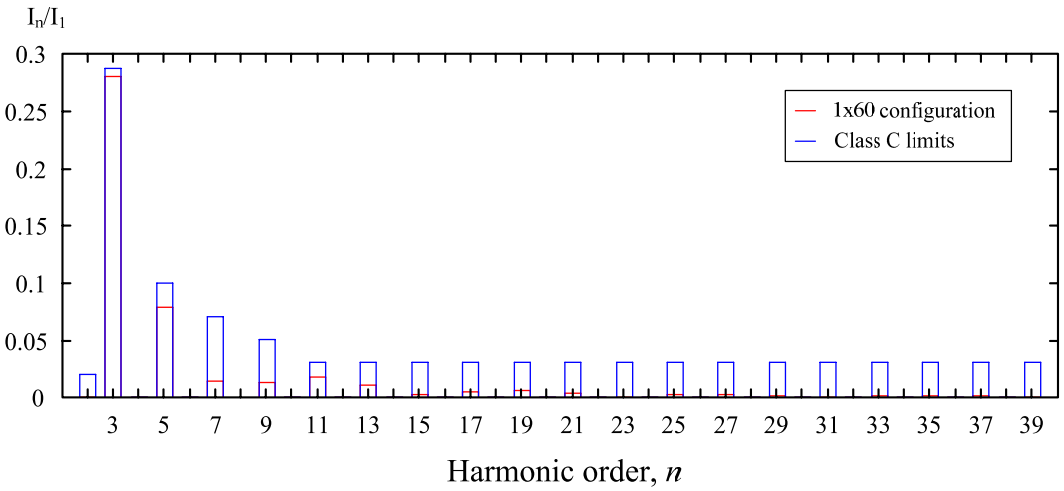

Fig. 7.23. Relative harmonic content of the line current and Class C limits for the 1x60 configuration under closed-loop nominal operation. First harmonic frequency: 50 Hz.

As can be observed from Fig. 7.23, only the 3rd harmonic is pushed upwards by the action of the control signal, but still within the Class C limits for harmonic content.

TABLE VII.IX
CLOSED-LOOP PERFORMANCE IN THE DIFFERENT LAMP CONFIGURATIONS

Lamp configuration		***Dragon Plus***	***Luxeon K2***	***Z-Power P4***	***XLamp XR-E***	***Nominal***
1x60 (1x350 mA) K_{DC} = 190	***PF***	0.954	0.954	0.955	0.955	0.957
	THD_I (%)	29.7	29.7	29.6	29.6	29.3
	3^{rd} (%)	28.5	28.5	28.4	28.4	28.0
	5^{th} (%)	7.8	7.8	7.8	7.8	7.9
	δ (%)	17.4	18.3	17.0	16.7	12.5
1x30 (1x700 mA) K_{DC} = 80	***PF***	0.956	0.955	0.956	0.956	0.958
	THD_I (%)	29.4	29.3	29.3	29.3	29.1
	3^{rd} (%)	28.1	28.1	28.1	28.1	27.9
	5^{th} (%)	7.8	7.8	7.8	7.8	7.8
	δ (%)	19.3	20.0	19.0	18.7	13.9
2x30 (2x350 mA) K_{DC} = 80	***PF***	0.956	0.957	0.957	0.957	0.958
	THD_I (%)	29.4	29.2	29.1	29.1	29.1
	3^{rd} (%)	28.2	27.9	27.9	27.9	27.8
	5^{th} (%)	7.8	7.8	7.8	7.8	7.8
	δ (%)	18.3	15.4	14.3	14.1	13.3

Hitherto, the optimal controller gain for reducing the output-current ripple with a low bus capacitance until the input-current harmonics are pushed up to the Class C limits has been determined. However, a small-signal analysis is still necessary in order to design the feedback loop and obtain the whole closed-loop small-signal model that will allow its dynamic behaviour to be determined. Therefore, the IBFC transfer function, $G_o(s)$, will be calculated for the

nominal junction temperature for each configuration along with the worst cases. This transfer function has already been calculated in Chapter 5. It is recalled here for better readability. The transfer function expression is expanded by substituting (5.10) and (5.24) into (5.23) and rearranging:

$$G_o(s) = \frac{2I_o}{DR_DC_o} \cdot \frac{1}{s + \frac{V_\gamma + 2I_oR_D}{\left(R_DI_o + V_\gamma\right)R_DC_o}} \tag{7.36}$$

Fig. 7.24 shows the Bode plots of the transfer function $G_o(s)$ for the nominal operation point in each lamp configuration, this is, for the XLamp XR-E LED at 80 ºC junction temperature, including the worst-case conditions in order to determine the limits of the loop-gain and closed-loop dynamics.

As can be inferred from Fig. 7.24, a fast-dynamics converter has been achieved, provided that the IBFC bandwidth is located from a few kilohertz up to several kilohertz. However, an integrator-type controller will lead to a much slower closed-loop dynamic behaviour. Therefore, the loop-gain has to be studied. Besides, this loop-gain function will also set the minimum sampling frequency of a digital control. The loop-gain is defined as:

$$L(s) = K(s) \cdot G_o(s) \cdot H(s) \tag{7.37}$$

where $H(s)$ is the feedback block. However, this first study will assume unitary feedback. The next step is to obtain the transfer function of the controller in (7.34). This transfer function is easily obtained:

$$K(s) = K_{DC} \cdot \frac{1}{s} \tag{7.38}$$

Thus, the loop-gain transfer function can be obtained for all the limit operation conditions that have been previously discussed. Fig. 7.25 shows the loop-gain transfer function of the limit-case operation conditions for 1x60 and 1x30 configurations. Unity feedback is considered.

As can be seen from Fig. 7.25, the gain-crossover frequency, f_o, is below 100 Hz for all the operating conditions, being the phase margin (*PM*) around 90º for all the operation conditions. Moreover, the effects of bus voltage and junction temperature can be seen in the dynamic span of the loop-gain transfer function, as previously introduced in Chapter 2. The gain-crossover frequency and the *PM* values are gathered in Table VII.X.

The gain-crossover frequency will be used to set the sampling frequency of the digital control that will be implemented. Since the highest gain-crossover frequency is around 100 Hz, and provided that a practical value for the sampling frequency is from 20 to 40 times, a 4 kHz sampling frequency will be finally set. The block diagram of the digital controller is sketched in Fig. 7.26.

Finally, and in order to avoid aliasing produced by electrical noise in frequencies beyond 2 kHz, and especially, produced by the PWM dimming feature, an analogue first-order low-pass filter will be implemented. The cut-off frequency of this filter will be set to 2 kHz, since its phase-shift will be unnoticeable at the gain-crossover frequency. The loop-gain including this low-pass filter is depicted in Fig. 7.27.

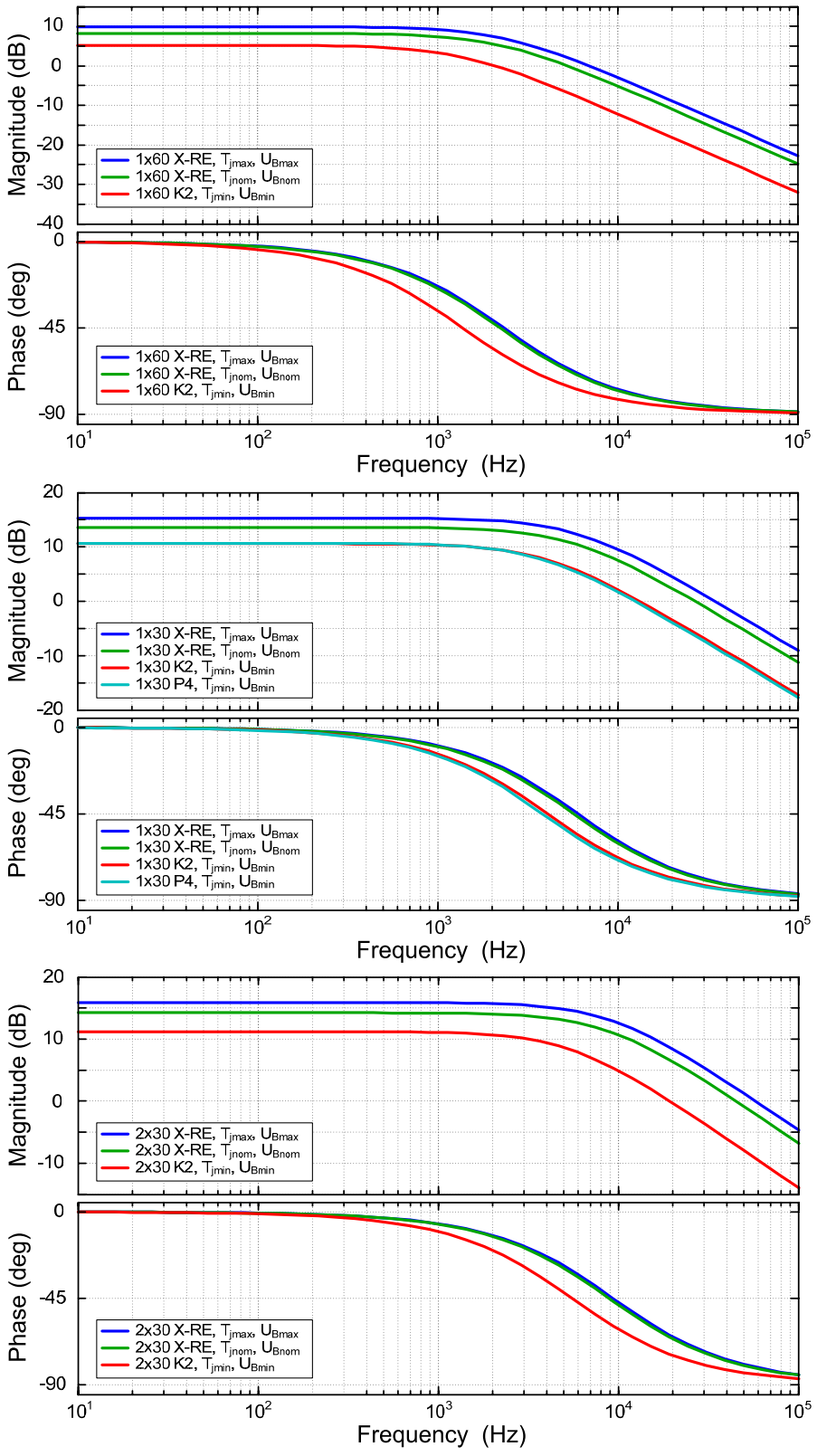

Fig. 7.24. Open-loop IBFC transfer functions for the limit and nominal operation points of each lamp configuration. Top: magnitude and phase plots for the 1x60 configuration. Centre: magnitude and phase of the 1x30 configuration. Bottom: magnitude and phase plots of the 2x30 configuration.

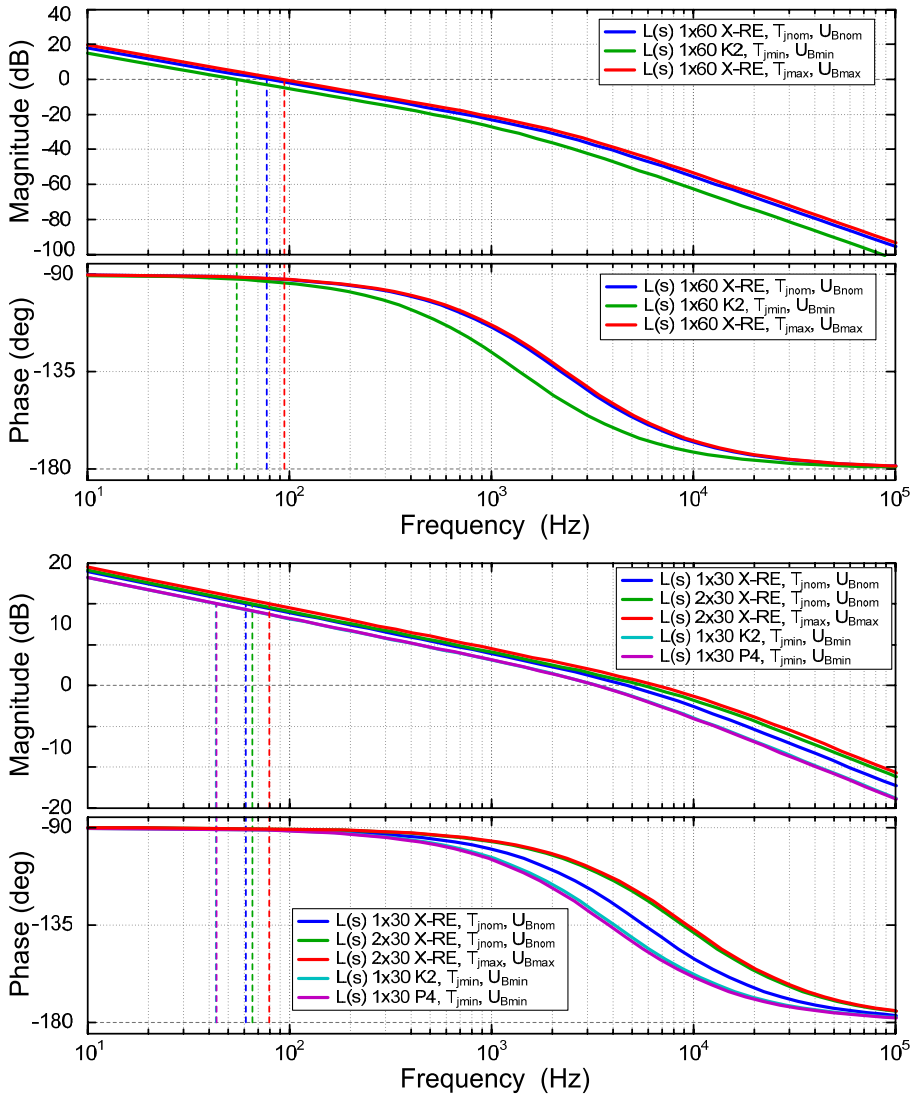

Fig. 7.25. IBFC loop-gain transfer functions for the limit and nominal operation points of each lamp configuration without sensor filter. Top: magnitude and phase plots for the 1x60 configuration. Bottom: magnitude and phase plots of the 1x30 and 2x30 configurations.

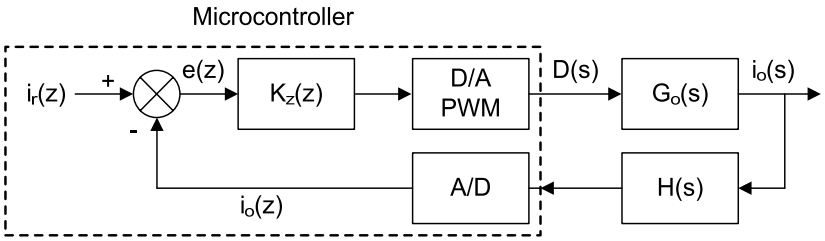

Fig. 7.26. Block diagram of the proposed IBFC LED driver including digital control.

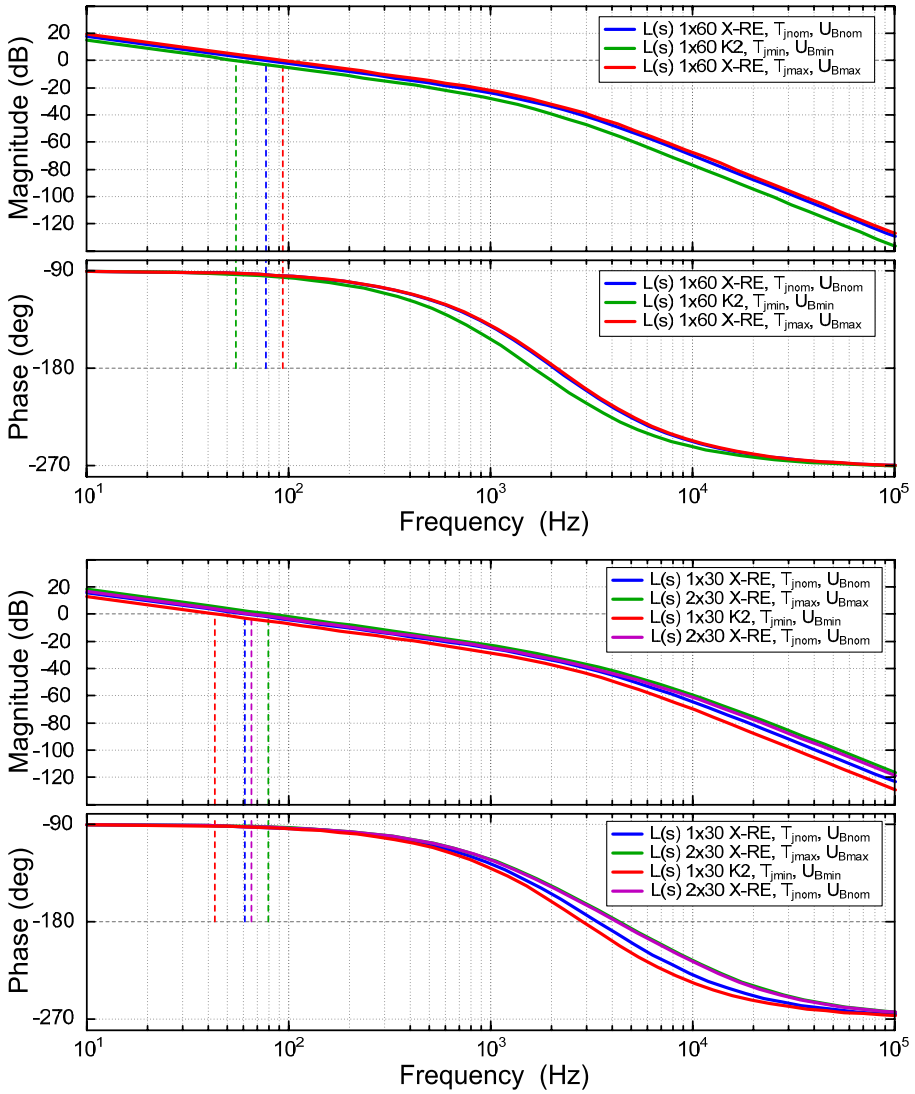

Fig. 7.27. IBFC loop-gain transfer functions for the limit and nominal operation points of each lamp configuration with a 2 kHz cut-off frequency sensor filter. Top: magnitude and phase plots for the 1x60 configuration. Bottom: magnitude and phase plots of the 1x30 and 2x30 configurations.

As can be seen from Fig. 7.27, both the *PM* and gain-crossover frequency are hardly affected.

In order to implement the digital controller, the *K(s)* function has to be discretised. Thus, by applying the Tustin transformation with a 250 µs sampling time, the following digital controllers are achieved for the 1x60 configuration:

$$K_{z60}(z) = \frac{0.02375z + 0.02375}{z - 1} \tag{7.39}$$

and for the 1x30 and 2x30 configurations:

$$K_{z30}(z) = \frac{0.01z + 0.015}{z - 1} \tag{7.40}$$

The implementation of the control loop, as well as the microcontroller finally employed will be discussed in subsequent sections.

TABLE VII.X
LOOP-GAIN TRANSFER FUNCTION PARAMETERS

K_{DC}	*Lamp configuration*	T_j	U_B	*LED*	*PM* (deg)	f_o (Hz)
190	***1x60***	Min.	Min.	K2	87.7	54.9
		Nom.	Nom.	XR-E	88.0	77.8
		Max.	Max.	XR-E	87.7	94.3
80	***1x30***	Min.	Min.	K2	89.4	43.2
				P4	89.3	43.6
		Nom.	Nom.	XR-E	89.4	61.1
	2x30	Nom.	Nom.	XR-E	89.6	65.6
		Max.	Max.	XR-E	89.5	79.5

7.6.2.1. Implementation of dimming feature

In order to provide the proposed LED driver with the highest flexibility, both analogue and PWM dimming techniques will be implemented in the prototype. The main purpose is to achieve at least a 10:1 dimming ratio.

With regard to the analogue technique, this can easily be implemented by a variable reference, as discussed and reported in Chapter 6. This will be covered in the next section.

Regarding PWM dimming, the HFS technique proposed in Chapter 6 will be implemented in the final prototype. The *K(s)H(s)* transfer function, as well as the control sensitivity function studied in Chapter 6 are illustrated in Fig. 7.28 for both controllers under nominal operation.

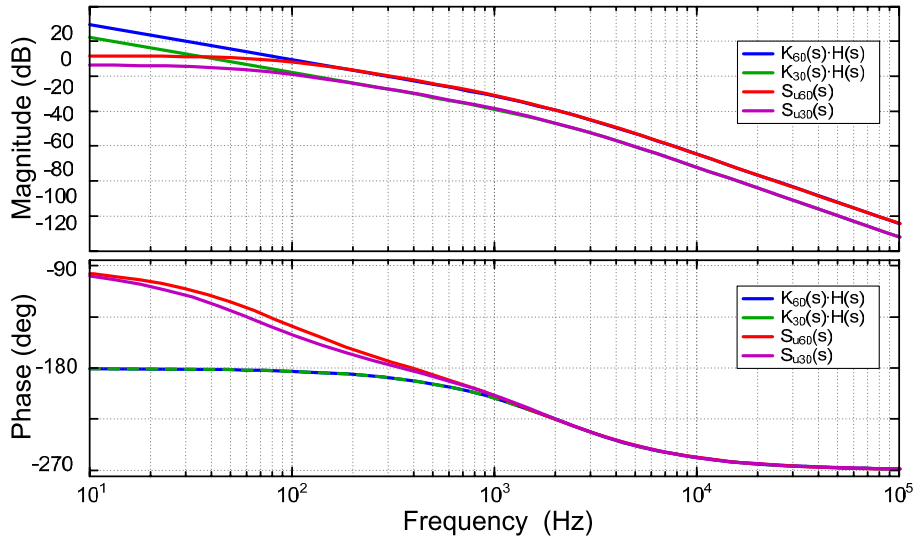

Fig. 7.28. Control sensitivity transfer function for the nominal operation of the 1x60 and 1x30 configurations. The *K(s)·H(s)* open-loop transfer functions are also depicted for the 1x60 and 1x30 controllers. The low-pass sensor filter is considered.

As can be verified from Fig. 7.28, there is a high attenuation at the switching frequency. Therefore, and as in the prototype evaluated in Chapter 6, the dimming frequency finally chosen is 50 kHz, which also simplifies the dimming implementation.

7.6.2.2. Implementation of the control loop

The control loop was implemented by means of a dsPIC 30F6014A, which features up to 30 MIPs operation, peripheral and external interrupts, five 16-bit and two 32-bit timers, a 12-bit A/D converter, 8 Capture/Compare/PWM (CCP) modules within the most representative characteristics. The implementation of the control loop makes use of the A/D converter in order to determine: i) the level of the external potentiometers that determine the duty cycle or dimming level, and ii) the output-current sensor measurement. Two CCP modules are also employed in order to set the main transistor and the dimming transistor PWM signals.

Four operation modes were developed for the laboratory prototype. These operation modes, which were switched by toggle buttons, are described as follows:

- Open loop: in this operation mode, the converter was operated in open loop, the duty cycle being selected by an external potentiometer. The dimming feature is disabled. The open-loop or closed-loop operation is switched by a toggle button.
- Closed loop: in this operation mode, the converter was operated in closed loop, the output current level, either 350 mA or 700 mA, and its corresponding controller being selected by a second toggle button. The dimming feature is enabled, set in analogue by default and switched from analogue to PWM by a third toggle button.
- Dimming mode: in this operation mode, the dimming potentiometer level is scaled to a 0 – 1 range in order to determine the dimming ratio. Afterwards, this scaled signal is multiplied by the output-current reference in order to generate the actual dimmed output-current reference. In the case of analogue dimming feature, the CCP module that drives the dimming transistor is set to a high-level output in order to keep the dimming transistor switched on. Otherwise, the scaled dimming level is directly applied as the dimming transistor duty cycle by the proper configuration of the corresponding CCP module.

The implementation of the control loop using the dsPIC 30F6014A is sketched in Fig. 7.29.

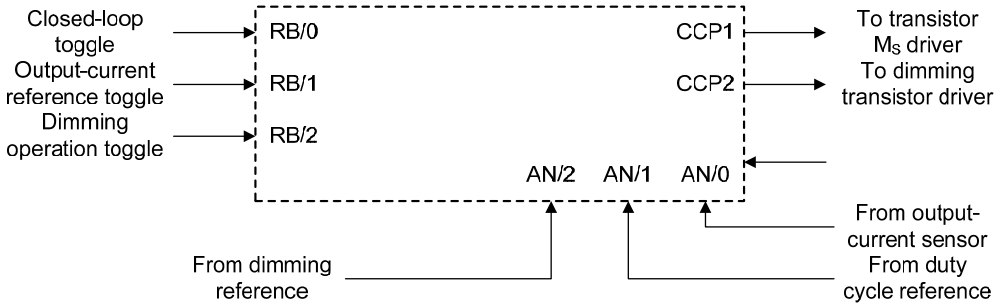

Fig. 7.29. Sketch of the control loop using the dsPIC 30F6014A.

As can be seen from Fig. 7.29, only three analogue inputs with one A/D converter, three digital inputs, and two CCP modules are needed. Therefore, smaller, simpler, less powerful microcontrollers can be employed.

7.6.3. Laboratory prototype

The final laboratory prototype includes an EMI filter consisting of two differential-mode inductors, two common-mode inductors, and four common-mode capacitors, in order to prevent differential- and common-mode conducted noise. A capacitor was also added in parallel to the rectifier-bridge output. The schematics are shown in Fig. 7.30 whereas the complete relation of components is listed in Table VII.XI.

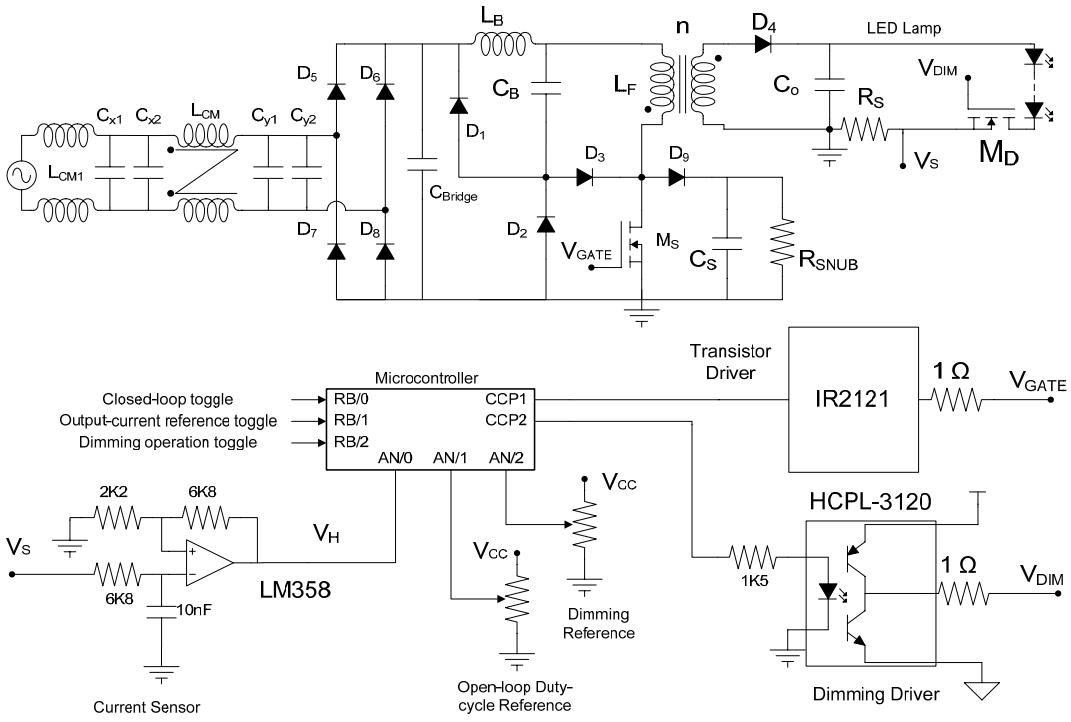

Fig. 7.30. Complete schematics of the entire final laboratory prototype.

The buck and flyback inductors were built using an RM14 core and N47 MnZn ferrite material from Siemens, which is suitable for power applications. In addition, litz wires were used in order to minimise the copper losses due to skin effect. With regard to the buck inductor, the selected strand and diameter were 66x0.08 mm. In relation to the flyback inductor, it was built using the interleaving technique in order to minimise the leakage inductance. A value of 2.05 μH was achieved, representing approximately a 1% of the magnetising inductance, which is satisfactory enough. Moreover, the strands and diameters of the litz wires used in the flyback inductor were 170x0.08 mm for the primary and 66x0.08 mm for the secondary.

The synchronous transistor is driven by means of an IR2121 MOSFET driver whereas the dimming transistor is driven by an optocoupled HCPL-3120 MOSFET driver.

Moreover, a dissipative RCD voltage-clamping snubber was implemented in order to prevent the synchronous transistor from damage due to the overshooting caused by the resonance between the flyback primary inductor and the MOSFET output capacitance. This RCD snubber was designed for a target power dissipation of 1 W under nominal operating conditions.

The output current is measured by means of a 1 Ω shunt resistor. Then, the voltage drop across the shunt resistor is measured by the feedback filter discussed in the previous sections.

The gain of the feedback filter is appropriately set in order to be below 5 V for the entire output-current range including the output-current ripple.

TABLE VII.XI
COMPONENTS OF THE LABORATORY PROTOTYPE

Component	Value
L_{CM1}	2 mH
L_{CM}	20 mH
C_{x1}, C_{y1}	15 nF
C_{x2}, C_{y2}	10 nF
C_{Bridge}	10 nF
D_5, D_6, D_7, D_8	MUR840
L_B	L=284.1 µH RM14 N47; N=40
L_F	L=171.0 µH RM14 N47; n=1.5; N_1=24; N_2=36
M_S	STW12NK80Z; Driver: IR2121
M_D	IRF840; Driver: HCPL-3120
D_1, D_2, D_4	MUR860
D_3	MUR840
C_B	80 µF/400 V
C_o	2x1.0 µF/250 V
D_9	MUR180
C_S	1.5 nF
R_{SNUB}	220 kΩ
R_S	1 Ω
Microcontroller	dsPIC 30F6014A

7.7. Experimental results

The performance of the prototype was tested for the four LED lamps considered at each configuration. Thus, the following points were experimentally verified: i) the open-loop operation in order to check the low-frequency behaviour and high-frequency waveforms; ii) closed-loop operation in order to determine the low-frequency behaviour regarding input current distortion and duty-cycle compensated output-current ripple; iii) closed-loop efficiency at full power for the entire line-voltage range considered, i.e. 184 – 276 V_{rms}; iv) closed-loop self-equalisation for the 2x30 configuration at full power; and v) closed-loop, dimmed operation at nominal line-voltage in order to determine the efficiency of the two techniques proposed and the self-equalisation for the 2x30 configurations.

Regarding the open-loop operation, Fig. 7.31 shows the low- and high-frequency waveforms for the bus voltage, output current and MOSFET drain-to-source voltage under 276 V_{rms} input voltage.

As can be observed in Fig. 7.31, the low-frequency operation is characterised by a significant bus-voltage ripple that is transmitted to the output current through the flyback converter ripple-gain factor. However, it can be seen that the bus-voltage ripple accounts for approximately 15% of the bus-voltage average value, with a peak-to-peak output-current ripple lower than 140 mA, as theoretically predicted. With regard to the high-frequency operation, the

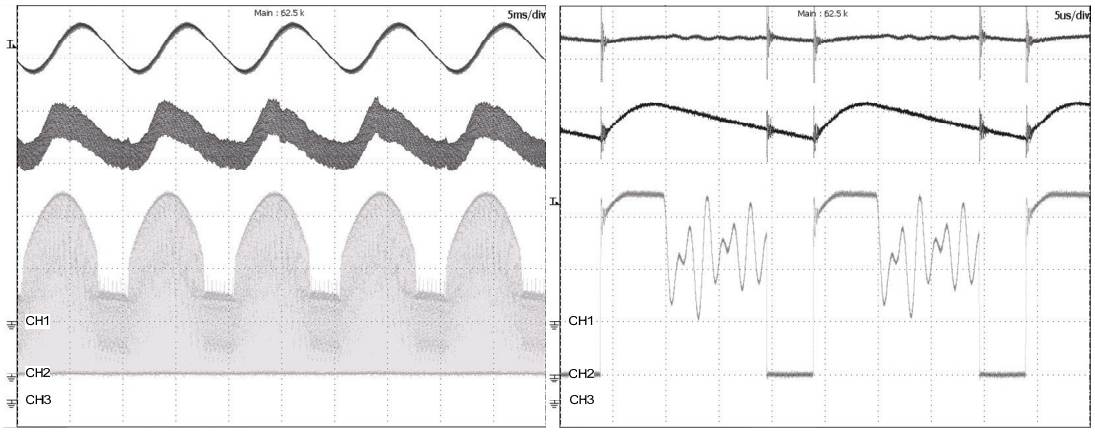

Fig. 7.31. Bus voltage (CH3, top trace), output current (CH1, centre trace), and MOSFET drain-to-source voltage (CH2, bottom trace) for the Golden Dragon Plus 1x60 configuration under 276 V_{rms} input voltage. Left: low-frequency waveforms. Right: high-frequency waveforms. Vertical scale: output current, 100 mA/div; bus voltage: 25 V/div; drain-to-source voltage: 200 V/div. Horizontal scales: 5 ms/div (left), 5 μs/div (right).

optimal operation of the RCD voltage-clamping snubber could be highlighted. Moreover, Fig. 7.32 shows the line voltage, input current, bus voltage, output current and input power for the XLamp XR-E 1x60 configuration, as well as the same results for open-loop operation in order to compare the feedback loop performance.

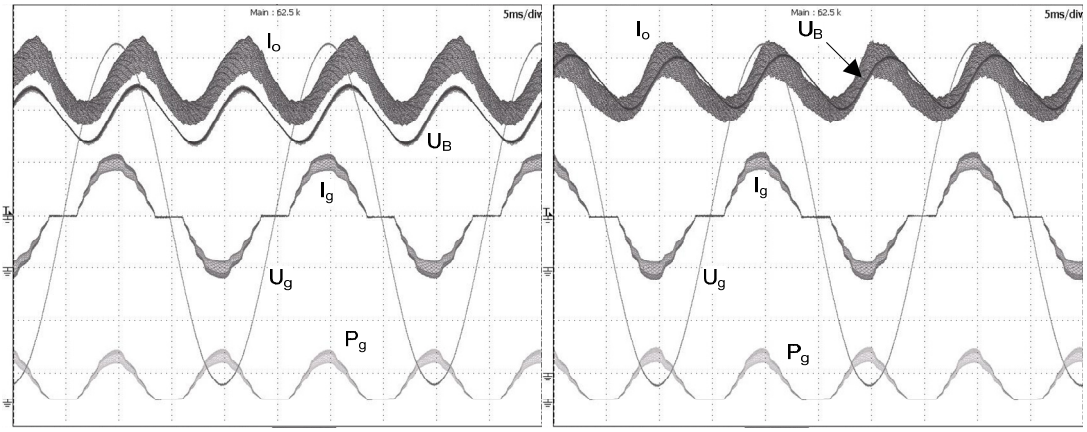

Fig. 7.32. Bus voltage (U_B), output current (I_o), line voltage (U_g), input current (I_g), and input power (P_g) for the XLamp XR-E 1x60 configuration at 230 V_{rms} under open-loop operation (left) and closed-loop operation (right). Vertical scale: output current, 100 mA/div; bus voltage: 25 V/div; line voltage: 100 V/div; input current: 500 mA/div; input power: 200 W/div. Horizontal scale: 5 ms/div.

It can be noticed from Fig. 7.32 that both the output-current and bus-voltage ripples are significantly reduced in closed-loop, whereas the input current is slightly sharpened, being slightly phase-advanced in comparison to open-loop operation. The performance of the feedback loop in the current-ripple compensation task can be further verified. This is shown in Fig. 7.33, where the output current, bus voltage, input current, and duty-cycle average, as measured at the transistor gate, are provided together with their theoretical predictions.

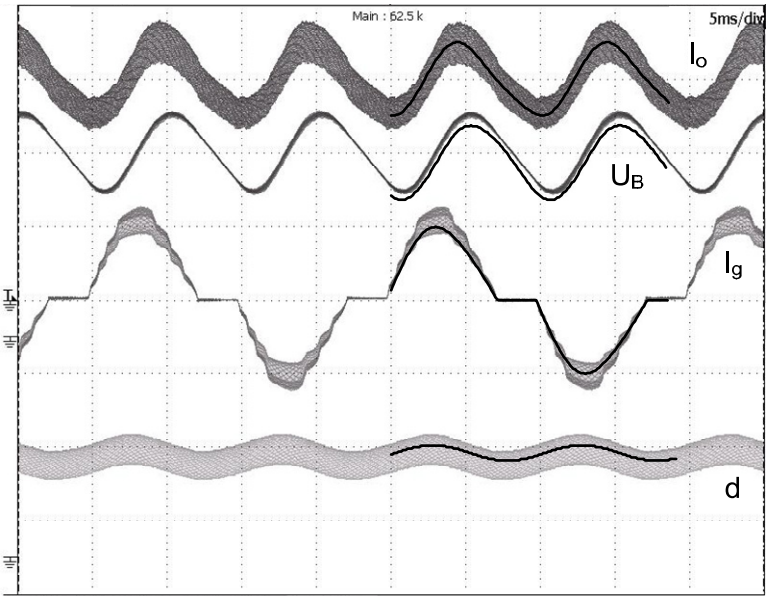

Fig. 7.33. Output current (I_o), bus voltage (U_B), input current (I_g), and averaged duty-cycle measured at the transistor gate (d) for the XLamp XR-E 1x60 configuration at 230 V_{rms} under closed-loop operation together with the theoretical values superimposed (solid lines). Vertical scale: output current, 100 mA/div; bus voltage: 25 V/div; duty cycle: 2 V/div. Horizontal scale: 5 ms/div.

As can be seen from Fig. 7.33, an excellent agreement between the theoretical and the experimentally measured values is achieved, which confirms the adequacy of the design procedure proposed in this work.

With regard to the PFC performance, Fig. 7.34 shows the effect of the feedback loop on the input current distortion. Thus, the input-current harmonic content up to the 7th harmonic measured for the XLamp XR-E 1x60 configuration in open loop and in closed-loop are depicted.

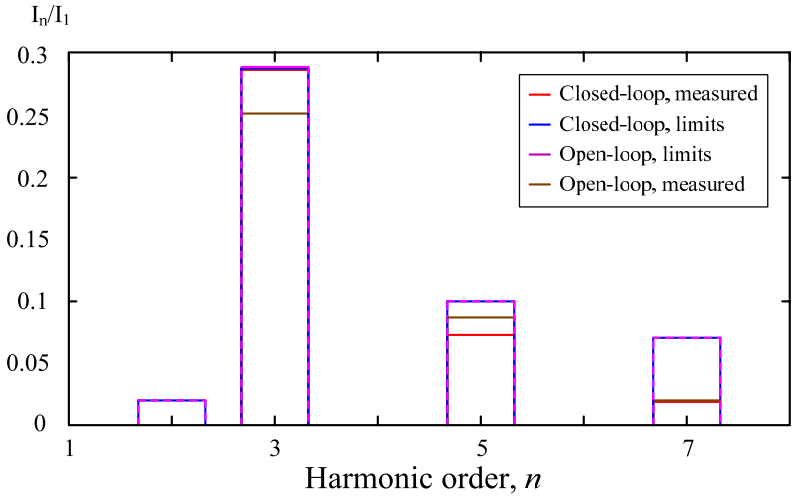

Fig. 7.34. Input-current harmonic distortion results for the XLamp XR-E 1x60 configuration under closed- and open-loop operation. Line frequency: 50 Hz.

As can be deduced from Fig. 7.34, the feedback loop increases the 3th harmonic and reduces the 5th, as theoretically predicted. With regard to the *PF*, it is slightly reduced as expected, due to the phase-shift that the feedback loop introduces in the input current.

Since the most compromising harmonic in order to comply with Class C regulation is the 3rd harmonic, the experimental results obtained at full power and under 230 V_{rms} line input for the four lamps at every configuration will be studied in order to determine the Class C compliance. This is depicted in Fig. 7.35. As can be seen, the IBFC featuring output-current-ripple feedback compensation successfully meets the Class C requirements for all the lamp configurations considered.

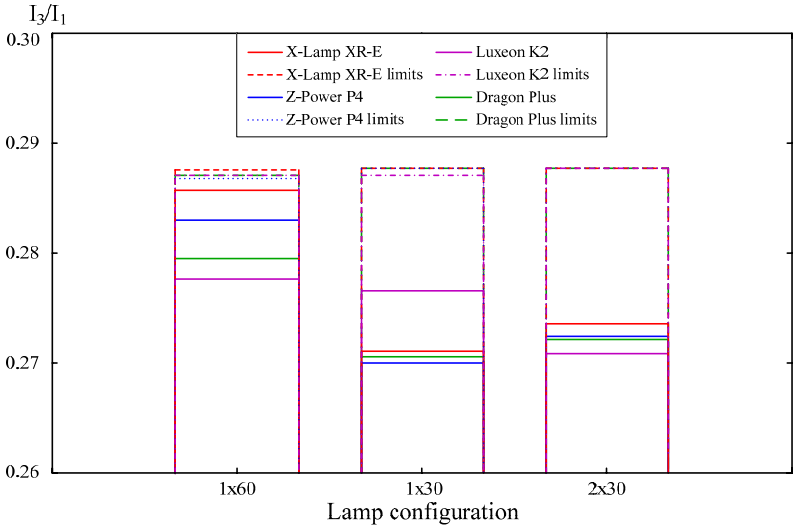

Fig. 7.35. Third harmonic (solid line) and third-harmonic limits (dotted-dashed lines) for each LED lamp configuration. Line frequency: 50 Hz.

Regarding the self-equalisation of the different LEDs employed, the four lamps were tested in the 2x30 configuration at ambient temperature and full power, and under nominal line voltage. Thus, the current through each paralleled string was measured the results being gathered in Table VII.XII.

TABLE VII.XII
FORWARD CURRENT DEVIATION FOR THE 2X30 CONFIGURATION

LED	V_D (V)	I_{D1} (mA)	I_{D2} (mA)	I_o (mA)	ψ (%)
Golden Dragon Plus	94.46	326.0	373.0	699.0	6.6
Luxeon K2	96.85	343.0	356.0	699.0	1.8
Z-Power P4	93.26	325.0	374.0	699.0	7.0
XLamp XR-E	91.59	325.0	372.0	697.0	6.8

As can be noticed, the results obtained from the laboratory prototype are worse than those obtained with the specific DC driver used to characterise the LEDs, with a significant increase in current mismatch for the Z-Power P4 and the Golden Dragon Plus devices, which doubles the difference between string currents. In the case of XLamp XR-E and Luxeon K2 devices, there is a slightly higher difference in current balancing, the Luxeon K2 being the only device that meets the 5% tolerance imposed. This worsening of the experimental results could likely be owed to the large ripple present in the output current, although further experimentation should

be developed in order to determine the effects of large ripples in current self-equalising. Nevertheless, it can be concluded that tightly-binned LEDs are suitable for self-equalisation even with large current ripples present.

With regard to the efficiency as a function of the line voltage, the Luxeon K2 1x60 and 1x30 lamp configurations were tested, since this LED features the highest forward voltage, thus leading to maximum voltage stresses on both the transistor and diode D_4. The lamps were tested at full power and the input voltage ranged from 184 V_{rms} to 276 V_{rms}. This is illustrated in Fig. 7.36.

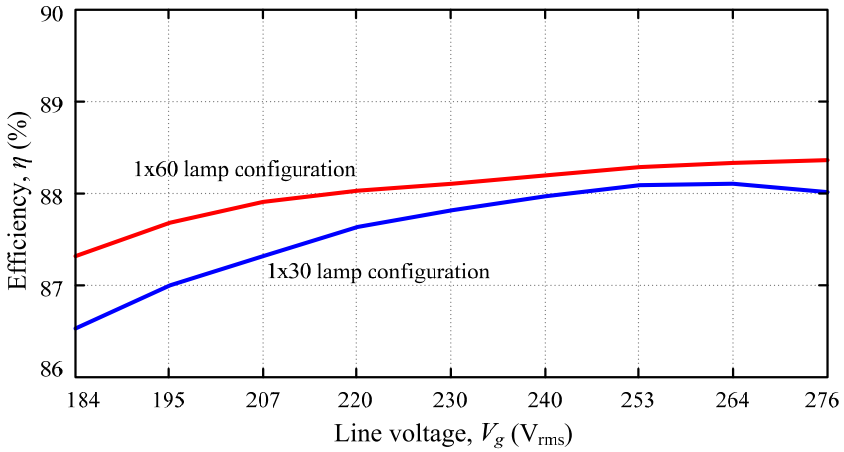

Fig. 7.36. Efficiency as a function of the line voltage for the Luxeon K2 LED in 1x60 and 1x30 configurations at full power.

As can be seen from Fig. 7.36, good efficiency has been achieved for both configurations, greater than 86% for the entire line voltage operation range, with approximately 88% efficiency at nominal line voltage. In addition, it has to be remarked that the 1x30 configuration is less efficient, although presenting only significant differences for the lowest line voltage values. These results are quite satisfactory, especially taking into account that buck-based PFC feature higher bus currents. Other proposals, such as the integrated double buck-boost, have reported 86% efficiency with the same operation characteristics [7.17].

Finally, and in regard to dimming operation, both analogue and HFS-PWM techniques were tested for the 1x60 and 1x30 lamp configurations. Only the results for the XLamp XR-E LED will be provided in order to avoid redundancy.

The high-frequency results of PWM dimming are shown in Fig. 7.37, which depicts the output current of the 1x60 configuration at four dimming levels: 90%, 50%, 10% and 5%.

As can be observed from Fig. 7.37, the HFS-PWM dimming technique provides the IBFC with high dimmability, with extremely fast rising and falling edges. In addition, a 20:1 CR has been finally achieved for the 1x60 lamp configuration, although the 1x30 configuration feature a slight instability for such a low dimming ratio. Nevertheless, a 10:1 CR has been achieved for all circumstances, which is satisfactory for general applications and meets the design requirements.

In relation to the input-current harmonic content, Fig. 7.38 shows the line voltage and the input current for the four operation points depicted in Fig. 7.37. As can be noticed from Fig. 7.38, the input current is hardly distorted, even for the 20:1 *CR*. Moreover, the harmonic content has been measured for the 1x60 and 1x30 configurations. It is illustrated in Fig. 7.39.

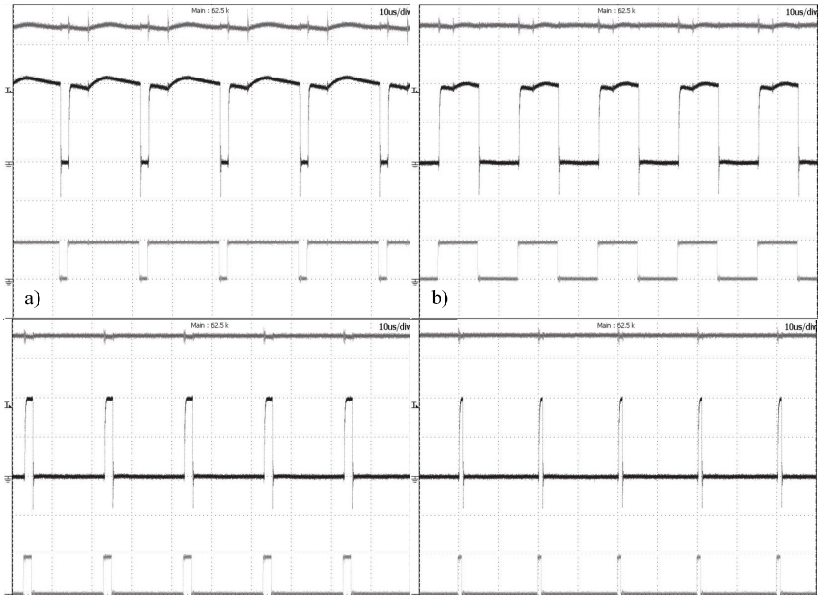

Fig. 7.37. Output voltage (upper trace), output current (centre trace) and PWM dimming signal (lower trace) under nominal line voltage for four operation points: a) 90% dimming ratio; b) 50% dimming duty cycle; c) 10% dimming duty cycle; d) 5% dimming duty cycle. Vert. scale: output voltage: 25 V/div; output current, 200 mA/div; dimming signal, 5 V/div. Horiz. scale: 10 μs/div.

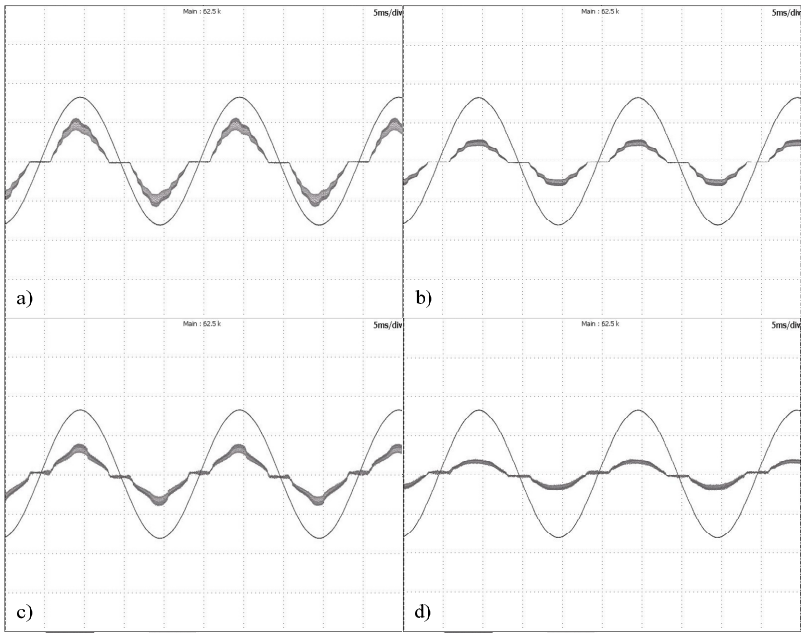

Fig. 7.38. Input current and nominal line voltage for four operation points: a) 90% dimming ratio; b) 50% dimming duty cycle; c) 10% dimming duty cycle; d) 5% dimming duty cycle. Vert. scale: line voltage: 200 V/div; input current: 500 mA/div (a, b), 100 mA/div (c, d). Horiz. scale: 5 ms/div.

As can be seen from Fig. 7.39, the THD_I is maintained approximately constant throughout the dimming range, except for the lowest relative-output values, as could be demonstrated in Chapter 6. The same behaviour is obtained for the power factor, which is depicted in Fig. 7.40.

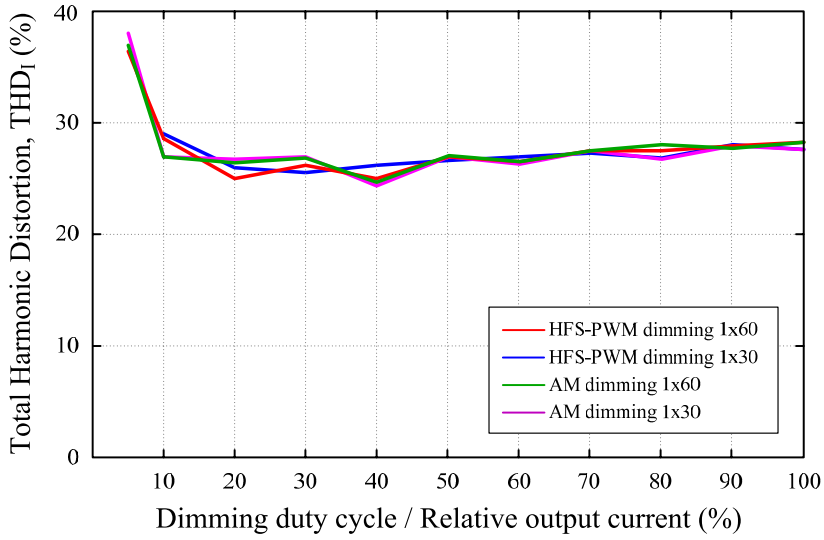

Fig. 7.39 Input current Total Harmonic Distortion (THD_I) results obtained from the laboratory tests of analogue and HFS-PWM dimming tests for the XLamp XR-E 1x60 and 1x30 configurations.

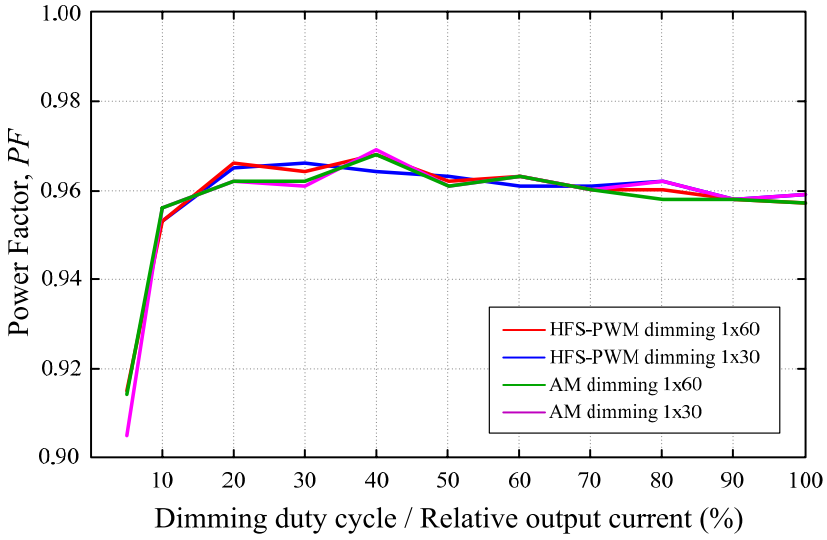

Fig. 7.40. Power factor (PF) results obtained from the laboratory tests of analogue and HFS-PWM dimming tests for the XLamp XR-E 1x60 and 1x30 configurations.

Finally, Fig. 7.41 shows the efficiency for the XLamp XR-E 1x60 and 1x30 configurations for HFS-PWM dimming, as well as for AM dimming.

As can be observed from Fig. 7.41, the efficiency remains fairly flat for most of the dimming range, although it is abruptly decreased for the highest dimming ratios. As discussed in Chapter 6, this is caused by the decrease in conduction losses due to the lower currents involved in dimmed operation, with the switching losses kept in similar values. This also explains the better efficiency of the 1x30 configuration at low dimming ratios, since the currents reach low levels, and the voltage stresses on semiconductors, specifically on the synchronous transistor and diode D_4, are lower than in the 1x60 configuration.

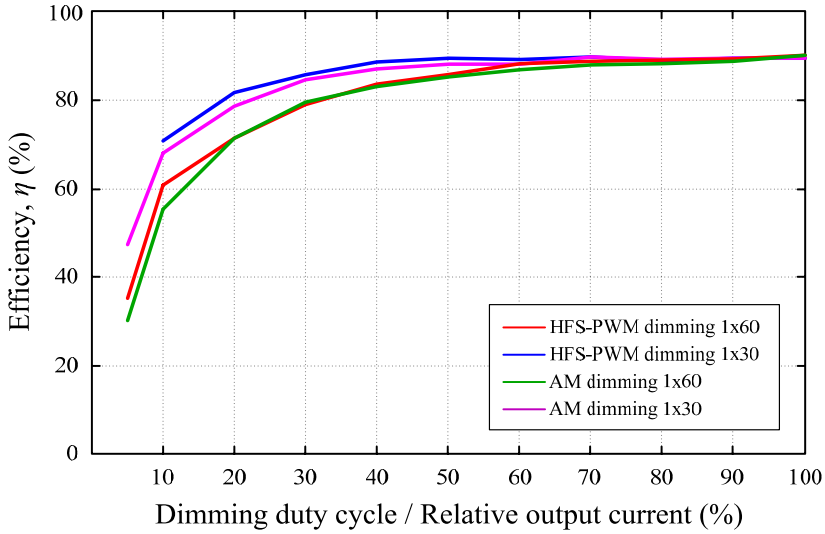

Fig. 7.41. Efficiency results obtained for analogue dimming (AM dimming) and high-frequency series PWM dimming (HFS-PWM dimming) with 1x60 and 1x30 XLamp XR-E lamp configuration.

7.8. Results discussion and conclusions

An optimised design of the IBFC as an LED driver has been dealt with in this chapter. This optimised design considers a multiple-fold approach. It starts with a study on efficiency, which considers the electrical stresses on semiconductors in order to determine the switching and conduction losses, which, together with other considerations regarding the design of the converter and the LED lamp, will allow the efficiency to be maximised. Afterwards, the parallel connection of LED strings has been studied in order to explore the feasibility of self-equalisation for a given number of series-connected LEDs. This study has been performed with the statistical approach that was firstly introduced in Chapter 2. The self-equalisation has been concluded to be feasible for tightly-binned LEDs, unbinned LEDs featuring high current mismatches between paralleled strings. Then, the design of the lamp finally includes three different configurations for a 70 W lamp: either 60 series-connected LEDs run at 350 mA, 30 series-connected LEDs run at 700 mA, or two paralleled strings of 30 series-LEDs run at 350 mA each.

Once the keystones of efficiency have been studied, the reduction of the bus capacitor, in order to avoid the use of electrolytic devices, has been researched. This way, the relation between the output-current ripple and the bus-voltage rippled has been obtained. Afterwards, the low-frequency flicker index has been studied in order to determine a reasonable level that sets the maximum bus-voltage ripple. However, as has previously been demonstrated, the bus-voltage ripple affects the input current, introducing a higher level of distortion. Therefore, the relation between the bus-voltage ripple and the input current has been established. Thus, the harmonic content of the input current has been studied for four dead angles, obtaining that reducing the dead angle highly improves the buck-converter PFC performance at the cost of a higher bus-voltage ripple. Finally, the conclusion that the optimal dead angle value is slightly below 25º has been yielded, since the PFC is improved and still provides margin for implementing a fast controller without a significant loss on bus-voltage ripple.

After the theoretical studies were developed, a laboratory prototype has been built. This prototype has been designed for the European line voltage supporting a flexible operation in

terms of temperature range, line-voltage tolerance and LED lamp. The dead angle has been set to a value slightly higher than 25º in order to improve PFC while still providing margin for enhancing the controller dynamics and enough duty-cycle headroom for dimming operation. Then, the converter could finally be designed with a non-electrolytic capacitor in order to extend its expected life-span to values similar to those of the LEDs. However, the output-current ripple target could not be met only by the bus capacitor considered, but a proper choice of a simple integrator controller could finally meet the ripple requirements imposed in the design. Moreover, a digital control was implemented in order to achieve a highly flexible control, which includes the optimal controller for each lamp configuration while simplifies the implementation of analogue and HFS-PWM dimming techniques.

With regard to the laboratory prototype, the experimental results matched the theoretical predictions, confirming the suitability of the proposed design procedure. Thus, the output current and bus-voltage ripple values have been correctly predicted, as well as the input current, which actually experienced a phase advance due to the bus-voltage ripple and the controller action. The laboratory prototype adequately meets Class C requirements as expected for the three lamp configurations. However, the self-equalisation capability of paralleled LED strings has been proven to be affected by the large current ripple, showing a higher mismatch in the four LED lamps, although tightly-binned LEDs still achieved reasonable self-equalisation results.

Regarding efficiency, a highly satisfactory performance for an IPC has been achieved, since the efficiency values are above 86% for the lowest line voltage considered, with a maximum value slightly beyond 88% for the 1x60 configurations, with slightly lower values for the 1x30 configuration.

Finally, the dimmed operation of the converter has been tested. Good results have been achieved, confirming the conclusions obtained in Chapter 6 in terms of PFC. In relation to the efficiency under dimmed operation, it has been concluded that the lower voltage stresses that the 30-series LEDs configuration yields better results for low-power operation, where the conduction losses are kept at a low level.

In conclusion, the IBFC has been proved to be a reliable, high-performance LED driver for general indoor/outdoor lighting applications where a low-cost, efficient converter is required.

7.9. References

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Chapter 8

Conclusions, Main Contributions, and Future Developments

This last Chapter firstly introduces the main conclusions achieved in this PhD Thesis work. Following are the contributions of this work and the future developments expected.

8.1. Conclusions

The main conclusions derived from the experimental work developed in this PhD Thesis and the results obtained can be resumed in the following topics, sorted by category:

With regard to the research about **LEDs as a power load**, it can be summarised that:

- Four LEDs from four different manufacturers, which account for a significant share of the worldwide LED market, have been deeply characterised. This characterisation is aimed on thermally modelling and statistically studying the LEDs in order to determine the forward voltage typical values for a given lamp configuration at any junction temperature.
- The LEDs junction temperature can be accurately determined by measuring the forward voltage drop of the lamp after the ensemble has been thermally modelled. However, significantly inaccurate results are obtained if the ensemble thermal model is applied to single, unbinned LEDs. In the case of binned LEDs, a ±10 ºC tolerance has been experimentally obtained. IR thermography has been applied, confirming this assumption.
- The LEDs parameters dependence upon junction temperature has been experimentally determined. This way, the reverse saturation current, ideality factor and series parasitic resistance have been determined as a function of temperature. However, several low-current test points are required in order to fit the reverse saturation current accurately.
- The LEDs forward voltage has been proven to be either almost linear or markedly quadratic, depending on the device structure
- The LEDs dynamic resistance has proven to be temperature dependent, with a different behaviour depending on the device structure. Thus, a higher-order fitting polynomial was obtained for the LEDs showing a higher quadratic forward-voltage thermal behaviour.
- The LEDs thermal behaviour has been demonstrated to affect the closed-loop operation and the output-current ripple of the LED driver.
- Self-equalisation of paralleled LED strings has been statistically studied for a minimum number of series-connected devices. It has been concluded that binned LEDs are more suitable for self-equalisation than unbinned LEDs, which require a large number of series-connected emitters.

Regarding the development of the **IBFC-based LED driver** and its optimisation, it can be concluded that:

- It has been theoretically calculated that the bus-capacitor size needed for buck-boost PFP is only slightly lower than that of a buck PFP for the same bus voltage. In addition, it has been theoretically, by means of a newly proposed harmonics map, and experimentally demonstrated that a buck converter PFP featuring a 25º dead angle meets the Class C harmonic limits with the highest bus voltage possible.
- It has been experimentally demonstrated that the integrated buck-flyback converter is a suitable LED driver featuring universal-range line voltage for lamps in the range of 70 W for outdoor general applications and street lighting.
- The ripple-gain factor has been derived. This parameter accounts for the bus-voltage to output-current gain and is very useful in order to calculate the required minimum bus capacitor.

- Regarding the operation of the IBFC, Full DCM operation is considered more satisfactory than DCM/CCM due to a lower ripple-gain factor and first-order dynamic behaviour. This yields lower bus-capacitor constraints and simpler closed-loop control.
- Three different lamp configurations have been considered in order to maximise the efficiency of the IBFC, resulting in a better efficiency with a single string of series-connected LEDs at 350 mA.
- The ripple-gain factor is a useful tool in order to study the maximum allowable bus ripple. Thus, by setting a moderate output-current ripple, MKP devices can be used for the DC storage.
- The bus-voltage ripple effect on the input-current distortion has been studied, concluding that significant ripples improve the PFC performance.
- The optimal dead-angle target has been obtained to be slightly lower than 25º, since the bus capacitor requirements are not significantly compromised whereas the harmonic-content margin is reduced.
- An integrator controller has been developed in order to compensate the output-current partially while still complying with Class C harmonic content limits. This way, two specific controllers have been developed for the two output currents considered.
- The proposed prototype has achieved an excellent performance, featuring an 80 µF bus capacitor, which is easily implementable by a non-electrolytic device, 20% output-current ripple, Class C compliance with a fast enough control loop under any operation condition, achieving around 88% efficiency.

Finally, the research on **PWM dimming schemes** has shown that:

- The traditional PWM dimming techniques, namely enable, series, and parallel dimming have been considered unsuitable for its application in slow-dynamics converters due to the high input-current distortion introduced, oscillation due to the controller action, and short-circuiting of the output capacitor, respectively.
- A new PWM dimming technique has been proposed, studied and experimentally tested and validated. This technique is based on the series scheme but performing the dimming action at a frequency much higher than the converter cross-over frequency, where the control sensitivity function highly attenuates the output-current disturbances, obtaining up to a 10:1 dimming ratio.

8.2. Contributions

The contribution of this PhD work is to develop a comprehensive set of tools for designing a high-performance, cost-efficient, fully-functional LED driver based on the IBFC for supplying LED lamps with an output power in the range of 70 W. These tools can be sorted according to the field of study.

With regard to the LED lamp analysis, this set of tools includes a complete LED thermal characterisation that assists to design the feedback loop and to prevent the output-current ripple shift; and a statistical tool for evaluating self-equalisation of paralleled LED strings.

With respect to the power stage design, this tool set provides with a harmonics map that helps to set the most appropriate dead angle of the buck PFP; a ripple-gain factor that gives the relation between the bus-voltage ripple and the output-voltage ripple; a set of input-current harmonics maps as a function of the bus capacitor and bus-voltage ripple; a set of input-current harmonics maps as a function of the dead-angle target; and a feedback loop design procedure

for complying with Class C requirements while partially compensating the output-current ripple. It also provides with a PWM dimming technique suitable for slow-dynamics converters.

The main contributions of this PhD work are listed as follows, the related published papers being detailed in Section 8.4.

- A method for obtaining the small-signal dynamic resistance and the threshold voltage for a given operation point. This method employs a superimposed small-signal perturbation on the DC LED current as introduced in [8.1] and further developed in [8.2], [8.3], and [8.4]. A statistical study has also been performed in order to determine the statistical relevance of the experimental results obtained.
- The experimental evidence that forward-voltage junction-temperature measurement method obtained from the entire lamp characterisation cannot be straightforwardly applied to unbinned LEDs in order to measure a single emitter temperature due to large estimation errors.
- Different forward-voltage and dynamic-resistance thermal behaviours have been documented depending on the LED internal structure, demonstrating that this parameters thermal dependence affects both the closed-loop operation and the output-current ripple [8.2], [8.3], [8.4].
- A complete set of equations and graphics, and a harmonics map for designing a DCM buck PFP regarding the bus voltage and input-current harmonic content [8.5], [8.6], [8.7], [8.8]. In addition, the IBFC has proven to be a successful LED driver for lamps in the range of 70 W [8.5], [8.6], [8.7].
- A parameter, namely the ripple-gain factor, which relates the bus-voltage-ripple to output-voltage-ripple converter gain, thus allowing the maximum allowable bus-voltage ripple to be calculated [8.8], [8.9], [8.11], [8.13], [8.13]. Further development of this parameter considering the LED lamp threshold voltage and dynamic resistance yields the relation between the output-current and the bus-voltage ripples.
- The evidence that Full DCM operation is more advantageous than DCM/CCM in ISSCs due to the lower ripple-gain factor [8.8], [8.9], [8.10], [8.11], [8.13], [8.13], which leads to lower DC-link capacitances for the same ripple, and first-order dynamics.
- A set of equations, graphs and harmonics maps for choosing the optimal theoretical dead angle with minimum capacitor required for a target output-current ripple.
- A design procedure for implementing a simple controller to compensate the output-current partially whilst complying with Class C harmonic-content requirements.
- The experimental evidence that low-frequency PWM dimming introduces high distortion in the input current of ISSCs [8.5], [8.6], [8.7], [8.14], [8.15], [8.16], regardless the dimming scheme.
- A High-Frequency-Series PWM dimming technique has been proposed in order to overcome the forehead mentioned issues of standard PWM techniques, based on the study of the control sensitivity function, and achieving 10:1 dimming ratio and even up to 20:1 dimming ratio for some operation conditions [8.14],[8.15],[8.16]. Two dimming modes are considered: either with fixed current-peak value or variable. This dimming technique has earned a Spanish patent [8.17].
- A statistical study procedure has been proposed for determining the minimum series-connected LEDs in paralleled strings for passive self-equalisation.
- A complete, fully-functional laboratory prototype has been built, featuring long operating life due to the MKP DC-link capacitor, 88% efficiency and up to 20:1

dimming ratio, while complying with Class C harmonic-content requirements for all the operation conditions considered.

8.3. Future developments

Besides this PhD Thesis presents a fully-functional long-life IBFC LED driver, a number of research lines arise for future work and development. These research lines are listed below:

- A statistical study on the dynamic-resistance, forward-voltage and threshold-voltage thermal dependence of single LEDs in order to obtain deeper information about average values and standard deviation for a given operation temperature range.
- A thermal analysis of the LED lamp arrangement in order to detect temperature gradients and eventually estimate the LED lamp parameters more accurately.
- A deeper study on passive self-equalisation taking into account the probability distribution function of threshold voltage and dynamic resistance, extending this analysis to the entire operation temperature range.
- An analysis of the influence of current ripple on current mismatches between paralleled strings.
- An ageing process of LED lamps in order to study the LED parameters shift with time.
- A study on the series-resistor needed for improving self-equalisation of strings.
- Research on more complex controllers for partially compensating the output-current ripple whilst complying with Class C harmonic-content requirements.
- Develop a line-frequency small-signal average model in order to determine the low-frequency dynamic behaviour of the IBFC, as introduced in [8.18] for the double buck-boost integrated converter.
- Analysis of different control techniques suitable for current-controlled loads, such as: free-wheeling control, namely DCM I_{MAX}-T_{OFF} and T_{ON}-I_{MIN} current-control schemes; CCM with peak-current control; or variable-frequency BCM, regarding the bus-capacitor requirements and the input-current harmonic distortion content, such as in [8.19], [8.20].
- Evaluation of the tapped-buck converter as the front-end PFP for universal input range with a bus voltage in the range of 12 – 48 V in order to integrate the IBFC with stand-alone power systems, micro-grids, and renewable micro-generation with local energy storage.
- Further development of the HFS-PWM dimming technique in order to reduce the dimming frequency to 20 kHz for reducing the switching losses.

8.4. Published papers

The papers related to the work developed in this PhD Thesis that have been published in national/international conferences, international journals, and international journals contained in the Journal Citation Index (JCR) are listed below:

[8.1] Garcia, J.; Calleja, A.J.; Corominas, E.L.; Gacio, D.; Ribas, J.; "Electronic driver without electrolytic capacitor for dimming High Brightness LEDs," in Conference Records of the 35th Annual Conference of IEEE Industrial Electronics, 2009. IECON '09, pp. 3518-3523. 3-5 November 2009.

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[8.5] Gacio, D.; Alonso, J.M.; Calleja, A.J.; Garcia, J.; Rico-Secades, M.; "A Universal-Input Single-Stage High-Power-Factor Power Supply for HB-LEDs Based on Integrated Buck–Flyback Converter," in Proceedings of the Twenty-Fourth Annual IEEE Applied Power Electronics Conference and Exposition, 2009. APEC 2009, pp. 570 – 576. 15 – 19 February 2009.

[8.6] Gacio, D.; Alonso, J.M.; Calleja, A.J.; Garcia, J.; Rico-Secades, M.; "Convertidor universal Buck-Flyback integrado con alto factor de potencia para aplicaciones de iluminación con diodos LED de alta eficiencia," in Actas del XVI Seminario Anual de Automática, Electrónica Industrial e Instrumentación 2009, SAAEI'09, pp. . 1 – 3 July 2009.

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[8.8] Alonso, M.; Gacio, D.; Calleja, A. J.; Sichirollo, F.; Silva, M. F.; Dalla Costa, M. A.; Prado, R. N.; "Reducing Storage Capacitance in Off-Line LED Power Supplies by Using Integrated Converters," in Conference Records of the 47th Industry Applications Conference, 2012, IAS Annual Meeting 2012. Las Vegas, Nevada, USA. October 2012.

[8.9] Alonso, J.M.; Vina, J.; Vaquero, D.G.; Martinez, G.; Osorio, R.; "Analysis and Design of the Integrated Double Buck–Boost Converter as a High-Power-Factor Driver for Power-LED Lamps," in IEEE Transactions on Industrial Electronics, vol. 59, Issue 4, pp. 1689 – 1697. April 2012.

[8.10] Alonso, J.M.; Viña, J.; Gacio, D.; Campa, L.; Martinez, G.; Osorio, R.; "Analysis and design of the quadratic buck-boost converter as a high-power-factor driver for power-LED lamps," in Conference Records of the 36th Annual Conference on IEEE Industrial Electronics Society, IECON 2010, pp. 2541 – 2546. Glendale, AZ, USA. 7 – 10 November 2010.

[8.11] Alonso, J.M.; Gacio, D. ; Garcia, J.; Rico-Secades, M.; Dalla Costa, M.A.; "Analysis and design of the integrated double buck-boost converter operating in full DCM for LED lighting applications," in Conference Records of the 37th Annual Conference on IEEE Industrial Electronics Society, IECON 2011, pp. 2889 – 2894. Melbourne, Australia. 7 – 10 November 2011.

[8.12] Alonso, J.M.; Viña, J.; Gacio, D.; Martinez, G.; Osorio, R.; "Doble Reductor-Elevador Integrado para Alimentación de Lámparas LED desde la Red Eléctrica con Alto Factor de Potencia," in Actas del XVIII Seminario Anual de Automática, Electrónica Industrial e Instrumentación 2011, SAAEI'11, pp. 7 – 12. 5 – 8 July 2011.

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[8.19] Garcia, J.; Calleja, A.J.; Corominas, E.L.; Gacio, D.; Campa, L.; Diaz, R.E.; "Integrated driver for power LEDs," in Conference Records of the 35th Annual Conference of IEEE Industrial Electronics, 2009. IECON '09, pp. 2578 – 2583.7-10 November 2010.

[8.20] Garcia, J.; Calleja, A.J.; Corominas, E.L.; Gacio, D.; Campa, L.; Diaz, R. E.; "Integrated Off-Line Ballast for High Brightness LEDs with Dimming Capability," in Circuits and Systems, vol. 2, Issue 4, pp. 338 – 351. October 2011.

Capítulo 8

Conclusiones, principales aportaciones y futuras líneas de desarrollo

Este último capítulo presenta las principales conclusiones obtenidas del trabajo de Tesis Doctoral. A continuación, se detallan las principales aportaciones realizadas para finalmente enumerar las futuras líneas de desarrollo propuestas.

8.1. Conclusiones

Las principales conclusiones que se pueden extraer del presente trabajo de Tesis Doctoral, así como los resultados obtenidos se pueden resumir en los siguientes apartados temáticos:

Con respecto a la investigación de los **diodos LED como carga de potencia**:

- Se han caracterizado cuatro dispositivos de diferentes fabricantes que representan una parte significativa del mercado. Esta caracterización busca modelar térmicamente y estadísticamente los diodos LED para determinar los valores típicos para una determinada configuración a cualquier temperatura.
- La temperatura de la unión se puede determinar con precisión mediante la medida de la tensión directa de la lámpara una vez se ha modelado térmicamente. No obstante, se pueden obtener resultados erráticos si el modelo para una lámpara completa se aplica a diodos LED individuales sin clasificar. En el caso de diodos LED clasificados, se ha comprobado experimentalmente una tolerancia de ±10 ºC. Este extremo se ha verificado experimentalmente mediante termografía infrarroja.
- Se ha verificado experimentalmente la dependencia térmica de los diversos parámetros de los diodos LED. De esta forma, se ha obtenido la variación de la corriente de saturación inversa, del factor de idealidad y de la resistencia serie frente a la temperatura de la unión. Sin embargo, se ha concluido que son necesarios más puntos de medida en la zona de baja corriente para poder realizar un ajuste satisfactorio de la corriente de saturación inversa.
- Se ha comprobado que la variación de tensión directa presenta una característica casi lineal o marcadamente cuadrática con la temperatura, en función de la estructura del dispositivo.
- Se ha demostrado experimentalmente la dependencia de la resistencia dinámica con la temperatura, presentando un comportamiento diferente en función de la estructura del diodo LED.
- Se ha demostrado la influencia de la variación de la temperatura de la unión en el comportamiento en lazo cerrado y en el rizado de corriente del convertidor.
- Se ha estudiado la auto-ecualización de cadenas de diodos LED en paralelo mediante una aproximación estadística para determinar el número mínimo de dispositivos en serie. Se ha concluido que los diodos LED clasificados son más adecuados para este propósito al necesitar un menor número de dispositivos conectados en serie.

Sobre el **convertidor reductor/retroceso para alimentación de lámparas LED**:

- Se ha comprobado teóricamente que el condensador de bus necesario para una topología tipo reductor/elevador es ligeramente menor que para una topología basada en el convertidor reductor para la misma tensión de bus. Por otra parte, se ha obtenido un mapa de armónicos que permite demostrar, junto con resultados experimentales, que un ángulo muerto de 25º permite el cumplimiento de la norma de Clase C con la mayor tensión de bus posible.
- Se ha demostrado experimentalmente que el convertidor reductor/retroceso integrado es válido para la alimentación de lámparas LED con una potencia de 70 W para aplicaciones generales de iluminación exterior y alumbrado público con tensión de entrada de rango universal.

- Se ha obtenido el factor de ganancia de rizado. Este parámetro relaciona la tensión de bus y la corriente de salida, resultando útil para calcular el condensador de bus necesario para un rizado de corriente determinado.
- Se ha determinado que el funcionamiento en MCD completo, es decir, ambos convertidores en MCD, es más ventajoso que en MCD/MCC debido a su menor factor de ganancia de rizado y dinámica de primer orden. Esto conlleva menores requisitos de capacidad de bus y un control más simple.
- Se han considerado tres diferentes configuraciones de lámparas para maximizar el rendimiento del convertidor. La mejor eficiencia se ha obtenido con una única cadena de diodos LED con una corriente de 350 mA.
- El factor de ganancia de rizado se ha erigido como una útil herramienta para estudiar el rizado máximo de bus. De este modo, limitando el rizado de corriente de salida a valores razonables, es posible utilizar condensadores de plástico metalizado para el bus.
- Se ha estudiado el efecto que el rizado de tensión de bus tiene sobre la distorsión de corriente de entrada, concluyendo que valores significativos de rizado mejoran la corrección de factor de potencia.
- Se ha comprobado que el ángulo muerto óptimo se halla en niveles ligeramente inferiores a 25º, puesto que la capacidad de bus necesaria no se ve significativamente elevada mientras que el contenido armónico de la corriente de entrada se reduce.
- Se ha desarrollado un regulador integral para compensar parcialmente el rizado de corriente de salida hasta los límites en los que se cumple la norma de Clase C. De esta forma, se han diseñado dos reguladores específicos para cada nivel de corriente de salida.
- El convertidor propuesto ha mostrado un funcionamiento satisfactorio, con un condensador de bus de únicamente 80 μF (fácilmente disponible mediante condensadores no electrolíticos), un rizado de corriente de salida del 20%, con un regulador suficientemente rápido que permite el cumplimiento de la norma de Clase C en toda condición de uso y un rendimiento máximo en torno al 88%.

Por último, se puede concluir que el estudio de la **regulación de flujo luminoso por modulación de ancho de pulso** ha demostrado que:

- Las técnicas tradicionales de *dimming* PWM, es decir, *dimming* por *Enable*, *dimming* en serie y *dimming* en paralelo no son aplicables a convertidores de dinámica lenta debido a la distorsión introducida en la corriente de red, la oscilación debido a la acción de control y el cortocircuito producido en el condensador de salida.
- Se ha propuesto, estudiado y validad experimentalmente una nueva técnica de *dimming*. En esta técnica, la frecuencia de *dimming* se halla muy por encima de la frecuencia de cruce de ganancia, donde la función de sensibilidad atenúa en gran medida las perturbaciones de corriente de salida. Se ha conseguido una relación de atenuación de hasta 10 a 1.

8.2. Principales aportaciones

La contribución de este trabajo de Tesis Doctoral consiste en el desarrollo de un completo juego de herramientas para el diseño de un convertidor de altas prestaciones, bajo coste y funcionalidad completa basado en el convertidor reductor/retroceso para alimentación de lámparas LED con una potencia aproximada de entre 60 y 70 W. Las citadas herramientas se pueden enumerar en función del campo de estudio y aplicación.

Con respecto al análisis de la lámpara LED, este juego de herramientas incluye una caracterización térmica completa que permite optimizar el diseño del regulador y condensador de bus para limitar el rizado de corriente de salida, y un estudio estadístico para evaluar la auto-ecualización de ramas de diodos LED en paralelo.

En relación al diseño de la etapa de potencia, este juego de herramientas proporciona un mapa de armónicos que ayuda a seleccionar el ángulo muerto más apropiado, un factor de ganancia de rizado que relaciona el rizado de tensión de bus con el rizado de corriente de salida, dos conjuntos de mapas de armónicos de la corriente de entrada en función del ángulo muerto de diseño y en función del condensador y rizado de tensión del bus y un procedimiento de diseño del regulador para compensar parcialmente el rizado de corriente de salida manteniendo la distorsión armónica de la corriente de entrada dentro de los límites impuestos por la norma de Clase C. También se proporciona una técnica de *dimming* PWM aplicable a convertidores de dinámica lenta.

Las principales contribuciones de este trabajo de Tesis Doctoral se detallan a continuación:

- Un método para obtener la resistencia dinámica de pequeña señal y la tensión de codo para un punto de funcionamiento dado. Este método emplea una perturbación senoidal superpuesta al nivel de continua de la corriente de LED, tal y como se planteó en [8.1] y se desarrolló en [8.2], [8.3], y [8.4]. Se ha realizado también un estudio estadístico para determinar la relevancia estadística de los resultados experimentales.
- La evidencia experimental de que la medida de la temperatura de la unión mediante la medida de la tensión directa de la lámpara no se puede aplicar directamente a dispositivos individuales sin clasificar debido al gran error de estimación cometido.
- Se han documentado diferentes comportamientos de la característica de tensión directa y resistencia dinámica frente a la temperatura dependiendo de la estructura interna del LED. También se ha demostrado que dicha dependencia afecta al funcionamiento en lazo cerrado del convertidor en términos de comportamiento dinámico y rizado de corriente de salida [8.2], [8.3], [8.4].
- Un completo sistema de ecuaciones y gráficas, así como un mapa de armónicos, para diseñar una etapa de corrección de factor de potencia basada en un convertidor reductor en MCD atendiendo a la tensión de bus y al contenido armónico de la corriente de entrada [8.5], [8.6], [8.7], [8.8]. Por otra parte, se ha demostrado que el convertidor reductor/retroceso integrado es adecuado para la alimentación de lámparas LED en el rango de 70 W [8.5], [8.6], [8.7].
- El parámetro denominado como factor de ganancia de rizado, que relaciona el rizado de tensión de bus con el rizado de tensión de salida, y que permite determinar el rizado máximo admisible en el bus [8.8], [8.9], [8.11], [8.13], [8.13] para un rizado determinado de corriente de salida si se tienen en cuenta los parámetros del modelo lineal de la lámpara LED: resistencia dinámica y tensión de codo.
- La prueba de que el funcionamiento en MCD completo es más ventajoso que el funcionamiento en MCD/MCC por su menor factor de ganancia de rizado [8.8], [8.9], [8.10], [8.11], [8.13], [8.13], por lo que se obtienen menores valores de capacidad de bus para el mismo rizado manteniendo una dinámica de primer orden.
- Un juego de ecuaciones, gráficos y mapas de armónicos para seleccionar el ángulo muerto teórico óptimo para el mínimo condensador de bus para un rizado de corriente de salida determinado.

- Un procedimiento de diseño para implementar un regulador simple que compense parcialmente el rizado de corriente de salida con incremento en la distorsión de la corriente de entrada limitado para cumplir con los requisitos de la Clase C.
- Las pruebas experimentales de la alta distorsión introducida en la corriente de entrada cuando se realiza *dimming* PWM a las frecuencias habituales en un convertidor integrado de una etapa [8.5], [8.6], [8.7], [8.14], [8.15], [8.16], independientemente de la técnica utilizada.
- Una técnica de dimming PWM a alta frecuencia que elimina las desventajas de los sistemas de dimming PWM más habituales, basada en el estudio de la función de sensibilidad de control. Se ha obtenido una relación de atenuación de 10 a 1 e incluso 20 a 1 para determinadas condiciones de funcionamiento [8.14],[8.15],[8.16]. Se han propuesto dos modos de dimming: uno con corriente de pico prefijada, y otro con corriente de pico ajustable. Esta técnica de dimming se ha registrado en la Oficina Española de Patentes y Marcas, habiendo sido aceptada como patente de invención con examen previo [8.17].
- Se ha propuesto un estudio estadístico para determinar el número mínimo de diodos LED conectados en serie en lámparas con varias cadenas en paralelo para conseguir auto-ecualización pasiva.
- Se ha construido un prototipo completo y completamente operativo de larga vida útil gracias al empleo de condensadores MKP. Se ha alcanzado un rendimiento del 88% con una relación de atenuación de hasta 20 a 1 con un contenido armónico de la corriente de entrada por debajo de los máximos admisibles por la Clase C en cualquier condición de funcionamiento.

8.3. Líneas futuras de desarrollo

A pesar que en este trabajo de Tesis Doctoral se han conseguido todos los objetivos inicialmente marcados con respecto al desarrollo de un convertidor para alimentación de lámparas LED, se podrían considerar diversas líneas de investigación y desarrollo, que se recogen a continuación:

- Un estudio estadístico completo de la dependencia térmica de la resistencia dinámica, tensión directa y tensión de codo de diodos LED con el objetivo de obtener información más precisa sobre los valores típicos y la desviación estándar para un determinado punto de funcionamiento.
- Un análisis térmico de la disposición de los LED en la lámpara para detectar gradientes de temperatura que influyan en la temperatura de la unión y ayuden a una mejor estimación de los parámetros de la lámpara LED.
- Un completo estudio de la auto-ecualización pasiva considerando la función de distribución de probabilidad de la tensión de codo y la resistencia dinámica, con la extensión de este estudio a un amplio rango de temperaturas de funcionamiento.
- Un análisis de la influencia del rizado de corriente de salida en la dispersión de corrientes entre varias cadenas de diodos LED en paralelo.
- Un proceso de envejecimiento de la lámpara LED para determinar la variación de sus parámetros con el tiempo.
- Un estudio de la resistencia serie necesaria para mejorar la auto-ecualización.
- Investigación de reguladores más complejos para compensar parcialmente el rizado de corriente de salida introduciendo menor distorsión armónica en la corriente de entrada.

- Desarrollo de un modelo de pequeña señal promediado a frecuencia de red para determinar el comportamiento dinámico del convertidor frente a variaciones de tensión de red, tal y como se plantea en [8.18] para un convertidor doble reductor/elevador integrado.
- Análisis de diferentes técnicas de regulación útiles para cargas controladas en corriente, tales como el control por corriente máxima y tiempo de apagado, control por tiempo de encendido y corriente mínima, control por corriente de pico a frecuencia constante, control por corriente máxima y corriente mínima nula (o funcionamiento en modo de conducción frontera), con respecto a los requisitos de capacidad de bus y al contenido armónico de la corriente de entrada, tal y como se enuncia en [8.19], [8.20].
- Evaluación de los convertidores con bobina con toma intermedia como correctores de factor de potencia con tensiones de bus en el rango entre 12 V y 48 V con el objetivo de facilitar su integración en sistemas autónomos, microrredes, y sistemas de microgeneración con energías renovables y almacenamiento local de energía.
- Desarrollo del sistema de dimming en serie a alta frecuencia para reducir la frecuencia de dimming a 20 kHz, limitando de esta forma las pérdidas en conmutación.

8.4. Artículos científicos publicados

Los artículos relacionados con el presente trabajo de Tesis Doctoral que se han publicado en revistas nacionales o internacionales contenidas en el SCI-JCR se muestran a continuación:

[8.1] Garcia, J.; Calleja, A.J.; Corominas, E.L.; Gacio, D.; Ribas, J.; "Electronic driver without electrolytic capacitor for dimming High Brightness LEDs," en Conference Records of the 35th Annual Conference of IEEE Industrial Electronics, 2009. IECON '09, pp. 3518-3523. Del 3 al 5 de Noviembre de 2009.

[8.2] Gacio, D.; Alonso, J.M.; Garcia, J.; Perdigao, M.S.; Saraiva, E.; Bisogno, F.E.; "Effects of the junction temperature on the dynamic resistance of white LEDs," en Proceedings of the Twenty-seventh Annual IEEE Applied Power Electronics Conference and Exposition, 2012. APEC 2012, pp. 1708 – 1715. Del 5 al 9 de Febrero de 2012.

[8.3] Gacio, D.; Alonso, J.M.; Garcia, J.; Perdigao, M.S.; Saraiva, E.; Bisogno, F.E.; "Effects of the junction temperature on the dynamic resistance of white LEDs," en IEEE Transactions on Industry Applications, vol. 49, nº 2, pp. 750 – 760. Marzo – Abril 2013.

[8.4] Gacio, D.; Alonso, J.M.; Garcia, J.; Perdigao, M.S.; Saraiva, E.; Bisogno, F.E.; "Efecto de la temperatura de la unión en la resistencia dinámica de diodos LED," en Actas del XIX Seminario Anual de Automática, Electrónica Industrial e Instrumentación 2012, SAAEI'12, pp. 729 – 734. Del 11 al 13 de Julio de 2012.

[8.5] Gacio, D.; Alonso, J.M.; Calleja, A.J.; Garcia, J.; Rico-Secades, M.; "A Universal-Input Single-Stage High-Power-Factor Power Supply for HB-LEDs Based on Integrated Buck–Flyback Converter," en Proceedings of the Twenty-Fourth Annual IEEE Applied Power Electronics Conference and Exposition, 2009. APEC 2009, pp. 570 – 576. Del 15 al 19 de Febrero de 2009.

[8.6] Gacio, D.; Alonso, J.M.; Calleja, A.J.; Garcia, J.; Rico-Secades, M.; "Convertidor universal Buck-Flyback integrado con alto factor de potencia para aplicaciones de iluminación con diodos LED de alta eficiencia," en Actas del XVI Seminario Anual de Automática, Electrónica Industrial e Instrumentación 2009, SAAEI'09. Del 1 al 3 de Julio de 2009.

[8.7] Gacio, D.; Alonso, J.M.; Calleja, A.J.; Garcia, J.; Rico-Secades, M.; "A Universal-Input Single-Stage High-Power-Factor Power Supply for HB-LEDs Based on Integrated Buck–Flyback Converter," en IEEE Transactions on Industrial Electronics, vol. 58, nº 2, pp. 589 – 599. Febrero de 2011

[8.8] Alonso, M.; Gacio, D.; Calleja, A. J.; Sichirollo, F.; Silva, M. F.; Dalla Costa, M. A.; Prado, R. N.; "Reducing Storage Capacitance in Off-Line LED Power Supplies by Using Integrated Converters," en Conference Records of the 47th Industry Applications Conference, 2012, IAS Annual Meeting 2012. Las Vegas, Nevada, USA. Octubre de 2012.

[8.9] Alonso, J.M.; Vina, J.; Vaquero, D.G.; Martinez, G.; Osorio, R.; "Analysis and Design of the Integrated Double Buck–Boost Converter as a High-Power-Factor Driver for Power-LED

Lamps," en IEEE Transactions on Industrial Electronics, vol. 59, nº 4, pp. 1689 – 1697. Abril de 2012.

[8.10] Alonso, J.M.; Viña, J.; Gacio, D.; Campa, L.; Martinez, G.; Osorio, R.; "Analysis and design of the quadratic buck-boost converter as a high-power-factor driver for power-LED lamps," en Conference Records of the 36th Annual Conference on IEEE Industrial Electronics Society, IECON 2010, pp. 2541 – 2546. Glendale, AZ, USA. Del 7 al 10 de Noviembre 2010.

[8.11] Alonso, J.M.; Gacio, D.; Garcia, J.; Rico-Secades, M.; Dalla Costa, M.A.; "Analysis and design of the integrated double buck-boost converter operating in full DCM for LED lighting applications," en Conference Records of the 37th Annual Conference on IEEE Industrial Electronics Society, IECON 2011, pp. 2889 – 2894. Melbourne, Australia. del 7 al 10 de Noviembre de 2011.

[8.12] Alonso, J.M.; Viña, J.; Gacio, D.; Martinez, G.; Osorio, R.; "Doble Reductor-Elevador Integrado para Alimentación de Lámparas LED desde la Red Eléctrica con Alto Factor de Potencia," en Actas del XVIII Seminario Anual de Automática, Electrónica Industrial e Instrumentación 2011, SAAEI'11, pp. 7 – 12. Del 5 al 8 de Julio de 2011.

[8.13] Alonso, J.M.; Calleja, A.J.; Gacio, D.; Cardesin, J.; Lopez, E.; "A long-life high-power-factor HPS-lamp LED retrofit converter based on the integrated buck-boost buck topology," en Conference Records of the 37th Annual Conference on IEEE Industrial Electronics Society, IECON 2011, pp. 2860 – 2865. Melbourne, Australia. Del 7 al 10 de Noviembre de 2011.

[8.14] Gacio, D.; Alonso, J.M.; Garcia, J.; Campa, L.; Crespo, M.; Rico-Secades, M., "High frequency PWM dimming technique for high power factor converters in LED lighting," en Proceedings of the Twenty-Fifth Annual IEEE Applied Power Electronics Conference and Exposition, 2010. APEC 2010, pp. 743 – 749. Del 21 al 25 de Febrero de 2010.

[8.15] Gacio, D.; Alonso, J.M.; Campa, L.; Crespo, M.; Calleja, A. J., "Dimming PWM en serie de alta frecuencia para convertidores de alto factor de potencia en aplicaciones de iluminación LED," en Actas del XVII Seminario Anual de Automática, Electrónica Industrial e Instrumentación 2010, SAAEI'10. Del 7 al 9 de Julio de 2010.

[8.16] Gacio, D.; Alonso, J.M.; Garcia, J.; Campa, L.; Crespo, M.; Rico-Secades, M., "PWM Series Dimming for Slow-Dynamics HPF LED Drivers: the High-Frequency Approach," en IEEE Transactions on Industrial Electronics, vol. 59, nº 4, pp. 1717 – 1727. Abril de 2012.

[8.17] Gacio Vaquero, D.; Alonso Alvarez, J. M.; Campa Monteserín, L.; Crespo Ramos, M.; Rico-Secades, M.; Sistema de dimming PWM en serie a alta frecuencia para aplicación en convertidores de dinámica lenta para lámparas de estado sólido," Patente española de invención con examen previo ES 2 364 308 B2. 13 de Marzo de 2012.

[8.18] Alonso, J.; Gacio Vaquero, D.; Sichirollo, F.; Seidel, A.; Costa, M.; "A Straightforward Methodology to Modeling High Power Factor AC-DC Converters," en IEEE Transactions on Power Electronics, 2012 (En espera para publicación).

[8.19] Garcia, J.; Calleja, A.J.; Corominas, E.L.; Gacio, D.; Campa, L.; Diaz, R.E.; "Integrated driver for power LEDs," en Conference Records of the 35th Annual Conference of IEEE Industrial Electronics, 2009. IECON '09, pp. 2578 – 2583.Del 7 al 10 de Noviembre de 2010.

[8.20] Garcia, J.; Calleja, A.J.; Corominas, E.L.; Gacio, D.; Campa, L.; Diaz, R. E.; "Integrated Off-Line Ballast for High Brightness LEDs with Dimming Capability," en Circuits and Systems, vol. 2, nº 4, pp. 338 – 351. Octubre de 2011.

Appendix A

Additional Experimental Results of the Light-Emitting Diodes Modelling

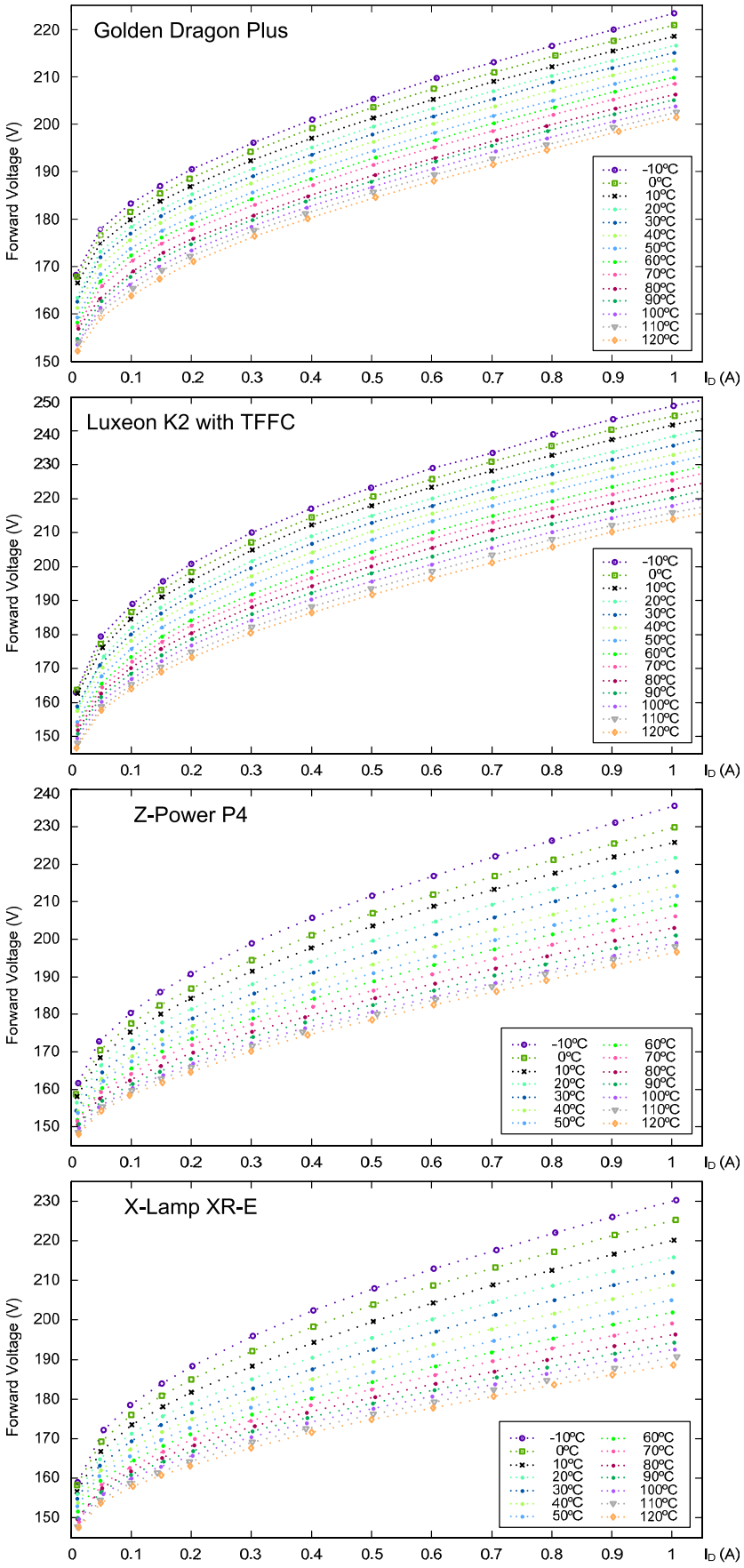

Fig. A.1. *I-V* curves for several junction temperatures.

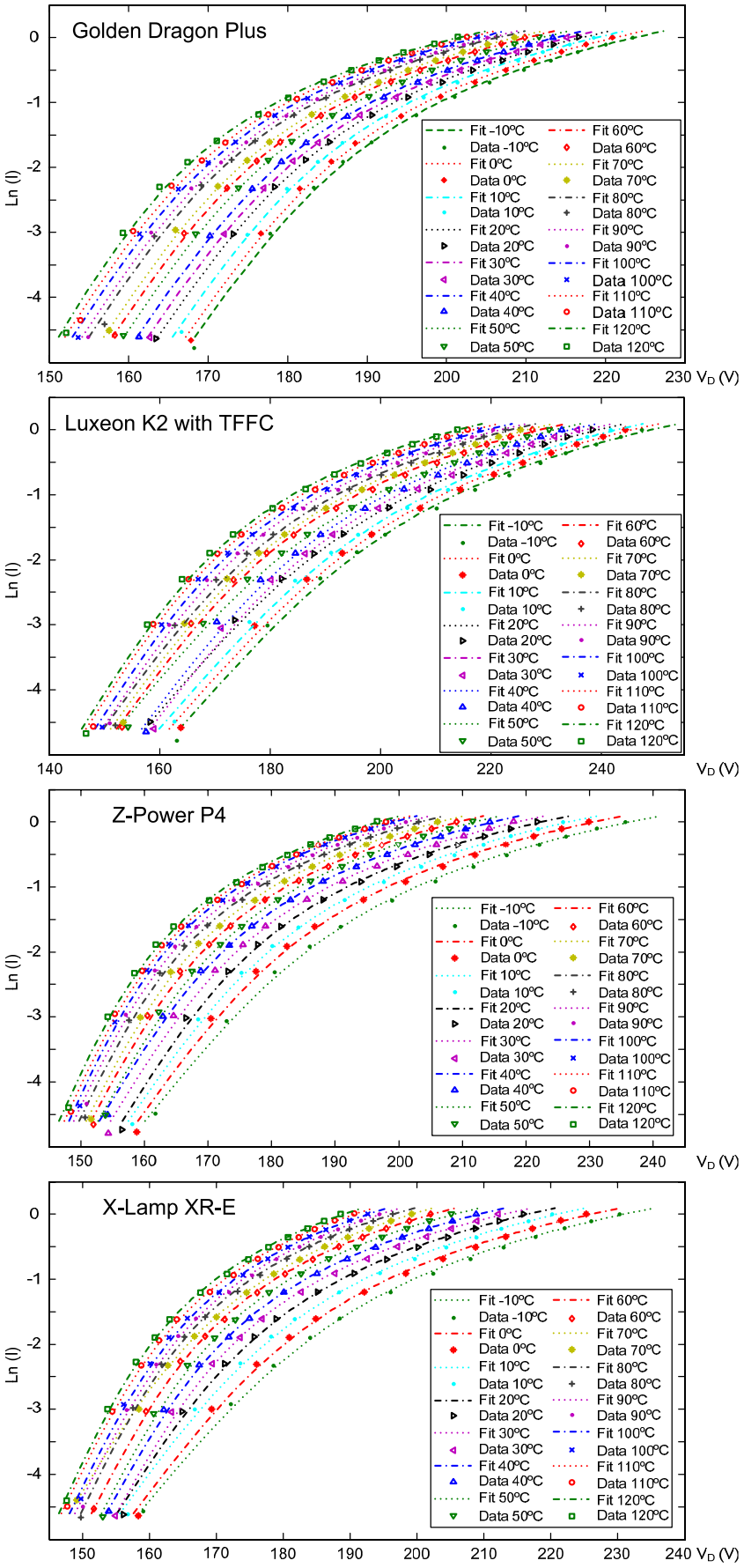

Fig. A.2. *LnI-V* curves for several junction temperatures.

TABLE A.I
AVERAGE TEST TEMPERATURE AND STANDARD DEVIATION. 60-SERIES LEDS LAMP TEST

T_j (ºC)	Golden Dragon		Luxeon K2		Z-Power P4		X-Lamp XR-E	
	T_A (ºC)	σ (ºC)	T_A (ºC)	σ (ºC)	T_A (ºC)	σ (ºC)	T_A (ºC)	σ (ºC)
-10	-10.2	0.12	-11.0	0.10	-11.5	0.05	-10.9	0.14
0	-0.7	0.05	0.0	0.05	0.1	0.05	-0.9	0.05
10	10.5	0.05	9.6	0.08	9.3	0.04	9.6	0.04
20	19.2	0.07	20.6	0.08	20.3	0.05	20.0	0.05
30	29.7	0.07	29.9	0.04	29.2	0.06	29.4	0.04
40	39.0	0.07	39.8	0.06	40.2	0.10	39.8	0.08
50	49.3	0.07	50.3	0.02	50.0	0.07	50.1	0.08
60	59.4	0.08	60.7	0.06	59.2	0.07	60.0	0.08
70	69.9	0.05	70.1	0.08	69.9	0.07	70.1	0.09
80	82.8	0.15	79.9	0.06	83.0	0.11	81.1	0.10
90	90.0	0.10	89.8	0.09	93.2	0.10	90.6	0.05
100	100.3	0.15	100.0	0.05	104.0	0.10	100.0	0.05
110	110.7	0.05	110.0	0.08	110.3	0.13	110.9	0.05
120	120.1	0.07	120.0	0.08	120.6	0.11	121.7	0.05

TABLE A.II
GOLDEN DRAGON PLUS PARAMETERS

T_j (ºC)	Entire Lamp				Average LED			
	I_s (A)	R_s (Ω)	η	r^2	I_s (A)	R_s (Ω)	η	r^2
-10.2	5.815E-16	30.30	244.0	0.9993	6.968E-16	0.502	4.080	0.9993
-0.7	5.190E-16	29.25	232.4	0.9991	3.784E-16	0.490	3.836	0.9991
10.5	6.059E-16	28.73	222.1	0.9994	6.304E-16	0.477	3.707	0.9994
19.2	6.749E-16	28.95	213.8	0.9996	9.154E-16	0.477	3.600	0.9996
29.7	8.481E-16	28.53	206.4	0.9997	6.432E-16	0.478	3.411	0.9997
39.0	9.019E-16	28.38	199.0	0.9997	1.027E-15	0.472	3.331	0.9997
49.3	6.769E-16	28.73	188.8	0.9998	1.282E-15	0.472	3.210	0.9998
59.4	9.005E-16	28.35	183.2	0.9998	1.067E-15	0.471	3.070	0.9998
69.9	7.007E-16	28.36	174.9	0.9997	4.718E-16	0.475	2.880	0.9997
82.8	6.934E-16	28.26	166.5	0.9993	3.553E-16	0.474	2.720	0.9994
90.0	6.472E-16	28.35	161.9	0.9994	6.457E-16	0.471	2.699	0.9994
100.3	6.992E-16	28.18	156.6	0.9994	3.066E-16	0.477	2.545	0.9994
110.7	5.367E-16	28.18	150.1	0.9993	2.609E-16	0.477	2.446	0.9993
120.1	1.472E-16	28.97	139.8	0.9991	3.633E-16	0.477	2.393	0.9990

TABLE A.III
LUXEON K2 WITH TFFC PARAMETERS

T_j (ºC)	Entire Lamp				Average LED			
	I_s (A)	R_s (Ω)	η	r^2	I_s (A)	R_s (Ω)	η	r^2
-11.0	6.748E-10	40.32	437.7	0.9981	5.164E-10	0.671	7.197	0.9881
0.0	7.262E-10	39.02	417.2	0.9981	6.098E-10	0.653	6.890	0.9981
9.6	7.409E-10	38.44	399.0	0.9983	5.801E-10	0.647	6.563	0.9983
20.6	7.263E-10	38.58	377.2	0.9986	9.283E-10	0.636	6.373	0.9987
29.9	8.655E-11	40.20	325.7	0.9977	3.832E-10	0.637	5.853	0.9979
39.8	8.534E-11	39.30	312.1	0.9978	2.255E-10	0.639	5.456	0.9977
50.3	7.614E-10	36.76	333.0	0.9984	5.688E-10	0.625	5.460	0.9985
60.7	8.686E-11	39.45	284.3	0.9984	4.212E-10	0.619	5.138	0.9983
70.1	8.298E-11	38.60	273.9	0.9984	2.755E-10	0.616	4.849	0.9981
79.9	8.716E-11	37.14	264.7	0.9981	3.988E-11	0.644	4.242	0.9983
89.8	9.477E-12	39.47	229.7	0.9986	8.125E-12	0.659	3.803	0.9986
100.0	8.240E-12	38.73	220.0	0.9987	7.537E-12	0.646	3.653	0.9987
110.0	9.562E-12	38.13	213.4	0.9989	9.576E-12	0.636	3.556	0.9990
120.0	8.880E-12	36.39	206.1	0.9989	7.874E-12	0.621	3.412	0.9990

TABLE A.IV
Z-POWER P4 PARAMETERS

T_j (ºC)	Entire Lamp				Average LED			
	I_s (A)	R_s (Ω)	η	r^2	I_s (A)	R_s (Ω)	η	r^2
-11.5	1.089E-11	41.06	343.2	0.9989	1.004E-11	0.686	5.700	0.9989
0.1	1.033E-12	40.40	292.8	0.9987	1.026E-12	0.674	4.879	0.9987
9.3	4.234E-13	39.43	270.1	0.9988	8.509E-13	0.647	4.628	0.9988
20.3	3.589E-14	39.03	234.3	0.9991	3.323E-14	0.652	3.894	0.9991
29.2	2.475E-14	37.74	221.6	0.9992	4.096E-14	0.623	3.759	0.9992
40.2	2.376E-14	35.98	211.1	0.9995	4.251E-14	0.593	3.592	0.9995
50.0	2.327E-15	35.45	188.1	0.9995	3.391E-15	0.587	3.173	0.9995
59.2	8.223E-16	34.95	175.3	0.9995	8.759E-16	0.582	2.927	0.9995
69.9	2.041E-16	33.90	161.5	0.9995	3.356E-16	0.561	2.733	0.9995
83.0	7.450E-17	32.93	149.6	0.9995	6.257E-17	0.550	2.481	0.9995
93.2	3.015E-17	32.26	140.7	0.9993	3.564E-17	0.537	2.357	0.9993
104.0	9.262E-18	31.75	131.4	0.9994	7.242E-18	0.531	2.175	0.9994
110.3	7.298E-18	31.78	127.7	0.9994	9.107E-18	0.528	2.141	0.9994
120.6	6.553E-18	31.17	123.3	0.9993	5.121E-18	0.521	2.041	0.9993

TABLE A.V
X-LAMP XR-E PARAMETERS

T_j (ºC)	Entire Lamp				Average LED			
	I_s (A)	R_s (Ω)	η	r^2	I_s (A)	R_s (Ω)	η	r^2
-10.9	1.100E-11	37.68	338.9	0.9991	6.643E-11	0.590	6.142	0.9990
-0.9	1.106E-12	37.19	292.4	0.9988	1.040E-12	0.621	4.861	0.9987
9.6	6.843E-13	35.18	272.2	0.9988	1.425E-13	0.609	4.270	0.9988
20.0	3.528E-14	34.80	232.3	0.9992	5.436E-14	0.575	4.076	0.9992
29.4	3.111E-16	35.42	190.8	0.9993	3.002E-16	0.591	3.176	0.9993
39.8	4.252E-16	33.16	184.5	0.9997	1.000E-15	0.545	3.157	0.9997
50.1	5.850E-17	31.67	167.1	0.9996	9.999E-17	0.524	2.828	0.9996
60.0	7.383E-17	29.86	161.7	0.9998	1.000E-16	0.495	2.719	0.9998
70.1	3.115E-14	25.78	188.5	0.9999	3.220E-14	0.429	3.146	0.9999
81.1	1.893E-17	26.77	144.4	0.9995	1.001E-17	0.451	2.365	0.9995
90.6	2.806E-17	25.47	141.5	0.9994	1.097E-17	0.431	2.297	0.9994
100.0	3.121E-17	24.51	137.6	0.9994	9.867E-18	0.416	2.220	0.9995
110.9	3.515E-17	23.78	133.1	0.9995	2.967E-17	0.398	2.208	0.9995
121.7	4.752E-18	23.73	121.8	0.9993	1.000E-17	0.391	2.072	0.9993

TABLE A.VI
THEORETICAL DYNAMIC RESISTANCE, R_D, (Ω) AT 350MA AND 700MA

T_j (ºC)	Dragon Plus		Luxeon K2		X-Lamp XR-E		Z-Power P4	
	350 mA	*700 mA*	*350 mA*	*700 mA*	*350 mA*	*700 mA*	*350 mA*	*700 mA*
-10	46.05	38.18	68.57	54.45	63.17	52.11	59.56	48.62
0	44.84	37.04	67.08	53.05	60.10	50.25	56.79	46.99
10	44.24	36.49	66.22	52.33	58.21	48.82	54.13	44.65
20	44.34	36.64	65.86	52.22	55.96	47.49	51.57	43.18
30	43.92	36.23	64.50	52.35	54.24	45.99	49.63	42.53
40	43.67	36.03	63.35	51.32	52.27	44.12	47.38	40.27
50	43.72	36.22	63.28	50.02	50.42	42.93	44.97	38.32
60	43.35	35.85	62.82	51.13	49.29	42.12	43.12	36.49
70	43.13	35.75	61.75	50.17	47.54	40.72	41.71	33.75
80	42.85	35.56	60.15	48.64	46.05	39.49	39.36	33.07
90	42.83	35.59	60.00	49.73	44.95	38.61	38.14	31.81
100	42.58	35.38	58.94	48.84	43.95	37.85	37.15	30.83
110	42.37	35.27	58.26	48.20	43.84	37.81	36.37	30.07
120	42.51	35.74	56.34	46.37	43.12	37.15	35.57	29.65

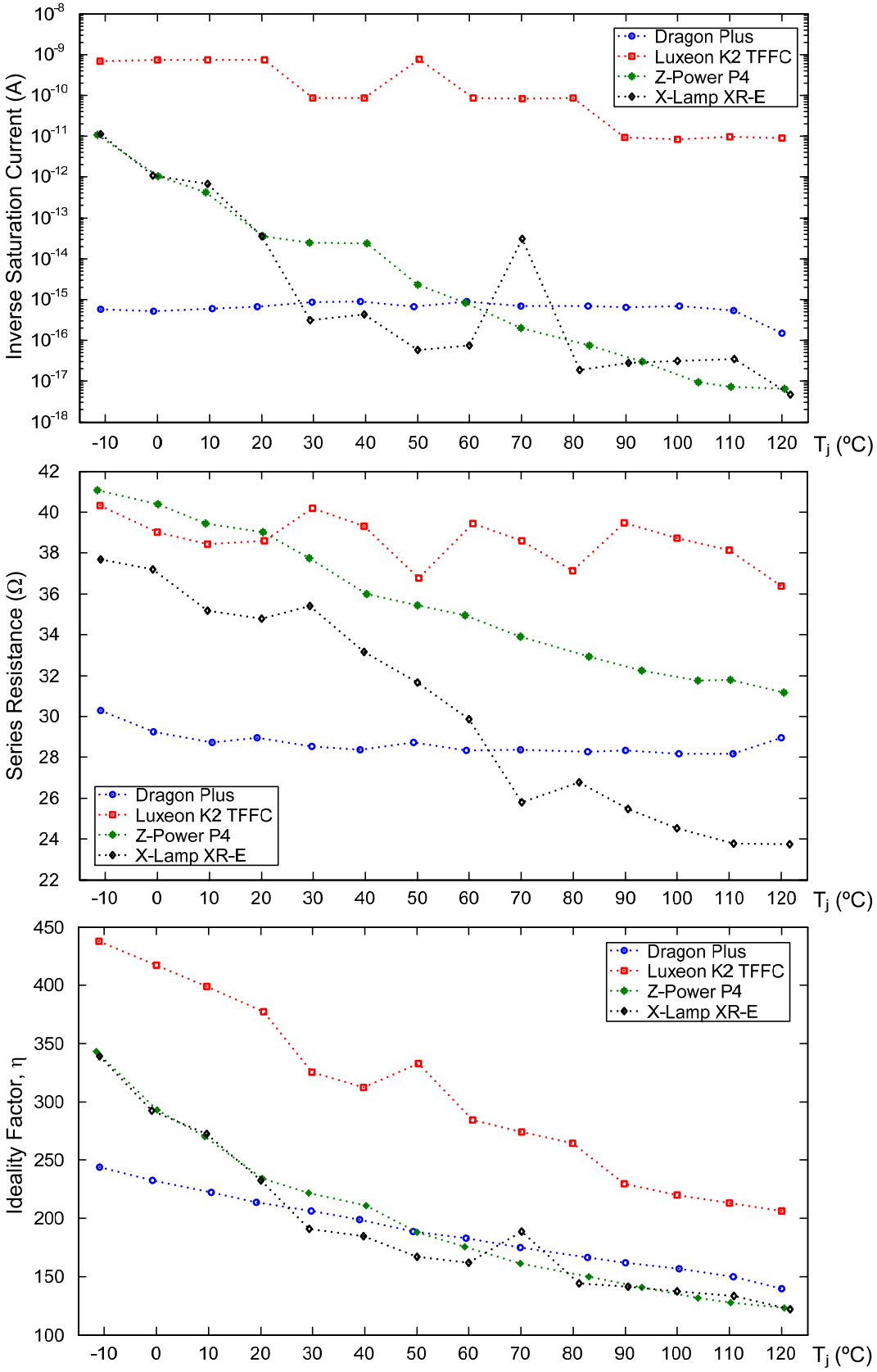

Fig. A.3. LED parameters extracted from the experimental results.

TABLE A.VII
GOLDEN DRAGON PLUS PARAMETERS, REDUCED DATA SET

T_j (ºC)	Entire Lamp				Average LED			
	I_s (A)	R_s (Ω)	η	r^2	I_s (A)	R_s (Ω)	η	r^2
-10.2	5.778E-14	28.11	282.9	0.9997	2.959E-14	0.475	4.606	0.9997
-0.7	5.864E-14	27.08	271.2	0.9995	2.977E-14	0.454	4.504	0.9995
10.5	5.949E-14	26.51	258.2	0.9996	2.996E-14	0.449	4.201	0.9996
19.2	4.515E-14	26.68	245.6	0.9996	3.010E-14	0.448	4.036	0.9997
29.7	5.920E-14	26.38	237.6	0.9996	3.024E-14	0.445	3.868	0.9997
39.0	3.334E-14	26.64	224.0	0.9998	3.037E-14	0.443	3.723	0.9998
49.3	4.429E-14	26.58	216.6	0.9999	3.051E-14	0.444	3.565	0.9999
59.4	3.025E-14	26.64	205.6	0.9999	3.080E-14	0.444	3.428	0.9999
69.9	6.309E-14	26.24	202.8	0.9999	3.125E-14	0.444	3.298	0.9999
82.8	6.494E-14	26.34	193.2	0.9999	6.741E-14	0.439	3.225	0.9999
90.0	6.758E-14	26.22	188.7	0.9999	6.834E-14	0.437	3.146	0.9999
100.3	6.853E-14	26.25	182.1	0.9999	7.016E-14	0.437	3.037	0.9999
110.7	7.050E-14	26.10	176.1	0.9999	7.254E-14	0.435	2.938	0.9999
120.1	5.923E-14	26.53	169.4	0.9997	7.559E-14	0.441	2.848	0.9997

TABLE A.VIII
LUXEON K2 WITH TFFC PARAMETERS, REDUCED DATA SET

T_j (ºC)	Entire Lamp				Average LED			
	I_s (A)	R_s (Ω)	η	r^2	I_s (A)	R_s (Ω)	η	r^2
-11.0	4.703E-8	32.46	565.4	0.9994	4.703E-8	0.541	9.423	0.9994
0.0	3.712E-8	32.47	527.4	0.9996	3.712E-8	0.541	8.790	0.9996
9.6	3.539E-8	32.11	502.2	0.9995	3.539E-8	0.535	8.370	0.9995
20.6	4.631E-8	31.30	484.9	0.9996	4.631E-8	0.522	8.082	0.9996
29.9	2.374E-8	31.89	445.7	0.9994	2.375E-8	0.531	7.428	0.9994
39.8	2.182E-8	31.52	424.5	0.9995	2.182E-8	0.525	7.075	0.9995
50.3	1.918E-8	32.36	401.5	0.9994	1.918E-8	0.539	6.693	0.9994
60.7	1.187E-8	32.88	371.9	0.9995	1.107E-8	0.550	6.171	0.9995
70.1	6.999E-9	33.26	347.1	0.9995	7.276E-9	0.553	5.799	0.9995
79.9	6.530E-9	32.61	332.6	0.9994	6.680E-9	0.543	5.551	0.9994
89.8	8.248E-10	34.73	284.9	0.9994	8.058E-10	0.579	4.742	0.9994
100.0	8.464E-10	34.33	274.6	0.9995	8.227E-10	0.573	4.569	0.9995
110.0	8.402E-10	33.67	264.6	0.9996	8.228E-10	0.562	4.406	0.9996
120.0	9.049E-11	35.70	228.2	0.9996	9.009E-11	0.595	3.803	0.9996

TABLE A.IX
Z-POWER P4 PARAMETERS, REDUCED DATA SET

T_j (ºC)	Entire Lamp				Average LED			
	I_s (A)	R_s (Ω)	η	r^2	I_s (A)	R_s (Ω)	η	r^2
-11.5	8.086E-10	36.35	422.5	0.9994	7.446e-010	0.608	7.011	0.9994
0.1	6.320E-11	37.06	349.4	0.9994	9.998e-011	0.611	5.952	0.9994
9.3	4.803E-11	35.80	329.4	0.9994	6.064e-011	0.593	5.551	0.9994
20.3	1.011E-11	35.38	291.5	0.9996	9.971e-012	0.590	4.856	0.9996
29.2	8.161E-12	34.16	276.6	0.9998	7.120e-012	0.571	4.583	0.9998
40.2	1.426E-12	33.70	245.5	0.9998	9.695e-013	0.566	4.030	0.9998
50.0	8.303E-13	32.43	231.2	0.9999	6.934e-013	0.543	3.827	0.9999
59.2	1.403E-13	32.63	208.1	0.9999	6.145e-014	0.551	3.367	0.9999
69.9	3.534E-14	31.80	190.4	0.9998	3.649e-014	0.530	3.178	0.9998
83.0	2.551E-14	30.64	179.6	0.9998	2.320e-014	0.511	2.984	0.9998
93.2	3.270E-14	29.57	174.8	0.9998	2.439e-014	0.495	2.884	0.9998
104.0	2.273E-15	29.92	154.3	0.9997	2.854e-015	0.497	2.590	0.9997
110.3	3.067E-15	29.73	152.4	0.9996	3.105e-015	0.495	2.541	0.9996
120.6	2.834E-15	29.19	147.2	0.9996	2.608e-015	0.487	2.446	0.9996

TABLE A.X
X-LAMP XR-E PARAMETERS, REDUCED DATA SET

T_j (ºC)	Entire Lamp				Average LED			
	I_s (A)	R_s (Ω)	η	r^2	I_s (A)	R_s (Ω)	η	r^2
-10.9	4.001E-10	33.95	401.9	0.9996	8.675E-10	0.549	6.978	0.9996
-0.9	1.001E-10	33.49	355.7	0.9994	9.998E-11	0.558	5.928	0.9994
9.6	3.296E-11	32.49	320.0	0.9995	4.575E-11	0.536	5.415	0.9995
20.0	1.036E-12	33.07	263.0	0.9997	4.479E-12	0.534	4.652	0.9997
29.4	2.050E-13	32.14	236.9	0.9998	4.293E-13	0.528	4.060	0.9998
39.8	5.016E-14	30.94	215.5	0.9999	4.617E-14	0.517	3.582	0.9999
50.1	6.944E-15	29.79	193.3	0.9999	6.256E-15	0.499	3.211	0.9999
60.0	3.382E-15	28.30	181.7	0.9999	3.386E-15	0.472	3.028	0.9999
70.1	3.894E-15	26.76	175.8	0.9999	7.385E-15	0.441	2.993	0.9999
81.1	4.143E-15	24.81	169.6	0.9999	6.109E-15	0.410	2.863	0.9999
90.6	4.210E-15	23.74	164.4	0.9997	2.779E-15	0.399	2.704	0.9997
100.0	1.160E-15	23.44	152.9	0.9997	1.715E-15	0.388	2.580	0.9997
110.9	4.666E-15	21.99	154.3	0.9996	1.849E-15	0.373	2.496	0.9996
121.7	1.048E-15	21.93	142.2	0.9996	1.839E-15	0.362	2.412	0.9995

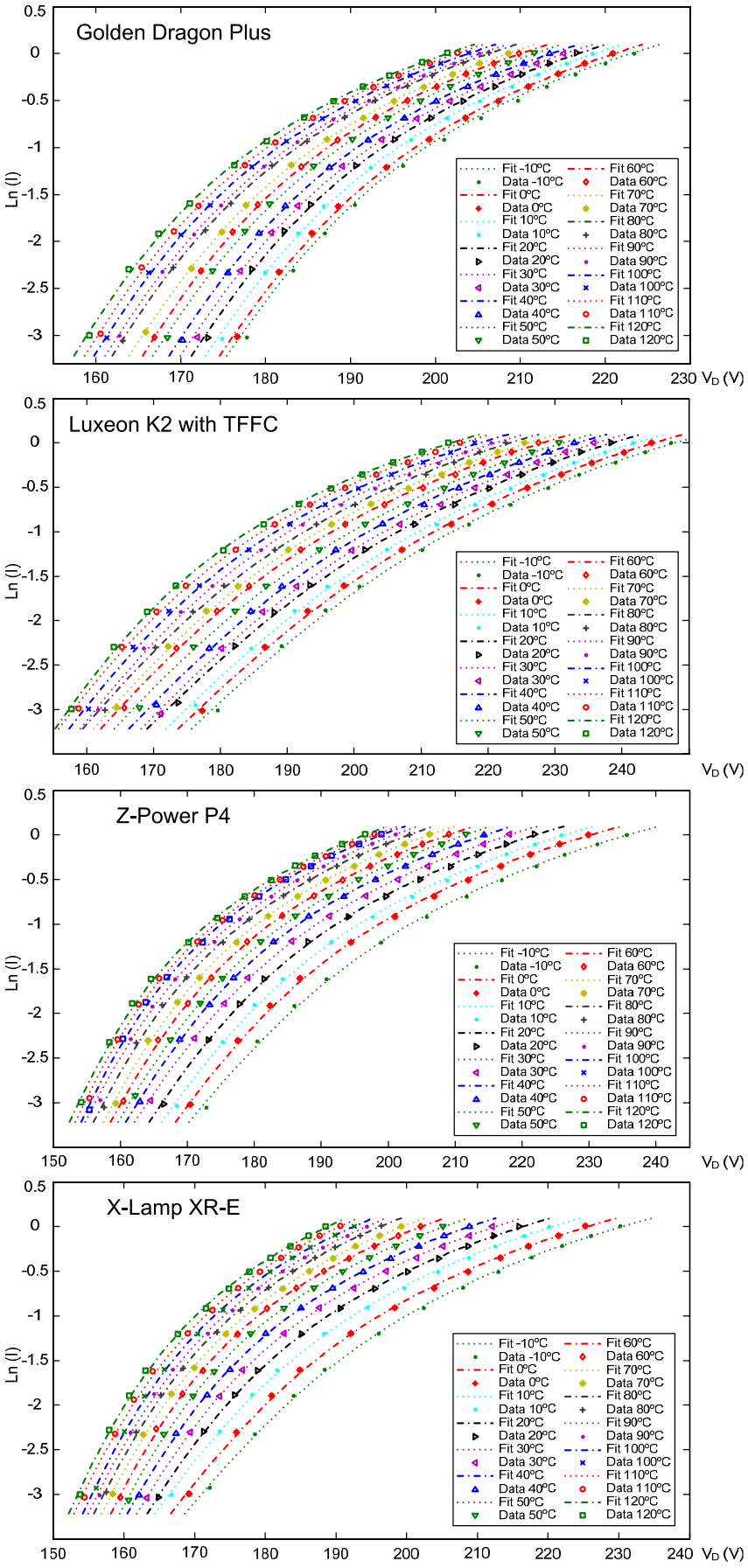

Fig. A.4. *LnI-V* curves for several junction temperatures, reduced data set.

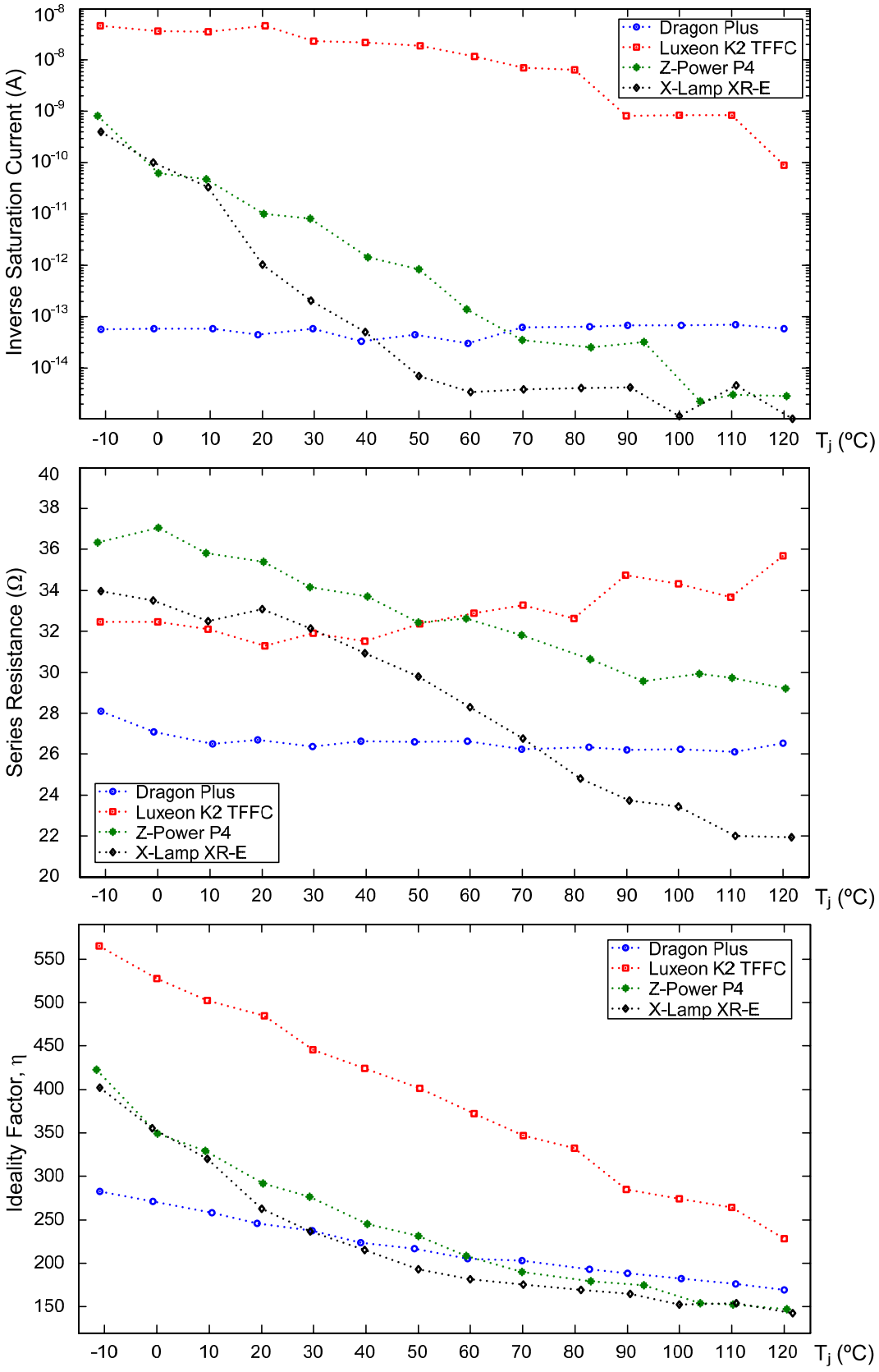

Fig. A.5. LED parameters extracted from the experimental results, reduced data set.

TABLE A.XI
THEORETICAL DYNAMIC RESISTANCE, R_D, (Ω) AT 350MA AND 700MA, REDUCED DATA SET

T_j (ºC)	Dragon Plus		Luxeon K2		X-Lamp XR-E		Z-Power P4	
	350 mA	*700 mA*	*350 mA*	*700 mA*	*350 mA*	*700 mA*	*350 mA*	*700 mA*
-10	46.38	37.24	68.95	50.71	63.57	49.96	59.90	46.93
0	45.27	36.18	67.94	50.20	60.57	48.81	57.33	45.41
10	44.54	35.53	67.07	49.59	58.71	47.25	54.77	43.63
20	44.36	35.52	66.37	48.84	56.44	45.91	52.05	42.56
30	44.10	35.24	65.15	48.52	54.75	44.46	49.79	40.96
40	43.86	35.25	64.23	47.87	52.64	43.17	47.54	39.24
50	43.78	35.18	64.33	48.35	50.82	41.63	45.17	37.48
60	43.47	35.06	63.45	48.16	49.66	41.14	43.20	35.75
70	43.37	34.80	62.59	47.93	47.88	39.84	41.62	34.19
80	43.27	34.81	61.52	47.07	46.39	38.51	39.60	32.21
90	43.09	34.66	60.19	47.46	45.34	37.45	38.46	31.10
100	42.99	34.62	59.56	46.94	44.25	37.08	37.49	30.46
110	42.74	34.42	58.63	46.15	44.12	36.92	36.58	29.29
120	42.93	34.73	57.79	46.74	43.46	36.33	35.75	28.84

TABLE A.XII
DRAGON PLUS V_D-T_J DEPENDENCE (POLYNOMIAL FIT)

I_D (mA)	$V_D=a\cdot T_j^2+b\cdot T_j+c$ (V)			r^2
	a (x10^{-6})	*b (x10^{-3})*	*c*	
100	2.301	–2.726	2.996	0.9989
200	3.825	–3.020	3.106	0.9989
300	3.450	–3.015	3.187	0.9988
350	4.082	–3.107	3.225	0.9993
400	4.544	–3.121	3.257	0.9998
500	3.974	–3.086	3.322	0.9994
600	3.980	–3.035	3.379	0.9992
700	4.584	–3.073	3.435	0.9991
800	5.185	–3.132	3.488	0.9980
900	6.309	–3.184	3.538	0.9992
1000	6.155	–3.248	3.591	0.9981

TABLE A.XIII
Z-POWER P4 V_D-T_J DEPENDENCE (POLYNOMIAL FIT)

I_D (mA)	$V_D=a\cdot T_j^2+b\cdot T_j+c$ (V)			r^2
	a (x10^{-5})	*b (x10^{-3})*	*c*	
100	1.041	–3.864	3.015	0.9985
200	1.252	–4.640	3.200	0.9990
300	1.579	–5.340	3.341	0.9986
350	1.696	–5.595	3.403	0.9986
400	1.916	–6.037	3.468	0.9985
500	2.014	–6.377	3.576	0.9967
600	2.244	–6.851	3.680	0.9989
700	2.310	–7.150	3.777	0.9989
800	2.447	–7.525	3.871	0.9993
900	2.492	–7.835	3.964	0.9991
1000	2.468	–8.075	4.057	0.9991

TABLE A.XIV
LUXEON K2 VD-TJ DEPENDENCE (POLYNOMIAL FIT)

I_D (mA)	$V_D=a\cdot T_j^2+b\cdot T_j+c$ (V)			r^2
	a (x10^{-6})	*b (x10^{-3})*	*c*	
100	4.021	–3.766	3.216	0.9986
200	4.694	–4.014	3.380	0.9987
300	4.101	–4.098	3.505	0.9990
350	4.855	–4.269	3.560	0.9988
400	4.102	–4.266	3.643	0.9991
500	3.456	–4.285	3.703	0.9990
600	4.898	–4.552	3.794	0.9986
700	2.608	-4.355	3.864	0.9993
800	4.359	–4.556	3.938	0.9985
900	3.254	–4.598	4.018	0.9992
1000	3.086	–4.643	4.089	0.9982

TABLE A.XV
X-LAMP XR-E VD-TJ DEPENDENCE (POLYNOMIAL FIT)

I_D (mA)	$V_D=a\cdot T_j^2+b\cdot T_j+c$ (V)			r^2
	a (x10^{-5})	*b (x10^{-3})*	*c*	
100	1.360	–3.838	2.914	0.9959
200	2.088	–5.399	3.076	0.9964
300	2.615	–6.640	3.213	0.9971
350	2.770	–7.082	3.274	0.9980
400	2.866	–7.445	3.331	0.9986
500	2.966	–8.070	3.440	0.9986
600	3.116	–8.613	3.524	0.9992
700	3.180	–9.021	3.623	0.9996
800	2.966	–9.120	3.705	0.9997
900	2.926	–9.365	3.785	0.9990
1000	2.814	–9.539	3.864	0.9993

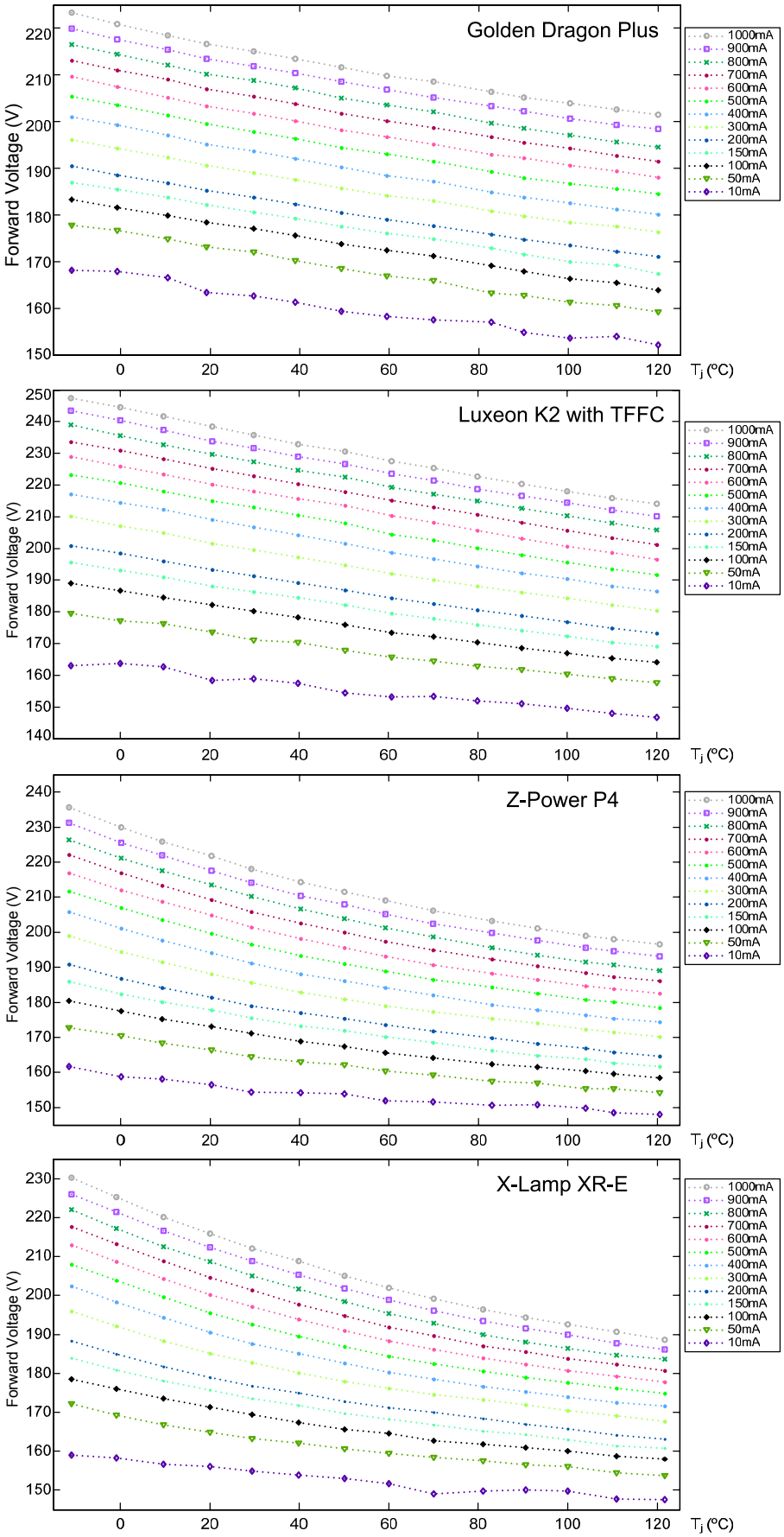

Fig. A.6. V_D-T_j curves for several forward currents, as obtained from the reduced data set *I-V* fits.

TABLE A.XVI
LAMP FORWARD VOLTAGE (V) AT 350MA AND 700MA (THEORETICAL), 60-LEDS LAMPS

T_j (ºC)	Dragon Plus		Luxeon K2			Z-Power P4		X-Lamp XR-E	
	350 mA	*700 mA*	*350 mA*	*700 mA*	*1000 mA*	*350 mA*	*700 mA*	*350 mA*	*700 mA*
-10	198.51	212.79	213.46	233.67	247.97	202.16	221.49	198.89	217.07
0	196.79	210.68	210.73	230.70	244.86	197.55	216.22	195.10	212.61
10	194.85	208.50	208.33	228.05	242.05	194.60	212.69	191.37	208.15
20	192.97	206.60	205.36	224.82	238.59	191.27	208.76	187.94	204.12
30	191.59	205.12	203.28	222.51	236.23	188.39	205.34	185.21	200.74
40	189.98	203.48	200.96	219.93	233.47	185.65	202.04	182.70	197.56
50	188.04	201.52	198.43	217.52	231.22	183.68	199.50	180.31	194.47
60	186.55	199.96	195.53	214.45	228.13	181.55	197.10	178.24	191.76
70	185.11	198.45	193.65	212.41	226.05	179.56	194.59	176.44	189.41
80	182.95	196.27	191.50	209.93	223.32	177.46	192.01	174.71	186.98
90	182.05	195.33	189.18	207.51	221.11	175.91	190.08	173.48	185.36
100	180.67	193.92	187.20	205.34	218.79	174.30	188.24	172.13	183.74
110	179.42	192.59	185.18	203.02	216.24	173.41	187.30	170.84	182.08
120	178.10	191.37	183.17	201.02	214.49	172.28	185.96	169.48	180.51

TABLE A.XVII
V_D-T_J CURVE AT 350MA, 60-LEDS LAMPS, POLYNOMIAL FIT

LED	$V_D=a\cdot T_j^2+b\cdot T_j+c$ (V)			r^2
	a (V/ºC^2)	*b* (V/ºC)	*c* (V)	
Golden Dragon Plus	2.372E-4	-0.1825	196.6	0.9996
Luxeon K2 with TFFC	2.496E-4	-0.2601	210.7	0.9998
Z-Power P4	1.061E-3	-0.3364	197.7	0.9993
X-Lamp XR-E	1.150E-3	-0.3427	194.7	0.9991

TABLE A.XVIII
V_D-T_J CURVE AT 700MA, 60-LEDS LAMPS, POLYNOMIAL FIT

LED	$V_D=a\cdot T_j^2+b\cdot T_j+c$ (V)			r^2
	a (V/ºC^2)	*b* (V/ºC)	*c* (V)	
Golden Dragon Plus	3.078E-4	-0.1965	210.5	0.9997
Luxeon K2 with TFFC	2.684E-4	-0.2800	230.6	0.9999
Z-Power P4	1.253E-3	-0.4012	216.4	0.9997
X-Lamp XR-E	1.327E-3	-0.4187	212.1	0.9998

TABLE A.XIX
GOLDEN DRAGON PLUS AND LUXEON K2 V_D-T_J LINEAR FIT AT 350 AND 700MA, 60-LEDS LAMPS

LED	$V_D= a\cdot T_j+b$ (V)		r^2
	a (x10^{-4}) (V/ºC)	*b* (V)	
Golden Dragon Plus (350 mA)	-0.1565	196.3	0.9967
Golden Dragon Plus (700 mA)	-0.1627	210.1	0.9952
Luxeon K2 with TFFC (350 mA)	-0.2328	210.4	0.9983
Luxeon K2 with TFFC (700 mA)	-0.2506	230.3	0.9984

TABLE A.XX
GOLDEN DRAGON PLUS DYNAMIC RESISTANCE AT 350 MA, 1 KHZ VS. JUNCTION TEMPERATURE AND RIPPLE

Current Ripple							
10%		***20%***		***30%***		***40%***	
T_j (ºC)	R_D (Ω)	T_j (ºC)	R_D (Ω)	T_j (ºC)	R_D (Ω)	T_j (ºC)	R_D (Ω)
7.4	43.13	7.9	43.46	8.3	43.69	7.6	43.68
15.9	43.15	17.2	43.43	16.4	43.51	15.9	43.82
24.8	43.27	24.7	43.57	24.9	43.66	24.5	43.80
35.2	43.12	35.1	43.57	34.7	43.60	34.1	43.83
48.5	43.49	48.1	43.64	47.6	43.77	47.7	44.04
52.9	43.49	53.8	43.91	53.9	43.97	54.4	44.07
63.2	43.57	63.6	44.03	62.3	44.13	62.2	44.12
72.3	43.47	72.8	43.93	72.4	44.09	73.4	44.18
82.2	43.59	82.6	44.29	83.4	44.28	83.7	44.37
90.3	43.73	91.4	44.23	91.2	44.35	90.6	44.53
96.8	44.03	98.0	44.59	97.2	44.32	97.3	44.52
107.4	44.32	106.5	44.65	106.6	44.74	107.5	44.93
112.3	45.24	111.6	45.90	112.3	46.01	113.8	45.71
116.4	45.75	116.4	46.26	117.6	45.70	119.0	45.94

TABLE A.XXI
LUXEON K2 DYNAMIC RESISTANCE AT 350 MA, 1 KHZ VS. JUNCTION TEMPERATURE AND RIPPLE

Current Ripple							
10%		***20%***		***30%***		***40%***	
T_j (ºC)	R_D (Ω)	T_j (ºC)	R_D (Ω)	T_j (ºC)	R_D (Ω)	T_j (ºC)	R_D (Ω)
0.7	63.46	0.5	64.42	1.1	64.62	1.5	64.95
9.9	62.62	9.1	63.87	8.7	64.11	9.3	64.30
18.7	62.26	18.3	63.08	17.9	63.06	17.6	63.45
28.1	61.27	27.4	62.31	27.2	62.33	29.0	62.44
41.0	61.30	40.9	62.18	40.9	62.52	40.7	62.66
47.1	60.51	47.1	61.35	47.2	61.66	47.6	61.90
56.8	59.72	56.6	60.21	57.2	60.68	57.4	61.00
67.7	59.43	67.8	59.60	67.9	59.82	67.7	60.11
79.2	57.36	79.1	58.08	79.8	57.95	80.2	58.37
89.8	56.67	89.5	56.89	90.2	57.16	89.5	57.46
98.6	54.89	99.6	55.44	100.3	55.63	99.8	55.96
109.6	54.69	110.9	54.78	112.1	54.64	112.3	54.75
118.9	53.46	119.0	53.88	120.5	53.47	120.3	53.74

TABLE A.XXII
Z-POWER P4 DYNAMIC RESISTANCE AT 350 MA, 1 KHZ VS. JUNCTION TEMPERATURE AND RIPPLE

Current Ripple							
10%		***20%***		***30%***		***40%***	
T_j (ºC)	R_D (Ω)	T_j (ºC)	R_D (Ω)	T_j (ºC)	R_D (Ω)	T_j (ºC)	R_D (Ω)
1.7	60.17	1.9	60.64	1.6	60.78	2.8	60.83
9.8	58.16	10.6	58.88	10.1	58.55	9.8	59.14
18.9	56.18	19.2	56.95	18.8	56.50	19.5	57.21
27.0	54.53	28.0	54.87	28.4	54.97	26.5	55.54
38.6	52.55	39.0	52.73	39.0	52.66	38.5	52.82
45.3	50.95	44.8	51.57	45.4	51.62	45.3	51.83
54.1	49.54	54.0	50.05	53.2	50.47	53.9	50.53
60.7	48.82	60.6	49.37	61.1	49.27	61.1	49.41
72.1	47.26	71.4	48.06	70.4	48.01	70.7	48.43
78.1	46.57	77.4	47.33	77.6	47.18	77.6	47.60
85.0	46.22	85.5	46.69	86.7	46.60	87.4	46.80
101.4	45.25	101.5	45.64	99.7	45.71	102.0	45.80
107.1	45.03	109.5	45.30	110.2	44.98	112.2	45.23
119.8	44.44	120.8	44.53	119.9	44.64	117.9	45.01

TABLE A.XXIII
X-LAMP XR-E DYNAMIC RESISTANCE AT 350 MA, 1 KHZ VS. JUNCTION TEMPERATURE AND RIPPLE

Current Ripple							
10%		***20%***		***30%***		***40%***	
T_j (ºC)	R_D (Ω)	T_j (ºC)	R_D (Ω)	T_j (ºC)	R_D (Ω)	T_j (ºC)	R_D (Ω)
-4.4	56.58	-4.7	57.11	-4.4	56.98	-5.0	57.39
2.8	54.89	4.1	55.41	4.7	55.26	3.8	55.90
12.2	52.54	13.1	53.21	11.9	53.43	12.3	53.79
22.1	50.44	22.1	51.09	21.3	51.24	21.6	51.32
33.2	47.69	33.7	48.08	33.3	48.31	33.5	48.51
41.2	45.83	41.1	46.33	41.6	46.47	40.9	46.74
48.2	44.42	48.0	44.74	48.2	44.54	49.0	44.75
59.2	42.21	58.5	42.36	57.8	42.36	58.3	42.73
65.5	40.78	65.8	41.03	65.1	41.19	65.2	41.43
73.2	39.41	73.0	39.83	73.4	39.76	73.6	40.03
81.1	38.36	80.4	38.94	80.1	38.74	80.7	39.01
89.6	37.44	90.3	37.88	90.0	37.96	89.5	38.04
97.9	36.91	98.1	37.19	100.7	36.89	101.2	37.21
109.5	36.46	109.3	36.58	111.5	36.53	111.2	36.66
117.9	35.95	121.1	36.12	116.1	36.24	117.6	36.40

TABLE A.XXIV
GOLDEN DRAGON PLUS DYNAMIC RESISTANCE AT 700 MA, 1 KHZ VS. JUNCTION TEMPERATURE AND RIPPLE

Current Ripple							
10%		***20%***		***30%***		***40%***	
T_j (ºC)	R_D (Ω)	T_j (ºC)	R_D (Ω)	T_j (ºC)	R_D (Ω)	T_j (ºC)	R_D (Ω)
48.1	32.33	48.4	32.46	48.4	32.44	48.6	32.64
57.5	32.55	56.6	32.68	56.5	32.57	56.9	32.77
65.2	32.55	65.1	32.73	63.7	32.70	65.5	32.85
72.9	32.92	72.7	32.91	72.7	32.91	70.8	33.05
82.8	33.21	83.5	33.12	83.0	33.10	83.1	33.19
89.8	33.01	90.2	33.20	90.5	33.18	90.2	33.23
96.1	33.07	96.7	33.24	96.8	33.25	97.9	33.46
104.2	33.44	104.4	33.52	105.2	33.53	105.7	33.66
111.5	33.75	111.2	33.78	111.7	33.78	111.8	33.89
117.2	33.86	117.7	34.06	117.6	34.01	118.0	34.06

TABLE A.XXV
LUXEON K2 DYNAMIC RESISTANCE AT 700 MA, 1 KHZ VS. JUNCTION TEMPERATURE AND RIPPLE

Current Ripple							
10%		***20%***		***30%***		***40%***	
T_j (ºC)	R_D (Ω)	T_j (ºC)	R_D (Ω)	T_j (ºC)	R_D (Ω)	T_j (ºC)	R_D (Ω)
19.4	44.51	20.8	44.51	21.3	44.65	21.4	44.77
30.4	43.8	30.0	44.10	31.7	44.36	30.8	44.55
42.7	43.86	41.7	43.97	41.9	43.82	41.1	44.06
52.2	43.34	52.6	43.54	51.3	43.61	52.4	43.63
66.6	43.25	67.3	43.26	66.6	43.45	67.0	43.59
72.5	43.05	72.8	43.16	72.4	43.27	72.5	43.32
83.8	42.52	84.2	42.68	84.2	42.80	84.6	42.96
94.5	42.17	95.1	42.09	95.5	42.19	95.8	42.38
107.8	41.27	107.7	41.50	107.6	41.36	107.5	41.56
119.2	40.37	119.6	40.53	119.5	40.54	119.8	40.75

TABLE A.XXVI
Z-POWER P4 DYNAMIC RESISTANCE AT 700 MA, 1 KHZ VS. JUNCTION TEMPERATURE AND RIPPLE

Current Ripple							
10%		***20%***		***30%***		***40%***	
T_j (ºC)	R_D (Ω)	T_j (ºC)	R_D (Ω)	T_j (ºC)	R_D (Ω)	T_j (ºC)	R_D (Ω)
29.4	41.98	30.8	41.96	30.8	42.07	31.2	42.12
38.0	41.03	37.8	41.13	37.8	40.98	38.7	41.05
46.6	40.24	45.8	40.20	46.6	40.02	46.7	40.24
53.5	39.25	53.9	39.16	54.6	39.12	54.2	39.23
66.1	38.16	66.0	38.08	66.6	38.16	66.4	38.32
70.5	37.99	73.0	37.78	70.9	37.98	71.4	37.89
79.8	37.19	79.3	37.29	80.0	37.38	80.0	37.43
88.0	36.91	89.0	36.99	89.3	36.80	89.1	36.95
98.1	36.45	99.1	36.35	99.0	36.53	99.9	36.60
106.8	36.22	108.3	36.35	109.1	36.25	110.9	36.25
118.3	35.96	121.1	36.05	123.9	35.89	125.0	36.08

TABLE A.XXVII
X-LAMP XR-E DYNAMIC RESISTANCE AT 700 MA, 1 KHZ VS. JUNCTION TEMPERATURE AND RIPPLE

Current Ripple							
10%		***20%***		***30%***		***40%***	
T_j (ºC)	R_D (Ω)	T_j (ºC)	R_D (Ω)	T_j (ºC)	R_D (Ω)	T_j (ºC)	R_D (Ω)
18.1	39.36	17.3	39.52	17.9	39.49	18.1	39.58
26.2	38.26	26.9	38.28	23.7	38.20	27.1	38.34
35.0	36.92	34.6	37.04	36.5	36.77	36.1	37.04
44.0	35.68	43.5	35.72	44.7	35.60	45.1	35.52
56.2	33.92	56.0	33.95	56.2	34.03	56.5	33.97
62.4	33.11	62.7	33.24	63.0	33.19	62.9	33.25
72.0	32.04	71.5	32.08	71.7	32.21	71.7	32.20
78.5	31.26	79.6	31.30	79.7	31.27	79.7	31.21
87.4	30.46	90.2	30.11	89.1	30.43	89.5	30.34
97.2	29.67	98.2	29.68	96.7	29.70	97.5	29.80
106.4	29.04	107.0	29.12	108.5	29.08	108.6	29.04
120.0	28.44	119.0	28.67	119.6	28.46	119.6	28.58

TABLE A.XXVIII
GOLDEN DRAGON PLUS DYNAMIC RESISTANCE AT 350 MA, 100 HZ VS. JUNCTION TEMPERATURE AND RIPPLE

Current Ripple							
10%		***20%***		***30%***		***40%***	
T_j (ºC)	R_D (Ω)	T_j (ºC)	R_D (Ω)	T_j (ºC)	R_D (Ω)	T_j (ºC)	R_D (Ω)
7.9	41.59	8.5	42.03	7.8	42.43	7.4	42.61
23.3	41.84	17.5	42.35	16.8	42.38	16.8	42.49
26.9	41.96	24.6	42.42	25.1	42.33	25.2	42.56
35.3	41.65	35.3	42.46	36.0	42.45	36.4	42.77
48.2	42.13	47.0	42.64	47.8	42.48	47.6	42.84
51.8	42.23	54.1	42.64	53.7	42.73	54.9	42.93
63.9	42.53	62.3	42.89	62.3	42.91	62.6	43.01
71.7	42.58	73.1	42.70	73.1	43.06	73.1	43.17
82.1	42.62	83.3	43.11	83.4	43.08	83.7	43.48
90.7	42.95	91.2	43.30	91.2	43.41	91.6	43.59
96.9	43.03	97.3	43.45	97.4	43.23	97.6	43.58
106.4	43.41	107.3	43.76	107.1	43.81	107.8	43.91
110.8	44.39	111.9	44.84	112.3	44.95	114.8	44.47
117.8	44.46	117.5	44.80	116.9	45.05	118.7	44.88

TABLE A.XXIX
LUXEON K2 DYNAMIC RESISTANCE AT 350 MA, 100 HZ VS. JUNCTION TEMPERATURE AND RIPPLE

Current Ripple							
10%		***20%***		***30%***		***40%***	
T_j (ºC)	R_D (Ω)	T_j (ºC)	R_D (Ω)	T_j (ºC)	R_D (Ω)	T_j (ºC)	R_D (Ω)
2.8	61.31	1.8	62.16	2.2	62.52	2.2	62.46
7.7	60.76	8.7	61.58	8.6	61.93	8.6	61.95
16.8	60.34	17.6	60.93	18.2	61.43	19.5	61.45
27.2	59.18	27.9	59.87	26.4	60.11	28.3	60.43
39.0	59.29	39.0	60.04	39.5	60.34	39.8	60.46
47.2	58.62	47.0	59.73	46.9	59.66	47.0	59.74
58.1	57.77	56.6	58.69	56.6	58.75	56.9	58.99
66.1	57.39	68.4	57.94	65.9	58.05	68.2	58.29
79.9	55.78	79.5	56.45	79.2	56.20	79.9	56.76
90.1	54.72	89.3	55.39	89.6	55.31	89.9	55.91
100.1	53.29	100.2	53.91	100.6	54.19	100.2	54.39
108.6	52.86	112.1	53.07	112.1	53.10	111.8	53.60
117.6	51.78	119.6	52.44	120.0	52.21	120.6	52.23

TABLE A.XXX
Z-POWER P4 DYNAMIC RESISTANCE AT 350 MA, 100 HZ VS. JUNCTION TEMPERATURE AND RIPPLE

Current Ripple							
10%		***20%***		***30%***		***40%***	
T_j (ºC)	R_D (Ω)	T_j (ºC)	R_D (Ω)	T_j (ºC)	R_D (Ω)	T_j (ºC)	R_D (Ω)
1.6	57.26	2.0	57.72	1.9	57.31	2.6	57.65
9.8	55.33	10.2	56.01	9.5	55.77	9.4	56.12
19.6	53.42	19.5	54.32	18.4	54.3	18.5	54.53
27.4	51.85	27.8	52.40	27.4	52.29	26.0	53.01
39.1	49.89	38.8	50.73	38.9	50.79	39.1	50.80
44.7	49.12	45.9	49.55	45.2	49.74	45.5	49.90
54.1	47.82	53.7	48.30	53.4	48.62	53.6	48.86
61.0	47.04	60.8	47.58	60.6	47.58	61.3	47.67
73.0	45.80	71.0	46.46	70.4	46.56	70.9	46.76
78.2	45.11	78.1	45.96	78.1	45.86	77.2	46.14
86.2	44.79	86.0	45.10	86.7	45.32	87.4	45.25
97.2	43.65	101.7	44.23	100.9	44.26	101.4	44.50
108.7	43.23	109.5	43.91	111.0	43.84	111.4	43.93
119.1	43.10	119.2	43.32	117.6	43.37	119.5	43.66

TABLE A.II-XXXI
X-LAMP XR-E DYNAMIC RESISTANCE AT 350 MA, 100 HZ VS. JUNCTION TEMPERATURE AND RIPPLE

Current Ripple							
10%		***20%***		***30%***		***40%***	
T_j (ºC)	R_D (Ω)	T_j (ºC)	R_D (Ω)	T_j (ºC)	R_D (Ω)	T_j (ºC)	R_D (Ω)
-5.4	54.50	-5.8	55.10	-5.7	55.06	-5.2	55.29
4.9	52.36	3.7	53.11	3.0	53.42	2.9	53.51
12.2	50.64	11.9	51.62	13.3	51.24	12.7	51.51
22.6	48.76	23.1	49.14	22.9	49.03	23.3	49.17
33.2	46.08	33.8	46.59	33.3	46.76	33.6	47.08
41.8	44.47	41.4	44.89	41.8	44.98	41.0	45.25
49.1	42.91	49.1	43.18	49.0	43.29	48.2	43.58
58.9	40.91	58.1	41.37	58.0	41.26	57.8	41.74
65.0	39.74	65.2	40.19	65.3	40.11	64.9	40.38
74.4	38.41	73.2	38.64	72.9	38.75	73.6	38.88
81.4	37.52	81.3	37.90	81.0	38.06	79.7	38.08
90.2	36.61	89.9	36.90	89.9	37.10	89.8	37.18
97.3	36.01	99.4	36.25	100.2	36.30	101.1	36.51
105.7	35.57	108.9	35.66	110.3	35.70	112.7	35.85
115.0	35.21	115.6	35.45	116.1	35.33	117.1	35.54

TABLE A.XXXII
GOLDEN DRAGON PLUS DYNAMIC RESISTANCE AT 700 MA, 100 HZ VS. JUNCTION TEMPERATURE AND RIPPLE

Current Ripple							
10%		***20%***		***30%***		***40%***	
T_j (ºC)	R_D (Ω)	T_j (ºC)	R_D (Ω)	T_j (ºC)	R_D (Ω)	T_j (ºC)	R_D (Ω)
47.8	30.58	49.0	30.93	48.6	31.07	48.6	31.19
56.3	30.82	56.6	31.14	56.3	31.18	55.5	31.33
63.8	31.19	64.1	31.32	64.6	31.44	66.1	31.46
70.7	31.46	70.7	31.61	71.7	31.61	72.3	31.75
84.2	31.72	84.7	31.88	83.8	31.85	83.2	31.96
90.1	31.69	90.5	31.84	89.9	31.85	90.2	31.95
96.5	32.01	97.1	31.99	98.0	32.20	97.3	32.27
104.5	32.24	105.2	32.19	104.4	32.41	105.2	32.48
110.1	32.47	110.1	32.70	111.0	32.64	112.0	32.82
116.3	32.69	117.7	32.83	117.5	32.92	117.6	33.07

TABLE A.XXXIII
LUXEON K2 DYNAMIC RESISTANCE AT 700 MA, 100 HZ VS. JUNCTION TEMPERATURE AND RIPPLE

Current Ripple							
10%		***20%***		***30%***		***40%***	
T_j (ºC)	R_D (Ω)	T_j (ºC)	R_D (Ω)	T_j (ºC)	R_D (Ω)	T_j (ºC)	R_D (Ω)
21.7	41.77	21.3	41.75	21.4	42.02	21.7	42.17
30.4	41.66	30.1	41.85	31.4	41.68	30.9	42.00
40.3	41.27	41.2	41.54	40.1	41.40	42.0	41.60
51.5	41.19	53.2	41.15	52.7	41.16	51.7	41.35
64.8	40.10	67.6	41.27	68.4	41.19	67.8	41.36
72.1	40.74	72.4	41.05	72.3	40.97	73.2	41.08
82.4	41.02	83.5	40.76	84.1	40.73	84.7	40.75
95.3	40.17	95.2	40.31	95.1	40.07	95.7	40.21
107.1	39.26	107.5	39.33	107.5	39.42	107.0	39.64
119.1	38.66	119.5	38.88	119.5	38.85	119.6	38.91

TABLE A.XXXIV
Z-POWER P4 DYNAMIC RESISTANCE AT 700 MA, 100 HZ VS. JUNCTION TEMPERATURE AND RIPPLE

Current Ripple							
10%		***20%***		***30%***		***40%***	
T_j (ºC)	R_D (Ω)	T_j (ºC)	R_D (Ω)	T_j (ºC)	R_D (Ω)	T_j (ºC)	R_D (Ω)
30.3	38.72	30.7	38.54	31.0	38.74	31.1	38.75
38.0	38.05	38.0	37.94	38.5	38.08	38.2	38.15
47.1	37.34	46.0	37.20	48.0	37.31	47.1	37.44
54.6	36.57	54.8	36.78	54.0	36.76	53.3	36.99
66.1	36.03	66.0	36.05	66.3	35.96	66.8	36.02
70.9	35.73	71.1	35.85	71.4	35.83	71.9	35.77
79.8	35.25	79.4	35.33	80.5	35.43	80.5	35.41
86.9	35.04	88.2	35.20	89.4	35.03	89.0	35.11
97.5	34.82	98.7	34.87	99.1	34.72	99.4	34.83
107.3	34.77	109.5	34.71	109.5	34.69	110.8	34.69
115.1	34.45	124.3	34.43	123.0	34.35	123.4	34.45

TABLE A.XXXV
X-LAMP XR-E DYNAMIC RESISTANCE AT 700 MA, 100 HZ VS. JUNCTION TEMPERATURE AND RIPPLE

Current Ripple							
10%		***20%***		***30%***		***40%***	
T_j (ºC)	R_D (Ω)	T_j (ºC)	R_D (Ω)	T_j (ºC)	R_D (Ω)	T_j (ºC)	R_D (Ω)
16.2	37.35	17.4	37.28	17.5	37.15	18.1	37.22
26.8	36.16	23.1	36.13	27.6	35.99	27.0	36.13
35.1	34.86	35.8	34.90	34.4	35.07	35.4	35.07
45.0	33.66	43.8	33.98	45.6	33.69	45.2	33.86
56.6	32.27	56.4	32.46	57.0	32.33	56.3	32.42
63.0	31.59	62.5	31.81	62.8	31.73	63.4	31.79
71.2	30.71	71.0	30.68	71.0	30.90	71.3	30.88
79.4	30.05	79.3	29.98	79.9	30.00	79.9	30.05
86.9	29.43	88.0	29.27	88.9	29.27	89.4	29.25
97.1	28.61	97.6	28.66	97.6	28.64	95.8	28.86
105.4	28.17	108.1	28.11	107.6	28.11	108.2	28.17
117.2	27.75	120.0	27.58	118.0	27.67	119.2	27.80

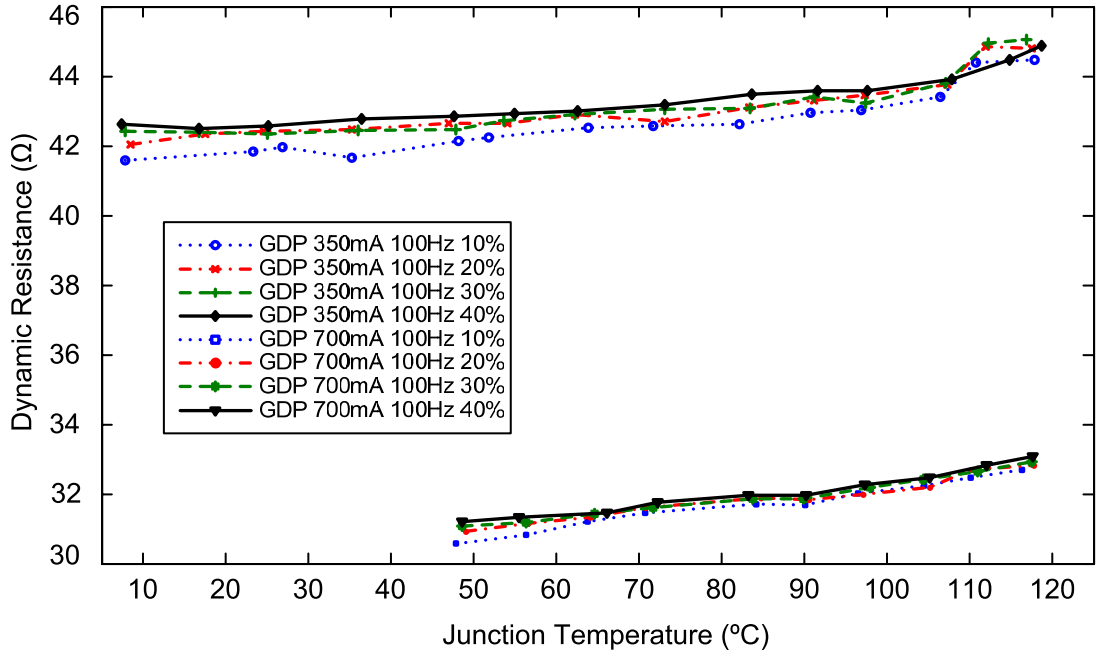

Fig. A.7. Experimental results for the dynamic resistance as a function of the junction temperature and the 100 Hz current ripple for the Golden Dragon Plus device.

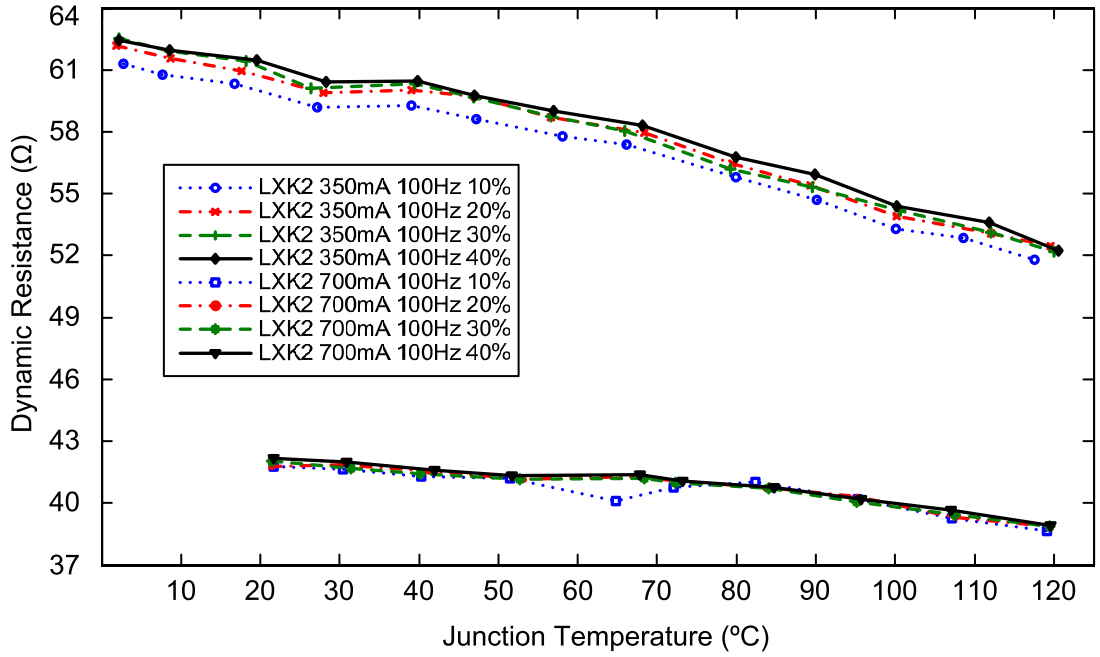

Fig. A.8. Experimental results for the dynamic resistance as a function of the junction temperature and the 100 Hz current ripple for the Luxeon K2 with TFFC device.

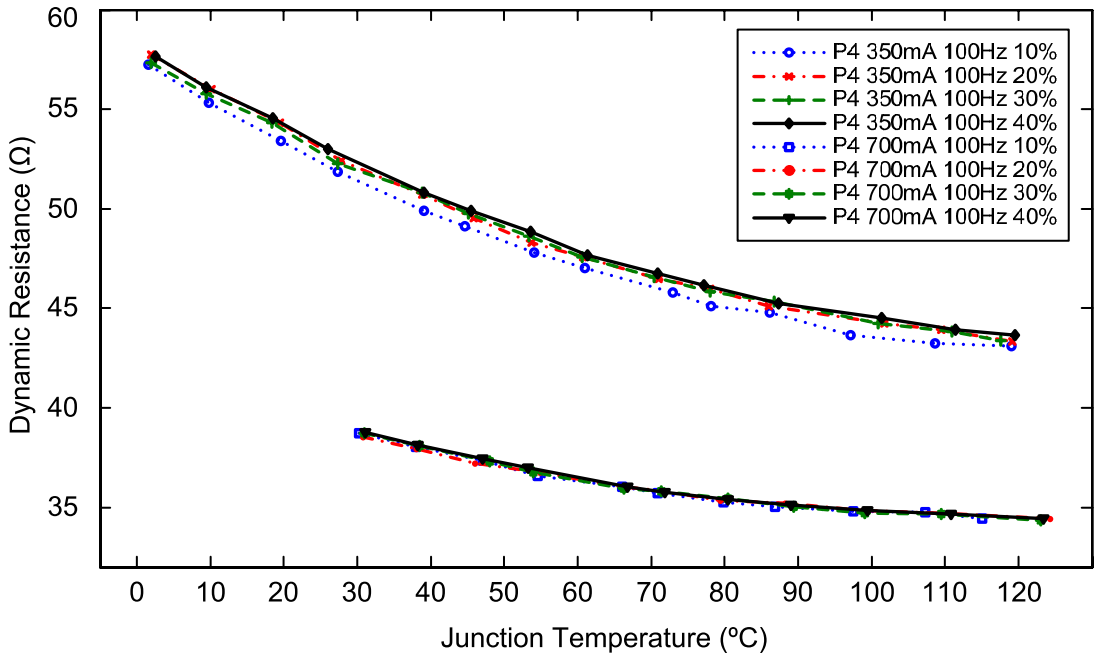

Fig. A.9. Experimental results for the dynamic resistance as a function of the junction temperature and the 100 Hz current ripple for the Z-Power P4 device.

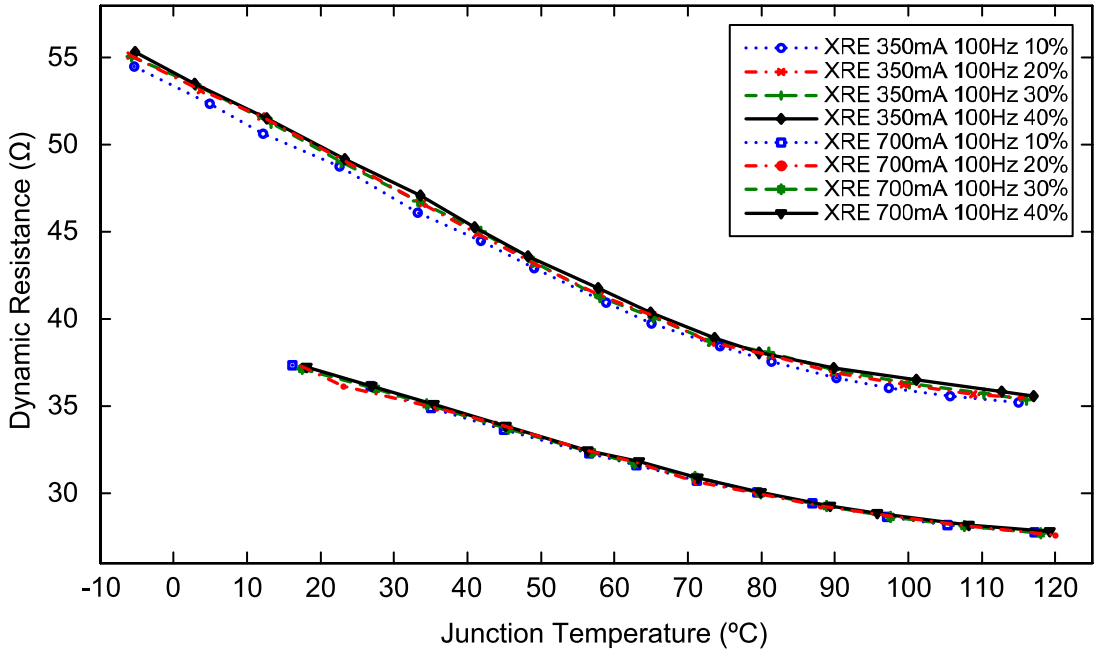

Fig. A.10. Experimental results for the dynamic resistance as a function of the junction temperature and the 100 Hz current ripple for the XLamp XR-E device.

TABLE A.XXXVI
GOLDEN DRAGON PLUS DYNAMIC RESISTANCE: POLYNOMIAL FIT, 100 HZ, 60-LEDS LAMPS TEST

Current level	***Current ripple***	$R_D=a\cdot T_j^3+b\cdot T_j^2+c\cdot T_j+d$ (Ω)				r^2
		a (mΩ/ºC^3)	***b*** (mΩ/ºC^2)	***c*** (mΩ/ºC)	***d*** (Ω)	
350 mA	***10%***	0	0.2434	-7.737	41.82	0.9342
	20%	0	0.2613	-12.14	42.43	0.9138
	30%	0	0.3231	-20.00	42.67	0.9069
	40%	0	0.2012	-7.763	42.67	0.9610
700 mA	***10%***	0	0	29.07	29.24	0.9815
	20%	0	0.1233	5.294	30.45	0.9607
	30%	0	0.1644	-1.509	30.79	0.9899
	40%	0	0.2056	-8.245	31.14	0.9862

TABLE A.XXXVII
LUXEON K2 WITH TFFC DYNAMIC RESISTANCE: POLYNOMIAL FIT, 100 HZ, 60-LEDS LAMPS TEST

Current level	***Current ripple***	$R_D=a\cdot T_j^3+b\cdot T_j^2+c\cdot T_j+d$ (Ω)				r^2
		a (mΩ/ºC^3)	***b*** (mΩ/ºC^2)	***c*** (mΩ/ºC)	***d*** (Ω)	
350 mA	***10%***	0	-0.3572	-38.45	61.14	0.9927
	20%	0	-0.3453	-40.81	61.97	0.9896
	30%	0	-0.2876	-51.81	62.45	0.9921
	40%	0	-0.3715	-38.82	62.36	0.9951
700 mA	***10%***	0	-0.2076	0.4172	41.73	0.8691
	20%	0	-0.3248	16.64	41.51	0.9735
	30%	0	-0.2601	6.955	41.77	0.9722
	40%	0	-0.2525	4.586	42.05	0.9817

TABLE A.XXXVIII
Z-POWER P4 DYNAMIC RESISTANCE: POLYNOMIAL FIT, 100 HZ, 60-LEDS LAMPS TEST

Current level	***Current ripple***	$R_D=a\cdot T_j^3+b\cdot T_j^2+c\cdot T_j+d$ **(Ω)**				r^2
		a **(mΩ/ºC^3)**	***b*** **(mΩ/ºC^2)**	***c*** **(mΩ/ºC)**	***d*** **(Ω)**	
350 mA	***10%***	0	0.8859	-226.9	57.51	0.9994
	20%	0	0.8753	-227.5	58.21	0.9992
	30%	0	0.7770	-212.4	57.74	0.9993
	40%	0	0.8291	-220.3	58.20	0.9998
700 mA	***10%***	0	0.5665	-131.4	42.19	0.9964
	20%	0	0.4418	-111.1	41.49	0.9970
	30%	0	0.5000	-123.3	42.06	0.9972
	40%	0	0.5082	-124.4	42.14	0.9987

TABLE A.XXXIX
X-LAMP XR-E DYNAMIC RESISTANCE: POLYNOMIAL FIT, 100 HZ, 60-LEDS LAMPS TEST

Current level	***Current ripple***	$R_D=a\cdot T_j^3+b\cdot T_j^2+c\cdot T_j+d$ **(Ω)**				r^2
		a **(mΩ/ºC^3)**	***b*** **(mΩ/ºC^2)**	***c*** **(mΩ/ºC)**	***d*** **(Ω)**	
350 mA	***10%***	8.369E-3	-0.5051	-209.6	53.39	0.9997
	20%	9.449E-3	-0.6671	-208.0	53.99	0.9995
	30%	8.465E-3	-0.5143	-213.0	54.01	0.9991
	40%	8.990E-3	-0.5995	-210.3	54.22	0.9993
700 mA	***10%***	2.976E-3	-5.808E-2	-135.3	39.61	0.9996
	20%	4.084E-3	-0.3488	-113.0	39.16	0.9985
	30%	3.638E-3	-0.2501	-119.9	39.34	0.9999
	40%	4.103E-3	-0.3098	-119.2	39.48	0.9998

TABLE A.XL
GOLDEN DRAGON PLUS DYNAMIC RESISTANCE: LINEAR FIT 350 MA, 100 HZ, 60-LEDS LAMPS TEST, T_J<100ºC

Current level	***Current ripple***	$R_D=a\cdot T_j+b$ **(Ω)**		r^2
		a **(mΩ/ºC)**	***b*** **(Ω)**	
350 mA	***10%***	17.60	41.34	0.9412
	20%	13.54	42.00	0.9212
	30%	11.86	42.13	0.8881
	40%	12.79	42.31	0.9391

TABLE A.XLI

EXPERIMENTAL V_D-T_J FITTING POLYNOMIALS (SINGLE-EMITTER, NORMALISED LED)

LED	$V_D = a \cdot T_j^{2+} b \cdot T_j + b$ **(V)**			r^2
	a	***bx10^{-3}***	***c***	
Dragon Plus (350mA, single emitter)	4.082E-6	-3.107	3.225	0.9993
Dragon Plus (350 mA, normalised)	3.953E-6	-3.042	3.277	0.9996
Dragon Plus (700mA, single emitter)	4.584E-6	-3.073	3.435	0.9991
Dragon Plus (700 mA, normalised)	5.130E-6	-3.275	3.508	0.9997
Luxeon K2 (350mA, single emitter)	4.855E-6	-4.269	3.560	0.9988
Luxeon K2 (350 mA, normalised)	4.160E-6	-4.335	3.512	0.9998
Luxeon K2 (700mA, single emitter)	2.608E-6	-4.355	3.864	0.9993
Luxeon K2 (700 mA, normalised)	4.473E-6	-4.667	3.843	0.9999
Z-Power P4 (350mA, single emitter)	1.696E-5	-5.595	3.403	0.9986
Z-Power P4 (350 mA, normalised)	1.768E-5	-5.607	3.295	0.9993
Z-Power P4 (700mA, single emitter)	2.310E-5	-7.150	3.777	0.9989
Z-Power P4 (700 mA, normalised)	2.089E-5	-6.687	3.607	0.9997
X-Lamp XR-E (350mA, single emitter)	2.770E-5	-7.082	3.274	0.9980
X-Lamp XR-E (350 mA, normalised)	1.917E-5	-5.712	3.245	0.9991
X-Lamp XR-E (700mA, single emitter)	3.180E-5	-9.021	3.623	0.9996
X-Lamp XR-E (700 mA, normalised)	2.212E-5	-6.978	3.535	0.9998

TABLE A.XLII

EXPERIMENTAL R_D-T_J FITTING POLYNOMIALS (SINGLE-EMITTER, NORMALISED LED)

LED	$R_D = a \cdot T_j^{3+} b \cdot T_j^{2+} c \cdot T_j + d$ **(V)**				r^2
	a **(mΩ/ºC^3)**	***b*** **(mΩ/ºC^2)**	***c*** **(mΩ/ºC)**	***d*** **(Ω)**	
Dragon Plus (350mA, single emitter)	0	0	-0.0506	0.6904	0.3804
Dragon Plus (350 mA, normalised)	0	0.0052	-0.3632	0.7248	0.8648
Dragon Plus (700mA, single emitter)	0	0.0026	-0.2190	0.5256	0.8947
Dragon Plus (700 mA, normalised)	0	0.0017	0.0737	0.5322	0.9359
Luxeon K2 (350mA, single emitter)	0	-0.0023	-0.4118	0.9684	0.9599
Luxeon K2 (350 mA, normalised)	0	-0.0057	-0.7187	1.0543	0.9865
Luxeon K2 (700mA, single emitter)	0	-0.0023	-0.1980	0.7065	0.9907
Luxeon K2 (700 mA, normalised)	0	-0.0047	0.0384	0.738	0.9767
Z-Power P4 (350mA, single emitter)	2.004E-4	-0.0144	-2.6799	1.1404	0.9983
Z-Power P4 (350 mA, normalised)	0	0.0174	-4.3217	1.0112	0.9991
Z-Power P4 (700mA, single emitter)	0	0.0119	-3.1060	0.9063	0.9943
Z-Power P4 (700 mA, normalised)	0	0.0113	-2.8017	0.7735	0.9979
X-Lamp XR-E (350mA, single emitter)	6.384E-4	-0.0673	-4.1584	1.0706	0.9981
X-Lamp XR-E (350 mA, normalised)	1.394E-4	-0.0067	-3.8833	0.9258	0.9996
X-Lamp XR-E (700mA, single emitter)	4.391E-4	-0.0803	1.0101	0.7600	0.9993
X-Lamp XR-E (700 mA, normalised)	0.635E-4	-0.0030	-2.4450	0.7018	0.9999