Design-Oriented Analysis and Performance Evaluation of a Low-Cost High-Brightness LED Driver Based on Flyback Power Factor Corrector

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***Abstract*—This paper presents a new control strategy for power factor correctors (PFCs) used to drive high-brightness light-emitting diodes (HB-LEDs). This control strategy is extremely simple and is based on the use of standard peak-current-mode integrated controllers (PCMICs), reducing its cost and complexity in comparison to traditional PFC controllers. In fact, this method is an alternative implementation of the one-cycle control to PFCs belonging to the flyback family of converters, without introducing high complexity for reducing the total harmonic distortion. In this case, the use of a simple exponential compensation ramp instead of a linear one is the proposed solution for drawing a sinusoidal input current. Moreover, the line current is cycle-by-cycle controlled, and therefore, the input-current feedback loop is extremely fast, which allows the use of this type of control with high-frequency lines. The proposed idea is to apply this simple control to a one-stage PFC in order to design a low-cost ac–dc HB-LED driver. However, the application of this control strategy to PFC belonging to the flyback family of converters is not obvious. Design-oriented considerations about its implementation in PCMIC will be provided. Finally, an experimental prototype of this driver was developed.**

***Index Terms*—AC–DC power conversion, current control, harmonic distortion, light-emitting diodes, power factor (PF), rectifiers, switched-mode power supplies.**

I. Introduction

In THE LAST years, solid-state lighting technology progress has changed traditional solutions in lighting. Nowadays, high-brightness light-emitting diodes (HB-LEDs) are very attractive light sources due to their excellent characteristics: high efficiency, high longevity, and low-maintenance requirements [1], [2]. Also, HB-LED packages are more and more robust, introducing higher reliability than traditional light sources (fluorescent lamps, incandescent lamps, etc.). Since HB-LEDs are diodes, the default method for driving them is controlling the dc forward current through the semiconductor. If the primary energy source is the ac line, then some type of ac–dc converter must be placed between the line and the HB-LEDs [3]–[6]. It is known that, if the total power handled by these converters is higher than 25 W, then the low-frequency harmonic content of the line current must comply with specific regulations. For lighting equipment, the most widely used standards are EN 61000-3-2, Class C [7], [8] and ENERGY STAR program [9]. These regulations establish a very strict harmonic content, such that only very sinusoidal line waveforms are able to comply with the aforementioned regulations. Therefore, the only practical method to comply with these regulations is to use active high-power-factor (PF) converters, commonly called PF correctors (PFCs).

The classical control method of PFCs operating in continuous conduction mode (CCM) for obtaining a perfectly sinusoidal line waveform is based on two feedback loops (an input-current feedback loop and an output-voltage feedback loop) and a multiplier [Fig. 1(a)] [10], [11]. However, the main disadvantage of this option is the complexity of the control circuitry and its cost. Several controllers can be used for this purpose, but they are not cheap, particularly in comparison with standard controllers for switching-mode power supplies (SMPSs). If the converter has to be a very low-cost one, the use of PFC controllers based on a multiplier becomes relatively expensive.

With HB-LEDs being increasingly used in low-cost lighting applications, the necessity for ac–dc drivers with optimized control circuitry that reduces their cost becomes more important. In the last years, a number of authors have proposed different low-cost control strategies for PFCs operating in CCM and wide input-voltage range [12]–[17]. The goal of these control strategies is to simplify the existing control circuitry based on a multiplier. The most significant one is the one-cycle control (OCC) technique [Fig. 1(b)] [14]–[17]. It is important to say that the OCC has not only been used in ac–dc converters. The significance of the OCC has been extended to other converters, e.g., three-phase rectifier [18], [19], inverters [20], and bidirectional converters [21], due to its simplicity. In ac–dc conversion, this low-cost control technique is focused on boost

Manuscript received December 5, 2011; revised March 9, 2012; accepted April 15, 2012. Date of publication April 30, 2012; Date of current version February 28, 2013. This work was supported by the Spanish Ministry of Education and Science under Consolider Project RUE CSD2009-00046, Project DPI2010-21110-C02-0, Grant AP-2008-03380, and European Regional Development Fund grants.

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Digital Object Identifier 10.1109/TIE.2012.2196905

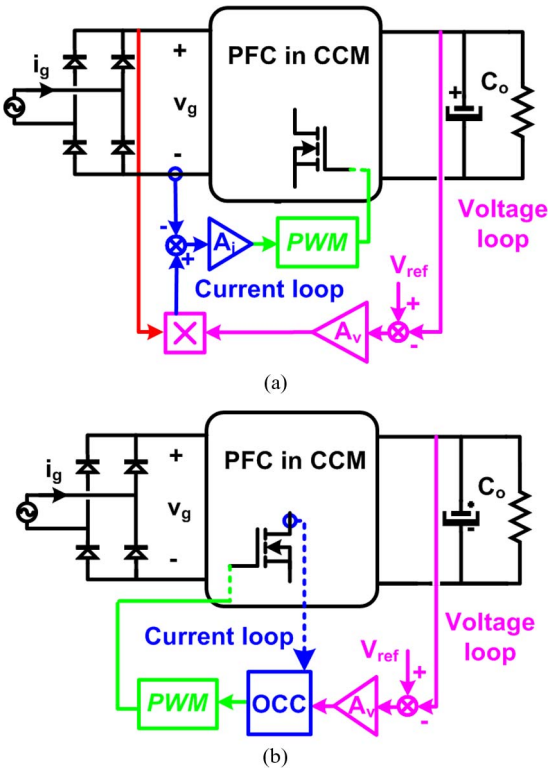

Fig. 1. Two control methods for PFCs operating in CCM. (a) Multiplier-based control. (b) OCC.

topology as the first stage of high-PF ac–dc power supplies because its implementation is quite simple. In this case, a second stage is needed to introduce galvanic isolation and adequate output voltage. Therefore, the cost and complexity of the power supply increase. Following the main idea of this paper (i.e., propose a low-cost solution), an isolated one-stage PFC can be a possibility. However, if this control technique is applied to PFCs based on converters belonging to the flyback family (i.e., buck–boost, single-ended primary-inductor converter, Cuk, and Zeta), then the input current is distorted. In order to solve this drawback, the cost and complexity of the control circuitry must be increased because a complex specific matching must be used [16], [17]. This fact makes OCC less attractive for this family of PFCs.

A new low-cost control strategy for PFCs belonging to the flyback family is presented in this paper. This method is an alternative implementation of the OCC to this family of PFCs, avoiding its traditional complexity. Only an exponential compensation ramp is used in order to reduce the total harmonic distortion (THD). It allows the use of standard peak-current-mode integrated controllers (PCMICs) for SMPS to control PFCs operating in CCM. Moreover, with this control strategy, the input current is cycle-by-cycle controlled. Therefore, the input-current feedback loop is extremely fast, thereby allowing this type of control to be used with relatively high-frequency lines (e.g., 400-Hz lines). The price to pay for these advantages is the quality of the line waveform, which will be very sinusoidal at full load but will be less sinusoidal when the load decreases during dimming operation. However, this input-current distortion becomes slight. For the aforementioned reasons, this control strategy applied to single-stage PFCs with galvanic isolation becomes a good option to design low-cost and simple ac–dc drivers for HB-LEDs.

However, the practical implementation of the proposed solution in standard PCMIC is not obvious. For this reason, in both Sections III-A and B a design-oriented procedure will be provided.

Also, the proposed solution to design an ac–dc driver for HB-LEDs (i.e., flyback PFC as a one-stage solution) presents an additional drawback: the output capacitor design. As it is known, a large capacitance is needed in PFC in order to balance the pulsating input power and the dc output power [10], [11]. Therefore, an electrolytic capacitor must be used as an output capacitor. In the case of one-stage PFC solutions, the electrolytic output capacitor cannot be replaced by other technology (i.e., Metallized Polypropylene Film (MKP), Metallized Polyester Film (MKT) and ceramic capacitors) in order to increase its lifetime. This is due to the fact that the increase of the cost and size of the output capacitor is unaffordable. The Appendix of this paper presents the limits of the output capacitor design in flyback PFCs regarding lifetime, cost, and size considerations.

II. Proposed Control Technique. Principle of Operation

Fig. 2(a) shows the control circuitry and the main control waveforms of OCC applied to boost PFCs. It is known that the peak value $(v_{\rm rp})$ of the linear compensation ramp (v_r) must coincide with the output voltage of the voltage feedback loop (v_A) at the end of the switching period in all operating situations for the control to work properly [14] [see waveforms in Fig. 2(a)]. For this reason, the integrator time constant of the ramp generator must match the switching period. Therefore, a simple specific matching has to be used. It is known that, if this control strategy is applied to PFCs belonging to the flyback family of converters, the input current is distorted [Fig. 2(b)]. If a sinusoidal input current is needed, then two matched integrators or a current sensor with an integrator equipped with a reset mechanism must be used in order to generate a parabolic compensation ramp, where its peak value is equal to v_A at the end of the switching period in all operating situations [16], [17]. In other words, two specific matching circuits have to be used, thereby increasing the cost and complexity of the control. Considering again the waveform shown in Fig. 2(b), it should be noted that the highest distortion is located near the zero crossing of the input current. This means that the duty cycle generated in these zones is excessive. If an exponential compensation ramp is used instead of a traditional linear ramp, then this excessive duty cycle can be reduced. The controller used is the same as the one shown in Fig. 2; the only difference is the ramp generator, which generates now an exponential ramp. Fig. 3(a) shows the main waveforms of the OCC with exponential ramp generator. Moreover, Fig. 3(b) shows the alternative implementation of OCC proposed in this paper to apply this control strategy in standard PCMICs. As you can see in Fig. 3(b) and (c), with this implementation, no specific matching circuits have to be used in order to force $v_{\rm rp}$ to be equal to v_A at the end of the switching period. If the exponential compensation ramp is

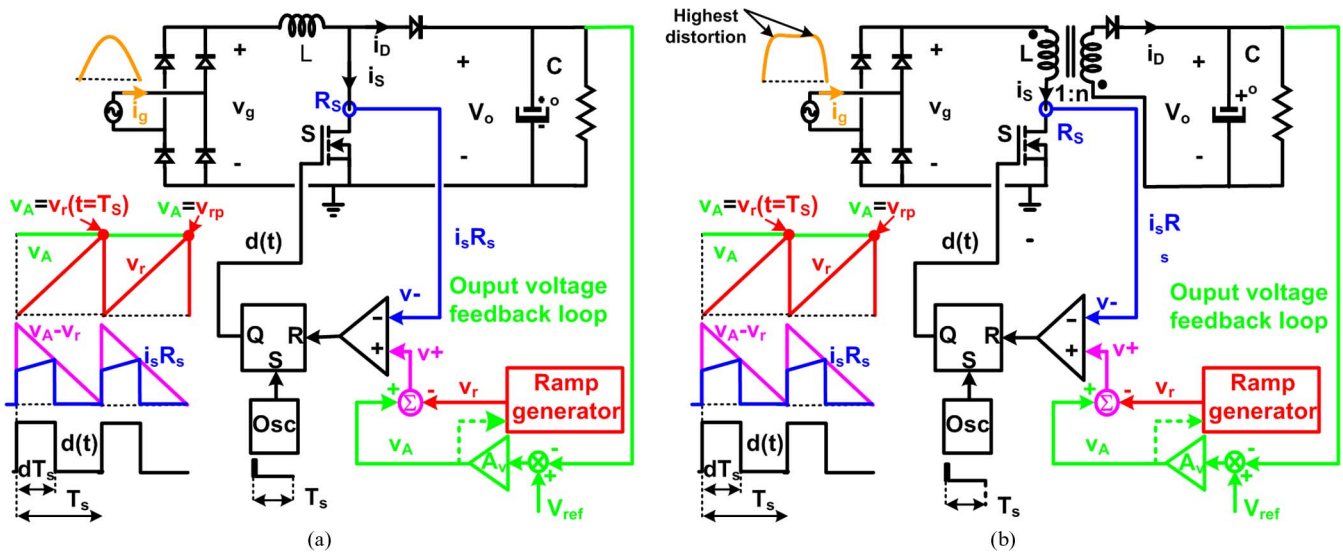

Fig. 2. (a) OCC with a linear ramp generator for a boost PFC. (b) OCC with a linear ramp generator for the flyback PFC.

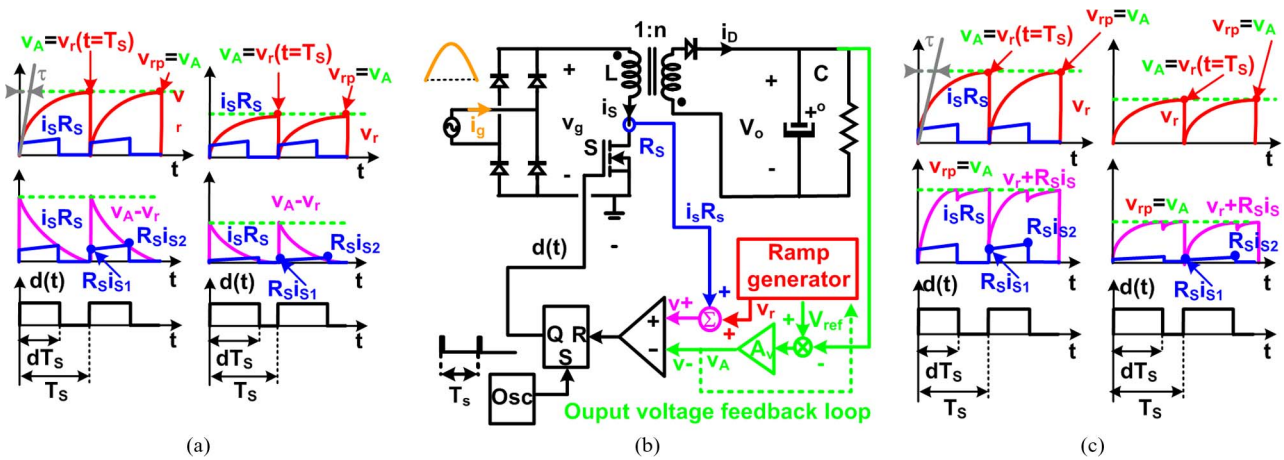

Fig. 3. (a) Main waveforms of the control in Fig. 2(b) with an exponential ramp generator. (b) New implementation of OCC with an exponential compensation ramp for the flyback family of PFCs. (c) Main control waveforms of new implementation of the OCC.

generated by v_A using an RC circuit as a ramp generator, then the peak value of the compensation ramp is known and almost equal to the v_A at the end of the switching period if the time constant defined by RC is high enough. In this case, the duty cycle is determined by the instant when $v_r + i_S R_S$ equals v_A [Fig. 3(c)], which is equivalent condition to the OCC one shown in Fig. 3(a) ($v_r - v_A$ equals $i_S R_S$) [14]. Also, Fig. 3(c) shows the main control waveforms at full and low loads.

The expression of the exponential compensation ramp shown in Fig. 3(a) (magenta color) can be easily obtained

$$v_r = v_{\rm rp} \cdot \frac{e^{-\frac{t}{\tau}} - e^{-\frac{T_S}{\tau}}}{1 - e^{-\frac{T_S}{\tau}}} = v_{\rm rp} \cdot \frac{e^{--\frac{t}{\tau}} - e^{-\mu}}{1 - e^{-\mu}} \tag{1}$$

where $v_{\rm rp}$ is the peak value of the exponential compensation ramp (v_r), τ is the time constant of the exponential compensation ramp [Fig. 3(a) and (c)], T_S is the switching period, and μ is defined as

$$\mu = \frac{T_S}{\tau} = \frac{1}{(\tau \cdot f_S)} \tag{2}$$

where f_S is the switching frequency.

The expression of the current through the magnetizing inductance of the flyback transformer at the end of the magnetizing period (i.e., i_{S2} in blue color in Fig. 3(a) at $t = T_S d$) can be calculated when v_r equals $R_S i_{S2}$

$$i_{S2} = \frac{v_{\rm rp}}{R_S} \cdot \frac{e^{-d\mu} - e^{-\mu}}{1 - e^{-\mu}} \tag{3}$$

where R_S is the gain of the controlled switch current sensor and d is the duty cycle.

Applying Faraday's law to the magnetizing inductance of the flyback transformer operating in CCM during the magnetizing period yields

$$v_g = L f_S \frac{i_{S2} - i_{S1}}{d} \tag{4}$$

where v_g is the rectified input voltage (i.e., $v_g = V_{gP}|\sin(\omega_L t)|$) and L is the magnetizing inductance of the flyback transformer. Analyzing also the demagnetizing period of the flyback, we obtain

$$V_o = n L f_S \frac{i_{S2} - i_{S1}}{1 - d} \tag{5}$$

where V_o is the output voltage and n is the turn ratio of transformer of the flyback (i.e., $n = n_2/n_1$). By using (4) and (5), the expression of the duty cycle can be expressed as

$$d = \frac{V_o}{V_o + V_{gP}\sin(\omega_L t)\cdot n}. \tag{6}$$

Taking into account (3) and (4), the average input current is defined as follows:

$$i_{\text{gav}} = \frac{(i_{S2}+i_{S1})d}{2} = \left(\frac{v_{\text{rp}}(e^{-d\mu}-e^{-\mu})}{R_S(1-e^{-\mu})} - \frac{V_{gP}\sin(\omega_L t)d}{2Lf_S}\right) d. \tag{7}$$

Three parameters will be defined in order to simplify the study of this static analysis

$$K = \frac{2Lf_S v_{\text{rp}}}{(R_S V_{gP})} \tag{8}$$

$$M = \frac{V_o}{nV_{gP}} \tag{9}$$

$$i_n = \frac{V_o}{Lf_s} \tag{10}$$

where K is a dimensionless parameter used to study the boundary between CCM and discontinuous conduction mode (DCM), M is the conversion ratio at the peak of the line voltage (V_{gP}), and i_n is used in order to normalize significant currents of this static study. From (6)–(10), we can normalize i_{gav}

$$i_{\text{gav}} = i_n \frac{\left[\frac{e^{-\frac{M}{(M+\sin(\omega_L t))}\mu} - e^{-\mu}}{1-e^{-\mu}}K - \frac{M\cdot\sin(\omega_L t)}{(M+\sin(\omega_L t))}\right]}{2\,(M+\sin(\omega_L t))\cdot n}. \tag{11}$$

Using the same procedure used to calculate i_{avg} [i.e., using (3), (4), (6), and (8)–(10)], we can normalize the expression of the current through L at the beginning of the switching period [i.e i_{S1} in blue color in Fig. 3(a)]

$$i_{S1} = \frac{i_n}{2}\left[\frac{e^{-\frac{M}{(M+\sin(\omega_L t))}\mu} - e^{-\mu}}{1-e^{-\mu}}K - \frac{2M\cdot\sin(\omega_L t)}{(M+\sin(\omega_L t))}\right]. \tag{12}$$

In the case of operating in DCM, (4) is also valid (with $i_{S1} = 0$); however, (5) and (7) become

$$V_o = nLf_S\frac{i_{S2}}{d'} \tag{13}$$

$$i_{\text{gav}} = \frac{i_{S2}}{2}d \tag{14}$$

where $d'T_S$ defines the demagnetizing period of L.

The final expressions of i_{gav} and i_{S2} in DCM as a function of the line angle ($\omega_L t$) may be deduced using the same procedure used in CCM but using (3), (4) with $i_{S1} = 0$, (8)–(10), (13) and (14). Thus, we obtain a transcendent equation that must be numerically solved.

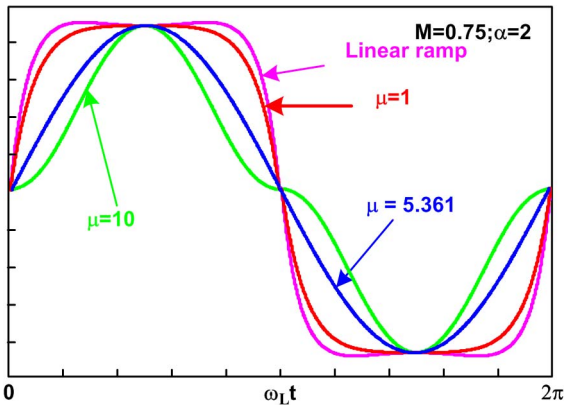

Fig. 4. Normalized line current for different values of μ.

The limit between CCM and DCM can be calculated by setting $i_{S1} = 0$ (12). Therefore, the critical value of K that defines the boundary between CCM and DCM can be calculated as

$$K_{\text{crit}}(\omega_L t) = \frac{2M\cdot\sin(\omega_L t)}{(M+\sin(\omega_L t))}\frac{1-e^{-\mu}}{e^{-\frac{M}{(M+\sin(\omega_L t))}\mu} - e^{-\mu}}. \tag{15}$$

As (15) shows, $K_{\text{crit}}(\omega_L t)$ has different values, depending on the line angle ($\omega_L t$). Hence, the maximum value of $K_{\text{crit}}(\omega_L t)$ is

$$K_{\text{crit\_max}} = \frac{2M(1-e^{-\mu})}{\mu e^{-\mu}} \tag{16}$$

and the minimum value of $K_{\text{crit}}(\omega_L t)$ is

$$K_{\text{crit\_min}} = \frac{2M}{(M+1)}\frac{1-e^{-\mu}}{e^{-\frac{M}{(M+1)}\mu} - e^{-\mu}}. \tag{17}$$

Finally, we define two dimensionless parameters

$$\alpha = \frac{K}{K_{\text{crit\_max}}} = \frac{K\mu e^{-\mu}}{2M(1-e^{-\mu})} \tag{18}$$

$$\alpha_{K\,\text{min}} = \alpha(K_{\text{crit\_min}}) = \frac{K_{\text{crit\_min}}}{K_{\text{crit\_max}}}. \tag{19}$$

The design parameter α defines three operating modes: If $\alpha > 1$, PFC operates always in CCM ($K > K_{\text{crit\_max}}$); if $\alpha < \alpha_{K\,\text{min}} K < K_{\text{crit\_min}}$), it operates always in DCM; and if $1 > \alpha > \alpha_{K\,\text{min}}$, it operates in both modes ($K_{\text{crit\_min}} < K < K_{\text{crit\_min}}$).

At this point, the input current of the PFC can be represented. Fig. 4 shows the normalized input current for several values of μ for the same PFC design ($M = 0.75$ and $\alpha = 2$). As you can see, when an exponential compensation ramp is used, there is an optimum value of μ that minimizes the THD of the line current (Fig. 4) for each design (α and M) at nominal conditions (i.e., nominal input voltage and full load). When μ is chosen (Fig. 4), the design parameter α must be calculated greater than unity in order to ensure CCM operation during the entire line angle at nominal conditions and therefore draw a very sinusoidal input current. Nevertheless, even if the PFC is designed to operate in CCM during the entire line angle at nominal conditions, it should be noted that it will pass

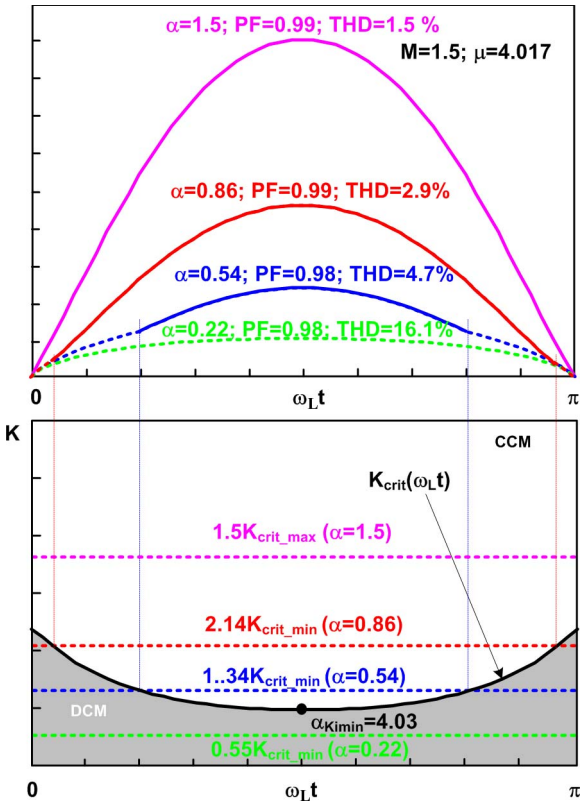

Fig. 5. Line current waveforms for different operation points, defined by K value versus $K_{\rm crit}$, when the optimum value of the exponential ramp ($\mu = 4.017$) is selected for $\alpha = 1.5$ and $M = 1.5$ design.

through different operating modes if the operating point of the PFC changes. If the PFC operates at undervoltage or heavy-load situations (i.e., α increases $\alpha > 1$), it remains in CCM during the entire line angle, drawing a very sinusoidal input current. However, if the load decreases or the input voltage increases, α decreases. If α decreases to below unity ($\alpha < 1$), then two operation modes are possible (see the waveforms shown in Fig. 5): CCM (solid line) and DCM (dotted line). Therefore, Fig. 5 could represent dimming operation of the ac–dc HB-LED driver, where $\alpha = 1.5$, 0.86, 0.54, and 0.22 represent the operation points at $P_{\rm max}$, $0.5P_{\rm max}$, $0.25P_{\rm max}$, and $0.125P_{\rm max}$, respectively. As you can see, the input current is slightly distorted in these operation situations. However, it remains very sinusoidal, making the proposed control strategy suitable for dimming operation. In order to adequately check this slight distortion, Fig. 6 shows the PF and THD versus α different PFC designs. Even if α decreases, the distortion of the input current remains slight.

III. Practical Considerations for AC–DC HB-LED Driver Design Based on the Proposed Solution

As was aforementioned, a proper design of a PFC belonging to the flyback family of converters based on the proposed control strategy should be an option to design an ac–dc HB-LED driver. In the following section, the practical considerations of its design will be provided. The design considerations of the output capacitor are provided in the Appendix.

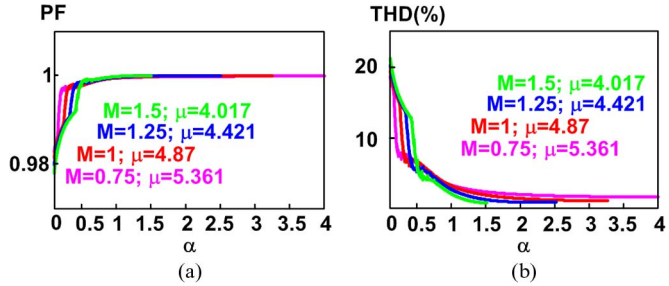

Fig. 6. (a) PF versus α for several flyback optimum PFC designs. (b) THD versus α for several flyback optimum PFC designs.

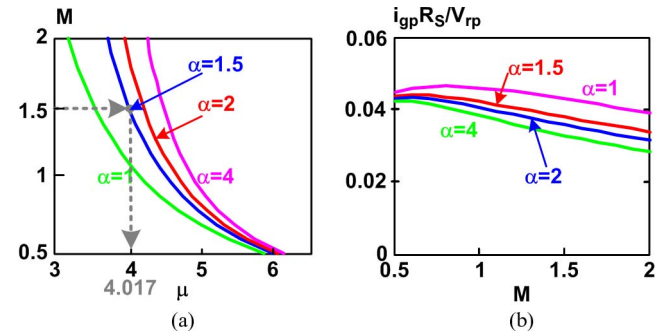

Fig. 7. (a) Values of μ to minimize the THD for different design conditions (M and α). (b) $i_{\rm gp}R_S/V_{\rm gp}$ value as a function of M and α.

A. Design Procedure

The design procedure of a PFC belonging to the flyback family of converters with the proposed control strategy is very simple. The inputs of this design are the output voltage V_o, the peak value of the input voltage $V_{\rm gp}$, and the maximum output power $P_{\rm max}$.

First, M must be calculated from (9) choosing n according to a tradeoff between current and voltage stress in both the power transistor and diode. As in any PFC belonging to the flyback family of converters, the voltage across the main switch must be bounded. This is the main restriction.

Second, α must be chosen. This value should be selected greater than one, which guarantees CCM for the entire line angle at nominal conditions. Once M and α are known, determine the value of μ according to the plot given in Fig. 7(a), which defines the optimum values of μ for different PFC designs. As you can see, the μ factor is between three and six (which means that τ is between three and six times the switching period (T_S)) in order to minimize THD of the input current for many standard designs.

Third, the quotient $V_{\rm rp}/R_S$ must be calculated. For this purpose, a perfect sinusoidal line waveform is assumed ($i_{\rm gp} = 2P_{\rm max}/V_{\rm gp}$), which is a reasonable approach when the right value of μ has been chosen. Thus, the value of $i_{\rm gav}$ at $\omega_{Lt} = \pi/2$ and full load obtained from (11) must be equal to the value of $i_{\rm gp}$ calculated from the power balance. From this equality and taking into account (9) and (18), the value of the quotient $V_{\rm rp}/R_S$ can be easily calculated. To make this calculation even easier, a plot of $i_{\rm gp}R_S/V_{\rm gp}$ as a function of M and α is given in Fig. 7(b). Once the value of $V_{\rm rp}/R_S$ has been calculated, the

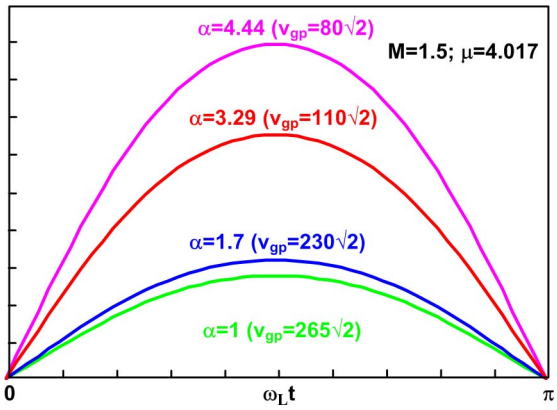

Fig. 8. Normalized line current waveforms for a universal input-voltage design ($\mu = 4.017$, $\alpha = 1$, and $M = 1.5$).

individual values of $V_{\rm rp}$ and R_S can be chosen freely but taking into account that they must be compatible with the controller voltage levels.

Finally, we have to calculate the value of the PFC inductance L. Once the value of the quotient $V_{\rm rp}/R_S$ is known, the value of L can be easily calculated from the definitions of K (8), $K_{\rm crit\_max}$ (16), and α (18).

As was mentioned in the previous section, the distortion of the input current is negligible for α values greater than the design value (Fig. 6). This conclusion is very important and permits the use of this control strategy in the case of PFCs working within the universal range of input voltages. In this case, the design criterion is very simple: The PFC must be designed to have the desired high PF and low THD at the highest nominal input voltage, for example, $M = 1.5$, $\alpha = 1$, and $\mu = 4.017$ in Fig. 8. Note that the PF and THD will have better values at the lowest input voltage because α increases (Fig. 6).

As it is well known, the current control mode is unstable, operating in CCM when the duty cycle is greater than 0.5. To avoid this problem, a compensation ramp is introduced. In this case, the slope of the compensation must be high enough to avoid instabilities. However, in DCM, the current is zero at the beginning and end of each switching period. Therefore, the current is reset at the beginning of the switching period, and no instabilities take place. In the proposed control strategy, the slope of the compensation ramp is constantly changing due to the fact that an exponential ramp is used to reduce the THD of the input current. At this point, the stability of the proposed control strategy must be checked when both $d > 0.5$ and the flyback PFC is operating in CCM. The stability condition is well known applied to flyback

$$m_c = \left.\frac{\partial v_r}{\partial t}\right|_{t=dT_S} > 0.5(m_2 - m_1) = \frac{0.5R_S}{L}\left(v_g - \frac{V_o}{n}\right) \tag{20}$$

where m_c is the slope of the compensation ramp, m_1 is the slope of the inductor current during the magnetizing period, and m_2 is the slope of the inductor current during the demagnetizing period. The stability condition can be normalized by using (6) and (8)–(9)

$$2K\mu e^{-\frac{M}{(M+\sin(\omega_L t))}\mu} > (\sin(\omega_L t) - M)\,(1 - e^{-\mu}). \tag{21}$$

Once (21) is calculated, the stability condition for each flyback PFC design using the proposed control strategy can be easily checked in CCM (i.e., $K > K_{\rm crit}(\omega_t)$) when $d > 0.5$. Mathematical software has been used to check (21) for realistic designs of flyback PFC (i.e., $M = [0, 1.5]$, $K = [K_{\rm critmax}, 4K_{\rm critmax}]$, and $\mu = [3, 6]$). The results show that no instabilities appear operating in CCM. Therefore, this control strategy is stable for any ac–dc HB-LED driver design.

Moreover, this concept can be easily explained that the value of the compensation ramp slope will be always enough to avoid instabilities when the converter is operating in CCM. From Fig. 3(a), it can be easily deduced that the slope of the exponential compensation ramp is higher than m_2 for a value of the duty cycle in the middle range. When the duty cycle tends to unity and the converter is still operating in CCM, then both m_1 and m_2 tend to zero, whereas the slope of the compensation ramp is never zero, due to the selected value of μ (in fact, this slope would be zero only if μ was the infinity). Therefore, instabilities never take place.

B. Implementation of the Proposed Control Strategy in Standard and Low-Cost PCMICs

Summarizing the considerations in Section II, this control strategy can be implemented by using only four blocks: an oscillator, an error amplifier (subtractor included), a pulsewidth modulator, and a ramp generator with its reset. The three first blocks are included in any standard [i.e., UC3824, Fig. 9(a)] or low-cost [i.e., UC3843, Fig. 9(b)] PCMIC for SMPS. Moreover, the ramp generator with its reset can be easily built with a few discrete analog components. The values of the resistors $R_{\rm ramp}$ and the capacitor $C_{\rm ramp}$ have been chosen in order to generate an adequate compensation ramp to minimize the THD of the input current (i.e., defining the optimum μ value). This compensation ramp is an exponential waveform generated by v_A. Due to this fact, the asymptotic value of compensation ramp is equal to v_A, which makes very easy to obtain the desired values of μ [typically in the range of three to six; see Fig. 7(a)]. Therefore, the specific matching circuit that assures OCC operation is extremely simple in the proposed implementation.

Due to fact of being an HB-LED driver, the dc output current (instead of the output voltage) is controlled by the feedback loop [green circuitry in Fig. 9(a)]. A potentiometer $P_{\rm ref}$ is used to change the reference of the current regulator to perform analog dimming. Furthermore, resistors R_{o1} and R_{o2} and transistor Q_o generate an adequate voltage to compensate the chip comparator offset and the base–emitter voltage drop of transistor which generates the compensation ramp (i.e., $Q_{\rm ramp}$). Moreover, using a UC3824, the clock signal must be adapted in order to reset the compensation ramp (C_r and R_r circuit). The values of R_D, R_{F1}, $R_{\rm CL1}$, and $R_{\rm CL2}$ and the values of C_{F1},

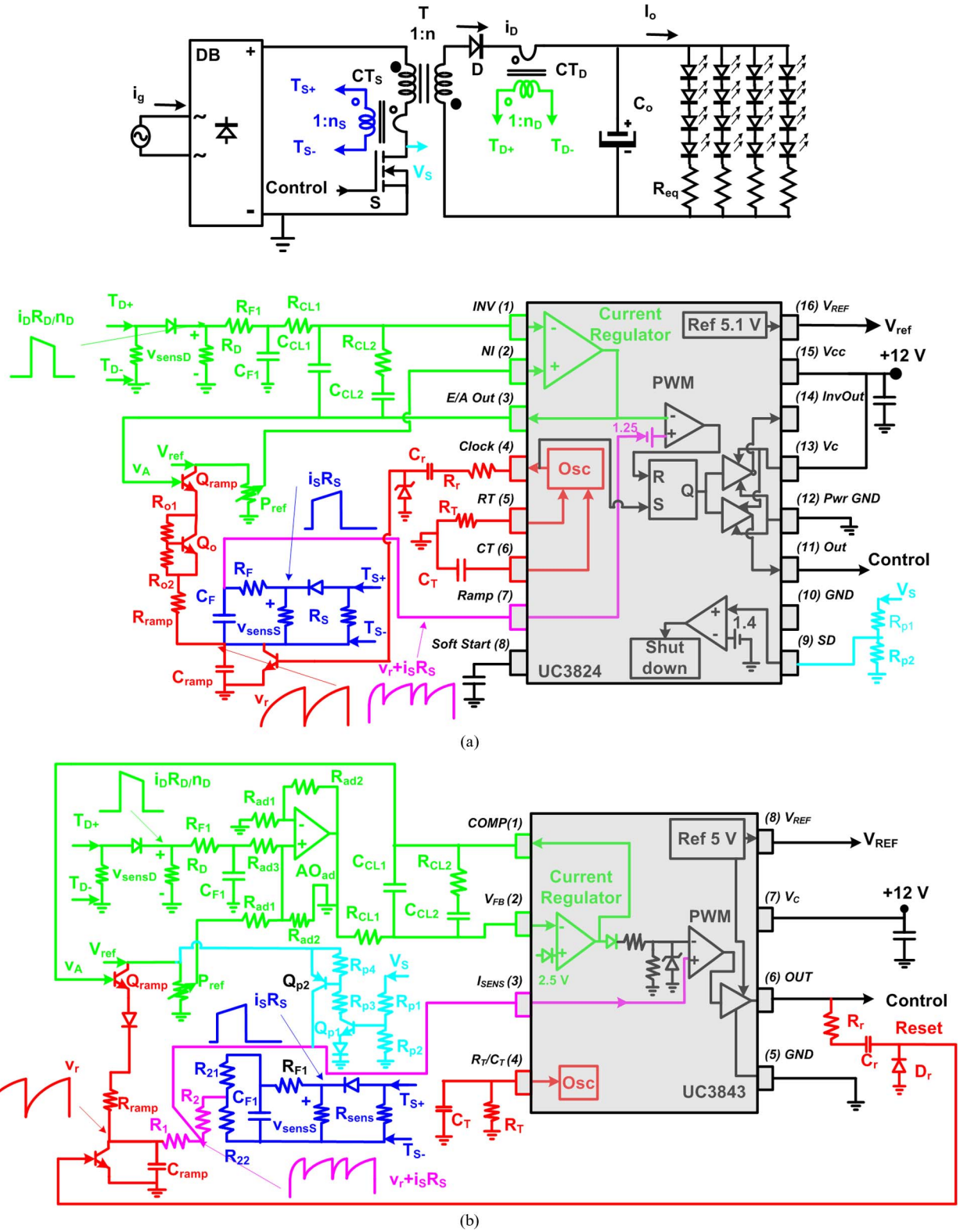

Fig. 9. Two possible implementations of the proposed control strategy with commercial PCMIC. (a) UC3824. (b) UC3843.

C_{CL1}, and C_{CL2} complete the output current feedback loop. Finally, a protection circuit (resistors R_{p1} and R_{p2}) has been implemented to detect open circuit operation at the output due to an HB-LED failure. It should be noted that this protection circuit is needed because the converter operates as a current source.

Another possibility is to use a standard PCMIC with a minimal external-part count (i.e., UC3843) in order to reduce to cost of the ac–dc HB-LED driver [Fig. 9(b)]. These kinds of ICs present some drawbacks to implement this control strategy: The pin for clock signal is not available, the reference of the voltage regulator is a constant value, and the pin for circuitry

TABLE I
LIST OF COMPONENTS OF THE EXPERIMENTAL PROTOTYPE

Fig. 9 reference	Value	Description
S	STP4NA80	MOSFET 4A; 800V
D	8TQ100	Schottky100V 8A
DB	GBU8J	Diode bridge 600V;4A
T	RM14 N47 material	50:5 turn ratio L_m=1.15 mH
C_o	200 µF 25 mF	2x10µF MKT 100V 1x10000 µF elect. 25V 1x15000 µF elect. 25 V
CS_D, CS_T	RCC12.5/5 3F3 material	1:50 turn ratio

protection is not available. Therefore, dimming operation seems not to be possible. However, these drawbacks can be overcome [Fig. 9(b)]. The clock signal needed to reset the compensation ramp can be obtained from a derivative circuit connected to the output (C_r, R_r, and D_r). With resistors R_{p1}, R_{p2}, R_{p3}, and R_{p4} and transistors Q_{p1} and Q_{p2}, a protection circuit can be built to detect open circuit operation at the output. Finally, the adder circuit implemented using the operational amplifier A_{Oad} allows a control of the output current level and, therefore, dimming operation.

IV. EXPERIMENTAL RESULTS

A prototype of a flyback PFC as an ac–dc HB-LED driver was built and tested. It was controlled by the proposed control strategy which was implemented using a commercial PCMIC (UC3824). The circuit has been performed according to the scheme shown in Fig. 9(a), and the components are detailed in Table I. The converter output is connected to four strings of four HB-LEDs LXK2PW14T00 (Luxeon). A simple resistor (0.33 Ω/6 W) has been used to equalize the current of each string [Fig. 9(a)]. This method of driving multiple strings of HB-LEDs introduces additional power losses. In order to solve this drawback, other equalization methods can be used decreasing power losses generated by the equalization circuit [22]. It should be noted that the converter has been designed for analog dimming which is simpler than other dimming techniques and therefore the most adequate for low-cost applications [23]. The main drawback is that the peak emission wavelength of HB-LEDs tends to shift with the forward current, which can lead to color variations. However, this problem only imposes significant challenge when the HB-LEDs are used for applications where color stability is of primary concern (liquid crystal display). The rated operating conditions of this converter are as follows: $v_{\mathrm{gRMS}} = 110$ V, $I_o = 2{-}0.8$ A, $P_g = 30{-}10$ W, and $V_o = 14{-}13$ V.

The control circuitry has been designed to obtain a high PF value just when the converter stabilizes its temperature (HB-LEDs at room temperature). Fig. 10 shows the evolution of the PF, the THD, and the HB-LED temperature (measured on the heat sink at 3 mm from one HB-LED lead) during the warm-up process. As this figure shows, the final operation temperature is reached after 70 min of operation. During the warm-up process, the voltage across the HB-LEDs becomes

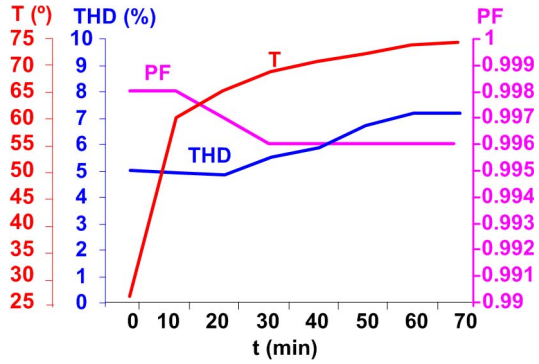

Fig. 10. Evolution of the PF, THD, and temperature during the warm-up process.

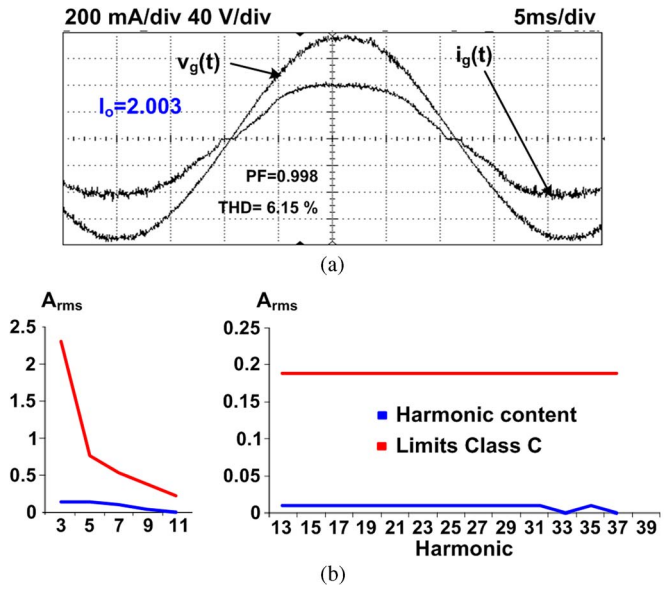

Fig. 11. (a) Line current at the end of the warm-up process. (b) Harmonic content of the ac–dc HB-LED driver prototype.

lower, and therefore, the power handled by the converter decreases. Due to the very simple control circuitry proposed, the line current remains more or less constant during the warm-up process. This fact is reflected in the evolution of the PF and THD, which change from 0.998 and 5.1 (at the beginning of the warm-up process) to 0.996 and 7.8 (at the end of this process), respectively. Fig. 11(a) shows the line current waveform corresponding to the end of the warm-up process. The harmonic content at the end of the warm-up process is shown in Fig. 11(b), where it is compared with the limits imposed by the EN 61000-3-2 regulation in Class C. As this figure shows, the prototype complies with the aforementioned regulations.

Fig. 12 shows the experimental waveforms of the line current obtained in analog dimming operation when the currents across each string are 0.4, 0.3, 0.2, and 0.1 A, corresponding to output currents of 1.6, 1.2, 0.8, and 0.4 A. The dimming operation is performed by changing the position of the potentiometer P_{ref}. These figures show that the experimental PF (black color) is very high in all operating conditions. Also, the experimental results have been compared with the theoretical ones (in red

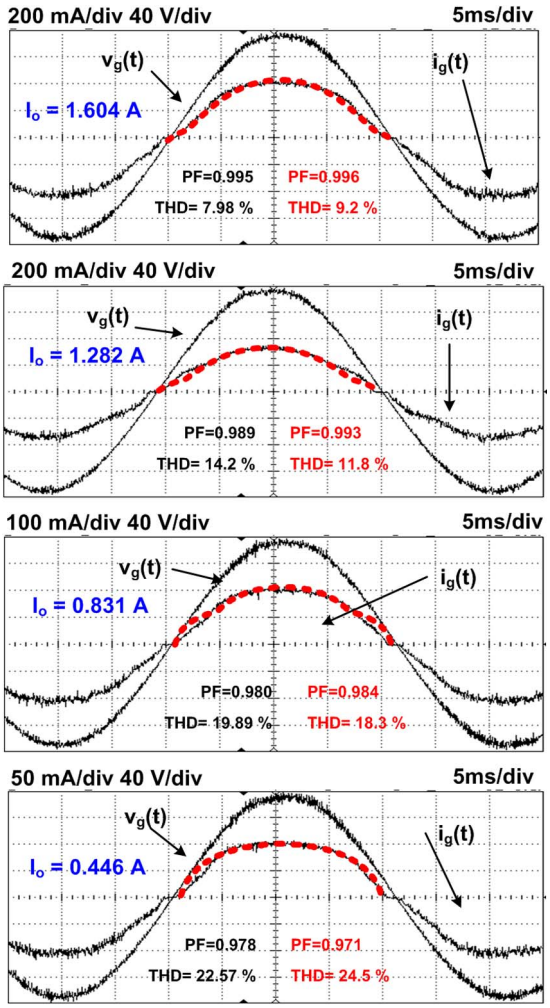

Fig. 12. Line current during dimming operation.

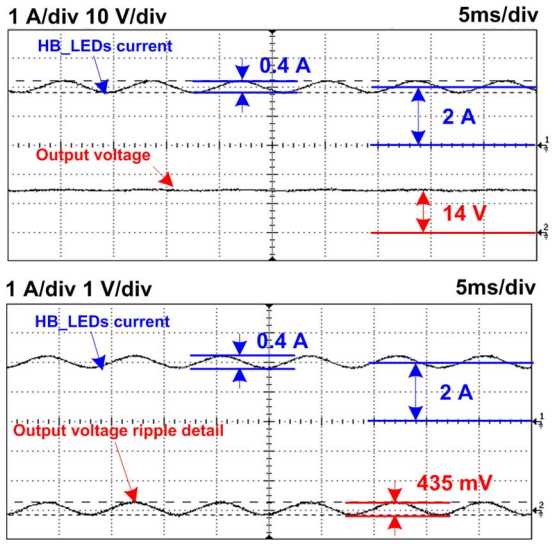

Fig. 13. Output voltage and current through the HB-LEDs.

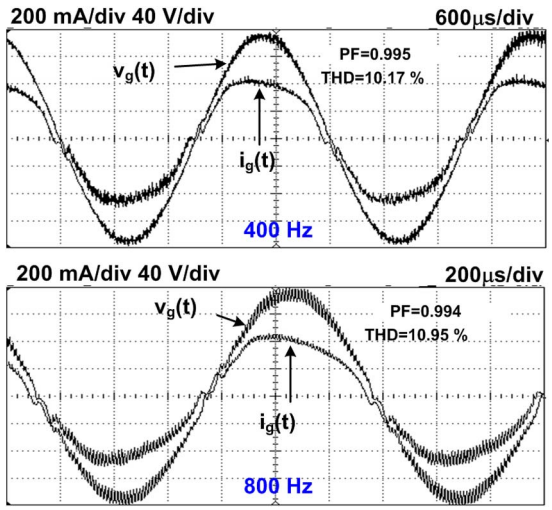

Fig. 14. Line current for different line frequencies.

color). As you can see, the theoretical waveforms match with the experimental ones. Moreover, the PF and THD results, both experimental and theoretical, are very close.

Fig. 13 shows the output voltage and the current through the luminaire formed by four strings of HB-LEDs. As can be seen, a significant low-frequency ripple appears in the output current. As it is known, this is due to the energy transfer process of PFCs used as a one-stage PFC. The only way to reduce this ripple is to increase the output capacitance. Therefore, the electrolytic capacitor cannot be removed, and the lifespan of the ac–dc HB-LED driver is reduced. However, this is the price to pay of using a simple and low-cost solution for designing an ac–dc HB-LED driver.

Another interesting feature of the proposed control circuitry is its ability to operate with high-frequency lines (like the 400-Hz line used in avionics). This is due to the fact that the peak-current-mode control provides cycle-by-cycle control of the input current. The results obtained for different line frequencies are given in Fig. 14.

V. Conclusion

A new method to control PFCs belonging to the flyback family of converters has been presented in this paper. The method is based on the use of standard PCMICs without multiplier. In fact, this method is an alternative implementation of the OCC to the PFCs belonging to the flyback family of converters. Only an exponential compensation ramp is used in order to reduce THD. As a consequence of its simplicity, the input current at different operation points to the nominal one is slightly distorted. Moreover, the input-current feedback loop is extremely fast, which allows us to use this type of control with relatively high-frequency lines.

This control strategy applied to single-stage PFCs makes sense in the case of relatively low-power and wide-input-voltage-range applications, such as ac–dc HB-LED drivers. However, the application of this control strategy to PFC belonging to the flyback family of converters is not obvious. Both the static analysis of this control strategy and the design-oriented considerations about its implementation in PCMIC have been provided. Finally, an experimental prototype has validated all theoretical results presented in this paper.

APPENDIX
DESIGN CONSIDERATIONS OF THE OUTPUT CAPACITOR IN CONVERTERS BELONGING TO THE FLYBACK FAMILY OF PFCS

There are limits in the design of the output capacitor in PFCs belonging to the flyback family of converters. It is known that the output capacitor of PFCs balances the pulsating input power and the dc output power. A large capacitance is needed, and therefore, an electrolytic capacitor is often used. This makes it quite bulky, and its size increases as either a low voltage level or a very low output voltage ripple is specified for a given power. Capacitor size is a further limitation for the use of a flyback PFC as a one-stage solution to design a complete ac–dc power supply due to the fact that this capacitor is the output capacitor of the power supply [24], [25].

Also, the lifetime of the electrolytic capacitor is very limited due to its liquid electrolyte. This fact can be another obstacle to the design of an ac–dc power supply for long-lifetime loads, for example, ac–dc HB-LED drivers. Some authors have presented solutions to replace this electrolytic capacitor by other technology (i.e., MKT, MKP, and ceramic). However, these solutions are suitable for ac–dc power supplies based on two-stage structures [26], [27]. The first stage is a boost PFC that draws a sinusoidal input current allowing relatively high low-frequency output-voltage ripple. In this case, the output capacitance can be reduced, and a nonelectrolytic capacitor is used. The second stage both gives galvanic isolation and reduces the low-frequency output-voltage ripple to adequate the output voltage to HB-LEDs. However, in the case of a flyback PFC, the electrolytic capacitor cannot be replaced by other technologies because the increase of the size and cost of the output capacitor becomes unaffordable. Therefore, the only solution is to increase the lifetime of the output electrolytic capacitor. Next, we are going to evaluate the limits of the commercial electrolytic capacitors.

Lifetime models of electrolytic capacitors are composed by some datasheet parameters given by manufacturers and some operation stresses defined by application as temperature, ripple current, and applied voltage. The most common structure of a lifetime model is the following [28]:

$$L_X = L_0 \cdot K_T \cdot K_R \cdot K_V \tag{A1}$$

where L_0 is the nominal lifetime, K_T is the temperature factor, K_R is the current ripple factor, and K_V is the voltage factor.

L_0 is the lifetime of the electrolytic capacitor for given ambient temperature, ripple current, and voltage. These data are given by manufacturers in their datasheets. The typical nominal lifetime of an electrolytic capacitor is 12 000 h at 85 °C. However, nowadays, manufacturers present long-lifetime capacitors useful at 140 °C, which present L_0 greater than 15 000 h at 85 °C (e.g., B41692 and B41792 of EPCOS [29]).

K_T defines the effect of temperature in the lifetime of electrolytic capacitors. The manufacturers establish the well-known Arrhenius law: A drop of the ambient temperature by 10 °C doubles the lifetime

$$K_T = 2^{\frac{T_0 - T_a}{10}} \tag{A2}$$

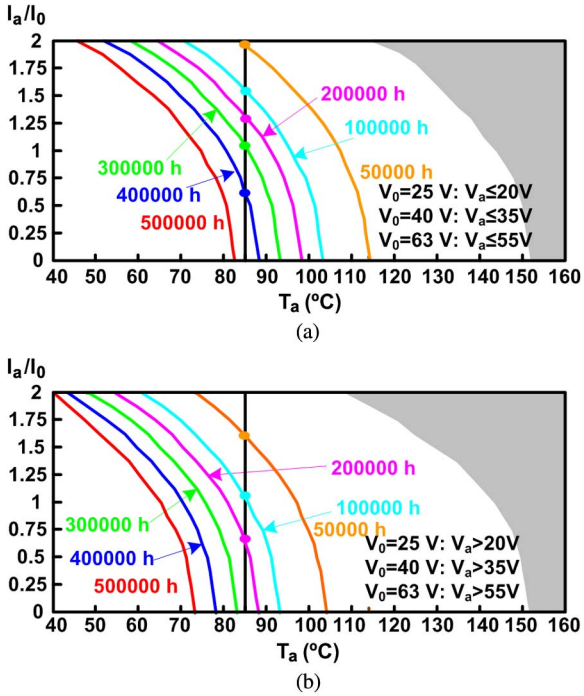

Fig. 15. Parameterized lifetime diagrams for EPCOS series B41692 and B41792. (a) With derating voltage. (b) Without derating voltage.

where T_0 is the rated temperature given by manufacturers in the datasheets and T_a is the ambient temperature.

K_R defines the impact of the applied ripple current on the self-heating of the electrolytic capacitor and, therefore, on its lifetime. K_R depends on the ratio between the ripple current of the application (I_a) and the nominal ripple current established by manufacturers in datasheets (I_0). Different manufacturers define different K_R models in their products, but all of them coincide in the same point: Operating ripple currents below the rated ripple current (i.e., $I_a/I_0 < 1$) cause less temperature stress in electrolytes. This fact may extend the lifetime of electrolytic capacitors (i.e., $K_R > 1$). The frequency dependence of the ripple current is taken into account by correction factors given by manufacturers in their datasheets.

K_V estimates the influence of the applied voltage in the lifetime of electrolytic capacitors. In fact, K_V is a multiplier for voltage derating. In other words, if the applied voltage (V_a) is lower than the rated voltage specified by manufacturers in datasheets (V_0), then the stress in the dielectric layer decreases. This fact makes less consumption in the electrolyte by self-heating, and therefore, the lifetime of the electrolytic capacitor is increased (i.e., $K_V > 1$).

To provide the users of their products with some useful tools for the lifetime estimation of electrolytic capacitors, manufacturers provide lifetime diagrams to simplify the calculation. These lifetime diagrams consider the aforementioned model and show permissible combinations of model parameters (i.e., T_0, I_a/I_0, and V_a/V_0) graphically. Fig. 15(a) and (b) shows these lifetime diagrams. As you can see, lower values of I_a/I_0, V_a/V_0, and T_0 increase the lifetime of electrolytic capacitors.

Now, the idea is to investigate the increase of lifetime commercial capacitors by minimizing their stresses (i.e., decreasing

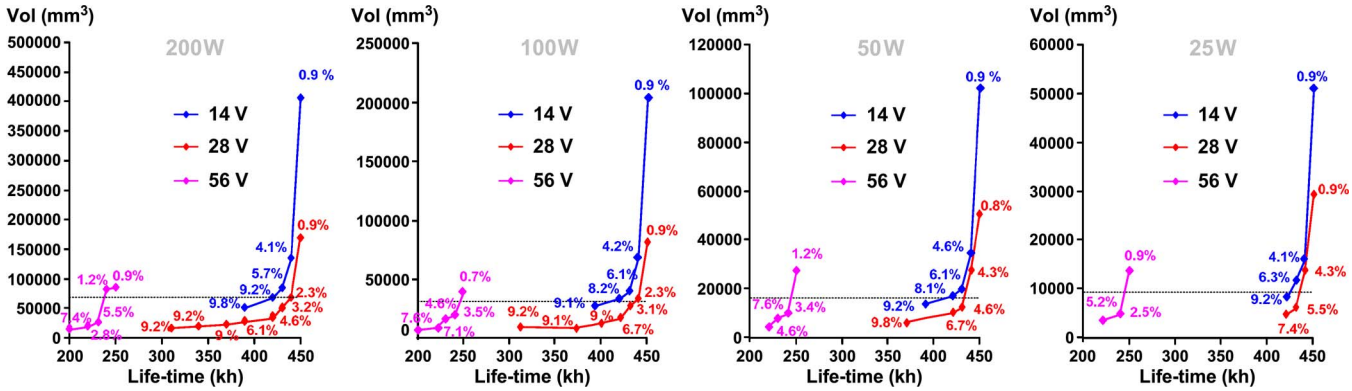

Fig. 16. Minimum volume of commercial capacitors versus the lifetime for some output power processed by the flyback PFC and some output voltages.

I_a/I_0, V_a/V_0, and T_a and increasing K_R, K_V, and K_T factors). In our study, T_0 is constant and equal to 85 °C, which is the ambient temperature specified in HB-LED applications. Decreasing I_a/I_0 factor implies either to increase I_0 or to decrease I_a by putting some capacitors in parallel. Both actions imply a size increase in the electrolytic capacitor. Also, the size of the electrolytic capacitor increases as either the applied voltage decreases (V_a) for a given power or the rated voltage increases. In other words, the size of the electrolytic capacitor increases as the capacitor is maximized to derate its lifetime.

A commercial series of electrolytic capacitors was investigated: B41692 and B41792 of EPCOS [29]. Capacitor exploitation factor (EF) was considered in this study [24], [25]. This concept is closely related to the fact that commercial capacitors have capacitance values and rated voltage values that vary in discrete steps. Therefore, the closer the design values to the commercial values are, the lower the size of the storage capacitor is. For this reason, 25-, 40-, and 63-V electrolytic capacitors were selected for output-voltage applications of 14, 28, and 56 V, respectively (corresponding to strings of 4, 8, and 16 HB-LEDs). A sinusoidal output-voltage ripple was considered in order to simplify the study. Also, maximum 10% output-voltage ripple is defined. Furthermore, the output power range defined for this study is between 25 and 200 W.

Let us explain how the optimization process of minimization of the commercial capacitor volume is. The output capacitance of the flyback PFC is calculated for each output power, output voltage, output-voltage ripple, and lifetime. The maximum capacitance and maximum diameter of the commercial electrolytic capacitor are selected for each rated voltage. First, the number of commercial capacitors necessary to obtain flyback PFC capacitance is calculated according to the EF. Then, these capacitors are tested against output current. If output current is greater than the level specified by the commercial capacitors, then higher number of lower capacitors in parallel should be used. As a consequence, each single capacitor has smaller capacitance and diameter to comply with the output current values.

Finally, Fig. 16 describes the minimum volume of commercial capacitors versus lifetime for different output voltages (solid lines). Each graph has been drawn for different output powers processed by the flyback PFC. The volume of the flyback PFC magnetic component is included in the plots (dotted lines) as reference to compare the volume of the output capacitor for each particular power supply design. This will help to decide when the capacitor volume is excessively high. ETD cores were used for the magnetic component designs. Each magnetic component design depends on the choice of the boundary between the CCM and DCM: 33% of the power processed in our case. All the capacitor designs are highlighted by points in each graph. As you can see, each design introduces an output-voltage ripple. In addition, the graphs in Fig. 11 highlight a number of important conclusions.

1) The capacitor volume lines show that high lifetime capacitor designs, in the range of 25–200-W output power, are possible at 85 °C for flyback PFCs: around 200 000 h for 56-V output voltages and around 400 000 h for both 28- and 14-V output voltages. Also, the volume of these designs is reasonable in comparison to the magnetic component (dotted lines). The main drawback of these designs is their cost because these long useful life capacitor series are more expensive than traditional electrolytic capacitors.
2) The lifetime of the output capacitor depends strongly on the output voltage of the flyback PFC and does not depend on the output power. As you can see, the maximum lifetime achieved at 56-V output voltage is 250 000 h. However, the maximum lifetime achieved at either 28- or 14-V output voltage is 450 000 h. This is due to the fact that the output capacitors at low output voltage can be highly derated. Therefore, lower V_a/V_0 factor can be achieved introducing greater voltage multipliers in the lifetime model (K_V). This concept can be easily explained in Fig. 15. The maximum lifetime achieved at 85 °C depends on the derating of the output voltage: 450 000 h with output-voltage derating [Fig. 15(a)] and 250 000 h without derating [Fig. 15(b)].
3) The capacitor volume lines show an asymptotic lifetime value not dependent on the output power: 250 000 h for 56-V output voltage and 450 000 h for both 28- and 14-V output voltages. This means that the output capacitor of flyback PFC cannot be infinitely derated in order to increase its lifetime (e.g., either using more small capacitors in parallel or using higher rated output-voltage capacitors).

4) The asymptotic lines of capacitor volume versus the lifetime show optimum designs at the zone of slope change. Each design in the diagram is defined by an output-voltage ripple. Therefore, an optimum lifetime design at 56-V output voltage must be done with a specification of the output-voltage ripple between 2% and 3%. In the case of 14- and 28-V output voltages, the output-voltage-ripple specifications are between 4% and 5% and between 3% and 4%, respectively. Also, the capacitor volume and the magnetic volume are very close in the design zones for the 14- and 28-V output voltages. However, capacitor volume is lower than the magnetic volume in the design zones for the 56-V output voltage.

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