A linear assisted DC/DC converter for Envelope Tracking and Envelope Elimination and Restoration applications

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***Abstract*—In recent years, there has been a great effort in the development of fast and efficient DC/DC converters in order to follow the envelope of communication signals for increasing the efficiency of Radio Frequency Power Amplifiers by using techniques such as Envelope Tracking and Envelope Elimination and Restoration. However the bandwidth and slew-rate required by modern communication signals are higher than the maximum ones achievable by switching DC/DC converters made for this purpose. The slew-rate of these switching DC/DC converters can be improved by combining it with the use of a linear stage, thus establishing a trade-off between slew-rate and overall efficiency. This paper presents a simple way of combining the use of both a switching DC/DC converter, the Multiple Input Buck Converter, and a linear stage to obtain slew-rates above 100 V/μs, with a moderate decrease in the overall efficiency (81% efficiency tracking the envelope of an EDGE standard signal). Finally, a prototype of the complete system (including the digital control for both stages) is presented in this paper.**

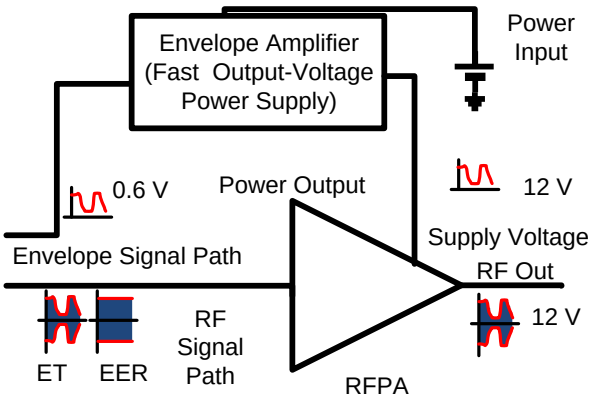

Fig. 1: Scheme of the ET/EER techniques

I. Introduction

MODERN communication standards employ signals which present phase and envelope variations, which require a linear amplifier in order to achieve the power levels required to be transmitted. As is well known, the efficiency of linear RF Power Amplifiers (RFPAs) is very low so there is a great effort to increase their efficiency or to replace them with more efficient amplifiers.

On the one hand, the Envelope Tracking (ET) technique has been proposed to improve the efficiency of a linear RFPA by adapting the power supply voltage of the RFPA to the peak value of RF voltage at the drain of the RFPA main transistor [1]. Envelope Elimination and Restoration (EER) [2] employs a non linear high-efficiency RFPA that processes a constant envelope and phase modulated signal. The information on the envelope is supplied by varying the supply voltage of the non-linear RFPA. With the appropriate control, the overall system behaves like a high-efficiency linear amplifier. The scheme of Fig.1 describes correctly ET and EER techniques, the only difference between them being that the RFPA is a linear amplifier in the case of the ET technique while a switching mode amplifier (Class D, Class E or Class F) is employed in the case of the EER technique. Thus the signal in the RF signal path, just at the input of the RFPA, is a non-constant envelope, phase modulated RF signal in the case of ET technique while it is a constant envelope, phase modulated signal in the case of the EER technique. The power converter is often known as Envelope Amplifier and can be linear, switching or a combination of both. Other approaches, similar to ET, do not try to reproduce the envelopes with great accuracy, but try to adapt the supply levels to the neeeds of the transmitter under different requirements (different transmission speeds (for voice or data) require different power levels [3]).
This power supply has to reproduce the envelope of a communications signal. When only a switching mode DC/DC converter is used as power supply, the slew-rate of the supply voltage is limited to a few V/μs. However, a slew-rate in the range 100 V/μs (or even higher) is required in some cases. This slew-rate can be achieved by combining the use of this switching DC/DC converter with a linear stage, thus establishing a trade-off between slew-rate and overall efficiency. This trade-off is due to the fact that the linear stage works on the fast transients where the switching stage cannot behave correctly. The linear stage has low efficiency, but since it has to process low power, the overall efficiency can remain high. Figure 2 shows a general scheme of this idea.

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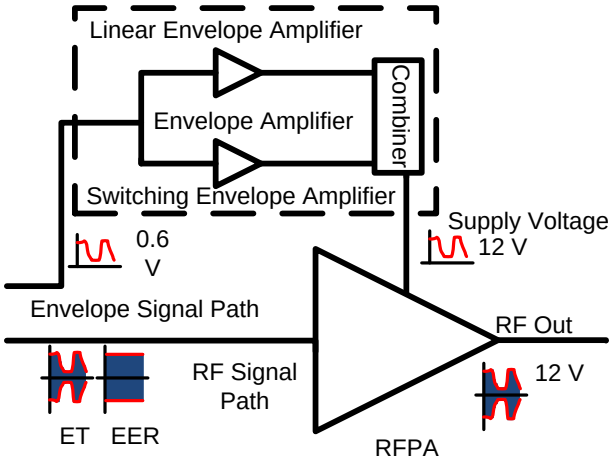


Fig. 2: Scheme of the ET/EER techniques with linear assisted Envelope Amplifier

As has been mentioned, some of the signals used in modern communications (WCDMA, OFDM, EDGE, etc) require higher slew-rates and bandwidths than the ones that are achieved by current switching-mode DC/DC converters ([4]–[7]). As has already been stated [1], the main part of the power of many communication envelope signals is placed in the lowest part of the spectrum. Thus with a high-efficiency switching DC/DC converter reproducing the most of the power, placed at the lowest frequencies, the linear stage only has to process a low power, and then the efficiency of the overall system remains high. Several combinations of switching mode DC/DC converters and linear stages have been proposed to achieve a good trade-off between efficiency and slew-rate and bandwidth ([8]–[11]).

Thus a series combination of switching and linear stages has been presented in [11]. In this case, the bandwidth and the slew-rate obtained meet the requirements, but as all the current flows through the linear stage there are always losses in it. Parallel combinations of switching and linear stages have also been proposed [8], with the linear stage controlling the switching stage (a Buck converter). Other approaches [9] employ a band separation scheme, which strongly depends on the modulation employed, or needs a complex control [10]. Recently, a DC/DC converter (named Multiple Input Buck Converter, MIBuck [6]) has been proposed for envelope amplifier. Excellent efficiency (92% at 4.6 MHz of switching frequency) and small output voltage ripple (0.2%) can be achieved using this converter. The slew-rate obtained is about 6 V/μs. In order to achieve slew-rates in the range of 100 V/μs, the MIBuck converter must be combined with a linear stage. The Parallel-connected solution proposed in [8] for the Buck converter cannot be easily implemented for the case of the MIBuck converter. Therefore, a new method to combine the switching stage (MIBuck) and a linear stage in parallel must be developed, which is the main objective of this paper.

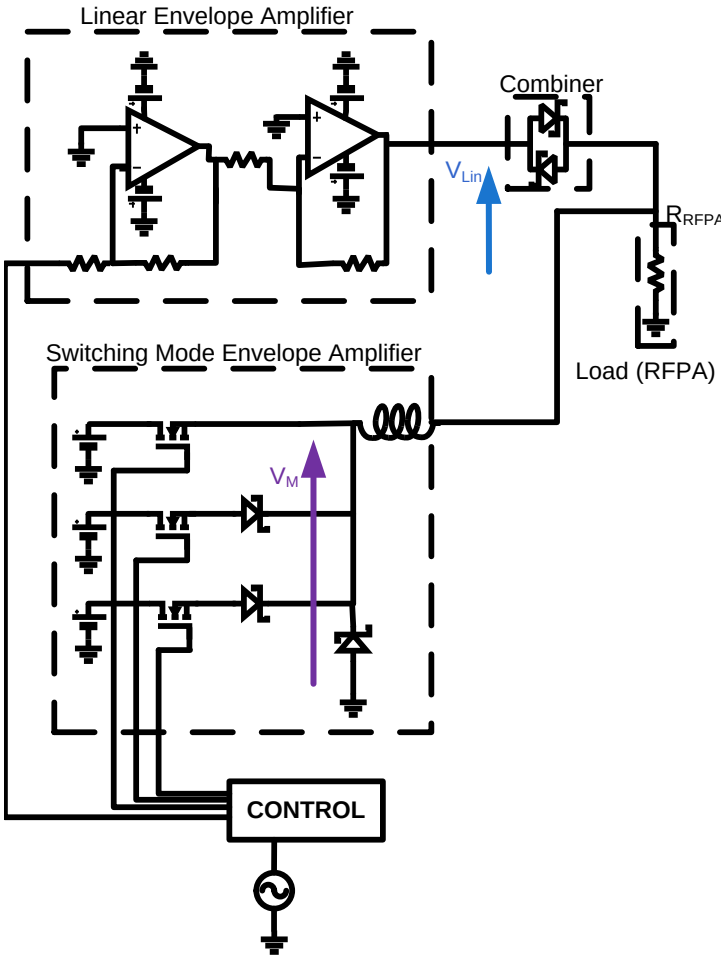


Fig. 3: Proposed schematic

II. Proposed Architecture of the System

A. Principle of Operation

As can be seen in Fig.3, the linear stage is placed in parallel to the load as in [8], but it does not control the switching stage, thus both stages are independent. The other main difference, and the key point of this design, are the diodes in antiparallel placed between the load and the linear stage, which are the combiner block in Fig.2 and in Fig.3. The signal generator depicted in Fig.3 generates the envelope of a communication signal while the resistor placed as the load of the DC/DC converter represents the RF Power Amplifier (RFPA).

The main idea is that the MIBuck and the linear stage try to give the same voltage to the load, following a common reference. However, the MIBuck have more limited slew-rate and bandwidth than the linear stage due to its low-pass output filter, which is performed by the inductor L and the load (in fact, a LC filter whose capacitor is the decoupling capacitor $C_{Decoupling}$ in Fig.4a). Taking into account its inherent more limited speed (explained in section III), the voltage reference given to the MIBuck control is a bandwidth-limited version of

the reference given to the linear stage. The higher frequency of this reference is $f_{ref\_M\_max}$. This bandwidth-limited reference can be perfectly reproduced by the MIBuck because the cutoff frequency of its low-pass output filter $f_{cutt\_off\_M}$ is much more lower than the switching frequency f_{SW}. In summary, the relationship among $f_{ref\_M\_max}$,$f_{cutt\_off\_M}$ and f_{SW} is the following:

$$f_{ref\_M\_max} < f_{cutt\_off\_M} << f_{SW}. \tag{1}$$

The overall system operation strongly depends on the bandwidth of the signal to be reproduced. The first case corresponds to a signal with maximum bandwidth f_{max} lower than $f_{ref\_M\_max}$. In this case, it is clear that the signal will be faithfully reproduced at the MIBuck output. Therefore, the voltage V_{RFPA} over the load is equal to the average value of V_M in a switching period, $\langle V_M \rangle_{T_{sw}}$:

$$V_{RFPA} = \langle V_M \rangle_{T_{sw}}\,. \tag{2}$$

In this case, the linear stage also generates a faithful reproduction of the reference signal due to its superior speed and, therefore, its output voltage V_{Lin} is also equal to V_{RFPA}:

$$V_{Lin} = V_{RFPA}. \tag{3}$$

This situation has been depicted in Fig.4c.

However, all the current demanded by the load comes from the MIBuck, because no current can be supplied by the linear stage due to the real characteristics of the diodes placed in the combiner. In fact, the ideal diodes placed in series with the knee voltage sources V_γ are reversed biased by these voltage sources. In summary, no power is supplied at all by the linear stage and all the power comes from the switching stage, thus achieving high efficiency in this case.

The second case corresponds to a signal with maximum bandwidth f_{max} higher than $f_{ref\_M\_max}$. In this case, only the linear stage can generate a faithful reproduction of the reference signal due to its superior bandwidth and, therefore, V_{RFPA} will be determined by the linear stage and by the knee voltage sources V_γ as follows:

$$V_{RFPA} = \begin{cases} V_{Lin} - V_\gamma & \text{when } I_{Lin} > 0 \\ V_{Lin} + V_\gamma & \text{when } I_{Lin} < 0, \end{cases} \tag{4}$$

being I_{Lin} the current through the linear stage. As the value of V_γ is relatively low (especially if Schottky diodes are used), V_{RFPA} is very similar to V_{Lin}, thus having a overall system bandwidth determined by the linear stage.

In this case, $\langle V_M \rangle_{T_{sw}}$ is not a faithful reproduction of the reference signal due to the inherent speed limitation (see Fig.4d). The current supplied for the MIBuck will depend on the waveforms of V_{RFPA} and $\langle V_M \rangle_{T_{sw}}$ and on the value of the inductor L, according to Faraday's Law. The remainder load current will be supplied by the

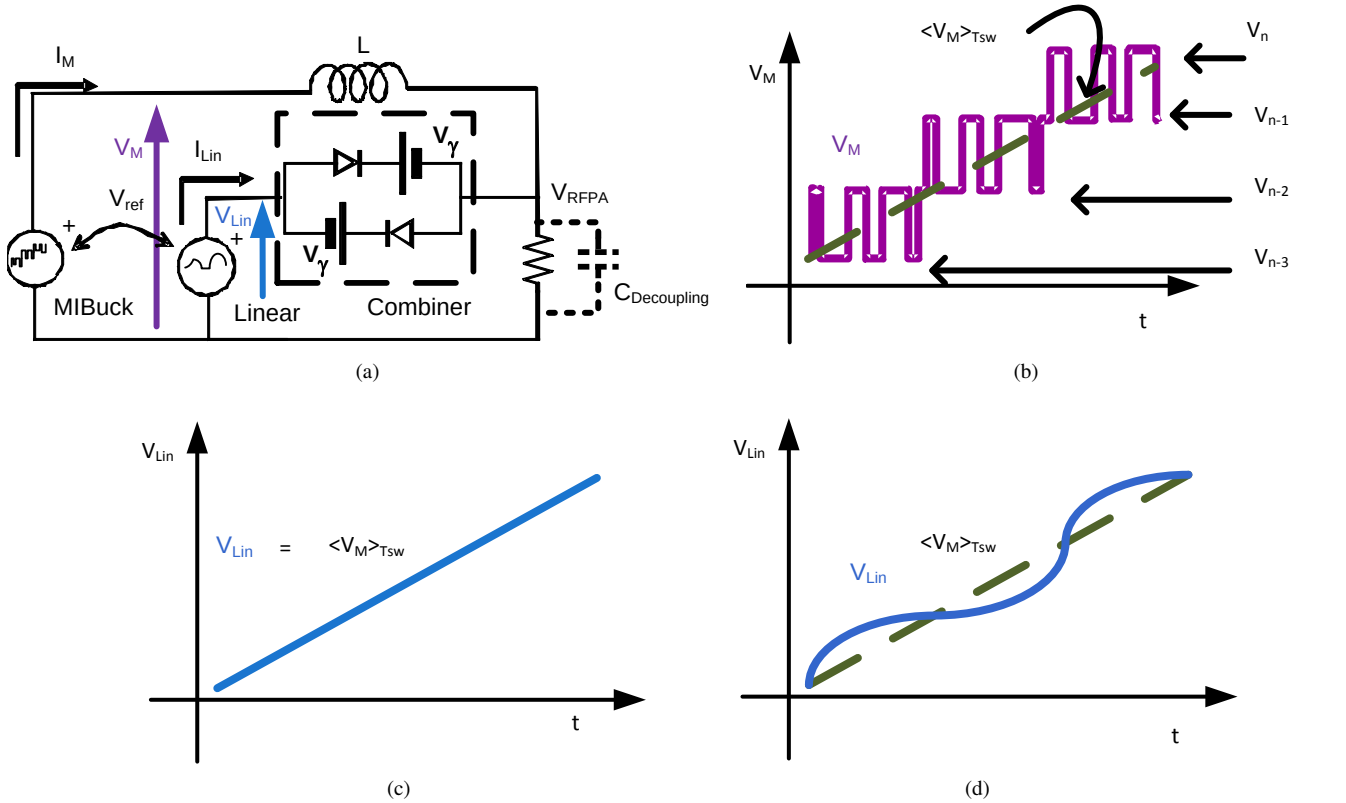


Fig. 4: (a) Behavioral Model. (b) Voltage in the switching node. (c) Voltage of the linear stage when the MIBuck can reproduce the reference. (d) Voltage of the linear stage when the MIBuck cannot reproduce the reference.

linear stage. In this case, the overall efficiency will be lower due to the part of the total power processed by the linear stage.

Figure 5 shows the idealized waveforms under a pulse in the reference voltage. The sharp edges of the pulse cannot be followed by the output current of the switching stage, I_M, due to the aforementioned MIBuck limitations in bandwidth and slew-rate. Then the linear stage provides the current necessary to make the output voltage follow the reference, with the only limitation that the voltage V_{RFPA} is the voltage provided by the linear stage, V_{Lin}, minus V_γ, according to (4). When the current of the switching stage I_M reaches the load current, the corresponding diode stop conducting and the linear stage does not apport any current. When the voltage in the reference drops, the excess of current provided by the inductor L is absorbed by the linear stage and then the voltage V_{RFPA} is V_{Lin} plus V_γ, also according to (4). Therefore the linear stage provides the current necessary in the fast transients, allowing better slew-rates than the switching stage.

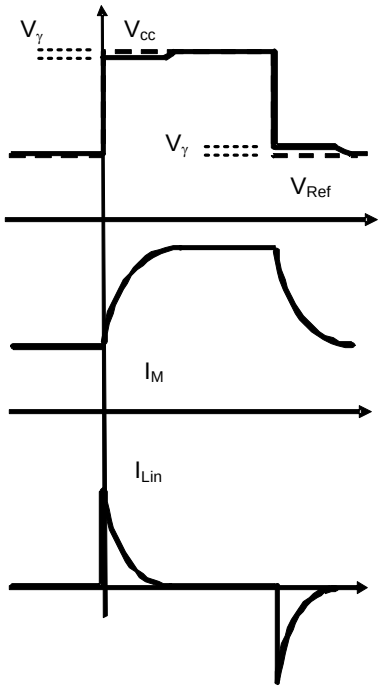


Fig. 5: Idealized waveforms

B. Linear stage

The linear stage (or linear envelope amplifier in Fig.3) is built around fast response, high-power operational amplifiers. These Op-Amp are commonly used in video distribution and can provide a significant amount of power over a wide bandwidth. There are two kinds of Op-Amps in this linear stage. The first one is a voltage amplifier and the second one is a current amplifier. The current through the first Op-Amp is low so there is not a lot of power dissipated and there are no special constraints about its design. The Op-Amp selected is a THS4001 from Texas Instruments. It is configured as an inverting amplifier. The values of the resistors are set up to provide the same voltage gain as the switching stage.

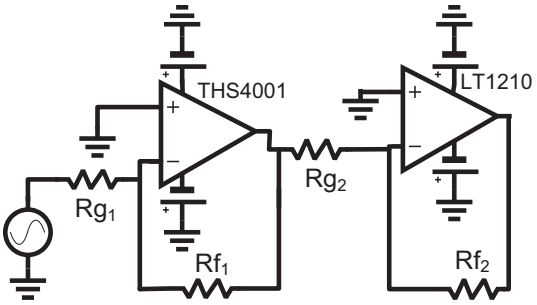


Fig. 6: Linear Stage schematic

The second one is a high power, high bandwidth Op-Amp. It provides current amplification and it is the main responsible for the efficiency of the linear stage, because it drives the highest current at the highest voltage. The amplifier selected is the LT1210 from Linear Technologies. It should be noted that the LT1210 is a Current Feedback Amplifier (CFB). As all of the CFBs, its slew-rate and bandwidth depend strongly on the feedback resistor R_{f2}. According to the manufacturer, the best results are obtained by configuring the Op-Amp as an amplifier with a gain of -1 with a resistance of 604 Ω. This is the reason why the first Op-Amp is also configured as an inverting amplifier. Moreover, the LT1210 is asymmetrically supplied in order to reduce the losses, taking into account that the envelopes of the signals are strictly positive. The positive supply voltage is set to 15 V, but the negative supply voltage can be set from -1.2 V to -15 V to ensure a good behavior. The higher the negative value of this voltage, the lower efficiency, but the higher slew-rate with a negative slope. A voltage of -3V were used for some of the tests.

C. Switching Stage

The switching stage is a Multiple-Input Buck Converter, fully described in [6], see Fig.7. It is based on the well known Buck converter, but each transistor switches between two near voltages (see Fig.4b), so switching losses are minimized and the switching frequency can be increased, allowing the capacity of reproducing fast varying signals.

The only difference between the MIBuck described in [6] and the one implemented here is that there is no output capacitor (only the decoupling capacitor $C_{Decoupling}$ of the RFPA is present). If the MIBuck output capacitor had not been removed, then it would have represented a capacitive load for the linear stage, which would have meant a limitation on both the bandwidth and the slew-rate.

The MIBuck input voltages are 12 V, 8 V and 4 V, allowing the output voltage to reach almost 12 V. The switching frequency is set up to 4 MHz but this frequency can be lowered thus increasing the efficiency and decreasing the switching stage bandwidth. It is important to remark that the MIBuck must be designed to operate in Continuous Conduction Mode

(CCM) to simplify its control. The process to calculate the inductor needed to maintain the operation in CCM can be found in [6], as well.

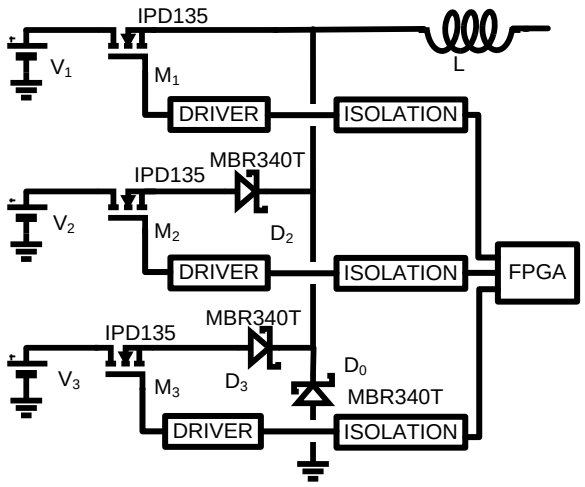


Fig. 7: Switching stage schematic

D. Combiner

In spite of its simplicity, one of the most important devices on this scheme is the combiner, which is made up of the antiparallel diodes which link the linear and switching stages. The forward voltage drop of these diodes will determine the error between V_{Lin} and V_{RFPA} when the linear stage is operating. So if a great accuracy between the desired envelope voltage and the actual is needed, very low forward voltage drop diodes can be selected. For this reason, Schottky diodes are recommended. The diodes selected here are MBRA130L which have a forward voltage drop of 0.4 V and can conduct up to 1 A. The voltage drop and the dynamic characteristics (reverse recovery time, etc) of the diodes play an important role in both the accuracy and the efficiency . The lower the voltage drop and the fastest the diodes, the greater the accuracy. However, this means that the power processed by the linear stage increases and then the efficiency decreases.

The accuracy of the reproduction of the envelopes will affect the distortion on the RF signal, although in ET and EER techniques there are more significant effects that have a more important impact on the distortion [13]. Correlation tests carried out on the prototype built, and shown on section IV, show that both good accuracy and efficiency are achieved at the same time. However the final requirement about accuracy has to be set by the maximum distortion allowed in the communication standard employed.

III. Control

The control scheme is depicted in Fig.8. The reference signal, generated by a signal generator, is digitized by an Analog to Digital Converter (ADC block) and introduced into the FPGA. Then this signal passes through a low-pass filter and it is introduced into the control stage of the MIBuck, which selects which transistors must be switching and what must be the converter duty cycle. Due to the fact that the MIBuck operates in CCM, the output voltage is only determined by the duty cycle and by the transistors which are switching at each moment [6]. As the MIBuck operates in open loop, a slight distortion may appear. However, this distortion will be corrected by the linear stage.

As a DC/DC switching converter behaves like a Digital to Analog Converter (DAC) transforming the digital information present in the duty cycle into an output voltage, frequencies above half the switching frequency should be avoided to prevent aliasing effects. These effects are even more serious due to the fact that a DC/DC switching converter is not an ideal DAC and, therefore, the alias problems occur at much lower frequencies. The low-pass filter (LPF block in Fig.8), implemented as a digital FIR (Finite Impulse Response) filter, is an anti-alias filter to prevent these effects. Its cut-off frequency was set at 300 kHz, so the MIBuck cannot reproduce spectral components above this frequency. However, most of the power of the envelope of communication signals is contained below this frequency.

The digitized reference is also routed through a delay stage to a DAC (Delay and DAC blocks in Fig.8) and then introduced into the linear stage. The mission of the delay is to synchronize the output voltage of the switching stage with the output voltage of the linear stage. This synchronization allows an efficient operation of the whole system. The gain of the linear stage has to be adjusted to minimize the power that processes. This can be done by monitoring the current trough the linear stage, while reproducing a signal well below the bandwidth of the switching stage. The gain is adjusted to obtain a very low current.

The sampling frequency was set at 15 MHz. Both the ADC and the DAC used in the prototype are evaluation boards provided by Texas Instruments. The ADC is a THS1530 and the DAC is an ADS5553. The control stage was written part in VHDL and part using Xilinx System Generator and programmed in a Xilinx Virtex 4 FPGA, but the design could be implemented easily in other kind of FPGAs with the

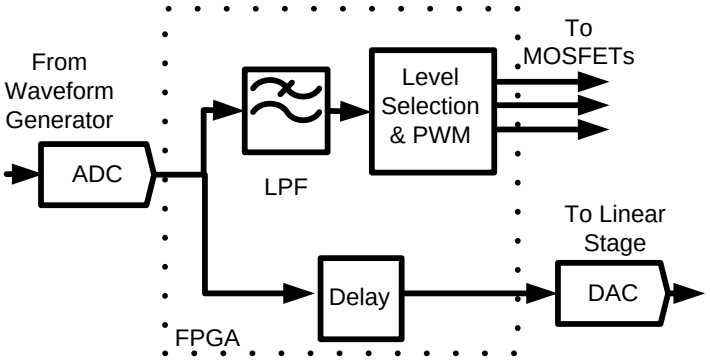


Fig. 8: Control scheme

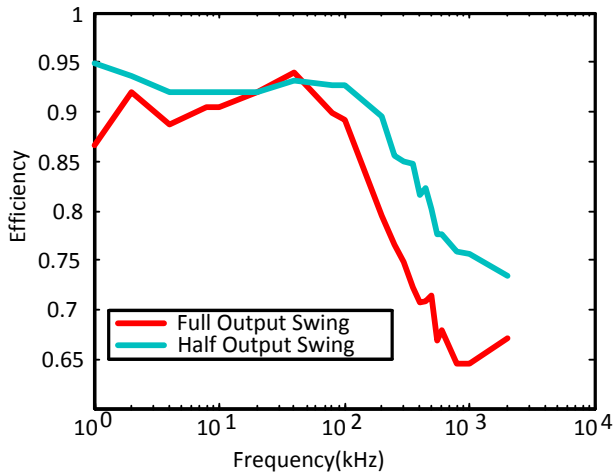


Fig. 9: Measurements of the efficiency

appropriate tools.

The decision to operate the MIBuck in an open-loop control relies on the higher bandwidth available [6]. The only requirement for proper operating in CCM is that the inductor on the switching stage must be big enough to operate in CCM under light loads, so the output voltage depends only on the input voltage selected (either V_1,V_2 or V_3) and the duty cycle used.

Although it is true that a closed-loop operation may improve efficiency as it avoids distortion on the switching stage (and, therefore, it minimizes the operation of the linear stage), the reduced bandwidth achieved may result in an actual lower efficiency than the one obtained from open-loop operation.

IV. Experimental Results

Several waveforms have been introduced into the proposed set-up and the results were compared with the MIBuck without the linear stage in order to compare the increasing in the bandwidth with the decreasing in the efficiency due to the use of the linear stage. The test signals are a single tone plus a DC component, the amplitude of AC component being always lower than the amplitude of the DC component to avoid negative values (0.5 and 0.25 times the DC component in Fig.9). The load (which represents the RFPA) was set to 6 Ω, the maximum input voltage is 600 mV in order not to saturate the ADC and the maximum output voltage is about 12 V. At low frequencies (1 kHz), the MIBuck can reproduce the waveform almost without distortion with an efficiency of 92%. By adding the linear stage the efficiency was lowered to 88%. At higher frequencies (1 MHz) the MIBuck only gives the DC component an all the high frequency components are given by the linear stage and the efficiency is 62% in this case. The maximum frequency used in this test was 2 MHz.

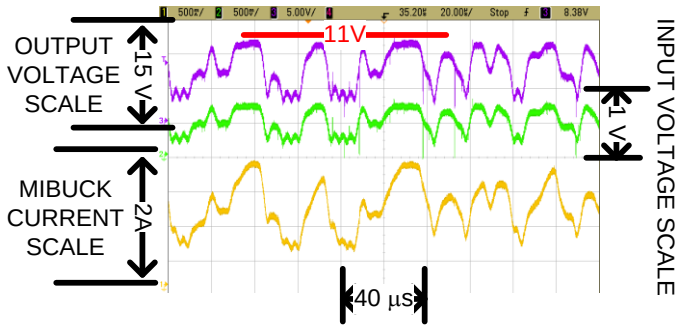
Although it can seem that the linear stage means an important drawback in terms of efficiency, the signals used in the first tests do not reflect some of the characteristics of the envelopes of communications signals. In these signals, the spectral components above few kilohertz carry very low power, not like the previously used signals, and then the linear stage processes very few power, so the drawback in efficiency is not as high as in the previous results. By using one of these signals, an EDGE standard envelope signal, it has been found that the system can reproduce almost without error the EDGE signal. Figure 10, shows the reference voltage (middle trace), the output voltage (upper trace), and the current apported by the switching stage (bottom trace), for an EDGE envelope (Fig.10a) and a WCDMA envelope (Fig.10b). By regarding the current waveform (Fig.10a-bottom trace) there can be seen that the current injected by the MIBuck sometimes cannot follow the small ripples in the output voltage (Fig.10a-upper trace) which the reference shows (Fig.10a-medium trace). The current necessary to reproduce that ripples over the resistive load is given by the linear stage. The efficiency obtained with the EDGE test signal was around 81%. The MIBuck alone cannot reproduce the EDGE signal with accuracy, however it provides a good approximation with an efficiency of 92%. By using a higher frequency envelope, a WCDMA signal envelope, it can be seen how the linear stage introduces a smoother current waveform (Fig.10b-bottom trace), while the output voltage (Fig.10b-upper trace), follows the fast variying reference (Fig.10b-medium trace) with accuracy. The efficiency measured with this system was slightly above 60%. Figure 10c shows the current through the switching and the linear stage. It can be noted how the linear current is centered in the origin while the current apported by the MIBuck has a significant DC component.

In order to measure the accuracy of the output voltage waveforms, correlation tests were done. The signals captured with the oscilloscope at the input and the output of the system were exported to MATLAB. There, they were normalized and the cross correlation between the input and the output were calculated. The cross correlation coefficient was over 90% for both the EDGE and the WCDMA envelopes. Therefore it can be said that the proposed system introduces very low distortion in the output waveforms.

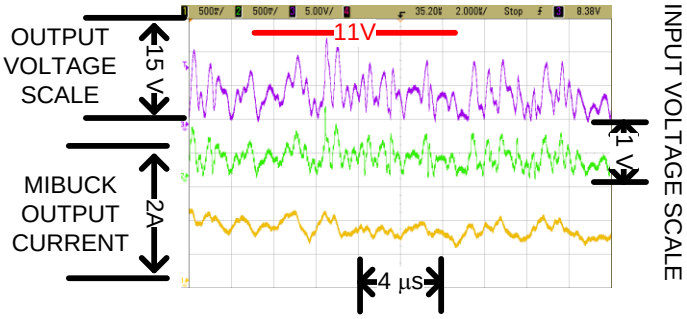
The other main advantage of adding a linear stage to a switching stage is the significant enhancement of the slew-rate. Without the linear stage, the MIBuck shows an slew-rate of 5.8 V/μs (Fig.11a - bottom trace). This value is improved to 130 V/μs with the aid of the linear stage (Fig.11b - upper trace). The efficiency is reduced from 95% to 90% so a minor drawback in efficiency leads to major improvement in slew-rate terms. The output pulse comes from 0 V to 12 V, with a pulse repetition frequency of 1 kHz.

Figure 12 explains the behavior of the system under high slew-rates. It is a simultaneous representation of voltage and current through the switching and the linear stage (the negative time scale is referenced to the trigger signal of the

oscilloscope). At the rising edge, the linear stage provides the current {red while the current from the MIBuck does not reach the value necessary to provide the desired voltage at the output. At the falling edge, the linear stage absorbs the excess of the current, thus maintaining the desired voltage at the output. It can be seen how this waveforms look-alike the theoretical ones in Fig.5.



(a)



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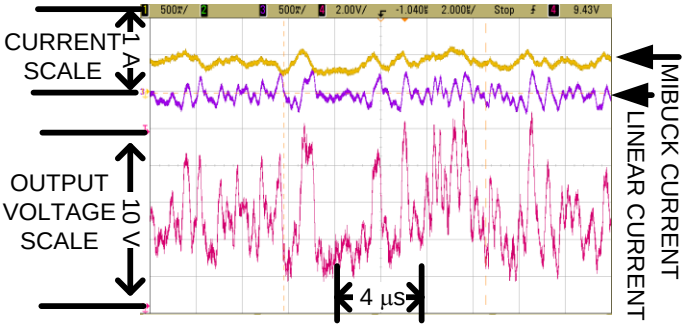
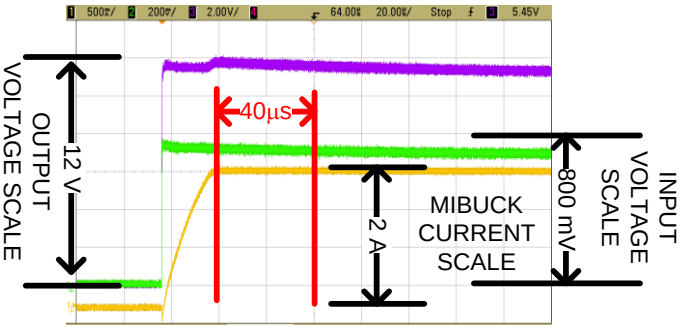


(c)

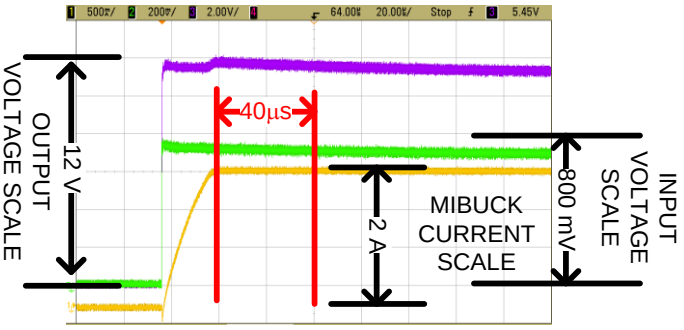
Fig. 10: (a) EDGE signal combination (b) WCDMA signal combination (c) Currents in another WCDMA example

V. Conclusions

A simple way of combining linear and switching stages for ET and EER applications has been presented in this paper. Using this technique the bandwidth and the slew-rate of the DC/DC converter has been extended from 5.8 V/μs to 130 V/μs, with minor drawbacks in efficiency. This approach establishes a good trade-off between efficiency, slew-rate and control simplicity.



(a)



(b)

Fig. 11: (a) slew-rate of combination (b) Close-up of Fig.(a)

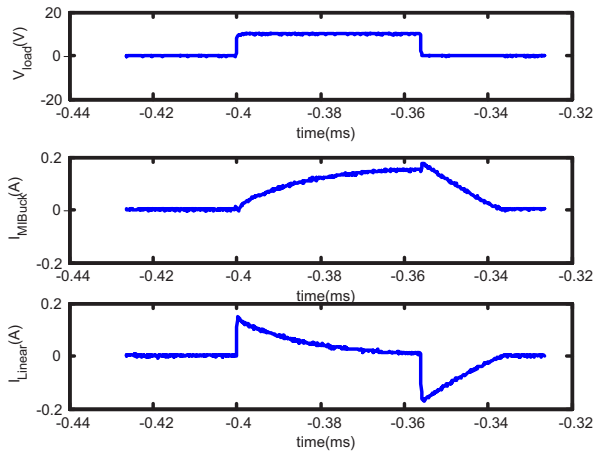


Fig. 12: Voltages and currents during pulsed operation

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