Aging Modeling and Simulation of the Gate Switching Instability Degradation in SiC MOSFETs

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***Abstract*—In order to conduct proper reliability investigations, aging models of silicon carbide (SiC) MOSFETs are needed to assess the possible effect that the degradation of these devices may have on the existing power electronic systems. These models should be able to accurately describe the long-term behavior of SiC MOSFETs. It has been recently discovered that (Gate Switching Instability) GSI is one of the most influential degradation processes. This work proposes the definition of a new model to describe the threshold voltage drift of SiC MOSFETs under GSI, from which a compact computational model is proposed to mimic this phenomenon. A new methodology is proposed to calibrate this computational aging model using experimental data, along with its extrapolation to a generic set of usage conditions. Compared to other proposed approaches, this model attempts to add new capabilities, such as the variation in the threshold voltage drift when using different application-related parameters (e.g., driving voltage and gate resistor).**

Keywords—reliability, device modeling, Silicon Carbide (SiC), Gate Switching Instability (GSI), MOSFETs, threshold voltage.

I. Introduction

In recent years, Silicon Carbide (SiC) MOSFETs are becoming increasingly popular in the field of power electronics. These devices offer several significant benefits compared to traditional silicon-based alternatives in high-power and high-voltage applications. Some of these advantages are their higher breakdown voltage, their better performance during the operation at higher switching frequencies and their enhanced thermal conductivity [1]. Furthermore, SiC devices are known for their high reliability and robustness, even in harsh environments [2]. Thus, SiC is suitable for applications that demand long-term performance and minimal maintenance, such as the electrical vehicle [3] and renewable energy systems [4].

Nevertheless, many degradation phenomena can cause SiC devices to not always operate at their optimum conditions. Aging processes in SiC MOSFETs often lead to a drift in the threshold voltage (V_{th}) of these devices, which yields to a negative impact on switching operation on real applications [5], [6]. In particular, it is reported that an increase in V_{th} is linked to an increase in the MOSFET turn-on resistance ($R_{ds\text{-}on}$), and as a consequence, to an increase in the conduction losses of the power application in which the device is being used, thus degrading its power efficiency. Therefore, degradation computational models that describe long-term behavior of SiC MOSFETs can be a useful method to conduct proper reliability investigations during the design process of power systems, to verify the possible effects that the device aging can introduce.

Among the multiple aging processes already reported in the literature, Hot Carrier Injection (HCI) degradation is worth mentioning. This phenomenon is caused by high energy carriers (electrons or holes) gaining sufficient kinetic energy to cause damage to the gate oxide of a MOSFET [7]. However, the degradation processes that most predominantly affect the operation of SiC MOSFETs are Gate Switching Instability (GSI) and Bias Temperature Instability (BTI) [6], [8]. BTI can be described as a degradation mechanism primarily associated with the DC biasing of a transistor gate, involving the long-term drift in V_{th} (ΔV_{th}). On the other hand, GSI, is a dynamic phenomenon that occurs during high-frequency gate switching events under bipolar gate switching conditions. This is depicted in Fig. 1, where different fitting curves and drift zones are used depending on the dominance of the degradation mechanism.

Different models have been proposed to explain and describe the drift ΔV_{th} caused by the BTI and GSI effects [7 - 10]. Nevertheless, these models may not address some aspects close to application, such as the different degradation of V_{th} that can be observed when different driving voltages are applied. Specifically, there is a concern in the design of power systems regarding the necessity for a phenomenological model that relies on various operating conditions rather than on the physical parameters of the device.

In this work, a new model to describe the degradation due to GSI in modern SiC MOSFETs is proposed. Furthermore, a methodology to adapt this model when different application-related aspects (e. g., different driving voltages and gate resistors) is proposed. This would be the

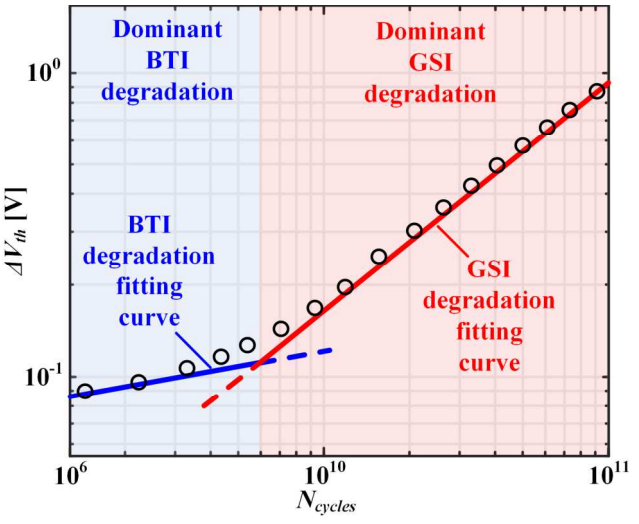


Fig. 1. Representation of the different drift regions and the dominance of BTI and GSI depending on the number of switching cycles.

foundation of a compact simulation model also presented in this work, where the V_{th} drift is modeled as a voltage-controlled voltage source which depends on the realization of the proposed model and the number of switching cycles.

The manuscript is organized as follows: Section II offers a comprehensive review of extant degradation models and their translation into computational frameworks. Section III presents a succinct account of the experimental methodology employed in this study, encompassing the delineation of the empirical model proposed herein. Section IV introduces the compact model proposal. Ultimately, Section V furnishes the principal conclusions derived from this investigation.

II. Modeling and Simulation of Aging in MOSFETs

A. State-of-the-art in MOSFET Degradation Modeling

According to the existing literature, the drift ΔV_{th} due to GSI is modeled with a power law [9], [10] which depends on the number of cycles N_{cycles} at which the device is stressed: Therefore, ΔV_{th} can be expressed as

$$\Delta V_{th}(N_{cycles}) = A_0 N_{cycles}{}^{n} \quad (1)$$

where A_0 and n are parameters which depend on the device and the experimental conditions and N_{cycles} is the number of switching cycles at which the degradation is measured. Nevertheless, experimental results show that a single law is not able to capture the degradation trend for a large number of switching cycles [11]. This is solved by using a different approach for different time intervals. In this way, the value of A_0 and n will vary depending on the value of N_{cycles}, just like in a piecewise function. This is also depicted in Fig. 1, where different fitting curves are used for the whole range of N_{cycles}, due to the dominance of different degradation mechanisms. Thus, the experimental data reported in literature and our own results suggest that the power law changes when $N_{cycles} \approx 10^8$, distinguishing two drift regions [9]. Roughly between 10^3 and 10^8 switching cycles, the increase in V_{th} is considered caused mainly by BTI. Above this number of cycles, GSI (i. e. the drift caused by the high-switching variations) plays an important role, and the effect that this degradation phenomenon introduces in ΔV_{th} becomes dominant.

The main drawback of this model is that these parameters can vary depending on the device or the operating conditions imposed by the application. Thus, the value of the long-term degradation is difficult to predict, since it is difficult to determine what is the best threshold in the number of switching cycles to separate the different drift regions. Aging models that include different power laws to introduce the saturation effect in ΔV_{th} are required to better describe the device degradation.

B. State-of-the-art in Model Implementation

Once the model that describes the degradation of SiC MOSFETs, different approaches can be followed to implement a circuit or a computational model. Many of the proposed approaches are applied to Silicon MOSFETs in digital and logical circuits [12]. Nevertheless, the same conclusions can be applied to the degradation of power devices.

Essentially, the device under simulation can be represented as a netlist in any simulation software which operates according to a set of predefined input stimuli. These inputs will depend on the operating conditions under which the simulation is performed (switching frequency, driving voltages, temperature, etc.). Depending on how they vary, two main strategies can be followed to develop an aging model: model card adaptations [13] and subcircuit models [14]. In the model card approach, the degradation parameters are part of the model itself, and as a result, it makes use of different parameters that will strongly depend on the underlying device model (geometry of the device, different physical conditions, etc.). Some of the disadvantages of this strategy are the inaccuracies that may appear when different conditions required by the application are imposed and the need for recalibration whenever these unforeseen conditions have to be simulated. However, if the aging simulation is performed within nominal conditions, it becomes a simple approach to be used in the design of power systems.

On the other hand, subcircuit-based approaches, also referred to as compact models, can be a promising alternative to implement an aging model. Though it introduces new nodes to the device model, increasing its complexity, it can be more flexible than the mode card alternative. In order to implement this kind computational model, dependent sources have to be added to model the degradation of different device parameters. For instance, the drift in V_{th} can be considered as a dependent voltage source which varies its magnitude depending on different parameters which depend on both the device and the operating conditions. Compact models may be precisely customized to accentuate specific degradation mechanisms, thereby yielding valuable insights into the aging process of semiconductor devices. This focused analytical approach contributes to a heightened comprehension and the efficient mitigation of potential reliability concerns.

Independently of the chosen approach, a relationship between the drift in V_{th} and the device parameters must be derived. Simulation-based predictions are commonly used to calibrate the different parameters that this relationship requires. Nevertheless, the aging data obtained as a result of analyzing the degradation of several SiC MOSFETs which have been operated under different driving conditions are used in this work to propose a compact model. The approach that is derived is based on the empirical aging model explained in the following sections.

III. New Empirical Model of Aging SiC MOSFETs

A. Description of the Experimental Conditions

In order to elaborate a proper empirical model, the first step is to obtain a set of experimental data of the Vth drift under different in accordance with the real application. For this purpose, a Gate Switching Stress (GSS) test is performed [15], [16]. The description of this test is depicted in Fig. 2. It must be considered that the switching frequency of this test f_{sw} should be close to the one used in a real application. In this case, f_{sw} equals 100 KHz. The GSS test basically consists in applying a pulsed gate stress in a SiC MOSFET while maintaining the drain and the source of the device short-circuited (Fig. 2(a)). After applying a series of pulses during a certain period, the Device Under Test (DUT) experiences a permanent degradation in V_{th} and R_{ds} because of this test. This degradation is mainly caused by the GSI phenomenon,

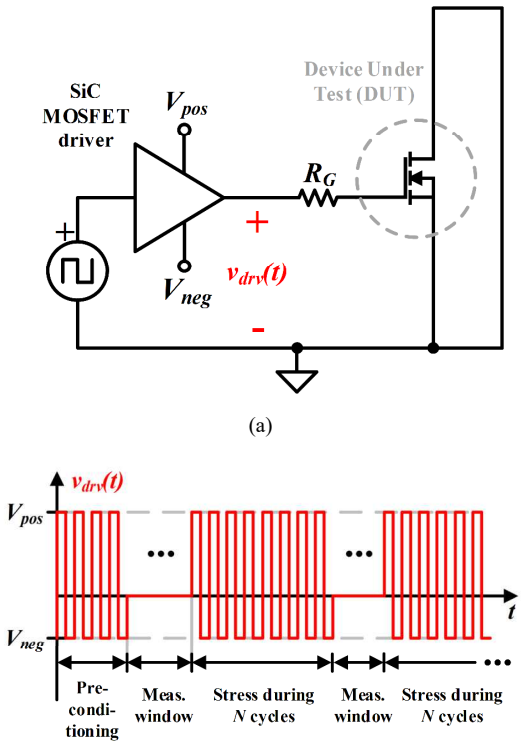


Fig. 2. Description of the GSS test to obtain empirical data on SiC MOSFET degradation: (a) Schematic of the experimental setup. (b) Gate driver signal and test sequence.

becoming dominant over BTI when a large number of switching cycles is considered.

It should be considered that a pre-characterization of the device must be performed according to the guidelines highlighted in [15]. After a stress period, the value of V_{th} is measured using a B1505A [17] power device analyzer following the recommendations of [18], and the measurement cycle is started again, with a corresponding preconditioning stage. The devices used for all experimental tests and simulations correspond to engineering samples of a 1200 V SiC MOSFET based on trench technology. This device is rated 117 A of continuous drain current. More details of the GSS experimental setup used for the collection of the experimental data of this work can be found in [19].

The different conditions under which the experiments have been carried out have been chosen considering the different stressors identified in the literature [11]. The two main orthogonal stressors (i.e. it is considered that there is no influence between them) identified in the literature are the negative driving voltage V_{neg} and the derivative in the gate-to-source voltage dv_{gs}/dt, which will be imposed by the parasitic capacitance of the device by the gate resistance R_G.

These two parameters can be adjusted or determined by the application (presumably a software or system setting). The observed changes in V_{th} over time can then be used to predict or estimate how V_{th} would evolve for other values that are dependent on the specific application in use. In this way, the behavior of V_{th} for the provided parameters serves as a reference, and this behavior can be extended or extrapolated to anticipate how the degradation might change for different, yet application-dependent, values.

The different values of the positive driving voltage V_{pos}, V_{neg} and R_G are summarized in Table I. The experimental data is shown in the following sections, where the fitting of this data according to the proposed model is introduced.

In experiments denoted as conditions #2 to #9, two devices underwent testing. Conversely, in the context of experiment #1, ten devices were subjected to testing, revealing a minimal spread in the threshold voltage differentials (ΔV_{th}) [19].

B. *Proposed Experimental model*

As it has been explained before, the models that describe the drift ΔV_{th} will strongly depend on the device and the experimental conditions.

In alternative approaches, the behavior of ΔV_{th} is defined as a piecewise function. However, this approach might encounter challenges when attempting to adapt to a more intricate computational model. This work suggests the use of a continuous function to represent the behavior of ΔV_{th}, that can be easily adapted to represent the degradation in SiC MOSFETs under different operating conditions.

The model proposed in this work results from the polynomial interpolation by representing in logarithmic scale the dependence of drift as a function of N_{cycles}. This model is represented by the generic function

$$\Delta V_{th}(N_{cycles}) = A_0 N_{cycles}^{x(Ncycles)} \quad (2)$$

where $x(N_{cycles})$ is a function which depends on n_1 and n_2 which are parameters derived from the polynomial interpolation mentioned before, and can be expressed as

$$x(N_{cycles}) = n_2 \cdot \log(N_{cycles}) + n_1 \quad (3)$$

As can be seen in (2), the exponent of the parameter N_{cycles} also varies according to this parameter, reproducing the auto-saturation effect in GSI already reported in the literature. The development of the complete model is considered as follows. First, it is sought to calibrate the degradation curve of the device in a generic way, with a given set of initial conditions. These conditions correspond to the data set of experiment #1 in Table I. Then, it is proposed to adapt the shape of the curve to the different experimental conditions, performing a vertical and horizontal scaling of the curve by means of the inclusion of the new parameters a and b, respectively. Thus, the new curve $\Delta V_{th}'$ can be described, according to the first curve described by (2), as

$$\Delta V_{th}' = a\left[\Delta V_{th}\left(\frac{N_{cycles}}{b}\right)\right] \quad (4)$$

TABLE I. EXPERIMENTAL CONDITIONS USED IN THE COLLECTION OF EMPIRICAL DATA

Experiment	#1	#2	#3	#4	#5	#6	#7	#8	#9
V_{pos} [V]	18	22	18	23	13	18	18	18	18
V_{neg} [V]	-8	-8	-3	-3	-8	-8	-8	-8	-5
R_G [Ω]	4.7	4.7	4.7	4.7	4.7	10	20	1	4.7

Table II shows the values used to calibrate the model for experiment #1, which is the calibration experiment. Table III presents the values of parameters *a* and *b* used for the calibration of experimental data with the model specified in equation (4). Figure 2 illustrates the fitting curves corresponding to various experimental outcomes, as determined based on the conditions outlined in Table I through the application of this methodology.

C. Experimental results

Fig. 3 shows both the degradation data obtained during the GSS experiments and the curve fitting using the proposed model. The results are organized as follows. Fig. 3 (a) corresponds to the results obtained for different values of Vpos. Two different families of curves are included: variation of the degradation when V_{pos} is changed (from 18 V to 22 V) while V_{neg} remains constant and equal to -8 V, and the degradation as a function of the variation of V_{pos} (from 18 V to 23 V) while V_{neg} is unchanged and equal to -3 V. As can be seen, the degradation increases as V_{pos} increases, but this change is significantly less than that suffered between the two families of curves.

Thus, the experimental results validate the hypothesis that one of the main stressors is the variation of V_{neg}. In addition, it can be observed, thanks to the proposed experimental model, that for small values of V_{neg}, the long-term degradation is significantly lower than for high values. This corresponds to the conclusions shown in [10] and [20] where it is proposed that the saturation behavior is not uniform with the variation of V_{neg}.

Fig. 3(b) shows different families of degradation curves are shown for a variation of V_{neg}. For low V_{neg} (V_{neg} = -3 V) values, the model predicts a saturation in V_{th} much lower than for higher V_{neg} values, where switching events seem to ramp up the drift. Nevertheless, for intermediate V_{neg} values a similar behavior can be appreciated for few switching cycles, but the saturation ΔV_{th} tends to be similar than for high V_{neg} values. More degradation curves are required to predict in a more accurate manner the trend for the variation of V_{neg}.

Finally, Fig. 3(c) corresponds to the experimental results and fitting curves obtained for different values of R_G, as an attempt to verify the evolution of ΔV_{th} with dv_{gs}/dt. For low values of R_G, the trend in the degradation of V_{th} is quite

TABLE II. VERTICAL AND HORIZONTAL SCALING FACTORS USED IN FIG. 2

A_0	n_2	n_1
$7.9433 \cdot 10^{-15}$	-0.09627	2.355

TABLE III. VERTICAL AND HORIZONTAL SCALING FACTORS USED IN FIG. 3

Experiment	*a*	*b*
#1	1.0000	1.0000
#2	1.1030	0.7643
#3	0.1105	1.5031
#4	0.1013	1.5210
#5	0.4914	0.8940
#6	1.0110	1.2310
#7	0.8519	0.8949
#8	1.2260	1.1810
#9	0.4505	1.2102

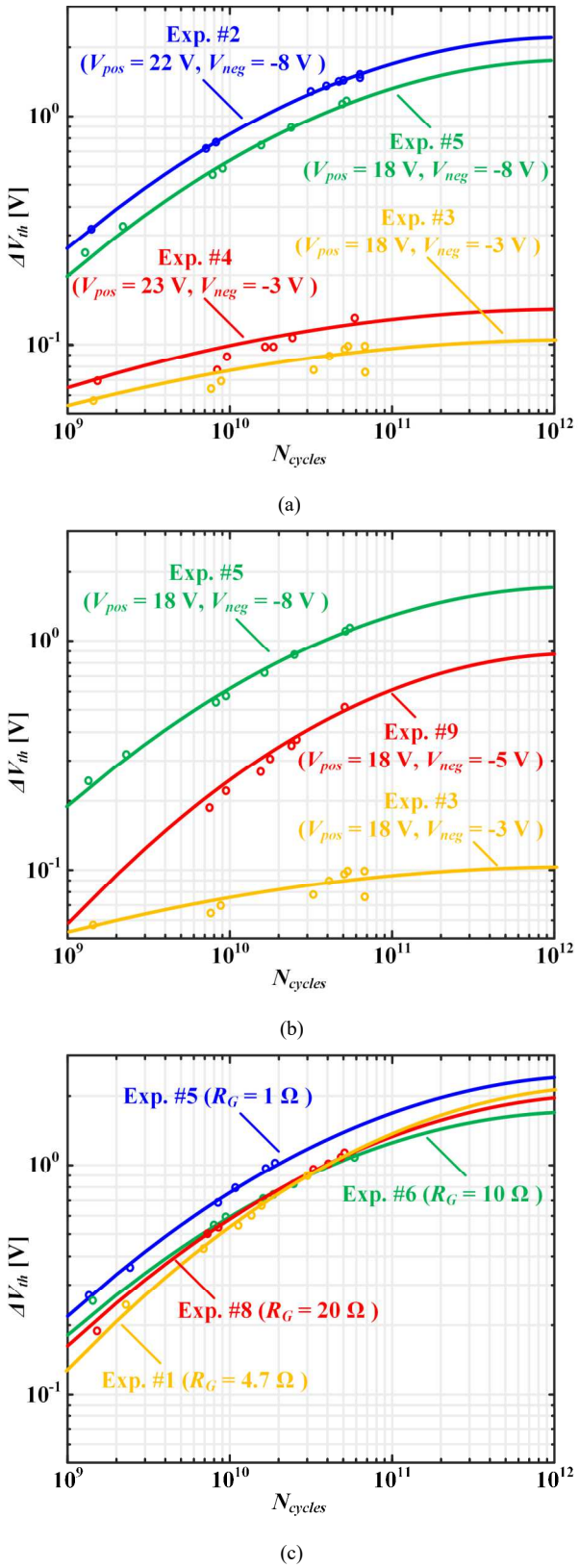


Fig. 3. Curve fitting of ΔV_{th} vs. N_{cycles} using the proposed model for the different experiments summarized in Table I. (a) V_{th} drift varying the positive gate voltage V_{pos} for V_{neg} = -3 V and V_{neg} = -8 V. (b) V_{th} drift varying the negative gate voltage V_{neg}. (c) V_{th} drift varying the value of the gate resistor R_G.

similar as the one observed for an increase in V_{pos}. In particular, similar evolutions can be observed for V_{pos} = 22 V, V_{neg} = -8 V, R_G = 4.7 Ω and for V_{pos} = 18 V, V_{neg} = -8 V, R_G = 1 Ω. As the value of R_G increases (R_G = 4.7 Ω, 10 Ω, 20

Ω), the ΔV_{th} trends determined by the fitting curves collapses around the same tendency, which, in this case, is the calibration curve (V_{pos} = 18 V, V_{neg} = -8 V, R_G = 4.7 Ω).

IV. Definition of the Compact Model

Once the models are calibrated for a set of experimental conditions, a compact simulation model such as the one shown in Fig. 4 [14] can be used to include V_{th} drift due to BTI. The implementation of this compact model, following a strategy based on the inclusion of dependent sources, is depicted in Fig. 4(a). As can be seen, the magnitude of this voltage source is the aging model described in this work, and it will depend on the number of switching cycles N_{cycles}. Thus, the main advantage of this approach is that it is not an iterative model, and the prediction in the long-term degradation can be easily estimated using the degradation model described in this work.

Fig. 4(b) shows the method that can be implemented to control the dependent voltage source that model the drift ΔV_{th}. It mainly consists in the use of an equation-controlled voltage source, which depends on the parameters a and b previously derived from the fitting of the experimental data. To obtain the value of the number of the switching cycles to be used in this model, the implementation of an edge detector is proposed. This can be easily coded in circuit simulation software, by counting the pulses of the gate-to-source voltage.

The estimation of the parameters a and b for a whole set of conditions would require more experimental tests. As described before, the evolution of the parameters of the proposed model may have a non-linear relationship with some of the stressors identified in this work. Nevertheless, an extrapolation can be performed based on the derived a and b values. This analysis is done in this work based on the two different identified stressors (i. e. V_{neg} and dv_{gs}/dt, which varies with R_G).

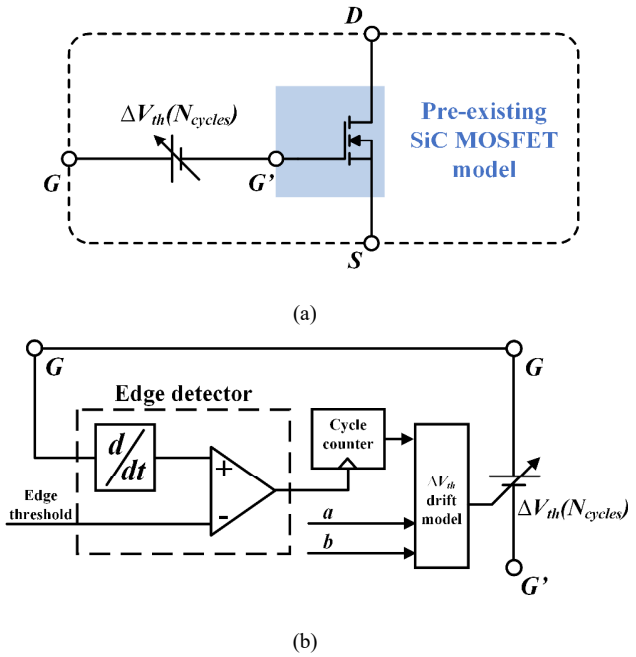


Fig. 4. Proposal of the compact model used to simulate the effect of the V_{th} drift in SiC MOSFETs. (a) Schematic of the compact model, where both the device model and the dependent voltage source are included. (b) Implementation of the compact model, where the schematic of the control of the voltage source is shown.

Fig. 5 shows the dependance of a and b with V_{neg}. The value of a (see Fig. 5(a)) decreases almost linearly as V_{neg} decreases, which is coherent with the experimental results obtained in Fig. 3. The expression which relates a with the variation of V_{neg} can be expressed as

$$a(V_{neg}) = -0.18 \cdot V_{neg} - 0.44 \quad (5)$$

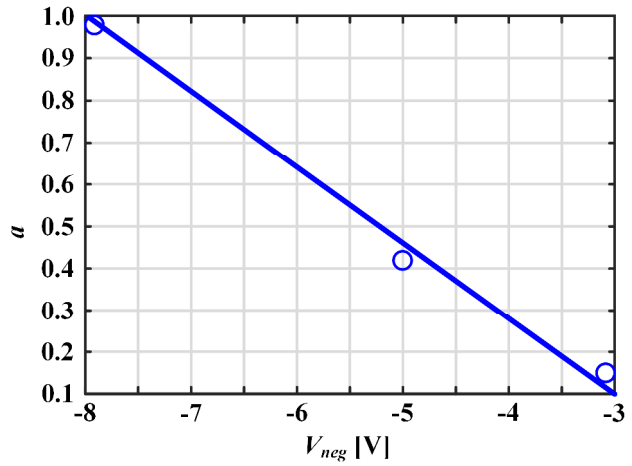
At the same time, there is not a linear relationship between b and V_{neg}. This observation aligns with findings in [11], where distinct degradation regions are discerned in relation to V_{neg}. Roughly, voltages surpassing -4 V demonstrate a constancy, whereas for voltages beyond -4 V, the drift escalates until reaching -16 V. Notably, the relationship obtained in this study is as follows:

$$b(V_{neg}) = 0.033343 \cdot (V_{neg})^2 + 0.468 \cdot V_{neg} + 2.604 \quad (6)$$

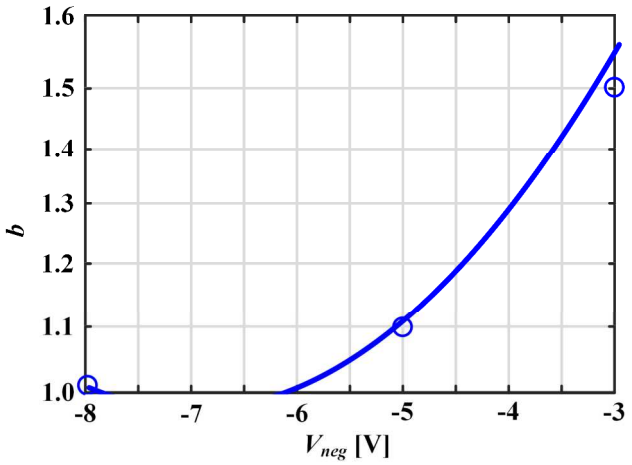
Regarding the dependance of a and b with the gate resistor R_G value (Fig. 6), it can be observed that a little variation is obtained as dv_{gs}/dt decreases with the increase of R_G. More precisely, the following equation can describe the variation of the model parameters with R_G:

$$a(R_G) = 0.0007974 \cdot (R_G)^2 - 0.03402 \cdot R_G + 1.222 \quad (7)$$

$$b(R_G) = -0.001355 \cdot (R_G)^2 - 0.01791 \cdot R_G + 1.094 \quad (8)$$



(a)



(b)

Fig. 5. Representation of the dependance of model parameters a and b vs. negative voltage driving V_{neg}: (a) a vs. V_{neg}. (b) b vs. V_{neg}.

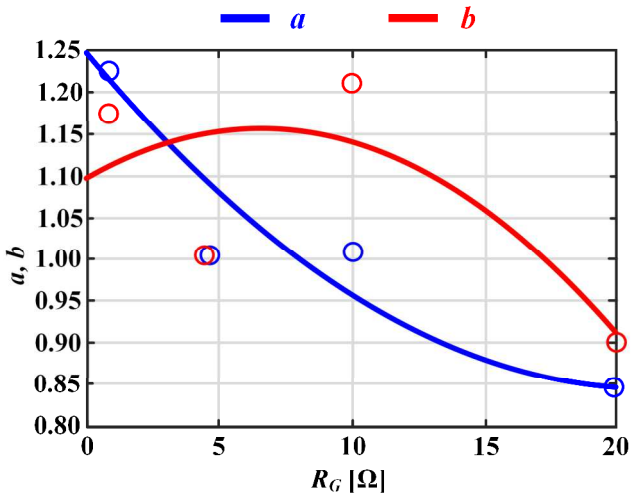


Fig. 6. Representation of the dependance of model parameters *a* and *b* vs. gate resistor R_G.

All these relationships can be implemented in a computational model as the one represented in Fig. 4. More sophisticated versions of this model can be implemented by means of a physical circuit, which can relate some model parameters with device structural parameters.

V. Conclusions

This study introduces a novel methodology for the formulation of models aimed at characterizing the GSI degradation in SiC MOSFETs. The proposed methodology is designed for flexibility, allowing adaptation to diverse experimental conditions contingent upon the specific requirements of the application. Additionally, the capability to adapt this model into a compact computational representation, exempt from the need for iterative description of the threshold voltage drift caused by GSI, is presented. Furthermore, an extrapolation of certain operating conditions to a more comprehensive model is achieved by establishing the relationship between the principal model parameters and the identified stressors.

Acknowledgments

This work was supported in part by Ministerio de Ciencia e Innovación, by Agencia Estatal de Investigación and by FEDER under Project PID2022-136969OB-I00, and in part by the Principality of Asturias under "Severo Ochoa" Program Grants no. BP20-181 and BP21-114 and under Project SV-PA-21-AYUD/2021/51931.

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