Improving the efficiency of SiC-based synchronous boost converter under variable switching frequency TCM and different input/output voltage ratios

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***Abstract* -- This paper is focused on the design of a high-voltage (800V) bidirectional boost converter with high efficiency at medium-low power levels. Triangular Current Mode (TCM) enhances the efficiency of the converter at low power thanks to soft-switching operation, but it requires variable switching frequency and large current ripple through the inductor. The former can be implemented by using SiC MOSFETs and the latter can be minimized by using interleaved modules.**

At low power, TCM requires high switching frequency, a minimum negative inductor current and a minimum dead-time to obtain ZVS. These values vary for different input/output voltage ratios and must be properly selected to reduce dead-time losses, normally neglected in literature since it is assumed that they have low impact. However, it can be relevant at high frequencies (especially for devices with high reverse conduction voltage drop, such as SiC MOSFETs). In this paper, dead-time losses are included in the proposed losses models and the selection of optimum values of dead-time and minimum inductor current to minimize these dead-time losses are analytically evaluated and experimentally validated.

***Index Terms*--Boost, efficiency, modularity, QSW, SiC, TCM.**

I. Introduction

Examples of established topics in current concerns related to power electronics are energy recovery systems, energy storage systems, renewable energies, dc distribution grids, smart grids or power electronic transformers [1]-[6]. In most of these applications, energy storage systems and bidirectional dc–dc power converters are needed. Besides, battery charging process is usually done in three stages [7], with a final stage in which the charging current is very low. Therefore, the previously mentioned power converters interconnecting the storage system must achieve high efficiency over a wide power range.

Related to these applications, an interesting topic is the integration of distributed energy resources in multilevel converters. By adequate design of the cells of multilevel converters (with voltage level at the cell usually around 1 kV), it is possible to integrate low voltage DC or AC power sources (such as Photovoltaics (PV) panels or wind turbines), loads or energy storage devices at the cell level [8]-[10].

Consequently, a power converter designed to integrate battery systems in a multilevel converter at cell level must withstand high voltage providing high efficiency. Some standards (i.e. NEMA PE 5-1997) require the use of isolation for some of battery chargers, which may be valid for certain applications. However, some others (i.e. IEEE P2405) consider that this aspect does not reflect the current state of art and refuse this requirement. The converter under analysis in this paper could be used in applications without galvanic isolation requirements.

The use of Wide Band Gap (WBG) semiconductors, especially Silicon Carbide (SiC) MOSFETs, allow the operation of power converters at high voltage and high switching frequency with high efficiency [11]. SiC MOSFETs and a variable switching frequency control technique providing Zero Voltage Switching (ZVS) have been used to improve the efficiency in a synchronous boost converter, especially at medium and light load operating at high voltage and high frequency [12], [13].

However, a high current ripple is the price to pay of this type of operation mode, which increases conduction losses, especially at full load. Modularization techniques are a possible solution to overcome up to a certain degree this problem.

Nevertheless, when the converter is working at low load, Triangular Conduction Mode, TCM, requires, on one side, high switching frequency and, on the other side, a minimum negative inductor current and a minimum dead-time to obtain ZVS. Since switching losses are predominant at low load (which corresponds to higher switching frequencies) these extra losses need to be considered in a proper loss power model to predict their impact if TCM is used. In this paper, dead-time losses are included in the proposed losses models and the selection of optimum values of dead-time and minimum inductor current to minimize these dead-time losses are analytically evaluated and experimentally validated.

It is worth to mention that the specifications of the bidirectional boost converter analysed in this paper are oriented to provide battery systems to a multilevel converter at cell level (Fig. 1). However, the conclusions can be applied to different applications where a non-isolated bidirectional converter with high efficiency for light loads and high-voltage operation is needed (e.g., wind energy generation with storage capability [10] or electric vehicle battery chargers [14], [15]).

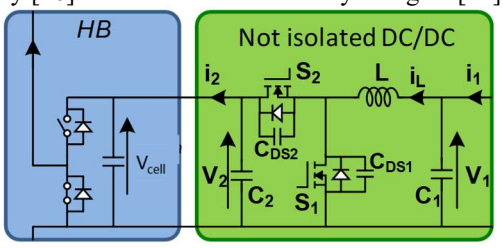

Fig. 1 Cell structure composed by not isolated bidirectional boost converter and Half-Bridge (HB).

Advantages and disadvantages of different conduction modes, a preliminary power loss model and the modularity concept will be reviewed and discussed in Section II. Furthermore, more analytical insight about the resonant period which is commonly neglected in the literature and the trade-off between negative current and dead-time when the converter works under different input/output voltage ratios are presented in Section III, which is the main contribution of this paper. Section IV shows the experimental results extracted and efficiencies for different conditions. Finally, conclusions are drawn in Section V.

II. CONTROL STRATEGIES TO OBTAIN HIGH FLAT EFFICIENCY IN A WIDE POWER RANGE

In order to get and maintain high efficiency over a broad power range, different strategies may be followed, for example, modifying the conduction mode for different load levels. To be able to select the proper operation mode of the bidirectional boost converter, a thorough power loss model considering any possible source of losses is needed. Besides, introducing modularization techniques can further extend the high efficiency working region.

A. Conduction Modes

The main characteristics of the two continuous conduction modes (CCM) providing the best performance from the efficiency point of view are presented (their main waveforms are shown in Fig. 2):

1) CCM Hard Switching (CCM-HS). Reduced current ripple and constant switching frequency (f). Its key advantage is the low current ripple (suitable for charging and discharging energy storage systems), performing low conduction losses. High-switching losses are the main drawback. At light loads, this mode can achieve ZVS (i.e. TCM at constant switching frequency).

2) TCM with minimum negative current to obtain ZVS (TCM-ZVS). Large current ripple (inductance current is negative at the turn-on of S_1) and variable switching frequency are its main characteristics. Full ZVS can be achieved with a proper selection of negative inductance current and dead time for different relations of input and output voltages [16], reducing switching power losses. This conduction mode is also known as pure QSW-ZVS [16] - [19] when the output voltage is twice the input voltage (ZVS is obtained easier).

B. Power loss models

The use of the aforementioned conduction modes depending on the load demand and the distribution of losses related to them are characterized in detail in [20] and [21], respectively. As a result, an efficiency comparison among the analysed conduction modes is possible for a wide power range (Fig. 3). To obtain this power model the specifications of the prototype (in this paper defined in Section IV) must be taken into account.

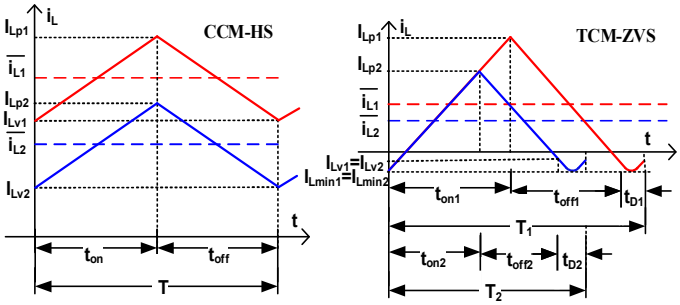

Fig. 2 Current through the inductor, $i_L(t)$, for CCM-HS and TCM-ZVS, pointing out the peak value ($I_{Lp\,x}$), average value ($\overline{i_{Lx}}$), valley value ($I_{Lv\,x}$) and minimum value ($I_{Lmin\,x}$) for two power demands (1 or 2), where t_{onx} represents the time S_1 is ON and S_2 is OFF, t_{offx} represents S_1 OFF and S_2 ON and t_{Dx} represents a certain dead-time.

The sources of losses taken into consideration in this paper are conduction, gate, switching and inductor losses, making special emphasis in differences among switching losses during turn-ons turn-offs depending on the conduction mode.

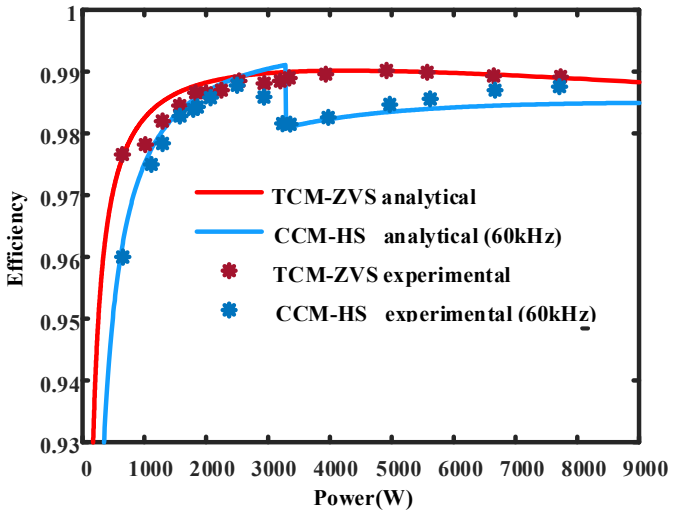

Fig. 3 Experimental and analytical efficiency comparison for different conduction modes [21].

In CCM-HS, the converter works at a fixed frequency of 60kHz and the current through the inductor is positive for level loads higher than 3000W. A dip in efficiency at 3000W takes place because, since the current ripple is fixed, the converter enters in TCM for load demands lower than 3000W (i_{Lv} is negative and ZVS is achieved). As the load demand decreases, the current through the inductor takes a more negative value, causing losses due to reactive current in the converter and this results in a faster decrease in efficiency.

Taking into account current ripple level through the inductors and since efficiencies between modes are close, it is proposed to use CCM-HS for power levels higher than 3000W and TCM-ZVS for lower power levels.

It is worth to mention that both the analytical and experimental results are accomplished under the condition $V_2=2\cdot V_1$, where V_1 is 400V and V_2 is 800V, and, therefore, pure QSW-ZVS is achieved.

However, for different input/output voltage ratios QSW-ZVS becomes TCM-ZVS with variable switching frequency

and some changes in the power model need to be included in order to take into account the minimum negative inductor current and the minimum dead-time needed to obtain ZVS, as it will be further explained in Section III.

C. Modularity

Despite TCM-ZVS and QSW-ZVS modes have the great advantage of reducing switching losses, both modes have the disadvantage of working with a large inductor current ripple. For batteries, supercapacitors or other energy-storage applications, this large charge current ripple may either reduce the life of the energy-storage system or diminish its functionalities. A possible way to overcome this problem is the use of synchronous boost converters connected in parallel, and, therefore, an interleaving approach can be applied in order to reduce the inductor current ripple.

In addition, this modular approach can also be used to increase the power managed by the system and the efficiency at medium and light load. At this point, an Input-Parallel-Output-Parallel (IPOP) modular converter, in which all the modules share the input and output voltage and the total input and output currents are the sum of the current of each single module, is suitable to overcome high current ripple if an interleaving control technique is applied to either TCM or QSW-ZVS modes.

Different modularization techniques might be applied:

1) Balanced master-slave technique

This technique does not take any advantage of the modular arrangement in terms of loss reduction at light load. However, the main advantage of this balanced technique is the input port current ripple reduction thanks to the interleaving control technique. It is very well known the relationship between the input current ripple as a function of the duty cycle (D) and the number of modules [22]. Depending on the value of D, the total input port current ripple may even be fully cancelled.

A master–slave approach can be considered to implement this balanced technique [23]. In this case, the variable controls of all the modules are the same, and they are generated and shared from the master module to the slave modules. The overall efficiency of the modular converter is equivalent to the efficiency of one module.

The complexity of the master module in TCM-ZVS is slightly higher than in CCM-HS, because this module has to generate more variable controls (i.e. switching frequency variations with the power level). All the modules work varying their switching frequency following master module variation, making also possible the interleaved technique. The main disadvantage of this technique is that the current sharing depends on the component tolerances and the differences among the modules.

As conclusion, balanced control technique using either TCM-ZVS or CCM-HS mode reduces the input current ripple. This technique is a very simple way to extend to higher power converters the high efficiency at light load thanks to the use of SiC power MOSFETs and TCM-ZVS.

2) Phase-shedding technique

Under this approach, only a certain number of modules needed to provide the total output power are working at the same time, being off if they are not used. Hence, when the output power increases, the number of active modules increases and vice versa. Therefore, the overall modular converter efficiency can be improved at medium and light load [24]. However, the input current ripple reduction is lower than the obtained for master-slave technique. This is because the number of active modules changes with the load, and, therefore, the phase shift among them in order to perform interleaving changes too, causing that the input port current ripple reduction will not be the optimum one. This drawback arises especially at light load, when only a few number of modules are active. More complex control techniques are needed to overcome the high current ripple problem if the phase-shedding technique is used.

As conclusion, this technique using either TCM-ZVS or CCM-HS mode reduces the input current ripple, especially at high load, and improve the efficiency al medium and light loads because the higher number of modules are working together.

As proof of concept, analytical and experimental efficiencies for the two modular approaches presented are shown in Fig. 4, based on [23].

However, the new proposal of using TCM-ZVS under different voltage ratios will be based on an IPOP configuration without including modularization techniques in order to reduce uncertainties and validate the suitability of the new strategy.

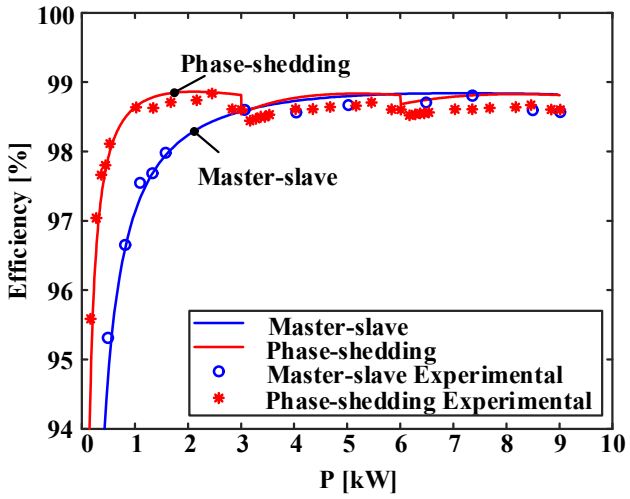

Fig. 4 Analytical and experimental efficiency results for different modular techniques [23].

III. Dead-time vs. Negative Current

As it was introduced in Section II, the efficiencies obtained in Fig. 3 and Fig. 5 are only valid if the condition $V_1=V_2/2$ is accomplished and pure QSW-ZVS is achieved.

When the bidirectional boost converter under analysis is used to integrate batteries at cell level in a multilevel converter,

the voltage conversion ratio varies due to the voltage fluctuation of batteries. If V_2 is not twice V_1 the efficiencies presented in Fig. 3 are not valid, because the inductance current could be different to assure ZVS. Two strategies might be followed when the voltage relation between V_1 and V_2 varies considerably.

On one hand, additional converters can be connected in cascade with the bidirectional boost converter under analysis to static regulate the battery voltage to 400 V. The efficiency of this converter (η_1) could be high because its conversion ratio is low, but, the global efficiency will be $\eta_T = \eta_1 \cdot \eta_2$, (being η_2 the efficiencies presented in Fig. 4 and Fig. 5), therefore, the whole performance might be compromised.

On the other hand, a wide input voltage range converter working at TCM-ZVS with variable switching frequency can be developed. Under this case of study, there are certain variables that must be properly selected, such as, the valley inductance current when S_2 is turned off (i_{Lv} in Fig. 5) and the propitious dead-time (t_D in Fig. 5). The dead-time is defined as the time from the negative edge of V_{GS2}(green waveform) to the positive edge of V_{GS1}(purple waveform). During this dead-time, the output parasitic capacitance of S_1 gets discharged, which is needed to obtain ZVS and the best attainable efficiency.

A. Resonant interval in TCM-ZVS

QSW-ZVS can be seen as a particular case of TCM-ZVS where i_{Lv} is equal to 0 (due to $V_2 = 2 \cdot V_1$). To fully understand the differences between these two conduction modes and the advantage of TCM under different V_1/V_2 ratios, it is important to analyse the resonant interval, generally neglected in literature since it is assumed that it has low impact in comparison to linear intervals.

The voltage in the switching MOSFET ($V_c(t)$) and the current through the inductor ($i_L(t)$), during the resonant interval can be obtained using (1)-(3) for boost and (2)-(4) buck behaviour (see Table I).

In this paper, boost behaviour is considered when the power flow goes from V_1 to V_2. In opposition, buck behaviour is considered when the power flows from the V_2 to V_1. Following the specifications of the prototype of Section V $V_c(t)$ and $i_L(t)$ are shown in Fig. 6 for different voltage ratios by plotting equations (1), (3) for diverse values of $|i_{Lv}|$.

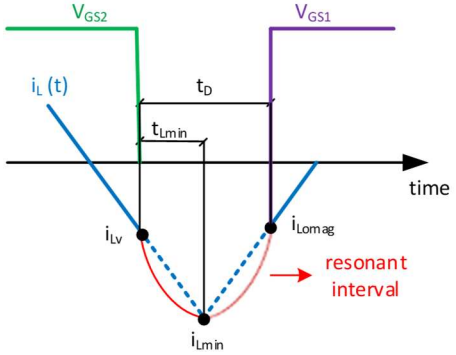

Fig. 5 Detail of $i_L(t)$ during the resonant interval.

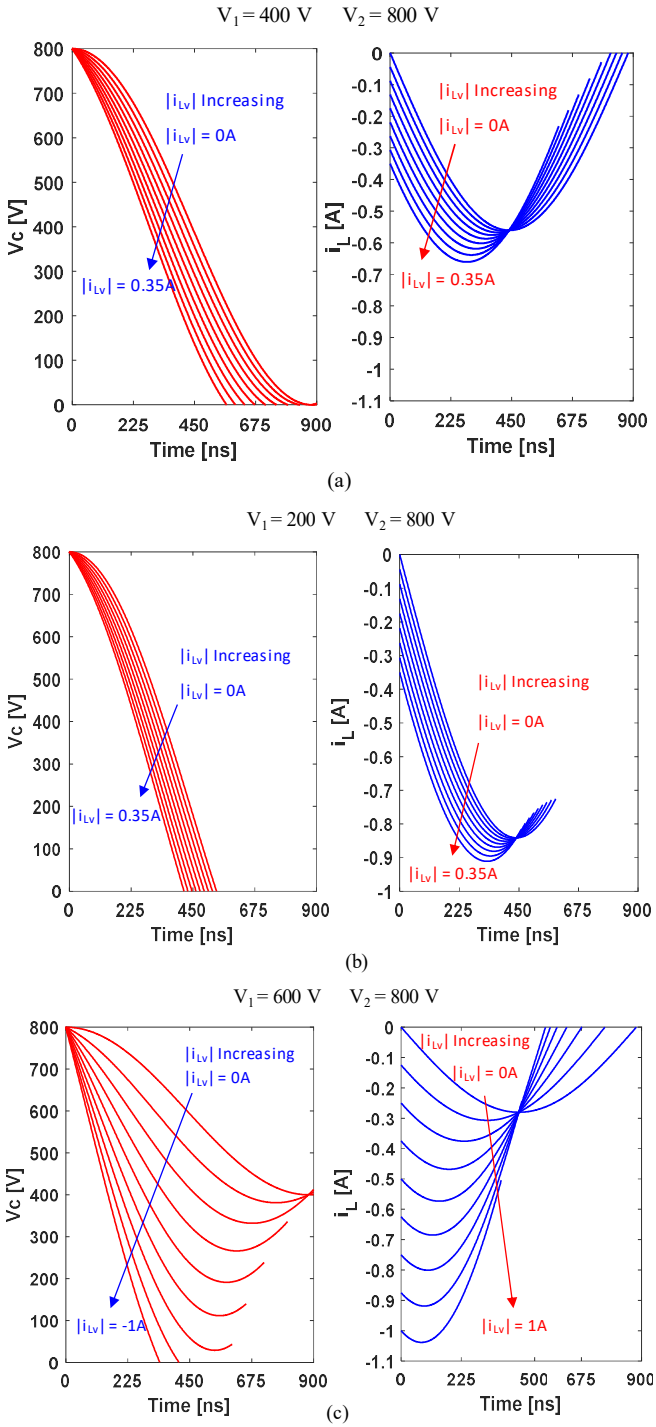

Fig. 6 $V_c(t)$ in red and $i_L(t)$ in blue for different V_1/V_2 voltage ratios. (a) 400V/800V (b) 200V/800V and (c) 600V/800V when the power is flowing defining a boost behavior.

In Fig. 6 (a), a voltage ratio $V_1=V_2/2$ is applied. This working condition corresponds to the well-known case of pure QSW-ZVS. In this case, ZVS can be achieved for any i_{LV} value below or equal to 0A provided a specific minimum t_D. It can be seen that the lower the value of i_{LV} (inductance current at the beginning of the resonant interval), the shorter the t_D needed to obtain $V_c(t)$ equal to 0V.

TABLE I EQUATIONS DURING THE RESONANT INTERVAL FOR BOOST AND BUCK CONVERTER.

BOOST		BUCK	
$V_C(t) = (V_2 - V_1) \cdot cos(w_0 t) + \left({}^{i_{Lv}}/_{C_{sw} \cdot w_0}\right) \cdot sin(w_0 t) + V_1$	(1)	$V_C(t) = V_2 \cdot \cos(w_0 t) + \left({}^{i_{Lv}}/_{C_{sw} \cdot w_0}\right) \cdot \sin(w_0 t) + V_1 - V_2$	(2)
$i_L(t) = i_{Lv} \cdot \cos(w_0 t) - C_{sw} \cdot w_0 \cdot (V_2 - V_1) \cdot \sin(w_0 t)$	(3)	$i_L(t) = i_{Lv} \cdot \cos(w_0 t) + C_{sw} \cdot w_0 \cdot V_2 \cdot \sin(w_0 t)$	(4)
$i_{Lv} = C_{sw} \cdot w_0 \cdot \sqrt{2 \cdot V_2 \cdot V_1 - V_2^2}$	(5)	$i_{Lv} = C_{sw} \cdot w_0 \cdot \sqrt{V_1^2 - 2 \cdot V_2 \cdot V_1}$	(6)
$t_D = {}^1/_{w_0} \cdot \left[\sin^{-1}\left(-\frac{V_1}{\sqrt{(V_2 - V_1)^2 + \left({}^{i_{Lv}}/_{C_{sw} \cdot w_0}\right)^2}} \right) - \tan^{-1}\left(\frac{C_{sw} \cdot w_0}{i_{Lv}} \cdot (V_2 - V_1) \right) \right]$	(7)	$t_D = {}^1/_{w_0} \cdot \left[\sin^{-1}\left(-\frac{(V_2 - V_1)}{\sqrt{V_2^2 + \left({}^{i_{Lv}}/_{C_{sw} \cdot w_0}\right)^2}} \right) - \tan^{-1}\left(\frac{C_{sw} \cdot w_0}{i_{Lv}} \cdot V_2 \right) \right]$	(8)
$i_{Lmin} = i_{Lv} \cdot \cos(w_0 t_{iLmin}) - C_{sw} \cdot w_0 \cdot (V_2 - V_1) \cdot \sin(w_0 t_{iLmin}) + V_1$	(9)	$i_{Lmin} = i_{Lv} \cdot \cos(w_0 t_{iLmin}) + C_{sw} \cdot w_0 \cdot V_2 \cdot \sin(w_0 t_{iLmin}) + V_1 - V_o$	(10)
$t_{iLmin} = {}^1/_{w_0} \cdot \cos^{-1}\left(\sqrt{\frac{1}{1 + \left(\left(\frac{C_{sw} \cdot w_0}{i_{Lv}} \right) \cdot (V_2 - V_1) \right)^2}} \right)$	(11)	$t_{iLmin} = {}^1/_{w_0} \cdot \cos^{-1}\left(\sqrt{\frac{1}{1 + \left(\left(\frac{C_{sw} \cdot w_0}{i_{Lv}} \right) \cdot V_2 \right)^2}} \right)$	(12)

Likewise, in Fig. 6(b), a voltage ratio $V_1<V_2/2$ is employed. Under this voltage conditions, ZVS is achieved using boost behaviour for any negative value of i_{LV} provided a certain t_D. In this case the t_D value is lower than in the boundary case (where $V_1=V_2/2$).

In the case of Fig. 6 (c), the voltage ratio used corresponds to $V_1>V_2/2$. In this situation, for boost behaviour not all the values for the pair i_{LV}-t_D are valid, according to (5) and (7). It must be assured a minimum i_{LV} below 0A to fully discharge the output capacitance of the device and obtain ZVS.

It must be mentioned, that the curves obtained in Fig. 6 following (1) and (3) and complying with (5) and (7) for a boost converter behaviour are analogous but inverse to those following (2), (4) , (6) and (8) for a buck converter behaviour. Therefore, in the case of a buck behavior, the most suitable working situation corresponds to $V_1<2 \cdot V_2$, while in the case of $V_1>2 \cdot V_2$ only some pairs of values i_{LV}-t_D (with i_{LV} sufficiently low) are proper to obtain ZVS.

B. Optimal pair of values i_{LV}-t_D

As it was before mentioned, depending on the operation point regarding the input/output voltage ratios, certain values for i_{LV} and t_D need to be calculated.

In addition, following the currents through the inductor expressions, $i_L(t)$, (3) and (4), it is possible to calculate the minimum value of the current during this resonance period, i_{Lmin}, (9)-(10) and the time needed to reach it, t_{iLmin}, (11)-(12), which is especially useful to make practical approaches of the current values needed to calculate the extra power losses during the negative part of $I_L(t)$ defined in (13).

In the modified loss power model, the extra dead-time losses due to the negative current going through the antiparallel diode of the MOSFET are considered by means of its characteristic I-V curve (Fig. 7),[25].

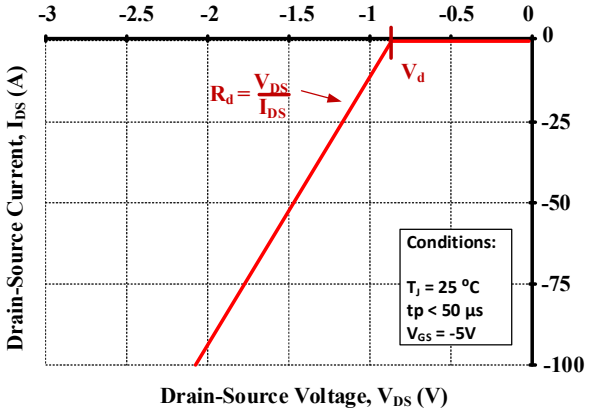

Fig. 7 Diode characteristic curve (given by Wolfspeed [25]) .

$$P_{dT} = V_d \cdot \bar{I}_{L\_tD} + I_{L\,rms\_tD}^2 \cdot R_d \quad (13)$$

where V_d and R_d are the knee voltage and conduction resistance of the diode respectively, and $\bar{I}_{L\_tD}$ and $I_{L\,rms\_tD}$ the average and rms current through the inductor during dead-time (times defined in Fig.5 and given by (7) and (8)).

Applying the new power loss model and regarding the case of a boost converter behaviour, where the voltage ratio is $V_1<V_2/2$ ($V_1>V_2/2$ for buck behaviour), the best option to achieve the highest theoretical efficiency is looking for an optimal value for i_{Lv} (i_{Lv_OPT}) and keeping always i_{Lv_OPT} equal to 0A. Under this condition, no extra dead-time power losses appear.

Conversely, when $V_1>V_2/2$, a certain pair of values i_{LV}-t_D need to be determined. In this paper, these values are calculated for the best theoretical efficiency (based on the modified power loss model) for a voltage ratio V_1/V_2 equal to 600V/800V, but expressions are valid for any other voltage ratio relation. As it can be observed in Table II and deducted

from (5)-(8), the expressions are independent of the power load. They are only circumscribed to the voltage ratio and some other characteristics variables, such as, w_o (which is defined as $\frac{1}{\sqrt{L \cdot C_{sw}}}$) or the effective output parasitic capacitance C_{sw} which is dependent of the device or the MOSFET module selected by the designer. In this particular case, the conditions needed to satisfy ZVS with the best possible theoretical efficiency are i_{Lv_OPT} equal to 0.795A and t_{D_OPT} equal to 533ns.

The practical values needed during the experimental measurements (Fig. 12) are also included (Table II) as example of the real error during the tests. There is certain deviation from the theoretical optimum values, since the resolution of the digital control only allows 10 ns steps for the t_D. Besides, an exact match of the analytical switching frequency and the optimal one is not always possible.

More pair of values for i_{Lv} and t_D have been explored, by increasing the minimum current at the beginning of the resonant period and decreasing correspondingly the dead-time needed, nonetheless, all of them incur in worse analytical efficiencies. This demonstrates the validity of the study, since values of $|i_{Lv}|$ or t_D different from $i_{Lv\ OPT}$ or $t_{D\ OPT}$ do not provide better results from an efficiency point of view.

TABLE II I_{LV} AND T_D VALUES FOR BEST THEORETICAL AND EXPERIMENTAL EFFICIENCY UNDER A 600V/800V VOLTAGE RATIO.

Power (W)	$i_{LV\ OPT}$ (A)	$t_{D\ OPT}$ (ns)	$i_{LV\ PRACT}$ (A)	$t_{D\ PRACT}$ (ns)
500	-0.795	533	-0.8	520
1000	-0.795	533	-0.79	550
2000	-0.795	533	-0.8	530
3000	-0.795	533	-0.85	510
4000	-0.795	533	-0.9	510

IV. EXPERIMENTAL RESULTS AND EFFICIENCIES

A. *Prototype and Set-up*

For testing and comparing the analytical and experimental efficiencies, a three module IPOP modular converter based on synchronous DC/DC boost converter has been built in the laboratory (Fig. 8 and Fig. 9).

The total output power is set up to 10 kW (a little more than 3 kW per module). The output voltage, V_2, is chosen as 800V, considering boost behaviour, while input voltage (V_1) varies between 200V and 600V. In addition, as power transistor, the SiC MOSFET module CCS050M12CM2 (three half-bridge six-pack module) by Wolfspeed ® is selected. It is important to note that each half bridge (HB) of the six-pack module is used to perform the switches of each module of the IPOP converter. In the new experimental results (i_{Lv} vs t_D analysis),

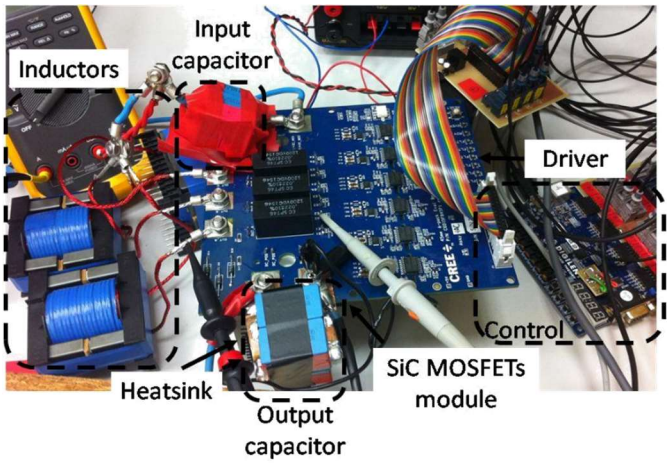

Fig. 8 Experimental prototype.

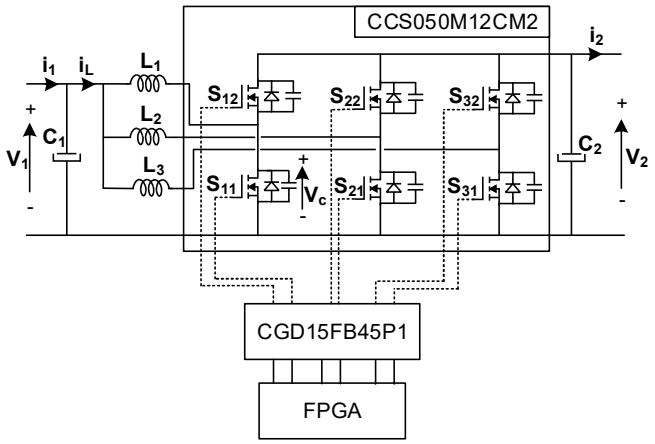

Fig. 9 Diagram of the prototype.

no modularization technique is applied, and the three HB receive the same control signals. Therefore, they withstand same voltages, currents and power, (the same as having a single converter with the inductance and MOSFETs formed by three in parallel). The commercial driver used is CGD15FB45P1, also manufactured by Wolfspeed ®.

The maximum switching frequency is 200 kHz and the inductors are constructed using Litz wire and an ETD59-3F3 ferrite core for each module.

B. *Efficiency results*

Some considerations must be remarked regarding the design of the converter for TCM-ZVS.

Initially, for a voltage ratio where V_1=400V and V_2=800V, the prototype was designed for a minimum switching frequency of 20kHz at maximum load, keeping it above the audible frequencies. In the same way the maximum switching frequency, limited by the driver, was stablished at 200kHz for very low load.

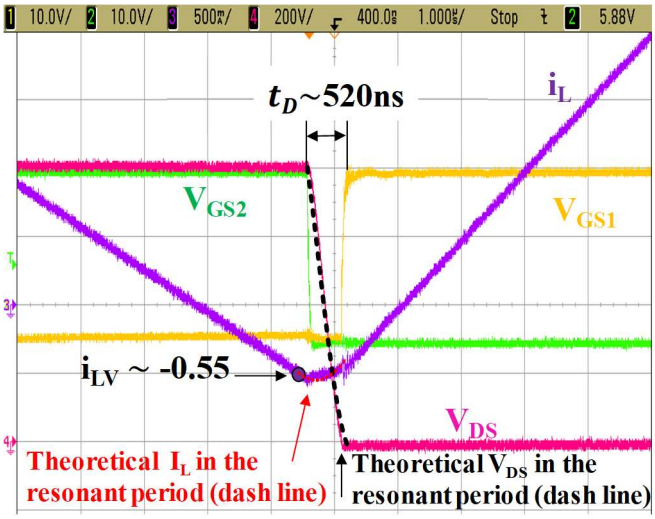

Fig. 10 Experimental waveforms of V_{GS1} (in yellow), V_{GS2} (in green), i_L (in purple), V_{DS} (in pink), theoretical I_L (in red dash line) and V_{DS} (in black dashed line) during the resonant period under a voltage ratio V_1/V_2 = 500V/800V.

As an example, some experimental waveforms of the most significative voltages and currents during the resonant period are shown in Fig. 10 for a voltage ratio V_1/V_2 equal to 500V/800V, where i_{LV_OPT}=-0.525A and t_{D_OPT}=500ns. Theoretical V_{DS} is included for comparison showing good match with the corresponding experimental waveform.

In Fig. 11, analytical and experimental efficiency results are compared for a particular voltage ratio condition $V_1<V_2/2$ where V_1=200V and V_2=800V. It should be remarked that two different experimental measurements are provided in the graph. On one side, those results, where an optimal value for i_{Lv} is set (i_{L_OPT}), match in a great extend with the expected theoretical values estimated. And, on the other side, results where the i_{Lv} value is different from the optimal. In this last case, the trend in efficiency is similar to the previous ones, yet efficiencies are slightly lower.

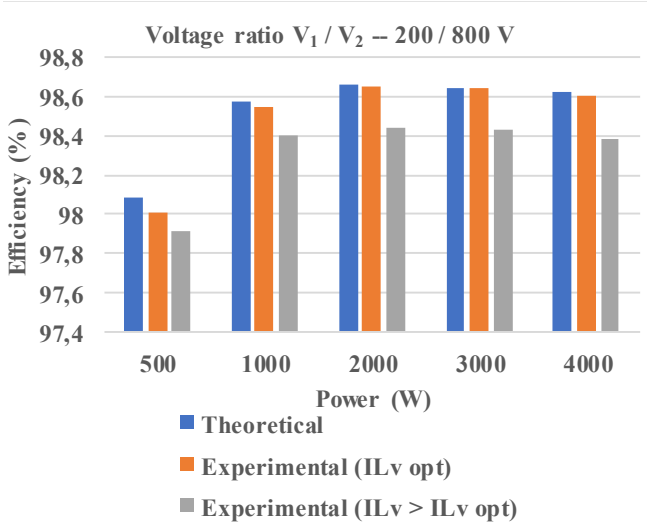

Fig. 11 Theoretical and experimental efficiencies under a 200/800V ratio. Theoretical (blue), experimental with optimum i_{Lv_OPT} (orange) and experimental with i_{Lv} not optimum (grey).

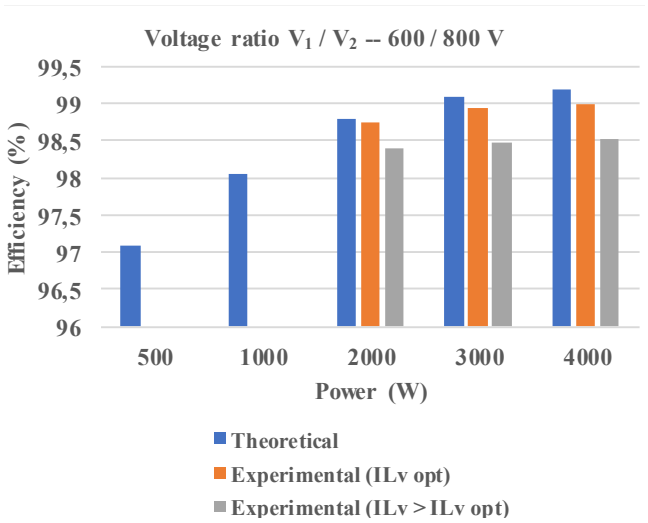

Fig. 12 Theoretical and experimental efficiencies under a 600/800V ratio. Theoretical (blue), experimental with optimum i_{Lv_OPT} (orange) and experimental with i_{Lv} not optimum (grey).

It is worth to remark that efficiencies are quantitatively rather close to those corresponding the initial conditions presented in the paper, where pure QSW-ZVS was possible since V_1=400V and V_2=800V.

In Fig. 11, equivalent efficiency results are presented for the case where $V_1>V_2/2$ where V_1=600V and V_2=800V. Again, the analytical values have good correspondence with the experimental results measured under the condition $i_{Lv}=i_{LvOPT}$, whereas efficiencies with i_{Lv} different from the optimum are to some degree lower.

Both in Fig. 11 and Fig. 12, only results for low and medium power are provided. This power range is the most interesting since higher switching frequencies are needed for lower loads and, therefore, more switching losses (including extra dead-times losses) will appear, resulting the study of i_{Lv} and t_D especially important in order to have an accurate power loss model.

Besides, even if differences among efficiencies may not seem really significant, the corresponding power loss that they cause at certain power ranges, can compromise the design and performance of the whole system.

V. CONCLUSIONS

Different conduction modes in a SiC-based synchronous boost converter, where good match is obtained between theoretical and experimental efficiency results, are revised. An accurate power losses model allows a proper selection of the conduction mode and some modularity techniques to improve the performance of the converter in a wide power range.

A study of the resonant period in a ZVS transition has been done, to provide knowledge about the voltage and current waveforms in the device corresponding to the switching point during this period, normally neglected, and the dead-time losses associated to it. Based on this study and by controlling the minimum negative current and the corresponding dead-time for different voltage ratios, ZVS is possible for this

topology without losing high flat efficiency for a wide power range.

Using the new analytical power loss model, where these extra dead-time losses are considered, and good match is achieved between theoretical and experimentally obtained results, the best value of i_{Lv} and dead-times can be obtained.

As future work, it will be studied the use of modularization strategies together with TCM-ZVS under different voltage ratios to overcome current ripple requirements coming from real applications.

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