Energization and start-up of CHB based modular three-stage Solid State Transformers

Mariam Saeed, José María Cuartas^{*}, Alberto Rodríguez, Manuel Arias and Fernando Briz University of Oviedo, Department of Electrical Engineering *INAEL Electrical Systems, Toledo, Spain

Abstract -- This paper discusses the energization and start-up process of modular three-stage Solid State Transformers (SSTs) based on a cascaded H-bridge (CHB) topology. A key element of the SST is the Auxiliary Power Supply (APS) feeding the auxiliary circuitry. Redundancy and simpler implementation can be achieved by powering the APSs from the cells DC-link capacitors, but at the expense of a more challenging start-up process of the SST. The first steps of this process must be performed before APSs are operative. This can result in undesired transient events (inrush currents, voltage sags in the capacitors voltages, etc.) which could prevent proper start-up of the SST or even jeopardize the power devices or other elements. A simple strategy for the energization and start-up of SSTs using this APSs structure is proposed. The method is valid both for grid-forming and grid-feeding operation of the SST, regardless of the energization port and without the addition of any extra circuitry. Simulation and experimental results are provided.

Index Terms—Solid State Transformers, modular-multilevel converters, start-up, auxiliary power supplies, grid forming, grid feeding.

I. INTRODUCTION

Line-Frequency Transformers (LFTs) are key elements in transmission and distribution systems to interface the different voltage levels in AC grids. Regardless of their appealing properties as cost competitiveness, high efficiency especially with high loads and reliability, LFTs suffer from several limitations. These would include voltage drop under load, sensitivity to harmonics, load imbalances and DC offsets, no overload protection and low efficiency when operating with low load levels or no load.

Solid State Transformers (SSTs), also called Power Electronic Transformers or Smart Transformers, are a power electronics-based alternative to LFTs. SSTs are equipped with controllable power semiconductors, sensors and controls, which enable them to provide several advanced functionalities, including: power flow control; reactive power, harmonics and imbalances compensation; smart protection and ride-through capabilities. Furthermore, SSTs can provide additional ports, e.g. low/high DC voltage, opening new fields of application, including interconnection with HVDC grids, integration of distributed resources, etc. In addition, the high switching frequencies of the semiconductors enable a significant reduction of the volume and weight of the core material used in their isolation stages [1]-[4]. There are several applications in which SSTs can be advantageous compared to standard LFTs. An example is smart-grid applications that require an efficient integration of distributed generation and storage resources, flexible routing mechanisms, active filtering and protection mechanism. Traction, off-shore and subsea systems are space-critical applications in which the improved performances and power density of SSTs compared to LFTs can be determinant [5], [6].

A large number of configurations can be found in literature referred to as SSTs. All of them have in common the replacement of the LFT by high frequency transformers (HFTs). There are two key aspects in the design of an SST: number of stages and modularity.

According to the number of stages, SSTs with one, two and three stages have been reported [4]–[7]. Three-stage configuration allows optimization of each converter stage to be performed independently. In addition, it enormously simplifies control and commutation strategies, thanks to the storage elements (capacitors) in the connections. Reduction of the number of stages implies the use of matrix-type topologies, which complicates the design of control and protections.

On the other hand, the use of modular multilevel SST topologies provides several advantages. Terminal voltages of the SST can be arbitrarily increased just by serializing more cells. Redundancy and consequently fault tolerant designs are possible by adding spare cells in the legs. Modular designs produce multilevel voltage wave shapes, allowing a reduction of the switching frequency (and consequently of the switching losses) [8], facilitating the design of the output filter, etc.

While there is an extensive literature on the design, modeling, control, fault tolerance, etc. of SSTs [9]-[13], very few works have discussed their energization and start-up. This includes 1) start-up of Auxiliary Power Supplies (APSs) feeding all elements used for control (digital controllers, sensors, drivers, etc.); 2) connection of the SST to the grids/loads through the corresponding pre-charge circuits, switchgears, etc. and 3) enabling the control-loops for normal operation of the SST. Furthermore, most of the work published on this topic deals with non-modular (even if they are multilevel) topologies. Charging the medium voltage (22 kV) DC-link from the LV side in a 3L-NPC is discussed in [14]. In [15], the SST is a three-stage topology composed of a rectifier, a dual half-bridge (DHB) and an inverter. The authors proposed a straightforward stage-by-stage start-up scheme, concluding that this method results in very high inrush current in the high-frequency transformer due to the voltage difference at the transformer terminals. Based on this conclusion, in [16], a scheme aiming at minimizing the charging current of the DClink capacitors during the start-up is proposed. It is based on

This work was supported in part by the European Commission FP7 Large Project NMP3-LA-2013-604057, under grant UE-14-SPEED-604057.

synchronizing their pre-charging process, resulting in effective reduction of the transformer inrush current. Strategies for the APSs design and start-up procedure in a modular three-stage SST is discussed in [17]. However, the work is focused on the validation of the APS but no simulation or experimental results of the SST start-up are provided.

A relevant issue in modular multilevel SSTs is the supply of the auxiliary circuitry of the stacked cells. APSs used for this purpose can be fed either externally from the AC grid or locally from the cell DC-links. Supplying from the low voltage DClinks enormously simplifies the design of the APS and contributes to keeping the modularity of the SST. However this adds difficulties for the SST start up.

This work studies the start-up of a modular three-stage SST based on cascaded H-bridges (CHBs) using distributed APSs. The proposed concepts are validated by simulation and experimental verification. The paper is organized as follows: Section II discusses the selected SST topology and the modes of operation. Section III addresses APS strategy selection. Cells and SST start-up are addressed in Section IV. Experimental results at the cell level are provided in Section V. As the final SST prototype is not operative yet, Section VI verifies the startup of the SST using the proposed method by means of simulation. Finally, conclusions are presented in Section VII.



Fig. 1: Modular CHB based SST topology. LVAC and HVAC grid filters are not shown for the sake of simplicity.

TABLE I: MAIN SST CHARACTERISTICS		
	Parameter	Value
SST	Rated power	105 kW
	Number of cells	21 (7 per phase)
	HV/LV grid voltage (L-L)	6 kV / 400 V
DAB	Rated power	5 kW
	Switching frequency	30 kHz
	HFT isolation	24 kV
СНВ	Rated power	5 kW
	V _{cell}	800 V
	Ccell	600 µF(film)
LV DC/AC	Rated power	105 kW
	V _{dcLV}	800 V
	CdcLV	1500 µF (film)
APS _{LV} & APS _{HV}	Input voltage	800 V
	Output voltage	24 V
	Threshold (turn-on)	350 V



Fig. 2: Modes of operation of the SST. a) Grid feeding in both ports; b) Grid forming at the LV side; c) Grid forming at the HV side. Sinusoidal voltage sources indicate that the corresponding AC port is formed externally.
Commands (*) and feedback signals required by the controls are indicated in each case. P and Q stand for active and reactive power respectively. For the sake of simplicity, feedback signals required for other purposes as grid synchronization, inner control loops and protection are not shown.

II. SST MODES OF OPERATION

The selected SST topology is shown in Fig. 1. It uses a three-stage configuration [19], [20]. Its main characteristics are shown in Table I. The high-voltage (HV) side front-end AC/DC stage uses a Cascaded H-bridge structure. The intermediate stage uses Dual Active Bridge (DAB) DC/DC converters which provide the required isolation between HV and low-voltage (LV) AC ports. The outputs of all DABs are connected in parallel to provide a LV, high-current DC-link, which is connected to the LV side DC/AC converter. HV side and isolating stages of the SST are seen to be fully modular, i.e. formed by identical stacked cells/modules. All the stages in Fig. 1 are controllable. Consequently, both HV and LV can operate either in a grid-feeding mode or in a grid-forming mode and with a bidirectional power flow. Grid-feeding is possible if the voltage in both ports is established externally by existing HV and LV AC grids. In grid-forming mode, the voltage in one port is established by the SST [19].

For proper operation of the SST, the grid must exist in at least one port, three potential working modes being possible:

1) Grid-forming in the HV (Fig. 2c). Voltage in the LV port is supplied externally. CHB stage establishes the voltage in the HV port. LV side DC/AC converter controls V_{dcLV} (Fig. 3a). DABs regulate cell voltages V_{cell} , while CHB stage controls HV side output voltage V_{acHV} .

- 2) Grid-forming in the LV side (Fig. 2b). Voltage in the HV port is supplied externally. CHB stage controls cell voltages V_{cell} , DABs regulate V_{dcLV} , while LV DC/AC stage controls the voltage in the LV port (Fig. 3b).
- 3) Grid-feeding in both sides (Fig. 2a). AC voltages in both sides (V_{acLV} and V_{acHV}) are established externally. In this case the LV-side DC/AC converter controls the LV DC-link (V_{dcLV}) and the CHB stage controls the cells voltage V_{cell} . Therefore, DABs connect two ports of constant voltage, behaving as a power source.

III. AUXILIARY POWER SUPPLIES

All configurations shown in Fig. 2 include auxiliary electronics (controls, sensors, drivers, etc.) in both sides of the DABs, which must be fed from APSs. Selection of the voltage source feeding the APSs is not trivial due to the high voltage levels and isolation requirements intrinsic to the modular design of the SST [18]. Two different approaches can be used, depending on whether APSs are fed from external AC ports or from internal DC-links.

A. APSs fed from AC ports

Such implementation when HV and LV sides APSs are fed from the LVAC port is shown in Fig. 4a.



Fig. 3: Schematic representation of the LV DC/AC power converter voltage control: a) grid feeding, b) grid forming.



Fig. 4: Schematic of one cell of the SST LV side DC/AC converter with different APS schemes. a) HV and LV sides APSs fed from the LVAC grid; b) APSs fed from the corresponding DC-links.

This configuration is therefore feasible only when the LVAC port is supplied externally (Fig. 2a and 2c), not being possible when the SST has to form the LV grid (Fig. 2b). Other variations of the scheme shown in Fig. 4a are possible as well. Feeding the APS from the HVAC will be required when the SST must form the LVAC grid. APSs with 2.2 kV input voltage are used in [21], [22]. APS with inductive power transfer are proposed in [23]-[24] for grid integration of a MV modular multilevel converter. This approach enormously simplifies start-up as full control of cells is possible at the instant of SST connection to the grid. However, it presents several relevant drawbacks:

- It requires isolation transformers (either separate or multicore structure, air core) of the same isolation level as the cell transformer, what results in bulky and expensive designs.
- Two independent APSs able to feed the auxiliary circuitry from both AC ports will be needed if the SST must provide all the operating modes shown in Fig. 2. This further increase cost and isolation concerns.
- Redundancy intrinsic to the modular design will be compromised if a central APS with multiple outputs is used [17].

B. APSs fed from DC-links

It is possible to feed the APSs from the corresponding cell DC-links. Isolation concerns are enormously alleviated if two separate APSs are used to feed each side of the DAB, as shown in Fig. 4b. Advantages of this solution are:

- Commercial, relatively cheap APSs can be used, especially for DC-link voltages <1 kV [25], as high voltage isolation is not needed.
- Redundancy of the SST modular design is not compromised.
- Enables a flexible configuration of SST modes of operation, i.e. grid-forming and grid-feeding.

The use of a single APS to feed both HV and LV sides cell circuitry is possible. However, this solution is much more problematic, as it requires a bulky isolation stage, and energization from both sides is not possible without additional start-up circuitry [17].

Regardless of its evident advantages, feeding APSs from DC-links implies a more complicated start-up procedure. The initial stages of SST energization process (i.e. since the switchgear/pre-charge resistors are connected, until the cell DC-links voltages reach the APS threshold voltage and the APSs start operating) occur without control. Furthermore, if the SST is intended to operate in a grid-forming mode, energization of the grid-forming side must be performed from the grid-feeding side through the isolation transformers of the DABs. Since all the electronics of grid-forming side are inoperative until the corresponding DC-link voltage reaches the APS threshold voltage, energization of the grid forming side must be performed through its freewheeling diodes and without any feedback. This can result in uncontrolled events as mentioned previously.

In this work, two APSs fed from the cell DC-links are placed in each cell to supply the primary and secondary side circuitry. Based on the APS input and output voltages in Table I, a commercial APS has been selected (see Table II).

IV. CELL AND SST START-UP

A methodology to start-up the cells and the SST using APSs fed from the DC-links is proposed in this section. The method is valid for all the three modes of operation described in Section II. Fig. 5 shows the cell structure which consists of two FBs in the HV side and one FB in the LV side. As already mentioned, APSs need a minimum input voltage to turn on. FBs in the HV side will be controllable once APS_{HV} turns on. All FBs in the LV and LV-side DC/AC power converter will become controllable once APS_{LV} turns on.

A. Pre-charge circuit

Pre-charge resistors are connected in both ports (see Fig. 5) to limit the inrush current flowing through freewheeling diodes (CHB stage or LV-side DC/AC) when the SST is connected to either HV or LV grids through the corresponding switchgear.



Fig. 6: Stage-by-stage SST start-up procedure for grid-forming in the LV side.

Pre-charging resistors are bypassed once the DC-links stabilize at the rectified voltage values. Pre-charging resistors and bypassing contactors in the LV side can be the same as those used normally in low-voltage DC/AC power converters. Two different options exist for the HV side. Pre-charging resistors and bypassing contactors can be connected at the input of the CHB stage (see Fig. 1). However, this solution requires high voltage resistors and contactors (6 kV in this case), significantly increasing the cost. Alternatively, charging resistors and contactors can be distributed along the cells (left side of Fig. 5). While this implementation obviously requires a larger count of resistors and contactors, they can be now low voltage components, which are significantly cheaper and easier to install. A distributed solution will be used in this work.

Selection of pre-charge resistors is made based on the desired time constant for the resulting RC circuit. A time constant of ≈ 600 ms has been selected. From the capacitors values shown in Table I, the values for the pre-charge resistors for the HV and LV sides are selected to be 1 k Ω and 450 Ω . Pre-charge circuit of cell capacitor is embedded in the cell. The corresponding bypassing contactor is controlled using the cell local control unit, being powered from the corresponding APS (see Fig. 5).

B. Start-up of three-stage SST strategies

1) Stage-by-stage start-up procedure

The simplest SST start-up scheme is the stage-by-stage method [19]. This is done by energizing the three SST converter stages in a sequential manner. This method can be used with any SST mode of operation (i.e. grid-forming and grid-feeding). Fig. 6 shows an example for this method applied to energization of the SST in grid-forming at the LV side. 1) CHB AC/DC converter stage is energized and controlled to reach the target V_{cell} voltage; 2) the DAB DC/DC stage FB1 is enabled to charge the other DC-link; 3) LV side DC/AC converter and FB2 are enabled and controlled according to this mode of operation.

This method is straightforward; however, its main inconvenience is the high inrush current associated with charging the DC-link capacitors and other parasitic elements through the isolation transformer. This inrush current is proportional to the voltage difference across the terminals of the transformer. In stage-by-stage start-up, at the instant of charging the DC-link (i.e. at (5) in Fig. 6), the voltage at one side of the transformer is the target voltage while at the other is zero, leading to high current peaks. This inrush current would implicate oversizing the power devices. This has been reported in literature [19], and therefore no results are provided in this work for the stage-by-stage method.

2) Synchronizing rectifier and DC/DC start-up

The term synchronize refers to the fact of charging DC-links simultaneously. One solution to decrease the start-up inrush current is to synchronize the charging of the DC-links in order to decrease the voltage difference at the terminals of the transformer [16].

In this modular SST topology with the selected APS strategy, it is not possible to apply this solution in grid-forming mode. The main reason is the APS threshold voltage. It is not possible to start charging both C_{cell} and C_{LV} at the same time because voltage is available only at one port of the SST. This solution is only possible in grid feeding mode as discussed in the following subsection.

3) Proposed energization and start-up procedure

The proposed procedure combines two concepts: partial synchronization of the DC-links charging to suppress the inrush current and soft-starting to avoid SST transients which could compromise continuous operation of APSs. Implementation of the proposed method for the three scenarios described in Section II is discussed in detail as follows.

Grid-forming in the HV side, grid-feeding in the LV side

This scenario assumes that the SST is connected to the LVAC grid and is required to create the MV/HVAC grid. The energization and start-up procedure is schematically shown in Fig. 7, and consists of seven steps:

- 1. Grid switchgear enabled: V_{dcLV} increases up to LVAC grid rectified voltage $V_{dcLV} = 650$ V. Transient time constant is determined by pre-charge resistors and C_{LV} .
- 2. Input voltage to APS_{LV} reaches the threshold voltage and turns on; DAB FB2 and LV side DC/AC converter become operative.
- 3. DAB FB2 is controlled to charge C_{cell} through FB1 diodes.
- 4. Input voltage to APS_{HV} reaches the threshold voltage and turns on. DAB FB1 and the CHB FB become operative.
- 5. V_{cell} and V_{dcLV} match the corresponding grid rectified voltage. Pre-charge resistors are bypassed.
- 6. V_{dcLV} and V_{cell} are boosted to their target by the LV DC/AC power converter and the DAB FB2 respectively.
- 7. SST control enabled. DABs controls V_{cell} by controlling the current transferred by the DAB, eq. (1), using phase-shift control, where *T* is half the switching cycle and L_{lk} is the leakage inductance. CHB stage forms the HVAC grid voltage.

$$i_{DAB} = \frac{d \cdot (1-d) \cdot T \cdot V_{dcLV}}{L_{uk}} \tag{1}$$

Fig. 8 shows the response of the proposed method obtained by means of simulation at the cell level. One observed inconvenience is the voltage sag in C_{LV} when the DAB starts charging C_{cell} which is readily observed from 8c (step 3). Another inconvenience is the voltage sag in V_{cell} in Fig. 8a when the CHB starts forming the voltage at the HV side (step 7). Both sags corresponds to the inrush current taking place at the same instant observed from 8b (step 3 and step 7). Being able to limit the peak inrush current, both sag magnitudes are not enough to switch off the corresponding APS. This can be done by reducing DAB FB2 duty-cycle, i.e. soft-starting [26]. To guarantee that the devices rated current is not surpassed, the inrush current magnitude can be estimated from (2), where V_L is the voltage across the transformer leakage inductance L and $\Delta i_L/\Delta t$ is the rate of change of the current.

$$V_L = L \cdot \frac{\Delta i_L}{\Delta t} \tag{2}$$

By replacing V_L with voltage applied on the transformer terminal (i.e. the grid-rectified voltage) and Δt with duty ratio times the switching period ($d \cdot 2T$), the inrush current peak value is obtained.



Fig. 8: Simulation results. Proposed start-up procedure for grid-forming in the HV side. a) Cell voltage V_{cell} , b) cell current i_{cell} , c) V_{dcLV} , d) APS_{HV} output voltage and e) APS_{LV} output voltage. Event numbers shown on top of the figure correspond to those shown in Fig. 7.

Validity of (2) has been confirmed by simulation and experimental verification, Fig. 9 shows the results for different

values of the duty. A duty cycle d=0.2 has been selected. This reduces the inrush current by a factor of ≈ 3 compared to the stage-by-stage method reported in [15] as shown in Fig. 10.



Fig. 10: Simulation results. Transformer inrush current comparing Stage-bystage method [15] and the proposed start-up method. SST was configured for grid-forming in the HV side.

Grid-forming in the LV side, grid-feeding in the HV side

The SST is connected to the MV/HVAC grid and is required to create the LVAC grid voltage. Energization and start-up procedure is schematically shown in Fig. 11. As in the previous case, it consists of seven steps:

 Grid switchgear enabled: Cell voltage increases up to the corresponding HVAC grid rectified voltage V_{cell}=606 V.

$$V_{cell} = \frac{\sqrt{2} \cdot V_{acHV-line}}{2 \cdot n_{cell}}$$
(3)

- 2. Input voltage to *APS_{HV}* reaches the threshold voltage and turns on; DAB FB1 and CHB FB become operative.
- 3. DAB FB1 is controlled to charge C_{LV} through FB2 diodes.
- 4. Input voltage to APS_{LV} reaches the threshold voltage and turns on. DAB FB2 and LV side converter become operative.
- 5. V_{cell} and V_{dcLV} match the corresponding grid rectified voltage. Pre-charge resistors are bypassed.
- 6. V_{cell} and V_{dcLV} are simultaneously boosted to their target by CHB FB and DAB FB1 respectively. Although CHB FB is operative at step (2), its control is not enabled until step (6) to avoid the control working in its critical limits.
- 7. SST control enabled. DAB controls *V*_{LV}, LV side DC/AC converter forms LVAC grid.

Fig. 12 shows the response of the proposed method in this mode of operation obtained by means of simulation at the cell level.







Fig. 12: Simulation results. Proposed start-up procedure for grid-forming in the LV side. a) Cell voltage V_{cell} , b) V_{dcLV} , c) cell current i_{cell} , d) APS_{HV} output voltage and e) APS_{LV} output voltage. Event numbers shown on top of the figure correspond to those shown in Fig. 11.



Fig. 13: Proposed start-up procedure when the SST operates in gridfeeding mode (i.e. Synchronizing rectifier and DC/DC start-up procedure).

LV and HV ports exist, SST operates in a grid-feeding mode

In grid-feeding operation mode, the SST is required to transfer power between two existing grids. Energization of the SST is relatively simpler in this case, it is discussed for completeness. The start-up in this case can use the solution of synchronizing the rectifier and DC/DC start-up [16]. The energization and start-up procedure is schematically shown in Fig. 13 and consists of five steps:

- 1. Grid contactors enabled at both ports: V_{cell} and V_{dcLV} increase synchronously up to the corresponding rectified voltages, V_{cell} =606 V and V_{dcLV} =650 V.
- 2. Input voltages to APS_{HV} and APS_{LV} reach the threshold voltages and turn on; all the three stages of the SST become operative.
- 3. Pre-charge resistors are bypassed.
- 4. *V_{cell}* and *V_{dcLV}* are simultaneously boosted to their target value by CHB FBs and LV converter.
- 5. SST control enabled. DABs control the power transfer between grids according to (1).

V. EXPERIMENTAL VERIFICATION OF CELL ENERGIZATION AND START-UP

The developed full-scale SST cell is shown in Fig. 14. Its design is the same as that schematically shown in Fig. 5. HFT provides 24 kV isolation between HV and LV sides. Cells are integrated in the SST shown in Fig. 15. SST structure is the same as in Fig. 1. Main characteristics of all the elements are listed in Table I, further constructive details can be found in Table II. Cell in Fig. 14 is fully operative; SST in Fig. 15 is currently at a commissioning stage, which mainly concerns communications with central control.



Fig. 14: Cell prototype.



Fig. 15: Three-phase CHB-based SST prototype, consisting of 21 cells (seven per phase).

TABLE II. MAIN CELE COMI ONEMIS			
	Manufacturer & characteristics	Reference	
DAB	ROHM 1.2 kV, 28 A SiC MOSFET	SCH2080KE	
	CREE 2-channel drivers	CGD15HB62P1	
СНВ	Infineon 1.7 kV Si IGBT + SiC diode	Not commercial	
	Infineon 2-channel drivers	2ED300C17-S	
FPGA	Xilinx Spartan 3E	XC3S250E-4TQG144I	
APS _{LV} &	Phoenix Contact, 60 W, 800 V	2906300	
APS _{HV}	(input voltage)		

The proposed method has been verified experimentally at cell level. Tests are performed for grid-forming in HV and LV sides. Grid-feeding is significantly easier and has been reported in the literature, so it is not discussed in this work.

Fig. 16 shows the cell start-up process performing gridforming the HV side (sequence in Fig. 7) at nominal conditions, i.e. LV grid rectified voltage of 650 V and a target DC-links voltage of 800 V. This corresponds to simulation results shown in Fig. 8. Fig. 17 shows the cell start-up process performing grid-forming the LV side (sequence in Fig. 11) at nominal conditions; HV grid rectified voltage of 606 V and a target DC-link voltage of 800 V. This corresponds to the simulation results shown in Fig. 12. Simulated and experimentally measured cell voltages for grid-forming in the HV side are overlapped in Fig. 18, the agreement being remarkable. Accuracy of simulation model is key for the validation of the whole SST start-up process by means of simulation discussed in Section VI.

VI. SIMULATION OF SST ENERGIZATION AND START-UP

SST start-up will be verified by means of simulation as the SST prototype is not operative yet. Accuracy of simulation models shown in the previous section is of paramount importance for this purpose.

SST simulation model includes grid filters, CHB balancing control.

Fig. 19 shows the simulation results of the whole SST in the case of grid-forming in the LV side according to the sequence described in Fig. 11. Fig. 20 shows the simulation results for grid-forming in the HV side according to the sequence described in Fig 7. Inrush currents and voltage sags are safely bounded and consequently turn-off of the APSs is avoided, confirming that the proposed method is valid for the energization of the modular three-stage SST.







Fig. 17: Experimental results. Grid-forming in the LV side. Top: V_{cell} and APS_{HV} output voltage; Bottom: V_{deLV} and APS_{LV} output voltage. Event numbers shown on top of the figure correspond to those shown in Fig. 11. Transition (7) is not shown in this test. Scale for V_{cell} and V_{deLV} is 200 Volts/div while for APS_{HV} and APS_{LV} is 20 Volts/div.





Fig. 18: Simulated and experimentally measured cell voltage during start-up performing grid forming the HV side.



Fig. 19: Simulation results. Proposed SST start-up in the case of grid-forming the LV side, a) V_{cell} voltage of the first cell in phase A, b) V_{dcLV} voltage, c) Cell current (i_{cell}), d) HVAC grid line currents (i_{acHV}) and e) HVAC grid line voltages (V_{acHV}). Event numbers on top of the figure correspond to those shown in Fig. 11



Fig. 20: Simulation results. Proposed SST start-up in the case of grid-forming the HV side, a) V_{cell} voltage of the first cell in phase A, b) Cell current (i_{cell}), c) V_{dcLV} voltage, d) HVAC grid line currents (i_{acHV}) and e) HVAC grid line voltages (V_{acHV}). Event numbers on top of the figure correspond to those shown in Fig. 7.

CONCLUSIONS

A procedure for energization and start-up of modular threestage CHB-based SSTs has been presented in this paper. APSs feeding the auxiliary circuitry is supplied from the cells DC links. Advantages of this strategy includes simplicity of implementation and maintaining modularity and redundancy intrinsic to CHB topology. This is at the expense of SST startup complexity. The presented method is capable of starting-up the SST bounding to safe limits undesired transients. This is without the addition of any extra circuitry and independent of the SST energization port. Simulation and experimental results showing the cell start-up at rated conditions have been provided, as well as simulation results for the SST have been provided to demonstrate the viability of the proposed concepts.

REFERENCES

- W. McMurray, "Power converter circuits having a high-frequency link," U.S. Patent 3517300, June 23, 1970.
- [2] J. W. van der Merwe and H. du T. Mouton, "The solid-state transformer concept: A new era in power distribution," in *AFRICON*, pp. 1–6, 2009.
- [3] E. R. Ronan, S. D. Sudhoff, S. F. Glover, and D. L. Galloway, "A power electronicbased distribution transformer," in *IEEE Trans. Power Del.*, vol. 17, no. 2, pp. 537– 543, Apr. 2002.
- [4] J. Kolar and G. Ortiz, "Solid-state-transformers: Key components of future traction and smart grid systems," in *Int. Power Electronics Conf. (IPEC)*, Hiroshima, Japan, 2014.
- [5] M. Steiner and H. Reinold, "Medium frequency topology in railway applications," in *Proc. European Conf. Power Electronics and Applications*, Aalborg, Denmark, pp. 1–10, 2007.
- [6] S. Falcones, M. Xiaolin, and R. Ayyanar, "Topology comparison for solid state transformer implementation," in *Proc. IEEE Power and Energy Society General Meeting*, pp. 1–8, 2010.

- [7] C. Zhao, D. Dujic, A. Mester, J. K. Steinke, M. Weiss, S. Lewdeni-Schmid, T. Chaudhuri, and P. Stefanutti, Philippe, "Power electronic traction transformer: Medium voltage prototype," in *IEEE Trans. Ind. Electron.*, vol. 61, no. 7, pp. 3257–3268, July 2014.
- [8] M. Malinowski, K. Gopakumar, J. Rodriguez and M. A. Perez, "A Survey on Cascaded Multilevel Inverters," in *IEEE Transactions on Industrial Electronics*, vol. 57, no. 7, pp. 2197-2206, July 2010.
- [9] G. Ortiz, M. G. Leibl, J. E. Huber and J. W. Kolar, "Design and Experimental Testing of a Resonant DC–DC Converter for Solid-State Transformers," in *IEEE Transactions on Power Electronics*, vol. 32, no. 10, pp. 7534-7542, Oct. 2017.
- [10] N. B. Y. Gorla, S. Kolluri, P. J. Chauhan and S. K. Panda, "A fault tolerant control approach for a three-stage cascaded multilevel solid state transformer," in 2017 IEEE 18th Workshop on Control and Modeling for Power Electronics (COMPEL), Stanford, CA, pp. 1-6, 2017.
- [11] S. Xu, S. Lukic, A. Q. Huang, S. Bhattacharya, and M. Baran, "Performance evaluation of solid state transformer based microgrid in FREEDM systems," in *IEEE Applied Power Electronics Conf. and Exposition (APEC)*, pp. 182–188, 2011.
- [12] T. Zhao, G. Wang, S. Bhattacharya, and A. Q. Huang, "Voltage and power balance control for a cascaded H-bridge converter-based solid state transformer," in *IEEE Trans. Power Electron.*, vol. 28, no. 4, pp. 1523–1532, Apr. 2013.
- [13] European Union. Advanced power converter for universal and flexible power management in future electricity networks, UNIFLEX, FP6, EC Contract n: 019794 (SES6) European Commission, Directorate J-Energy.
- [14] K. Mainali, S. Madhusoodhanan, A. Tripathi, D. Patel and S. Bhattacharya, "Startup scheme for solid state transformers connected to medium voltage grids," in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, Charlotte, NC, pp. 1014-1021, 2015.
- [15] X. Liu, L. Liu, H. Li, K. Corzine and T. Guo, "Study on the start-up schemes for the three-stage solid state transformer applications," in *IEEE Energy Conversion Congress and Exposition (ECCE)*, Raleigh, NC, pp. 3528-3532, 2012.
- [16] X. Liu, H. Li and Z. Wang, "A Start-Up Scheme for a Three-Stage Solid-State Transformer With Minimized Transformer Current Response," in *IEEE Transactions on Power Electronics*, vol. 27, no. 12, pp. 4832-4836, Dec. 2012.
- [17] L. B. Kehler, A. M. Kaminski, J. R. Pinheiro, C. Rech, T. B. Marchesan and R. R. Emmel, "Auxiliary power supply for solid state transformers," in *IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, Monte Carlo, pp. 193-196, 2016.
- [18] D. Cottet et al., "Integration technologies for a medium voltage modular multilevel converter with hot swap capability," in *IEEE Energy Conversion Congress* and Exposition (ECCE), Montreal, QC, pp. 4502-4509, 2015.
- [19] F. Briz, M. Lopez, A. Rodriguez and M. Arias, "Modular Power Electronic Transformers: Modular Multilevel Converter versus Cascaded H-Bridge Solutions," in *IEEE Industrial Electronics Magazine*, vol. 10, no. 4, pp. 6-19, Dec. 2016.
- [20] M. López, F. Briz, M. Saeed, M. Arias and A. Rodríguez, "Comparative analysis of modular multiport power electronic transformer topologies," in *IEEE Energy Conversion Congress and Exposition (ECCE)*, Milwaukee, WI, , pp. 1-8, 2016.
- [21] T. Meng, Y. Song, Z. Wang, H. Ben and C. Li, "Investigation and Implementation of an Input-Series Auxiliary Power Supply Scheme for High-Input-Voltage Low-Power Applications," in *IEEE Transactions on Power Electronics*, vol. 33, no. 1, pp. 437-447, Jan. 2018.
- [22] Tao Meng, Chunyan Li, Hongqi Ben, Xuesong Wang and Junbao Zhao, "An input-series multiple-output auxiliary DC/DC converter," in *IEEE 8th International Power Electronics and Motion Control Conference (IPEMC-ECCE Asia)*, Hefei, pp. 3056-3060, 2016.
- [23] D. Peftitsis, M. Antivachis and J. Biela, "Auxiliary power supply for mediumvoltage modular multilevel converters," in 17th European Conference on Power Electronics and Applications (EPE'15 ECCE-Europe), Geneva, pp. 1-11, 2015.
- [24] F. Van der Pijl, J. Ferreira, P. Bauer, and H. Polinder, "Design of an Inductive Contactless Power System for Multiple Users," in *IEEE Industry Applications Conference*, vol. 4, , pp. 1876–1883, Oct 2006.
- [25] A. Rodriguez et al., "Auxiliary power supply based on a modular ISOP flyback configuration with very high input voltage," in *IEEE Energy Conversion Congress* and Exposition (ECCE), Milwaukee, WI, pp. 1-7, 2016.
- [26] S. Inoue and H. Akagi, "A Bidirectional DC–DC Converter for an Energy Storage System with Galvanic Isolation," in *IEEE Transactions on Power Electronics*, vol. 22, no. 6, pp. 2299-2306, Nov. 2007.