Evaluation of Superjunction MOSFETs in Cascode Configuration for Hard-Switching Operation

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Abstract—**Superjunction MOSFETs in cascode configuration with low-voltage silicon MOSFETs are evaluated in this paper. The proposed structure combines the good switching performance provided by the cascode configuration with the benefits of the silicon technology such as its robustness, maturity and low-cost. This paper aims to explain and to demonstrate the reduction of switching losses of Superjunction MOSFETs in cascode configuration with respect to their standalone counterparts (directly driven). A detailed simulation analysis of power loss contributions is carried out under hard-switching operation. Moreover, experimental evidence is provided using a boost converter (100 V to 400 V) operating in continuous conduction mode for different switching frequencies (100 kHz to 400 kHz) and output power levels (180 W to 500 W).**

Index Terms— **High-frequency, high power density, high-efficiency, cascode configuration, Superjunction MOSFET, silicon.**

I. INTRODUCTION

DURING last decade, High-Voltage (HV) Superjunction MOSFETs (SJ-FETs) have dominated the market of power switching devices for a voltage that ranges between 600 V and 900 V. The wide use of these devices is related to three qualities: high reliability, high maturity and good balance between performance and cost. SJ-FET portfolios increased their complexity by offering application-oriented devices. Three main families of SJ-FETs can be identified in the market depending on the target application: hard-switching, soft-switching and fast reverse recovery.

Nowadays, a lot of research efforts are focused on increasing the power density of DC-DC power converters by increasing the switching frequency in order to miniaturize the required passive components. To fulfill this target, since their commercialization, each new generation of SJ-FET optimized for hard-switching operation overcomes the previous one by minimizing switching and conduction losses when operating in the first quadrant. For this purpose, the reduction of the on-state resistance (R_{ON-HV}) per unit of area (sR_{ON-HV}), the internal gate resistance (R_{G_INT}), the gate-to-drain charge (Q_{GD}) and the energy stored in the output capacitance (E_{OSS}) become crucial [1].

However, the continuous improvement of the SJ-FET technology is expected to reach important technological and physical limits in the following years. In fact, a stagnation of the current density capability has been theoretically predicted for forthcoming SJ-FET generations [2]. Consequently, a limit on lowering the SJ-FET parasitic capacitances will appear due to the restrictions in downsizing active area, thus limiting the operating switching frequency. Therefore, a research for alternative silicon solutions, different from shrinking the device cell-pitch, is mandatory in future for improving the performance without relinquishing the cost and the robustness provided by the silicon technology.

At this point, the use of transistors based on Wide-Bandgap (WBG) materials has emerged as the suitable option to increase the power density. In this sense, the Cascode Configuration (CC) with a Low-Voltage Silicon MOSFET (LV-FET) has become the preferred approach for some semiconductor companies to achieve normally-off Gallium Nitride (GaN) and Silicon Carbide (SiC) power transistors during last five years [3]-[6]. In the range of 600 V, GaN in CC (GaN-CC) has demonstrated superior switching performance than widely used SJ-FETs in standalone configuration [7]-[9]. However, recent works [10]-[11] state that most of the improvement achieved by the GaN-CC is due to the low input capacitance provided by the LV-FET rather than the WBG material. Hence, these works

conclude that a SJ-FET in CC with a LV-FET (SJ-CC) would be equally valid for switching performance enhancement (Fig. 1). At this point, there is an absence of insight and variety of operating conditions to demonstrate the SJ-CC possible benefits. Moreover, some statements, such as attributing the switching losses reduction achieved by the CC to the low input capacitance of the LV-FET, are questionable as will be demonstrated in this work. In this sense, there is a lack of prior art about high-voltage silicon devices in CC, with the exception of some 30-year old works regarding Bipolar Junction Transistors (BJT) in CC [12]-[13]. Although the efficiency improvement has not been demonstrated yet in specific applications, some contributions have recently revisited the topic. A theoretical model of the SJ-CC switching mechanism that pays special attention to the critical parasitic elements is detailed in [14]. Moreover, the third-quadrant performance improvement achieved by the SJ-CC is also presented in [15].

This paper aims to prove that the SJ-CC can outperform the SJ-FET in standalone configuration when the switching frequency is in the order of hundreds of kHz and operating under hard-switching and high-forward current conditions. As a result, an increase of the power density can be achieved without giving up on the low-cost, robustness and maturity of silicon technology. This paper extends [16] by showing that the benefits of the SJ-CC depend on the SJ-FET and LV-FET selection. Moreover, a detailed analysis of the LV-FET avalanche during the turn-off of the SJ-CC is carried out, including the effect of adding a capacitor between the drain and the source of the LV-FET to reduce the avalanche. In addition, the improvement achieved by the SJ-FET is evaluated performing a comparison to a commercial available GaN-CC, which stands out for its switching performance.

The paper is organized as follows. A brief description of the SJ-CC behavior during the on-state, the off-state, the turn-on transition and the turn-off transition is provided in section II, paying special attention to the avalanche process of the LV-FET body diode. An exhaustive analysis of the switching energy losses in the SJ-CC is given in section III. The mixed-mode simulations attached in this section support the comparison between the switching energy dissipated into a SJ-CC and in a SJ-FET in standalone configuration for different operating conditions. The section is completed identifying the operating conditions where the SJ-CC overcomes the SJ-FET in standalone configuration and determining the reasons of this improvement. Finally, a wide experimental study to corroborate the theoretical analysis is provided in section IV and the conclusions are gathered in section V.

II. OPERATING PRINCIPLE OF THE SUPERJUNCTION MOSFET IN CASCODE CONFIGURATION (SJ-CC)

A. Operating Principle During the On-State and the Off-State

The SJ-CC is made up of a SJ-FET and a LV-FET as high-voltage and low-voltage silicon transistors respectively. Moreover, a constant voltage source (V_A) connected between the gate of the SJ-FET and the source of the LV-FET is needed due to the positive threshold voltage of the high-voltage device.
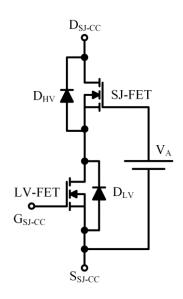

Fig. 1. Schematic circuit of a SJ-CC.

From a general point of view, the SJ-CC operates as a single switch that has an equivalent gate ($G_{SJ\text{-}CC}$), drain ($D_{SJ\text{-}CC}$) and source ($S_{SJ\text{-}CC}$) (Fig. 1).

During the on-state, the gate to source voltage of the LV-FET is fixed by the output voltage of the driver in high-state (i.e. V_{Dri}), while the gate to source voltage of the SJ-FET is the difference between the constant voltage source V_A and the voltage drop of the LV-FET channel during conduction, which can be neglected. Hence, both MOSFETs are conducting with a different contribution to the whole on-state resistance. In general, the SJ-CC is designed by using a LV-FET with an on-state resistance ($R_{ON\text{-}LV}$) almost equal to the 10% of the SJ-CC on-state resistance.

During the off-state, the SJ-FET blocks most of the voltage while the LV-FET blocks a voltage that is equal or lower than its avalanche voltage (V_{Aval}). The gate to source voltage of the LV-FET is equal to the output voltage of the driver in low-state, while the gate to source voltage of the SJ-FET corresponds to ($V_A - V_{Aval}$), which must be lower or equal to 0 V to properly achieve the off-state of the SJ-CC.

Table I summarizes the voltage stresses of the SJ-CC assuming that V_X is the voltage that the SJ-CC must block

TABLE I. VOLTAGE STRESSES AT THE SJ-CC DURING THE ON-STATE AND THE OFF-STATE

	Voltage stress (V)	
	On-State	**Off-State**
$V_{GS\text{-}LV}$	V_{Dri}	0
$V_{DS\text{-}LV}$	$I_X \cdot R_{ON\text{-}LV}$	$\leq V_{Aval}$
$V_{GD\text{-}LV}$	$V_{Dri} - I_X \cdot R_{ON\text{-}LV}$	$\geq -V_{Aval}$
$V_{GS\text{-}HV}$	$V_A - I_X \cdot R_{ON\text{-}LV}$	$\geq V_A - V_{Aval}$
$V_{DS\text{-}HV}$	$I_X \cdot R_{ON\text{-}HV}$	$\geq V_x - V_{Aval}$
$V_{GD\text{-}HV}$	$V_A - I_X \cdot (R_{ON\text{-}HV} + R_{ON\text{-}LV})$	$V_A - V_X$

during the off-state and that I_X is the conducted current during the on-state.

B. Description of the Turn-On and Turn-Off Transitions

Fig. 2 shows the schematic used to model the hard-switching mechanism of the SJ-CC, including the most relevant parasitic elements. Both MOSFETs are modeled as ideal switches with their body diodes (D_{HV} and D_{LV}) and with their parasitic capacitances between gate and source (C_{GS-HV} and C_{GS-LV}), drain and source (C_{DS-HV} and C_{DS-LV}) and gate and drain (C_{GD-HV} and C_{GD-LV}). In addition, this schematic considers the parasitic inductance (L_{PAR}) that appears between the source of the SJ-FET and the drain of the LV-FET in order to model a delay introduced by the layout during the turn-on and turn-off of the SJ-CC. The schematic also shows a current source (I_X) modeling the current that flows through the inductive load, the freewheeling diode (D_X) and the voltage source (V_X) that represents the voltage that the SJ-CC must block during the off-state, performing a traditional inductive load circuit. The driver of the LV-FET is modeled as a square waveform voltage source (v_{Dri}) that provides V_{Dri} and 0 V during the high-state and low-state respectively. Some considerations must be taken into account about the gate resistance of both MOSFETs (R_{G-LV} and R_{G-HV}). R_{G-LV} includes the internal gate resistance of the LV-FET, the output resistance of the driver and the external gate resistance. Regarding R_{G-HV}, it includes the internal gate resistance of the SJ-FET.

In order to support the explanation of different concepts that appear in the paper, a qualitative description of both transitions is necessary. This description simplifies the detailed analysis of [14] omitting some sections that do not have a crucial impact in the results that will be shown in this paper and detailing only the most remarkable 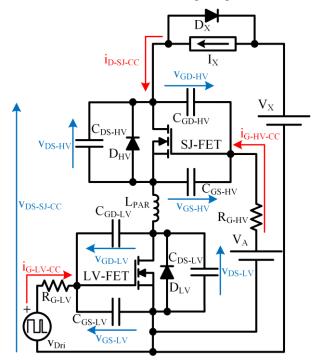facts of each stage. Fig. 3 shows the main voltage and current waveforms during both transitions highlighting the different stages.

Turn-On Transition

Before the turn-on transition starts, both MOSFETs are open circuit and I_X flows through D_X. The transition starts when v_{Dri} changes from 0 V to V_{Dri}.

Stage I (interval t_0-t_1): LV-FET delay period. The driver charges C_{GS-LV} and C_{GD-LV}. The stage ends when v_{GS-LV} reaches the threshold voltage of the LV-FET (V_{LV-TH}).

Fig. 2. Schematic circuit used to model the hard-switching mechanism of the SJ-CC.
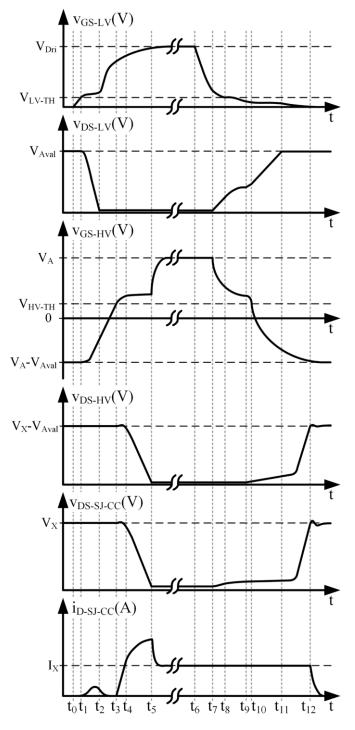

Fig. 3. Main voltage and current waveforms at the SJ-CC during the turn-on and the turn-off.

Stage II (interval t_1-t_2): the fall of the LV-FET drain to source voltage. When v_{GS-LV} reaches V_{LV-TH}, the LV-FET channel starts conducting and the current rises with v_{GS-LV}. This current discharges C_{DS-LV} while the voltage source V_A charges C_{GS-HV}. The rise of v_{GS-HV} is delayed with respect to the fall of v_{DS-LV} due to L_{PAR}. During this stage, the Miller effect occurs at the LV-FET (i.e. most of the current delivered by the driver flows through C_{GD-LV} while v_{GS-LV} remains almost constant). The stage ends when C_{DS-LV} is fully discharged.

Stage III (interval t_2-t_3): SJ-FET delay period. The Miller Effect of the LV-FET has finished and, therefore, both C_{GS-LV} and C_{GD-LV} are charged by the driver. Consequently, the resistance of the LV-FET channel falls until it reaches R_{ON-LV}. V_A keeps charging C_{GS-HV} and the stage ends when v_{GS-HV} reaches the threshold voltage of the SJ-FET (V_{HV-TH}).

Stage IV (interval t_3-t_4): the rise of the SJ-FET channel current. When v_{GS-HV} reaches V_{HV-TH}, the SJ-FET channel starts conducting and the current rises with v_{GS-HV}. This current comes from I_X and, as a consequence, the current through D_X falls. The stage ends when the whole drain current of the SJ-CC ($i_{D-SJ-CC}$) is equal to I_X.

Stage V (interval t_4-t_5): the fall of the SJ-FET drain to source voltage. The SJ-FET channel conducts I_X and also an extra level of current which comes from the discharge of C_{DS-HV}. The reverse recovery effect of D_X occurs and, therefore, the SJ-FET channel also conducts the current caused by this effect. During this stage, again the Miller effect occurs at the SJ-FET (i.e. most of the current delivered by the V_A flows through C_{GD-HV} while v_{GS-HV} remains almost constant). The stage ends when the drain to source voltage of the SJ-CC (i.e. $v_{DS-SJ-CC}$) falls to $I_X \cdot (R_{ON-HV}+R_{ON-LV})$.

<u>Turn-Off Transition</u>

Before the turn-off transition starts, the SJ-CC conducts I_X, while D_X blocks V_X. The transition starts when v_{Dri} changes from V_{Dri} to 0 V.

Stage I (interval t_6-t_7): LV-FET delay period. The driver discharges both C_{GS-LV} and C_{GD-LV}. The stage ends when v_{GS-LV} reaches a value that causes that the LV-FET enters into saturation region.

Stage II (interval t_7-t_8): saturation of the LV-FET channel current. The LV-FET channel current falls with v_{GS-LV} and it is not able to conduct the whole I_X. The remaining load current flows through several parasitic capacitances of the SJ-CC. In fact, this current partially charges C_{DS-LV} and discharges C_{GS-HV}. The stage ends when v_{GS-LV} achieves V_{LV-TH}.

Stage III (interval t_8-t_9): SJ-FET delay period. There is not current flowing through the channel of the LV-FET because v_{GS-LV} falls below V_{LV-TH}. During this stage, v_{GS-HV} and v_{DS-LV} keep decreasing and increasing respectively. The stage ends when v_{GS-HV} falls to a value that causes the SJ-FET entry into saturation region.

Stage IV (interval t_9-t_{10}): saturation of the SJ-FET channel current. The SJ-FET channel current falls with v_{GS-HV} and it is not able to conduct the whole I_X. The remaining load current charges and discharges C_{DS-HV} and C_{GD-HV} respectively. The stage ends when v_{GS-HV} falls to V_{HV-TH}.

Stage V (interval t_{10}-t_{11}): final rise of the LV-FET drain to source voltage. There is not current flowing through the channel of the SJ-FET because v_{GS-HV} falls below V_{HV-TH}. The stage ends when v_{DS-LV} achieves a value that causes that D_{LV} enters in avalanche state.

Stage VI (interval t_{11}-t_{12}): remaining charge of C_{DS-HV} and discharge of C_{GD-HV}. D_{LV} remains in avalanche state conducting most of the current that comes from the charge of C_{DS-HV}. C_{DS-HV} and C_{GD-HV} are strongly nonlinear versus v_{DS-HV}. Therefore, these capacitances suffer variations of several orders of magnitude during both transitions, being critical during the turn-off. According to [17], this phenomenon can be modeled as two different values of C_{DS-HV} and C_{GD-HV}. If the drain to source voltage of the SJ-FET is below a certain value (i.e. a frontier value that is typically fixed between 30 V and 60 V for a SJ-FET), both capacitances present a specific value close to nF range (C_{DS-HV1} and C_{GD-HV1}). On the other hand, if the voltage is above the frontier value, these values are in the order of pF (C_{DS-HV2} and C_{GD-HV2}). As a consequence, once v_{DS-HV} is higher than frontier value of the SJ-FET, the C_{DS-HV} and C_{GD-HV} values fall rapidly and a high increase of the $dv_{DS-SJ-CC}/dt$ arises. The stage ends when $v_{DS-SJ-CC}$ reaches a value that forward biases the freewheeling diode (i.e. equal to V_X plus the knee voltage of D_X).

C. LV-FET Avalanche Analysis

The avalanche of the LV-FET during the SJ-CC turn-off transition should be avoided in order to ensure reliability and to maximize the benefits of the CC. As it will be shown in this section, the avalanche depends on the charge that C_{DS-HV} stores (Q_{DS-HV}) and the sum of the charge that C_{GS-HV}, C_{DS-LV} and C_{GD-LV} store during the turn-off of the SJ-CC (Q_X). This phenomenon has also been reported for GaN-CC [18]. However, Q_{DS-HV} of a SJ-FET is higher than the GaN HEMT one, being the avalanche more critical in a SJ-CC than in a GaN-CC.

This section is focused on identifying the high number of elements that are involved in the avalanche process in order to support the energy analysis that will be presented in section III and the methodology that will be proposed in section IV to avoid it. Due to the high complexity of the SJ-CC turn-off mechanism, some simplifications are considered. It is assumed that R_{G-HV}, R_{ON-LV} and R_{ON-HV} values are negligible and the impact of L_{PAR} is obviated.

Fig. 4(a) shows the simplified circuit during the stage III of the turn-off. Until the end of this stage, C_{DS-HV} has not stored any charge because the SJ-FET is still fully turned on. However, according to the explanation of the previous section, C_{GS-HV}, C_{DS-LV} and C_{GD-LV} have already stored some charge during stages I (Q_{X_S1}), II (Q_{X_S2}) and III (Q_{X_S3}). Note that Q_{X_Si} defines the charge stored in C_{GS-HV}, C_{DS-LV} and C_{GD-LV} during the stage i, not the charge stored since the beginning of the turn-off until the end of stage i.

In stage IV, a part of I_X charges C_{DS-HV} because the channel of the SJ-FET is not able to conduct all the current. As Fig. 4(b) shows, the current that flows through the channel of the SJ-FET (i_{Ch-HV}) plus the current that charges C_{DS-HV} (i_{DS-HV}) is flowing

through C_{GS-HV} (i_{SG-HV}), C_{DS-LV} (i_{DS-LV}) and C_{GD-LV} (i_{DG-LV}). Therefore, the charge stored in C_{DS-HV} ($Q_{DS-HV-S4}$) is lower than the sum of the charge stored in C_{GS-HV}, C_{DS-LV} and C_{GD-LV} during this stage (i.e. Q_{X-S4}).

In stage V (see Fig. 4(c)), there is no difference between i_{DS-HV} and the sum of i_{SG-HV}, i_{DS-LV} and i_{DG-LV}. As a consequence, the charge stored in C_{DS-HV} during this stage ($Q_{DS-HV-S5}$) is equal to the sum of the charge stored in C_{GS-HV}, C_{DS-LV} and C_{GD-LV} (i.e. Q_{X-S5}). In this stage, there are two different possible final situations. In the first one, there is no avalanche and $v_{DS-SJ-CC}$ reaches a value which forward biases the freewheeling diode. This implies that the whole charge that C_{GS-HV}, C_{DS-LV} and C_{GD-LV} must store does not cause a v_{DS-LV} value equal or higher than V_{Aval} at the end of the stage V. In the second one, these capacitors are not able to store the required charge because it implies a final value of v_{DS-LV} higher than V_{Aval}, introducing the LV-FET body diode in avalanche stage. In this case, the stage VI must be considered (Fig. 4(d)). Here, the LV-FET can be
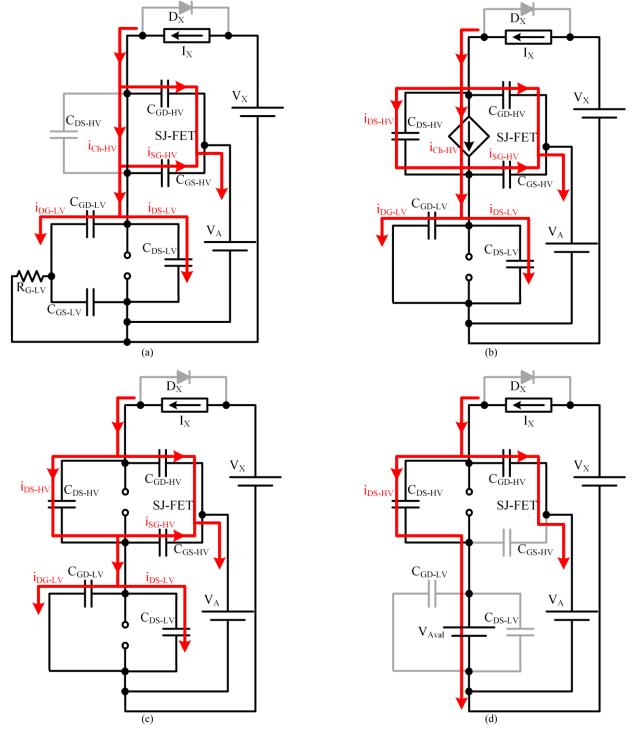

Fig. 4. Simplified circuit schematics of the main turn-off stages involved in the LV-FET avalanche, highlighting the load current distribution: (a) Stage III. (b) Stage IV. (c) Stage V. (d) Stage VI.

modeled as a constant voltage source equal to V_{Aval}. Note that the remaining charge of C_{DS-HV} (Q_{X-S6}) will flow through the LV-FET body diode. Therefore, the higher the Q_{X-S6} value, the higher the avalanche power losses.

It is important to remark that the charge that C_{GS-HV}, C_{DS-LV} and C_{GD-LV} must be able to store to avoid the LV-FET avalanche (Q_{X-Req}) is higher than Q_{DS-HV} due to two facts. The first one is that the charging process of C_{DS-HV} begins with a certain delay with respect to C_{GS-HV}, C_{DS-LV} and C_{GD-LV} due to the turn-off mechanism itself (stages I to III). The higher the delay, the higher the Q_{X-Req} value. The second one is that i_{DS-HV} is lower than the sum of i_{SG-HV}, i_{DS-LV} and i_{DG-LV} in the stage IV. Therefore, C_{GS-HV}, C_{DS-LV} and C_{GD-LV} store more charge than C_{DS-HV} during this stage. Finally, equation (1) defines Q_{X-Req}:

$$Q_{X-Req} = Q_{X-S1} + Q_{X-S2} + Q_{X-S3} + Q_{X-S4} - Q_{DS-HV-S4} + \\ + Q_{DS-HV}. \quad (1)$$

Although this detailed explanation about the avalanche of the LV-FET seems to be unnecessary now, Section III and Section IV will show that this phenomenon has a critical impact on the SJ-CC performance. In addition, the relation between the avalanche and the charge stored in the parasitic capacitances of the transistors is the key point to adequately select the SJ-FET and the LV-FET of the SJ-CC.

III. Energy Analysis

This section is focused on identifying the sources of power losses when a SJ-FET is used in CC or in standalone configuration. Later, the impact of each one with respect to the whole losses will be evaluated. The arguments presented are justified by accurate mixed-mode simulations, which combine the SPICE circuit shown in Fig. 2 with the Finite-Element (FE) structures shown in Fig. 5. These simulations are carried out in a commercial TCAD simulator that consistently solves circuit and physical equations by iterative methods, connecting electrodes in FE structures to circuit nodes [19]. The physical equations solved in the mesh of points for every FE structure are Poisson, electron and hole current continuity, being the drift-diffusion transport model activated for this purpose. On what concerns to the rest of physical models, all the default models for silicon are set with exception of the avalanche model (carrier generation) that has been adjusted to fit better the breakdown voltage in LV-FETs implemented for experimental prototypes.

The procedure to run the simulations is defined as it follows. Firstly, V_X is ramped to 400 V while the LV-FET gate is off.

Afterwards, V_X is fixed to 400 V and I_X ranges between 1.5 and 12 A in order to test different operating conditions. Two SJ-FETs are tested for the simulation comparison being analyzed both in standalone configuration and in CC with the same LV-FET. It is important to note that the external gate resistance (R_G) is always 6.8 Ω, being the one that provides the best results of the SJ-FETs in standalone configuration. In general, the lower the R_G value, the lower the switching losses of the SJ-FET in standalone configuration. However, mainly due to the parasitic inductors, a low value of R_G may cause oscillations of the gate to source voltage, reducing the performance. The main characteristics of the transistors used in the mixed-mode simulations are summarized in Table II. Both SJ-FETs are optimized for hard-switching operation. SJ-FET B provides an extremely low sR_{ON-HV}, but its architecture causes an increase of the Q_{OSS} value with respect to the SJ-FET A.

A. Source of Losses in a SJ-FET in Standalone Configuration and in CC

Traditionally, three kinds of power losses have been defined for power MOSFETs: conduction, switching and gate-drive losses. Since this work aims to deeply identify the sources of power losses when a SJ-FET is used in CC or in standalone configuration, these three global definitions will be split into smaller terms. Equation (2) defines the switching energy dissipated by a SJ-FET in standalone configuration (E_{Sw_Stand}) as the energy dissipated during the turn-on ($E_{Sw\_On\_HV\_Stand}$) plus the turn-off ($E_{Sw\_Off\_HV\_Stand}$). According to (3) and (4),
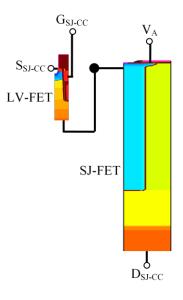

Fig. 5. FE structures in the SJ-CC model for mixed-mode simulation.

TABLE II. CHARACTERISTICS OF THE TRANSISTORS USED IN THE MIXED-MODE SIMULATIONS

	sR_{ON} (mΩ·cm²)	R_{ON} (mΩ)	BV_{DSS} (V)	R_{G_Int} (Ω)	Q_G [*1] (nC)	Q_{GS} [*1] (nC)	Q_{GD} [*1] (nC)	V_{TH} (V)	C_{iss} [*2] (pF)	C_{oss} [*2] (pF)	Q_{OSS} (nC)	Fast Reverse Recovery
SJ-FET A	38	100	600	1	146	22	77	3.5	1450	130	128	No
SJ-FET B	12	100	600	1	40	8	15	3.5	1020	40[*2]	155	No
LV-FET	-	10	30	0.5	-	-	-	6	450	-	12	No

[*1] at V_{GS} = 12 V, I_D = 12 A   [*2] at V_{GS} = 0 V, V_{DS} = 400 V

$E_{Sw\_On\_HV\_Stand}$ and $E_{Sw\_Off\_HV\_Stand}$ consider both the energy dissipation caused by the coexistence of voltage and current in the SJ-FET channel ($E_{Sw\_On\_HV\_Stand\_Coex}$ and $E_{Sw\_Off\_HV\_Stand\_Coex}$) and the energy dissipation caused by the charge and discharge of the SJ-FET input capacitance ($E_{Sw\_On\_HV\_Stand\_G}$ and $E_{Sw\_Off\_HV\_Stand\_G}$). Note that the input capacitance (i.e. C_{ISS_HV}) is equal to C_{GS_HV} plus C_{GD_HV}. In order to alleviate the understanding, it is important to clarify that the sum of $E_{Sw\_On\_HV\_Stand\_Coex}$ and $E_{Sw\_Off\_HV\_Stand\_Coex}$ is commonly noted as switching losses in literature, whereas the sum of $E_{Sw\_On\_HV\_Stand\_G}$ and $E_{Sw\_Off\_HV\_Stand\_G}$ is noted as gate-drive losses.

$$E_{Sw\_Stand} = E_{Sw\_On\_HV\_Stand} + E_{Sw\_Off\_HV\_Stand}, \quad (2)$$

$$E_{Sw\_On\_HV\_Stand} = E_{Sw\_On\_HV\_Stand\_Coex} + \\ + E_{Sw\_On\_HV\_Stand\_G}, \quad (3)$$

$$E_{Sw\_Off\_HV\_Stand} = E_{Sw\_Off\_HV\_Stand\_Coex} + \\ + E_{Sw\_Off\_HV\_Stand\_G}. \quad (4)$$

In the case of the CC, equation (5) defines the switching energy dissipated by the SJ-CC (E_{Sw_CC}) as the energies dissipated during the turn-on ($E_{Sw\_On\_HV\_CC}$ and $E_{Sw\_On\_LV\_CC}$) plus the turn-off ($E_{Sw\_Off\_HV\_CC}$ and $E_{Sw\_Off\_LV\_CC}$) of both the SJ-FET and the LV-FET. According to (6) and (7), $E_{Sw\_On\_HV\_CC}$ and $E_{Sw\_Off\_HV\_CC}$ consider both the energy dissipation caused by the coexistence of voltage and current in the SJ-FET channel ($E_{Sw\_On\_HV\_CC\_Coex}$ and $E_{Sw\_Off\_HV\_CC\_Coex}$) during its transitions and the energy dissipation caused by the charge and discharge of C_{ISS_HV} ($E_{Sw\_On\_HV\_CC\_G}$ and $E_{Sw\_Off\_HV\_CC\_G}$). According to (8) and (9), $E_{Sw\_On\_LV\_CC}$ and $E_{Sw\_Off\_LV\_CC}$ consider both the energy dissipation caused by the coexistence of voltage and current in the LV-FET channel ($E_{Sw\_On\_LV\_CC\_Coex}$ and $E_{Sw\_Off\_LV\_CC\_Coex}$) during the transitions, the energy dissipation ($E_{Sw\_On\_LV\_CC\_G}$ and $E_{Sw\_Off\_LV\_CC\_G}$) caused by the charge and discharge of the LV-FET input capacitance ($C_{ISS\_LV} = C_{GS\_LV} + C_{GD\_LV}$) and the energy dissipation caused by the avalanche period of the LV-FET ($E_{Sw\_Off\_LV\_CC\_Aval}$).

$$E_{Sw\_CC} = E_{Sw\_On\_HV\_CC} + E_{Sw\_On\_LV\_CC} + \\ + E_{Sw\_Off\_HV\_CC} + E_{Sw\_Off\_LV\_CC}, \quad (5)$$

$$E_{Sw\_On\_HV\_CC} = E_{Sw\_On\_HV\_CC\_Coex} + E_{Sw\_On\_HV\_CC\_G}, \quad (6)$$

$$E_{Sw\_Off\_HV\_CC} = E_{Sw\_Off\_HV\_CC\_Coex} + E_{Sw\_Off\_HV\_CC\_G}, \quad (7)$$

$$E_{Sw\_On\_LV\_CC} = E_{Sw\_On\_LV\_CC\_Coex} + E_{Sw\_On\_LV\_CC\_G}, \quad (8)$$

$$E_{Sw\_Off\_LV\_CC} = E_{Sw\_Off\_LV\_CC\_Coex} + E_{Sw\_Off\_LV\_CC\_G} + \\ + E_{Sw\_Off\_LV\_CC\_Aval}. \quad (9)$$

Fig. 6 shows the switching energies dissipated in both the SJ-FET in CC and in standalone configuration versus the inductive load current. According to Fig. 6(a), the increase of $E_{Sw\_On\_HV\_CC}$ with the current is much lower than in the case of $E_{Sw\_On\_HV\_Stand}$. It is important to note that $E_{Sw\_On\_HV\_Stand}$ is always higher than $E_{Sw\_On\_HV\_CC}$ for all the inductive load current levels. In the case of the turn-off (Fig. 6(b)), the improvement achieved by the CC does not seem to be remarkable until the inductive load current achieves a current level close to 6 A.

Fig. 7 shows the energy dissipated in the LV-FET during

both switching transitions versus the inductive load current. These energies are 1 or 2 order of magnitudes below the energies dissipated in the SJ-FET of the SJ-CC (see Fig. 6). It is important to note that the high value of the energy dissipated during the turn-off is due to the avalanche of the LV-FET. It is important to say that this energy remains almost constant with the current. The LV-FET is the same in both configurations, however, the avalanche losses are several times higher in the
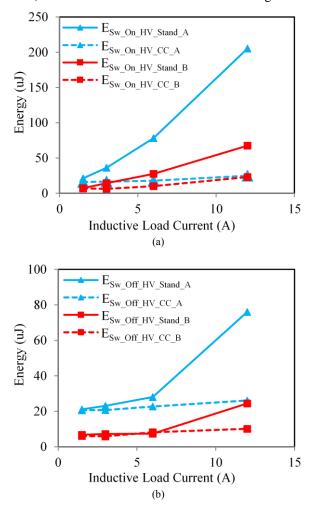

(a)

(b)

Fig. 6. Switching energy dissipated in the SJ-FET in both configurations: (a) Turn-on losses. (b) Turn-off losses.
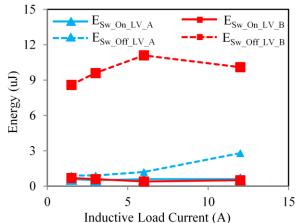

Fig. 7. Switching energy dissipated in the LV-FET.

case of the SJ-CC implemented with the SJ-FET B because of the higher value of Q_{X-Req} of the SJ-FET B, which can be estimated from (1) by using the Table II specifications.

Fig. 8 shows the total switching energy dissipated in both configurations (i.e. E_{Sw_Stand} and E_{Sw_CC}) versus the inductive load current. In the case of the SJ-FET A, the switching energy dissipated in standalone configuration is higher than in CC. Moreover, the difference rises exponentially with the inductive load current. In the case of the SJ-FET B, the switching energy dissipated in the standalone configuration is higher than in CC only when the current level is higher than current levels close to 6 A. Following section II.C analysis, this is due to the fact that the SJ-FET B causes higher avalanche losses of the LV-FET due to the higher Q_{OSS} value. The key point is that by increasing the current, these avalanche losses remain constant and the energy saved in the SJ-FET with respect to the standalone configuration rises. Therefore, the whole energy saved by the SJ-CC in comparison to the standalone configuration always rises with the current. Simulation results show that most of the switching losses of a SJ-FET in standalone configuration are caused by the coexistence of voltage and current in the device channel during both transitions. In the case of the SJ-CC, the energy dissipation caused by the coexistence of voltage and current at the LV-FET channel during transitions is negligible and the most relevant source of switching power losses is the coexistence of voltage and current at the SJ-FET channel, while the impact of the avalanche depends on the combination of SJ-FET and LV-FET. Moreover, the switching losses caused by the charge and discharge of any of the input capacitances are negligible in both configurations in comparison to previous ones. Taking into account these considerations, equations (2) and (5) can be simplified into (10) and (11) respectively. The two first terms of (10) and (11) are always lower for a SJ-CC. Therefore, the energy dissipated during the avalanche of the LV-FET determines if the total switching energy is lower either in the case of the CC or in the case of the SJ-FET in standalone configuration.

$$E_{Sw\_Stand} = E_{Sw\_On\_HV\_Stand\_Coex} + E_{Sw\_Off\_HV\_Stand\_Coex}, \quad (10)$$

$$E_{Sw\_CC} = E_{Sw\_On\_HV\_CC\_Coex} + E_{Sw\_Off\_HV\_CC\_Coex} + \\ + E_{Sw\_Off\_LV\_CC\_Aval}. \quad (11)$$

Fig. 9 shows the power saved when the same SJ-FET is used in CC instead of standalone configuration for different switching frequencies versus the inductive load current, including the extra conduction losses of the SJ-CCs that comes from the LV-FET. As the current rises, switching and conduction losses rise. Generally, the reason that explains the increase of the power saved by the SJ-CC when the current rises is the fact that the improvement achieved in the switching power saved has more impact than the increase of conduction losses related to the extra on-state resistance of the LV-FET. Moreover, as the switching frequency rises for a fixed value of the current, only switching losses rise. Due to this, the SJ-CC dissipates less power thanks to its superior switching behavior. However, this point is not valid when the SJ-FET B operates

with low current. Fig. 9(b) shows that the SJ-FET B in CC does not save power with respect to the standalone configuration when the current level is in the range of 1-3 A and the switching frequency is 100 kHz. The reason is that the avalanche of the LV-FET causes higher switching energy dissipation in the CC than in the standalone configuration. As a consequence, at these current levels, worst performance is obtained for higher
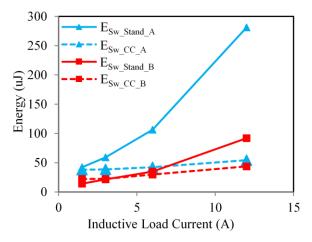

Fig. 8. Total switching energy dissipated in both configurations.
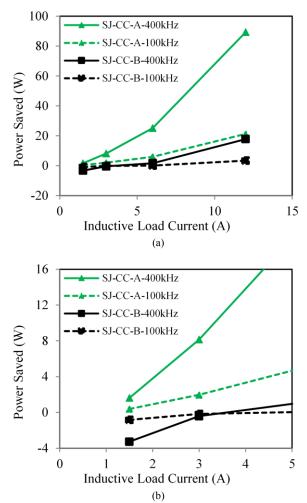

(a)

(b)

Fig. 9. Power saved when the same SJ-FET is used in CC instead of standalone configuration for different switching frequencies versus current: (a) General view. (b) Scope at low inductive load current.

switching frequencies. In the case of the SJ-FET A, at low current and when the switching frequency is 100 kHz, the power saved by the CC is negligible because conduction losses are predominant. Differently from the SJ-FET B, the power saved rises with the switching frequency when the current level is in the range of 1-3 A because the avalanche losses of the LV-FET are negligible in comparison to the energy saved at the SJ-FET (see Fig. 8).

It is concluded that the selection of the MOSFETs involved in the SJ-CC implementation is not trivial. A wrong combination of SJ-FET and LV-FET can deteriorate the performance by causing substantial avalanche losses. Another important conclusion is that by increasing the current, the SJ-CC always tends to overcome the standalone configuration regardless the selection of both MOSFETs for the SJ-CC implementation.

B. Reasons of the Energy Saved at the Turn-On in a CC

According to the previous conclusions, most of the improvement achieved by a SJ-CC appears during the turn-on due to the high reduction of the switching energy dissipated in the SJ-FET. This is due to the fast charge of C_{ISS_HV} achieved in the SJ-CC because of the low R_{G-HV} value. In order to facilitate the understanding, $R_{G-HV-CC}$ and $R_{G-HV-Stand}$ will be used to denote the SJ-FET gate resistance in CC and in standalone configuration respectively.

In both configurations, the SJ-FET gate resistance has major impact on the switching losses. In the standalone configuration, $R_{G-HV-Stand}$ limits the current delivered by the driver for charging C_{ISS_HV}. The effect is similar for the SJ-CC: $R_{G-HV-CC}$ limits the current delivered by V_A for charging C_{ISS_HV}. Note that the higher the SJ-FET gate resistance, the lower the gate current and the higher the time spent for charging C_{ISS_HV}, regardless the configuration. Since the SJ-FET gate current also depends on V_{Dri} and V_A in standalone configuration an in CC respectively, both values are going to be considered equal in order to ensure a fair comparison.

In the case of the CC, $R_{G-HV-CC}$ includes the LV-FET on-state resistance (negligible) and the internal gate resistance of the SJ-FET. The key point is that $R_{G-HV-Stand}$ is higher than $R_{G-HV-CC}$ because the first one includes not only the internal gate resistance of the SJ-FET, but also the output resistance of the driver and the external gate resistance. Even if a standalone design could operate without external gate resistance, the impact of the output resistance of the driver cannot be neglected.

The main ideal waveforms during the turn-on of the SJ-FET in both configurations are depicted in Fig. 10. Note that the current waveforms represented are the current though the channel of the SJ-FET in standalone configuration ($i_{Channel-HV-Stand}$) or in CC ($i_{Channel-HV-CC}$), which are not accessible in experimentation. It is important to highlight that, regardless the faster charge of C_{ISS_HV} in the SJ-CC, the SJ-FET in this configuration dissipates less energy during the turn-on because of the less voltage blocked during the off-stage (i.e. the peak of the instantaneous power dissipated during the turn-on is lower for the CC).
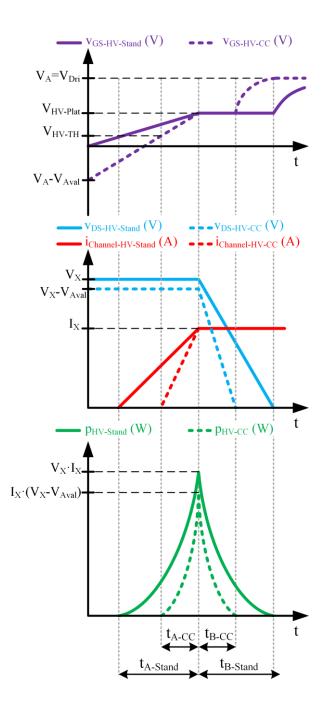

Fig. 10. Main ideal waveforms during the turn-on of the SJ-FET in both configurations.

Focusing on the switching energy dissipation, two stages can be distinguished:

Stage A: the rise of the current though the SJ-FET channel. Most of the gate current flows through C_{GS-HV} both in CC and in standalone configuration. During this stage, the current through the SJ-FET channel rises up to I_X. In addition, the faster the rise of v_{GS-HV}, the higher the slope of the current through the channel. Since $R_{G-HV-CC}$ is lower than $R_{G-HV-Stand}$, the SJ-FET gate current is higher in the case of the CC and, consequently, v_{GS-HV} rises faster. Therefore, the time duration of this stage is lower ($t_{A-CC} < t_{A-Stand}$). Fig. 11(a) and Fig. 11(b) show the equivalent circuits during this stage for both the standalone configuration and the SJ-CC respectively.
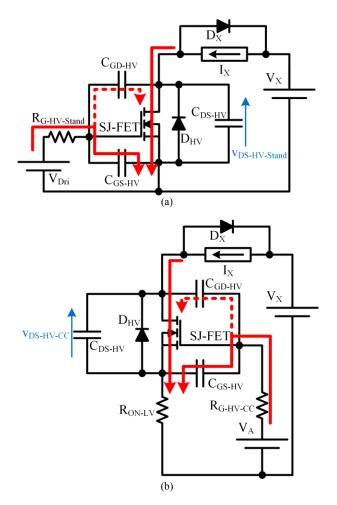
Fig. 11. Equivalent circuits during stage A: (a) Standalone configuration. (b) SJ-CC.

Fig. 12. Equivalent circuits during stage B: (a) Standalone configuration. (b) SJ-CC.

Stage B: the fall of the SJ-FET drain to source voltage. The Miller effect occurs in both configurations: most of the total gate current flows through C_{GD-HV}. The faster the rise of v_{GD-HV}, the faster the fall of v_{DS-HV}. As in the previous stage, the gate current is higher in the case of the SJ-CC due to the lower SJ-FET gate resistance. Therefore, v_{GD-HV} rises faster in this configuration and the time duration of this stage is lower ($t_{B-CC} < t_{B-Stand}$). Although C_{DS-HV} is discharged through the SJ-FET channel, this extra current level is not included in Fig.10 in order to simplify the explanation. Fig. 12(a) and Fig. 12(b) show the equivalent circuits during this stage for the standalone configuration and for the SJ-CC respectively.

An important conclusion can be extracted from this section: the LV-FET gate resistance (i.e. R_{G-LV}) has minor impact on the SJ-CC switching losses. The turn-on of the LV-FET is always much faster than the turn-on of the SJ-FET. Therefore, the effect of modifying the LV-FET transition speed by changing R_{G-LV} mainly affect $E_{Sw\_On\_LV\_CC\_Coex}$, but does not affect $E_{Sw\_On\_HV\_CC\_Coex}$, which is the main source of losses during the turn-on of the SJ-CC. Therefore, the requirements for the SJ-CC driver in terms of output current capability are lower than in the case of the standalone configuration.
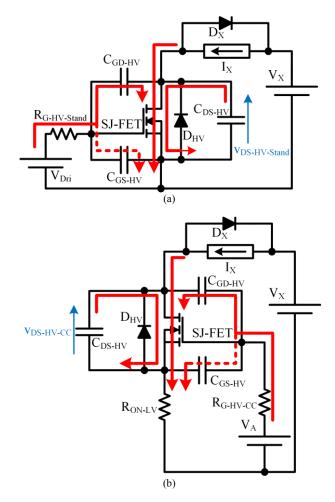
IV. EXPERIMENTAL RESULTS

A. DC-DC Power Converter Specifications

A boost converter in which the Device Under Test (DUT) is either a SJ-FET in standalone configuration or the same SJ-FET in CC is implemented to verify the previous analysis (Fig. 13). The input and output voltages are 100 V and 400 V respectively. To check the DUT behavior versus current, different operating points are compared: 180 W, 300 W, 400 W and 500 W, which correspond to an average current through the inductive load equal to 1.8 A, 3 A, 4 A and 5 A respectively. The inductance is designed to operate in Continuous Conduction Mode (CCM) for all tested switching frequencies (from 100 kHz to 400 kHz) and power levels. Moreover, the inductance value ensures low high-frequency ripple in order to make both switching transitions with a similar current level.

Several SJ-CCs are implemented into independent PCBs using Surface Mounted Devices (SMD). As Fig. 14 shows, a SMD capacitor is placed in parallel with the V_A voltage in order to stabilize it. The main characteristics of the SJ-FETs and the LV-FETs used to implement the SJ-CCs are shown in TABLE III and TABLE IV respectively. It is important to note that the SJ-FET 1, the SJ-FET 2 and the SJ-FET 3 are last generation devices optimized for hard-switching operation from three major manufacturers while the SJ-FET 4 is an irradiated device
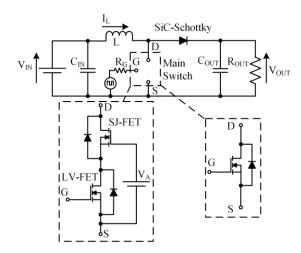
Fig. 13. Schematic circuit of the boost converter used for the experimental results.

Fig. 14. Plug-in board with a SJ-CC prototype.

optimized for fast reverse recovery.

The rest of the boost converter components are the same in all the comparative tests. The freewheeling diode is a 600 V SiC-Schottky in order to reduce the reverse recovery effect. The selected driver is the EL7104, which is connected to the SJ-FET in the standalone configuration and to the LV-FET for the SJ-CC with a 6.8 Ω gate resistor. The driver voltage during high state (i.e. V_{Dri}) is 11 V. In the case of the SJ-CC implemented with the LV-FET 1 or the LV-FET 3, V_{Dri} is 7 V due to the gate voltage requirements of these LV-FETs.

B. Efficiency Measurements

The efficiency of the converter is obtained by measuring the input and output voltages and currents. This kind of measurement allows us to know the total power losses of the converter. However, the power dissipated by the DUT cannot be identified. It is important to note that only the DUT is changed from one test to another. Hence, the differences that appear in the total power losses can be assumed that comes from the change of the main switch. At this point, it is important to
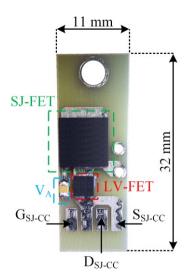
define the power saved as the power dissipated by the converter when a SJ-FET in standalone configuration is used as the main switch minus the power dissipated by converter when the same SJ-FET is used in CC. It is assumed that this difference can only be attributed to the DUT.

Although more than 30 SJ-CCs were implemented by changing the SJ-FET or/and the LV-FET, this section will show the most representative cases. Fig. 15 includes the four patterns that can be identified. This figure shows the power saved when the switching frequency and the current through the inductive load are modified. Note that the four cases use the same LV-FET with different SJ-FET. The results of the SJ-FET 1 and the LV-FET 1 are deployed in Fig. 15(a). This SJ-CC provides a higher improvement from an energetic point of view versus current through the inductive load and versus switching frequency rise. It is important to note that the comparison cannot be made under certain operating conditions, such as 300 kHz and 5 A, because the SJ-FET 1 in standalone configuration is not able to dissipate the generated power losses. The SJ-CC

TABLE III. CHARACTERISTICS OF THE SJ-FETs USED IN THE EXPERIMENTATION

	sR_{ON-HV} (mΩ·cm²)	R_{ON} (mΩ)	BV_{DSS} (V)	R_{G_Int} (Ω)	Q_G [*1] (nC)	Q_{GS} [*1] (nC)	Q_{GD} [*1] (nC)	V_{TH} (V)	C_{iss} [*2] (pF)	C_{oss} [*2] (pF)	C_{rss} [*2] (pF)	Q_{OSS} (nC)	Fast Reverse Recovery
SJ-FET 1	25.2	170	600	1	57	9	21	3	2043	45	7	120	No
SJ-FET 2	15.3	136	600	1.5	48	11	22	3.2	1680	40	7	152	No
SJ-FET 3	11.5	115	650	1	35	8	11	3.5	1670	26	-	239	No
SJ-FET 4	26.5	175	600	4	69	13	35	4	2100	80	10	128	Yes

[*1] at V_{GS} = 12 V [*2] at V_{GS} = 0 V, V_{DS} = 400 V

TABLE IV. CHARACTERISTICS OF THE LV-FETs USED IN THE EXPERIMENTATION

	R_{ON-LV} (mΩ)	BV_{DSS} (V)	R_{G_Int} (Ω)	Q_G (nC)	Q_{GS} (nC)	Q_{GD} (nC)	V_{TH} (V)	C_{iss} (pF)	C_{oss} (pF)	C_{rss} (pF)	Q_{OSS} (nC)
LV-FET 1	7.5	12	0.7	5.1 [*1]	0.98 [*1]	0.76 [*1]	0.8	767 [*1]	506 [*1]	43 [*1]	5.7
LV-FET 2	6.1	30	0.25	11.3 [*2]	1.97 [*2]	1.7 [*2]	1.7	655 [*2]	578 [*2]	50 [*2]	11
LV-FET 3	6.9	30	1.1	5.1 [*2]	1.8 [*2]	1.1 [*2]	1.3	735 [*2]	390 [*2]	29 [*2]	9.9

[*1] at V_{DS} = 6 V [*2] at V_{DS} = 15 V

overcomes the standalone configuration under all the analyzed operating conditions. The negative value of the power saved that appears when the current is 1.8 A and the switching frequency is 100 kHz is due to the impact of the conduction losses. Note that if this negative value were caused by the avalanche losses, the power saved should decrease by fixing the current and increasing the switching frequency. These experimental results match with the behavior that appeared in the simulation part (section III.A) for the SJ-FET A.

Fig. 15(b) shows the results obtained using the SJ-FET 2 in CC with the LV-FET 1. In this case, the experimental power saved is not as high as in the previous case. It is needed to increase the switching frequency to a higher value to obtain similar values of power saved. In this SJ-CC implementation, there are more situations where the power saved is negative. In all cases, it is due to the impact of the conduction losses, assuming the same reasoning used in last test: when the current is 1.8 A the power saved rises by increasing the switching frequency. Therefore, there is not major influence of avalanche losses. As in the previous case, the comparison cannot be made under certain operating conditions because the SJ-FET 2 in standalone configuration is not able to dissipate all the generated power losses.

Fig. 15(c) shows the results obtained using the SJ-FET 3 in CC with LV-FET 1. Differently from the two previous cases, the negative value of the power saved when the current is 1.8 A or 3 A is due to the impact of avalanche losses instead of conduction losses due to the fact that the power saved falls by increasing the switching frequency. This implies that the avalanche losses are greater than the power saved at the channel of the SJ-FET during turn-on and turn-off due the coexistence of voltage and current. These experimental results match with the results obtained in the simulation part (section III.A) for the SJ-FET B. As in the previous cases, the comparison could not be made under certain operating conditions. The difference is that now the SJ-CC limits the comparison because the LV-FET 1 is not able to dissipate the avalanche losses imposed by the use of this configuration with the SJ-FET 3.

According to Fig. 15(d), the highest improvement (i.e. highest power saved) is achieved using the SJ-FET 4. This situation has the highest room for improvement due to the low performance that the irradiated SJ-FET offers in standalone configuration in comparison to the SJ-FETs optimized for hard-switching operation. In this case, the standalone configuration is not able to operate with 300 kHz and 4 A. It is important to note that the highest power saved does not imply the lowest losses. Note that according to the power saved definition, each SJ-CC is compared to the same SJ-FET in standalone
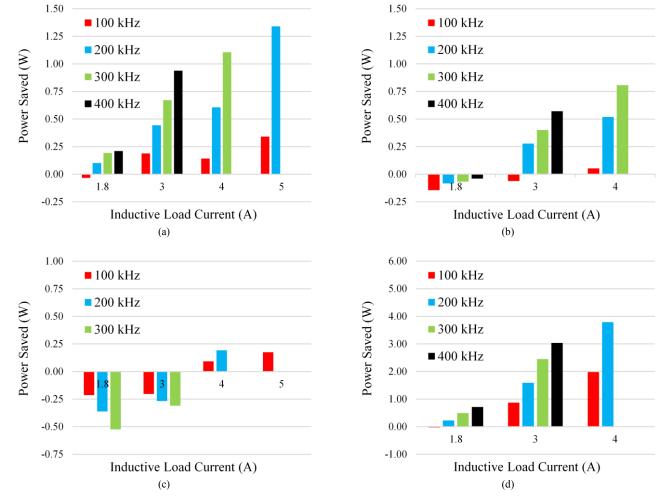

Fig. 15. Power saved when the same SJ-FET is used in CC with the LV-FET 1 instead of standalone configuration for different switching frequencies versus current: (a) SJ-FET 1. (b) SJ-FET 2. (c) SJ-FET 3. (d) SJ-FET 4.

configuration. For instance, in all the previous tests the lowest losses are achieved by the SJ-FET 1 in CC with the LV-FET 1.

Fig. 16(a) and Fig. 16(b) show the results obtained when using the SJ-FET 1 in CC with the LV-FET 2 and the LV-FET 3 respectively. By comparing Fig. 15(a) to Fig. 16, it can be stated that the LV-FET impact must be taken into account at low current levels, whereas it can be neglected at high current levels. When the inductive load current is 1.8 A, only the SJ-CC implemented with the LV-FET 1 (see Fig. 15(a)) obtains a positive power saved value. However, for higher current levels the power saved is positive in all cases and all SJ-CCs tend to obtain the same power saved value when the current level rises. For instance, when the current level is 3 A and the switching frequency is 200 kHz, the power saved obtained by the SJ-CC implemented with the LV-FET 1 (see Fig. 15(a)) is approximately twice that of the SJ-CCs implemented with the LV-FET 2 or the LV-FET 3 (see Fig. 16). Nevertheless, the three SJ-CCs obtain almost the same power saved when the current levels is 5 A and the switching frequency is 200 kHz. This is because the avalanche losses are different for each LV-FET. At low current levels, the avalanche losses impact is not negligible and, as a result, the power saved strongly depends on the LV-FET selection. However, at high current levels the

avalanche losses impact tends to decrease, which is translated into similar power saved values for the three implementations.

C. Waveform Analysis

In order to explain why some SJ-CC cases provide higher improvement than others, the waveforms of the most differentiated SJ-FET patterns observed in the section IV. B are analyzed. The differences between the SJ-FET 1, the SJ-FET 3 and the SJ-FET 4 are studied to identify and to estimate the sources of power losses. It is important to note that the switching frequency and the current are kept constant (i.e. 100 kHz and 3 A) in order to normalize the results.

According to conclusions at section II, most of the improvement achieved by the CC appears during the turn-on. As Fig. 17(a) shows, all the SJ-CCs improve the result during this transition with respect to the standalone configuration. The highest improvement is achieved by the irradiated one (SJ-FET 4) whereas the SJ-FET 1 and the SJ-FET 3 provide a similar improvement during this transition. In the case of the turn-off, Fig. 17(b) shows that the current level is not high enough to achieve a remarkable improvement in the SJ-FET 1 and the SJ-FET 3. Note that in the case of the SJ-FET 4, the improvement
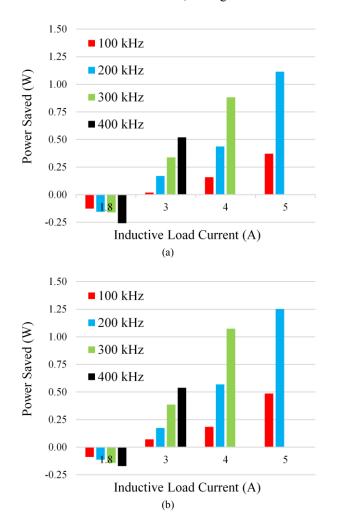

(a)

(b)

Fig. 16. Power saved when the SJ-FET 1 is used in CC with the LV-FET 2 (a) or the LV-FET 3 (b).
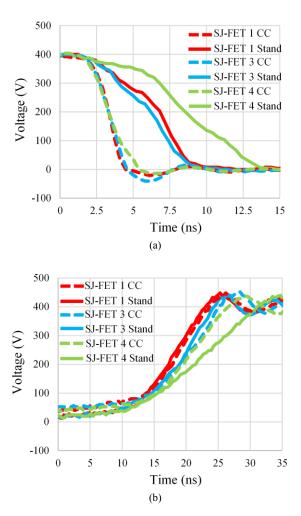

(a)

(b)

Fig. 17. Comparison between experimental waveforms of the drain to source voltage during the switching transitions of the SJ-FET 1, the SJ-FET 3 and the SJ-FET 4 in standalone configuration and in CC with the LV-FET 2: (a) Turn-on. (b) Turn-off.

is not negligible.

Fig. 18 shows a comparison of the LV-FET 2 avalanche for three SJ-CCs implementations which use different SJ-FETs. Note that the figure includes v_{DS-LV} and $V_{DS-SJ-CC}/8$. The comparison of the avalanche times in the case of the SJ-FET 1 and the SJ-FET 3 matches previous experimental results: power saved value is higher when using the SJ-FET 1. Note that the avalanche time for the SJ-FET 3 is more than 3.5 times higher than that of the SJ-FET 1. This is the consequence of the higher charge that C_{DS-HV} stores during the turn-off (Q_{OSS} of the SJ-FET 3 is almost twice that of the SJ-FET 1 according to Table III). The higher value of the avalanche losses causes an increase on the LV-FET temperature in the case of the SJ-FET 3 in CC, increasing $V_{Aval.}$. In the case of the SJ-FET 4, the avalanche losses are not negligible, but their impact is covered by the power saved at the SJ-FET, which is very high. For this reason, this implementation achieves the highest improvement.

The low impact of the LV-FET with respect to the SJ-FET at high current levels could also be deducted from the next waveforms. As Fig. 19(a) and Fig. 19(b) show, the energy saved during both transitions is independent from the LV-FET used. Finally, Fig. 20 shows that the switching energy differences can be attributed to the different avalanche losses of each implementation.

D. SJ-CC Improvement Evaluation

In order to evaluate the improvement achieved by the SJ-CC, a commercial available GaN-CC with similar on-state resistance (150 mΩ) is tested and compared to the best-in-class in the SJ-CC test: the SJ-FET 1 in CC with the LV-FET 1. The main characteristics of the GaN-CC are shown in TABLE V.

As it was explained in section IV.B, only the DUT is changed from one test to another. It is important to note that the driver is the same than in previous sections (i.e. EL7104), which provides similar characteristics to the driver proposed to control GaN-CCs in [20]. All tests compare the power saved either
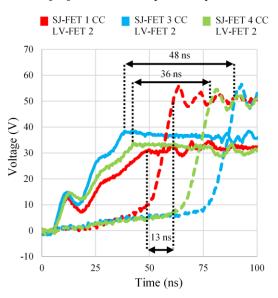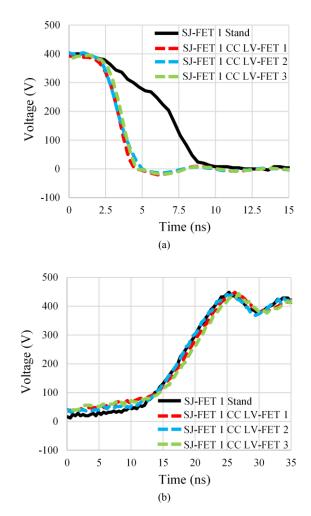

(a)

(b)

Fig. 19. Comparison between the experimental waveforms of the drain to source voltage during the switching transitions of the same SJ-FET in standalone configuration and in CC with the LV-FET 1, the LV-FET 2 or the LV-FET 3: (a) Turn-on. (b) Turn-off.
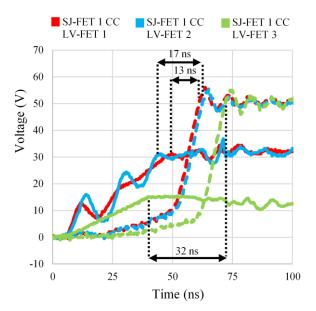

Fig. 18. Comparison between avalanche time in the SJ-FET 1, the SJ-FET 3 and the SJ-FET 4 in CC with the LV-FET 2. Note that the solid line is v_{DS-LV} and the dashed line is $v_{DS-SJ-CC}/8$.

Fig. 20. Comparison between avalanche time in the SJ-FET 1 in CC with the LV-FET 1, the LV-FET 2 and the LV-FET 3. Note that the solid line is v_{DS-LV} and the dashed line is $v_{DS-SJ-CC}/8$.

when the SJ-FET 1 in CC with the LV-FET 1 or the GaN-CC are used in comparison to the SJ-FET 1 in standalone configuration. According to Fig. 21(a) and Fig. 21(b), the improvement achieved by the SJ-CC is similar to the provided by a GaN-CC. To illustrate the results, the measurements are carried out at 3 A and 4 A.

Fig. 22(a) and Fig. 22(b) show a comparison of the drain-source voltage during both switching transitions. Note that these waveforms do not provide such information as in the previous cases in order to identify the impact of each losses source. The reason is that here, the compared switches are very different because the GaN HEMT provides a higher transconductance and lower parasitic capacitances than the SJ-FET and there is not information about the LV-FET used in the GaN-CC. Moreover, v_{DS-LV} is inaccessible and therefore the avalanche losses cannot be evaluated for the GaN-CC.

E. Avoiding the LV-FET Avalanche

In order to obtain a reliable switch that maximizes the switching benefits of the CC, the LV-FET avalanche must be avoided. A possible method consists in adding an external capacitor (C_{Ext}) in parallel with C_{DS-LV} (Fig. 23). According to the section II.D, this allows us to increase Q_X. By adopting this method, an equivalent drain to source capacitance of the LV-FET (C_{DS-LV}') could be defined considering $C_{DS-LV} + C_{Ext}$. Therefore, the difference between the charge that C_{GS-HV}, C_{DS-LV}' and C_{GD-LV} can store (i.e. Q_X), and the charge that they need to store in order to avoid the LV-FET avalanche (i.e. Q_{X-Req}) can be eliminated by increasing C_{Ext}.

It is important to note that since C_{Ext} slows down the switching mechanism, the method has some penalties. The first one is that the charge that C_{GS-HV}, C_{DS-LV}' and C_{GD-LV} must be able to store to avoid the LV-FET avalanche (i.e. Q_{X-Req}') is
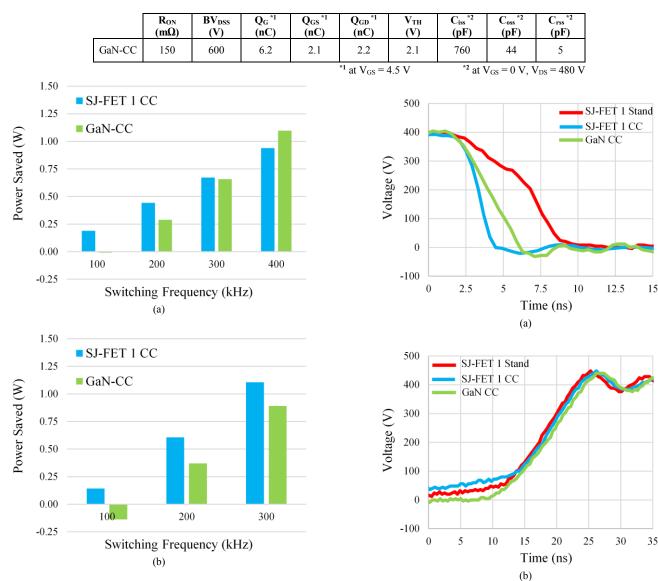
TABLE V. CHARACTERISTICS OF THE GaN-CC USED IN THE EXPERIMENTATION

	R_{ON} (mΩ)	BV_{DSS} (V)	Q_G[*1] (nC)	Q_{GS}[*1] (nC)	Q_{GD}[*1] (nC)	V_{TH} (V)	C_{iss}[*2] (pF)	C_{oss}[*2] (pF)	C_{rss}[*2] (pF)
GaN-CC	150	600	6.2	2.1	2.2	2.1	760	44	5

[*1] at $V_{GS} = 4.5$ V   [*2] at $V_{GS} = 0$ V, $V_{DS} = 480$ V

(a)

(b)

Fig. 21. Power saved either when the GaN-CC or the SJ-FET 1 in CC with the LV-FET 1 are used instead of the SJ-FET 1 in standalone configuration versus the switching frequency: (a) Results when the inductive load current is 3 A. (b) Results when the inductive load current is 4 A.

(a)

(b)

Fig. 22. Comparison between the experimental waveforms of the drain to source voltage during the switching transitions of the SJ-FET 1 in CC with the LV-FET 1 and the commercial GaN-CC: (a) Turn-on. (b) Turn-off.
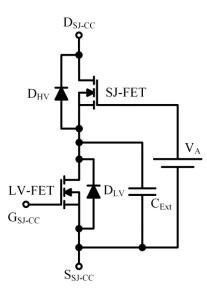
Fig. 23. SJ-CC with external capacitor (C_{Ext}) in parallel with C_{DS-LV}.

Fig. 24. Avalanche reduction achieved by adding C_{Ext}. Note that the solid line is v_{DS-LV} and the dashed line is $v_{DS-SJ-CC}/8$.

Fig. 25. Power saved when adding C_{Ext} to the SJ-FET 3 in CC with the LV-FET 2 in comparison to the same SJ-CC without C_{Ext}.

higher than in the case of not introducing C_{Ext} (i.e. $Q_{X-Req}'>Q_{X-Req}$). The reason is that at the end of stage III of the turn-off, the v_{DS-LV} value is the same in both situations (i.e. with or without C_{Ext}), but the charge stored is higher in the case of introducing C_{Ext} (i.e. $Q_{X-S1}' + Q_{X-S2}' + Q_{X-S3}' > Q_{X-S1} + Q_{X-S2} + Q_{X-S3}$). Note that due to the hard-switching operation, this extra stored charge is dissipated during the turn-on, increasing the power losses. The second penalty is that the introduction of C_{Ext} is equivalent to increasing C_{GS-HV}. Therefore, the time spent for charging and discharging C_{ISS-HV} rises, increasing also the power losses of the SJ-FET. It is concluded that there is a trade-off between the mitigation of the avalanche losses and the reduction of the energy saved at the SJ-CC (i.e. $E_{Sw\_Off\_LV\_CC\_Aval}$ falls but $E_{Sw\_On\_HV\_CC}$ and $E_{Sw\_Off\_HV\_CC}$ rise by increasing C_{Ext}).

In order to check this method experimentally, the SJ-FET 3 in CC with the LV-FET 2 is used due to its high avalanche losses. Fig. 24 shows the avalanche time reduction achieved by increasing C_{Ext}. Note that 6.6 nF is the lowest capacitance value needed to avoid the avalanche. Fig. 25 shows the power saved when C_{Ext} is added in comparison to the same SJ-CC without C_{Ext}. It can be seen that once C_{Ext} is higher than the required value to avoid the avalanche, the performance falls due to the increase of $E_{Sw\_On\_HV\_CC}$ and $E_{Sw\_Off\_HV\_CC}$.

V. CONCLUSIONS

The SJ-CC opens a new paradigm to extend HV silicon technologies to high-frequency domains (>100 kHz) and, consequently, enabling the adoption of SJ-FETs in applications exclusively conceived for WBG devices. The SJ-CC benefits not only from reducing switching times and energies, but also from ruggedness, maturity and cost of silicon.

Despite of the wide use of the CC in the radiofrequency scope, it has only been explored in the power electronics applications either for WBG high-voltage transistors or BJTs. This paper explains and demonstrates the switching behavior advantages of the SJ-FET in CC in comparison to the standalone configuration.
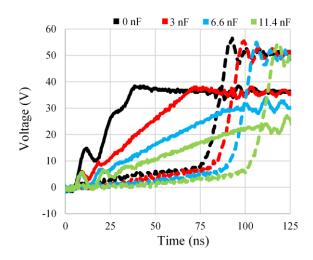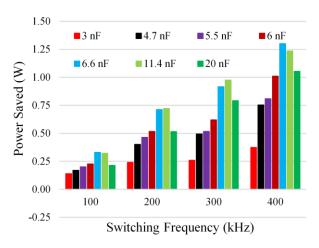
It has been concluded that the improvement achieved by the SJ-CC is due to the low SJ-FET gate resistance, which enables a fast charge of the SJ-FET equivalent input capacitance. This fact reduces the time in which there is coexistence of voltage and current in the SJ-FET. This implies that if the switching frequency is increased, the SJ-CC saves more power than the standalone configuration. In addition, SJ-CC is more efficient than standalone configuration as the current through the switch rises. This is because the penalization in the conduction losses due to the extra on-state resistance of the LV-FET has lower impact than the improvement achieved during the turn-on of the SJ-FET. In the case of the SJ-CC, the avalanche state of the LV-FET is an additional source of losses that does not appear in the standalone configuration. These losses depend on the SJ-FET and on the LV-FET involved in the SJ-CC implementation. As a result, some SJ-CC implementations do not overcome the standalone configuration under certain operating conditions. This mainly occurs for low current levels, where the avalanche losses of this SJ-CC implementations have higher impact than

the power saved in the SJ-FET. In order to mitigate avalanche losses, the method that consists in adding an external capacitor in parallel with C_{DS-LV} has been analyzed.

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