# A Study on the Control Loop Design of Non-Isolated Configurations for Hybrid Storage Systems

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*Abstract*—— **This work focuses on the control strategies for different configurations of Non-Isolated Hybrid Energy Storage Systems. Basic strategies are proposed, studied and compared. Parting from the standard parallel connection of bidirectional boost converter in hybrid storage systems, a comparison with alternate topologies is presented. These alternative schemes overcome the problems that arise in the original configuration due the high mismatch in voltage ratings of the individual storage systems. A strategy to design the control loops of the resulting Hybrid Energy Storage System is proposed, studied, simulated and experimentally implemented on a 1.5 kW demonstrator. The control strategy is implemented in the standard bidirectional boost converter approach and also in the series-parallel connection of the storage units. The reported results show how the proposed control strategy applied to the series parallel connection presents a good performance in terms of dynamic and steady state operation.**

*Keywords— Energy Storage System; Boost Converters; Hybrid; Series-Parallel Connection;*

## I. INTRODUCTION

Nowadays, the most common Energy Storage Systems (ESSs) implemented in DC microgrids are hybridized, thus combining a bulk ESS, usually presenting slow-dynamics (such as an electrochemical battery e.g. Lithium Ion Battery (LIB)) plus a high-power fast-dynamics storage module (e.g. a Supercapacitor Module, SM). Therefore, by using such a Hybrid ESS, the expected performance implies a decrease in the overall system costs (reducing the battery size and increasing the life span of the battery) and an increase in the system reliability (decreasing the stresses on the battery during transient stages) [1] – [15].

The simplest connection of the Hybrid ESS able to fully control the power flow from and into every storage device and the DC link is the Parallel Connection (PC), shown in Fig. 1, based on two bidirectional boost converters connected to the DC link itself. This scheme can also be defined as a H-bridge configuration [1]-[3], [6], [8], [9], [11], [15]. The main limitations of this connection come from the high voltage mismatch between the SM voltage ratings and the DC link bus voltage. Considering a battery rated voltage of around half the DC link voltage, then the duty ratio of the battery leg will be around 50%, thus optimizing the performance of such converter, in terms of stresses balancing, design complexity and control capability. However, provided that in some

applications the SM voltage ratings are ranged from 20V to 40V, then for DC bus voltage ratings ranged from 500V to 900V the required gains for the dedicated interfacing converter will reach values up to 40:1 or even higher.
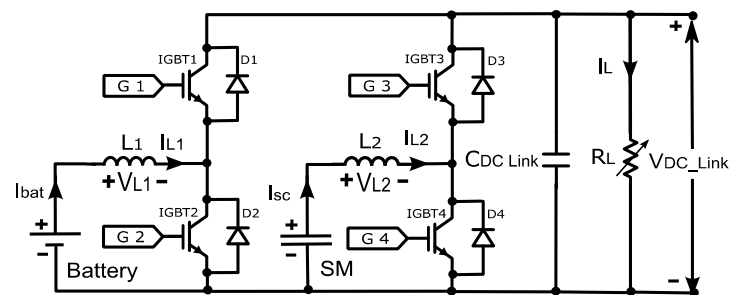


Fig. 1. Parallel Connection (PC) of two bidirectional boost converters connected to Lithium Ion Battery (LIB) and Supercapacitor Module (SM) and sharing the DC link.

Such requirements cannot be accomplished by the commonly used single-stage non-isolated converter topologies [16]. But even for practical gain values (say 10:1), the bidirectional boost converter experiences an increase in the stresses unbalancing on the IGBTs, a decrease the control margin of the converter, more sensitivity to parasitic elements, etc. [16]. To overcome these drawbacks, a solution without moving to more complex schemes (such as cascaded, multilevel or isolated approaches) is the Series-Parallel Connection (SPC) depicted in Fig. 2 [17]. The negative terminal of the SM is connected to the middle point of the leg connected to the battery.
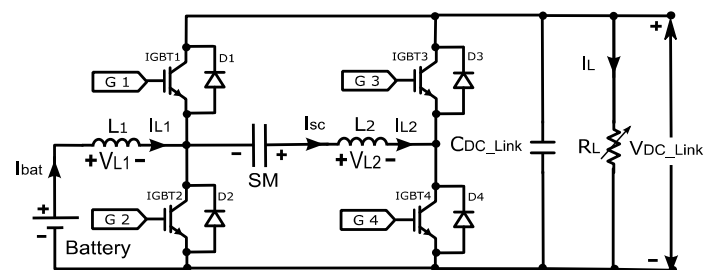


Fig. 2. Series-Parallel Connection (SPC) of two bidirectional boost converters connected to Lithium Ion Battery (LIB) and Supercapacitor Module (SM) and sharing the DC link.

## II. Comparison of Configurations

In order to demonstrate the operation of the proposed solution, the system under consideration has the following operating conditions: 300V nominal voltage battery (e.g. a Li-Ion battery), 30V rated SM voltage and 500V nominal voltage DC-link. The performance will be assessed in steady-state. Under PC scheme, the usual boost converter equations are fulfilled, therefore, the corresponding duty cycles at steady state for the IGBT 1 (at the leg connected to the battery) and IGBT 3 (at the leg connected to the SM), $D_{Bat}$ and $D_{SM}$, respectively, follow the following expressions:

$$D_{Bat} = \frac{V_{Bat}}{V_{DC\_Link}} = 60\ \% \tag{1}$$

$$D_{SM} = \frac{V_{SM}}{V_{DC\_Link}} = 6\ \% \tag{2}$$

where, $V_{Bat}$, $V_{SM}$ and $V_{DC\_Link}$ are the battery, the SM and the DC link voltage values in Volts, respectively.

Thus, IGBT 3 is turned on 6 % of the switching time, while the IGBT 4 is turned on 94 % of the switching time. The small duty cycle of the SM leg yields to thermal and electrical stresses mismatch on the switches. On the other hand, under SPC scheme, the following equation applies to the leg formed by IGBT 3 and IGBT 4:

$$V_{Bat} - V_{L1} + V_{SM} - V_{L2} = D_{SM} \cdot V_{DC\_Link} \tag{3}$$

Where, $V_{L1}$ and $V_{L2}$ are the voltages in the inductors connected to the battery and to the SM in Volts, respectively.

Upon steady state condition, the inductor voltages are null, therefore the value of the duty ratio at the SM leg is given by:

$$D_{SM} = \frac{V_{SM} + V_{Bat}}{V_{DC\_Link}} = 66\ \% \tag{4}$$

The value of the duty ratio at the battery leg is given by (1). With the same voltage values than in the PC case, IGBT 3 is turned on 66 % and IGBT 4 is turned on 34 % of the switching time in the SPC scheme. This yields to a balance in the thermal stress on the switches for the SM leg. In the aforementioned connection, the duty cycle of the IGBT 3 is a function of the supercapacitor voltage and battery voltage, not only of the supercapacitor voltage as in case of PC. Therefore, the stresses in the switches of the SM leg are much more balanced than in the previous case, yielding to a better performance in terms of reliability and increased control margin.

The main drawback is the appearance of circulating extra currents through the switches of the battery leg in the SPC. However, in the case of using a SM for transient compensation of power demands, where most of the time the current reference for the SM will be null, this issue is not a concern. Thus, the SPC is an option for some applications of Hybrid ESS with high voltage ratings mismatch. In order to assess its performance, a deep analysis of the control system required to govern the power flows in the converter is needed.

## III. Proposed Control of the Series-Parallel Connection

For the PC in Fig. 1 considering now transient state, the following relationships for the duty cycles are found:

$$D_{Bat} = \frac{V_{Bat} - V_{L1}}{V_{DC\_Link}} \tag{5}$$

$$D_{SM} = \frac{V_{SM} - V_{L2}}{V_{DC\_Link}} \tag{6}$$

Through the V-I characteristic of these inductors, two independent current control loops can be implemented for each of the storage devices, simplifying the control design. For instance, the bandwidth of the storage systems can be made significantly different, therefore limiting the di/dt of the battery, forcing the SM to cope with the fast power variations required by the DC-link. The instant value of the duty ratios in the converters states the capability of providing a given transient voltage to the inductors in the converters, therefore yielding to a given current by those inductors. In addition to stresses unbalance in the switches and poor performance due extreme duty ratios, the main problem in PC comes from the fact that in the SM leg, the starting value of the duty ratio is quite small (6%).

If a high SM charging current is required, the control system acts providing a high duty ratio to this leg (say 80%), and therefore, the resulting voltage in the SM inductor increases noticeably (up to 450-500V), and therefore a very high SM charging current can be achieved. But in the opposite case, when a high discharging SM current is desired, the duty ratio of the SM leg cannot be smaller than 0, and therefore the discharging voltage in this inductor is limited to the SM voltage (say 30V), and therefore the discharging current is significantly smaller than the charging one. This results in a non-symmetric behavior of the control, which is not admissible for a transient compensating scheme.

However, In SPC the duty cycle of the IGBT 3 is a function also of the voltage at the inductor connected to the battery. This ultimately yields to an extension on the values that the SM inductor might take, and therefore extending the range of symmetrical behavior. From (1) and (3), for SPC in Fig. 2, the following relationships of the duty cycles are found:

$$D_{Bat} = \frac{V_{Bat} - V_{L1}}{V_{DC\_Link}} \tag{7}$$

$$D_{SM} = \frac{V_{SM} - V_{L2} + V_{Bat} - V_{L1}}{V_{DC\_Link}} \tag{8}$$

The control strategy proposed and implemented is discussed ahead. This control considers that the DC bus voltage is controlled by an inverter connected to the grid (not represented in the figures 1 and 2). The aim of the control is the SM delivers or absorbs the transient peak power and the LIB delivers or absorbs the rest of the transient power in order to improve the recovery of the DC link due to load variations. Fig. 3 shows the control scheme of the PC; as it can be seen, the total ESS power reference is generated by measuring the load power and filtering through a High Pass Filter (HPF) [7], [18]. This total ESS power reference is not directly applied to the system. Instead, another SM power reference is generated by using a different HPF (with a higher cut-off frequency). A limiter is used to ensure that the SM power limits are not exceeded. This SM power reference is applied to the SM control loop. Finally, the power reference for the battery control loop is obtained as a difference between the total ESS power and the SM power reference [9], [15]. Another limiter is

used to ensure that the LIB limits are not exceeded. The power expressions are defined as following:

$$P_{L\_meas} = I_{L\_meas} * V_{DC\_meas} \qquad (9)$$

$$P_{ESS\_ref} = \frac{T_{ESS} * s}{1 + T_{ESS} * s} * P_{L\_meas} \qquad (10)$$

$$P_{SM\_ref} = \frac{T_{SM} * s}{1 + T_{SM} * s} * P_{L\_meas} \qquad (11)$$

$$P_{Bat\_ref} = P_{ESS\_ref} - P_{SM\_ref} \qquad (12)$$

where:

- $P_{L\_meas}$ is the measured power of the load in Watts,

- $P_{ESS\_ref}$, $P_{SM\_ref}$ and $P_{Bat\_ref}$ are the reference powers of the ESS, SM and LIB respectively in Watts,

- $I_{L\_meas}$ is the measured current of the load in Amps,

- $V_{DC\_meas}$ is the measured DC link voltage in Volts,

- $T_{ESS}$ is the time constant of the HPF of the ESS power in Secs,

- $T_{SM}$ is the time constant of the HPF of the SM power in Secs,

- s is the Laplace complex variable; s=σ+jωd.

Once the power reference values are obtained, the current references of the battery and SM loops are calculated by dividing by the battery and SM measured voltages, respectively. The current of the inductors connected to LIB and SM are the same the currents of the LIB and SM, respectively. As regulators, typical PI current controllers in ideal form (tuned by zero-pole cancellation considering the RL equivalents of the inductors) are used as in (13). The bandwidth (BW) of the SM current controller is higher than the BW of the battery current controller[2], thus guaranteeing that the SM will supply or absorb the peak transient power during load variations. The limits for the inductors voltage are calculated as in (13)-(16).
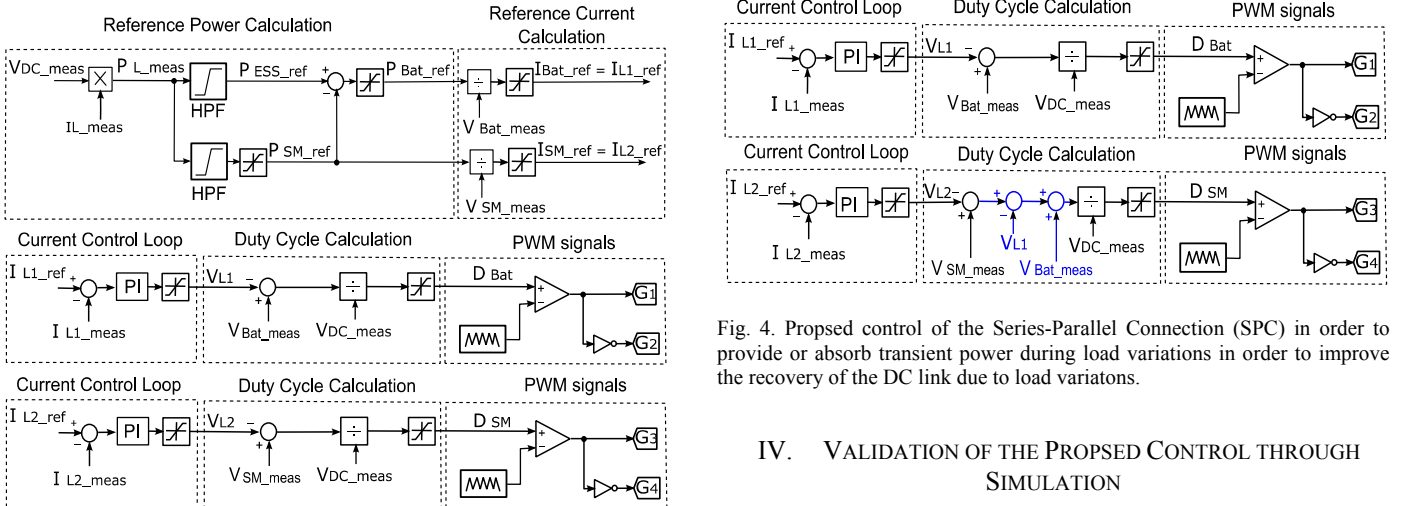


Fig. 3. Control of the Parallel Connection (PC) in order to provide or absorb transient power during load variations in order to improve the recovery of the DC link due to load variatons.

$$C(s) = K_p * (1 + \frac{K_i}{s}) \qquad (13)$$

where:

- C(s) is the transfer function of the PI controller,

- $K_p$ is the proportional gain,

- $K_i$ is the integral gain.

$$V_{L1\_min} = V_{Bat\_meas} - V_{DC\_meas} \qquad (14)$$

$$V_{L1\_max} = V_{Bat\_meas} \qquad (15)$$

$$V_{L2\_min} = V_{SM\_meas} - V_{DC\_meas} \qquad (16)$$

$$V_{L2\_max} = V_{SM\_meas} \qquad (17)$$

where:

- $V_{L1\_min}$, $V_{L1\_max}$, $V_{L2\_min}$ and $V_{L1\_max}$, are the minimum and maximum inductor voltages in Volts for the LIB and SM boost converters respectively.

- $V_{Bat\_meas}$ and $V_{SM\_meas}$ are the measured storage device voltages in Volts.

Figure 4 shows the proposed control in the SPC scheme, the difference between the two control schemes is the calculating of the duty cycle of the SM in each connection. The limits for the inductors voltage are the same as in (14), (15) and (17), however the maximum voltage of the inductor connected to the SM is calculated as following:

$$V_{L2\_max} = V_{SM\_meas} + V_{DC\_meas} \qquad (18)$$



Fig. 4. Propsed control of the Series-Parallel Connection (SPC) in order to provide or absorb transient power during load variations in order to improve the recovery of the DC link due to load variatons.

## IV. VALIDATION OF THE PROPSED CONTROL THROUGH SIMULATION

The simulations carried out for demonstrating the proposed control performance have been done for the full Hybrid ESS, both in PC and SPC schemes. A State of Charge (SOC) of the battery of 50% is considered, and the rated SM voltage value

used for calculating the reference power for the battery is the same in all cases. The parameters used in the operating conditions are listed in Table 1 and the control parameters used are in Table 2.

A sudden load step of ±50% in a 1.5kW rated converter operation has been simulated, both for the PC and SPC schemes. The DC link voltage is controlled by a inverter connected to the grid in order to maintain the DC link voltage around 500 V. It is seen in Fig. 5 that the performance of the two Hybrid ESS is similar, the load power is changed from 833.3 W to 1666.7 W at 0.5 seconds and again to 833.3 W at 2.5 seconds. The SM delivered the transient peak power and the LIB delivered the rest of the transient power at 0.5 seconds. At 2.5 seconds, the SM absorbed the transient peak power and the LIB absorbed the rest of the transient power.
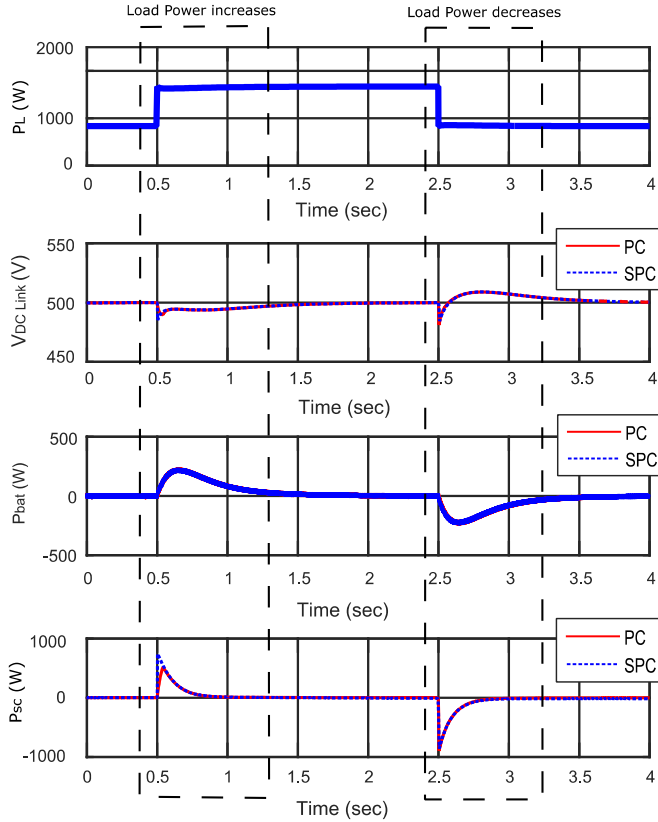


Fig. 5. Simulation results for the Parallel Connection (PC) and the Series Parallel Connection (SPC) where the load power is changed from 833.3 W to 1666.7 W at 0.5 seconds and then to 833.3 W again at 2.5 seconds.

Table 1. Parameters of the converters.

| Parameter | Symbol | Value |
|---|---|---|
| Nominal Battery voltage | $V_{Bat}$ | 300 V |
| Nominal SM voltage | $V_{SC}$ | 30 V |
| Capacitance of the SM | $C_{SC}$ | 165 F |
| DC link voltage | $V_{DC}$ | 500 V |
| Capacitance of the DC link | $C_{DC}$ | 470 μF |
| Maximum load power | $P_{L\ max}$ | 1666.7 W |
| Inductance of the inductors | L | 21 mH |
| Resistance of the inductors | R | 0.3 Ω |

Table 2. Parameters of the control of the converters.

| Parameter | Symbol | Value |
|---|---|---|
| HPF of the ESS Power | | |
| Cut off frequency | $F_{HPF\_ESS}$ | 0.7 Hz |
| HPF of the SM Power | | |
| Cut off frequency | $F_{HPF\_SM}$ | 1.5 Hz |
| Current Control Loop for LIB | | |
| Bandwidth | $BW_{LIB}$ | 300 Hz |
| Proportional gain | $K_{P\_LIB}$ | 39.564 |
| Integral gain | $K_{I\_LIB}$ | 22.8571 |
| Current Control Loop for SC | | |
| Bandwidth | $BW_{SC}$ | 500 Hz |
| Proportional gain | $K_{P\_SC}$ | 65.94 |
| Integral gain | $K_{I\_SC}$ | 22.8571 |

However, the duty cycle of the SM leg is different; for the SPC scheme, the duty cycle of the SM leg is 0.66, as shown in Fig. 6. All the aforementioned problems of the too narrow duty ratio obtained for PC scheme is therefore solved in the SPC configuration. This yields to decrease the thermal and electrical stresses on the switches.
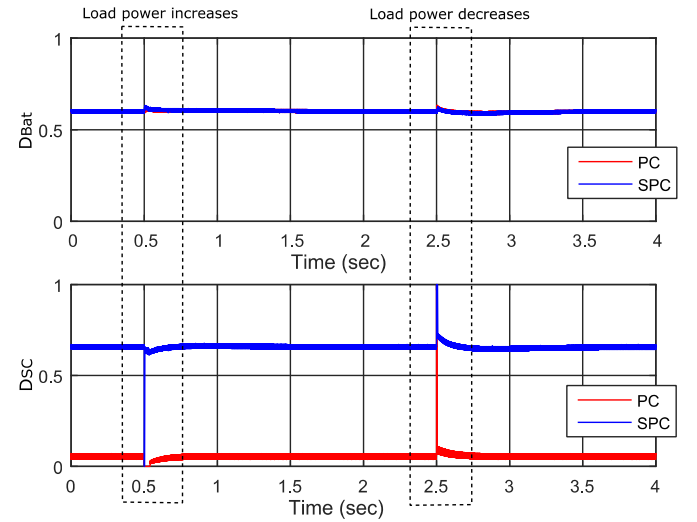


Fig. 6. Simulation Results of the Battery duty cycle ($D_{Bat}$) and Supercapacitor Module duty cycle ($D_{SM}$) for the Parallel Connection (PC) and the Series Parallel Connection (SPC) where the load power is changed from 833.3 W to 1666.7 W at 0.5 seconds and then to 833.3 W again at 2.5 seconds.

## V. VALIDATION OF THE PROPOSED CONTROL BY EXPERIMENTAL RESULTS

The Experimental results are done in a 2 KW demonstrator setup shown in Fig. 7. Considering the DC link voltage is controlled by the grid inverter to maintain the DC link voltage around 500 Volts. In order to demonstrate the merits and the feasibility of the SPC, the current control is tested for the PC and SPC. A 5 Amps LIB current reference and 10 Amps SM current reference are applied. As shown in Fig. 8 and Fig. 9, the collector-emitter voltage of IGBT 2 ($V_{CE2}$) and the

collector-emitter voltage of IGBT 4 ($V_{CE4}$) are representing the duty cycles of the LIB and SM, respectively. The duty cycle of SM in PC is a very small value compared to the duty cycle of the LIB as in Fig. 8. However, in Fig. 9 the duty cycle of the SM is a little bit higher than the duty cycle of LIB. This yields to decrease the thermal and electrical stresses and increasing the life time of the IGBTs and solving the problem of voltage mismatch.

In order to demonstrate the feasibility of the proposed control strategy, the PC and SPC are tested. Fig. 8 is showing the performance of the PC and SPC when the load power is changed from 833.3 W to 1666.7 W at 0.5 seconds and then to 833.3 W again at 2.6 seconds. It is fully matched with the results obtained in Fig. 5 from simulations.
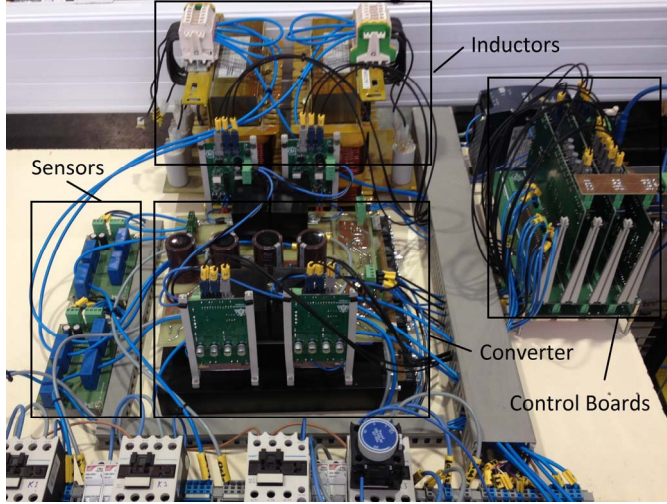


Fig. 7. Experimental setup and it can be Parallel Connection (PC) or Series-Parallel Connection (SPC).
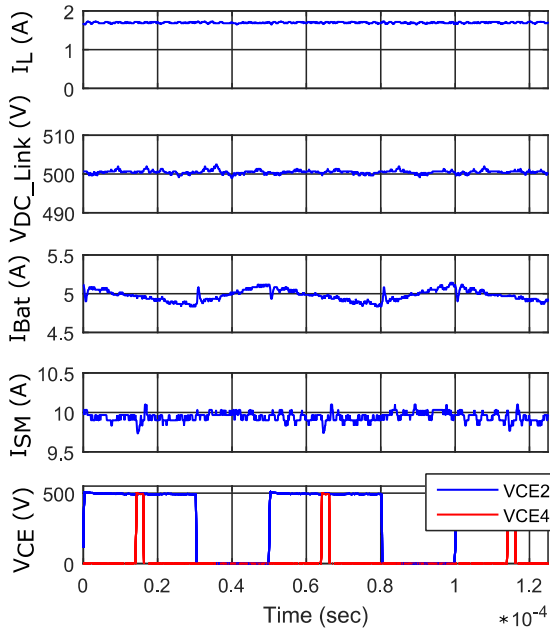


Fig. 8. Experimental results for the Parallel Connection (PC) where 5 Amps LIB current reference and 10 Amps SM current reference are applied and the DC link is controlled by the grid inverter.
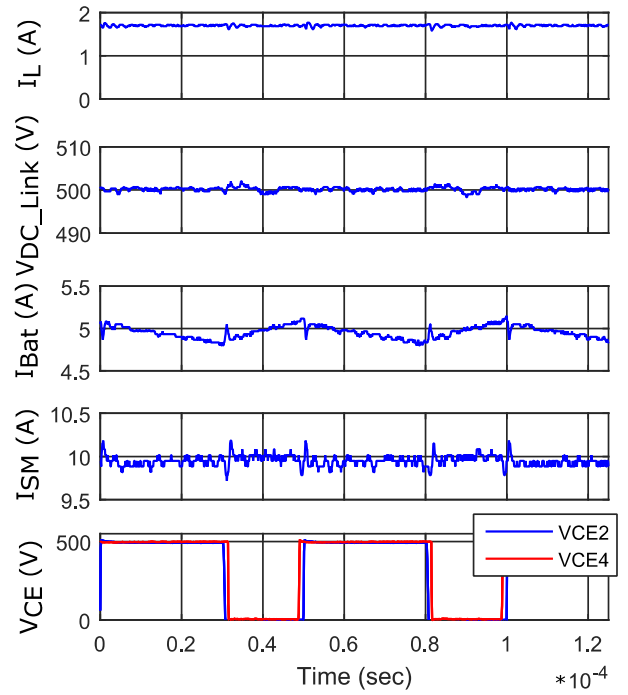


Fig. 9. Experimental results for the Series-Parallel Connection (SPC) where 5 Amps LIB current reference and 10 Amps SM current reference are applied and the DC link is controlled by the grid inverter.
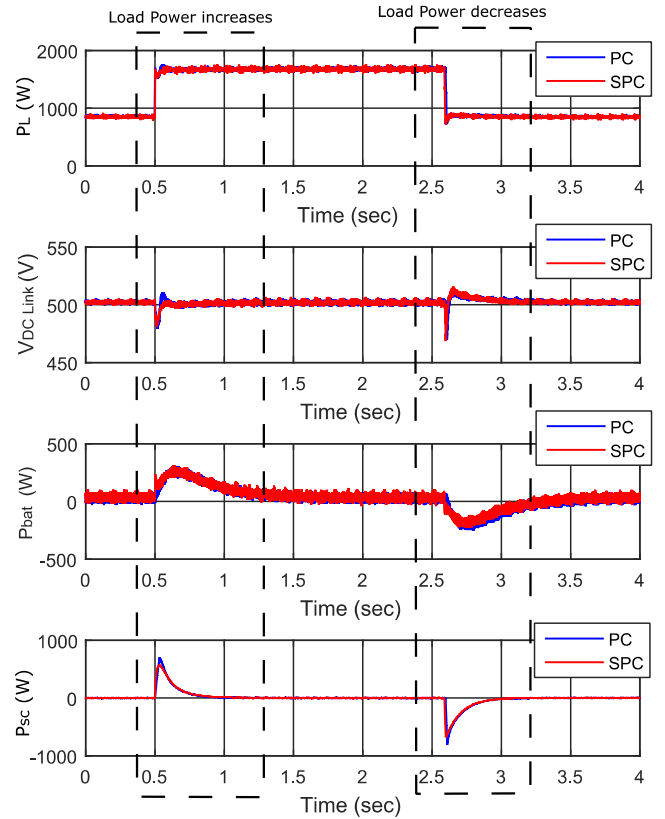


Fig.10. Experimental results for the Parallel Connection (PC) and the Series Parallel Connection (SPC) where the load power is changed from 833.3 W to 1666.7 W at 0.5 seconds and then to 833.3 W again at 2.5 seconds.

## VI. Conclusions and Future Developments

In this paper, a control loop design strategy for the series-parallel connection (SPC) of Hybrid ESS is proposed, studied, simulated and experimentally validated at 2 KW demonstrator setup. The performance of this strategy is compared to the original parallel configuration of the storage units. The results show that the proposed control for the SPC scheme keeps the DC-link under control upon sudden load variations, with a non-isolated, transformerless simple solution. This solution decreases the thermal and electrical stress on the switches by balancing the voltage on the switches. This solution can be used in high voltage mismatch application in hybrid systems.

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