Cosine Phase Droop Control (CPDC) for the Dual-Active Bridge in Lighting Smart Grids Applications.

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***Abstract*— Lighting Systems are suffering and important evolution with the introduction of LED lighting systems with new strategies of energy savings, incorporation of renewable energy sources and optionally a bidirectional interconnection with the mains (AC grid or DC interconnection bus). Lighting Systems are moving to Lighting Smart Grids and step by step integrating in Smart Cities strategies. In this context design of modular and efficient energy storage/recovery systems are gaining importance looking for future applications and new services. Thus, this work evaluates the use of Dual-Active Bridge (DAB) as energy storage/recovery system in the context of a Lighting Smart Grid. A complete study of this converters, design procedure in order to operate over the Optimal Line (no reactive power) and two simplified control strategy (Linear Phase Droop Control – LPDC and Cosine Phase Droop Control -CPDC) have been proposed, developing in this way a robust design with modular and self-equalization capability.**

Designs have been simulated and tested over a laboratory Lighting Smart Grid obtaining satisfactory results.

***Index Terms*— Lighting Smart Grid, Dual-Active Bridge, Renewable Energy, LED lighting, Energy Storage, Smart Cities**

I. Introduction

Lighting Systems are suffering and important evolution, moving to Lighting Smart Grids (LSG) and open the door to new capabilities and new services to citizens. Different strategies can be adopted thinking in a LSG [1] involving LED drivers, incorporation of renewable energy sources using Maximum Power Point Tracking (MPPT) strategies, capability of grid or DC bus interconnection in order to extract or deliver energy outside the lighting system and, of course, the energy storage/recovery systems focus of this work. All these elements are presented in figure 1 showing a typical LSG with all of this elements.

Each element in the system play a different role and behaviors are predictable or unpredictable depending of external, environmental decision or energy saving strategies.

Renewable sources operate with MPPT control, looking for extract as power as possible from sun, wind or any other renewable source. Power injected to the DC bus is unpredictable and depends on external conditions.

On the other hands, LED Lighting Systems represents the Power load, maximum power in known but control strategies depends also in environmental conditions, strategy for energy savings and so on. Also another type of power loads are possible in the context of a Smart City in order to provide new services to citizens (charges for different gadgets, for example).

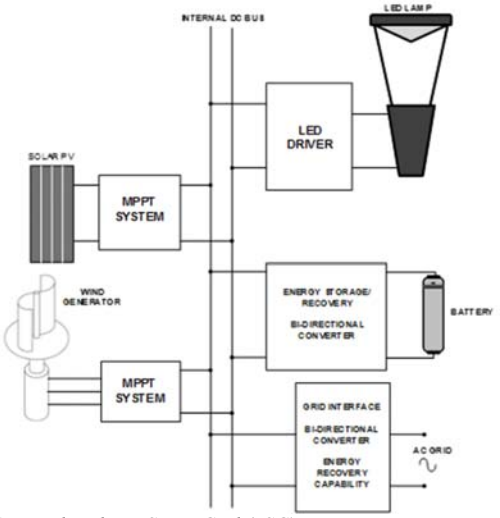

Fig. 1. *A typical Lighting Smart Grid (LSG) system.*

Interface with mains or DC bus is optional, isolated systems do not incorporate mains interface capability. In any case, power injection or extraction may depend of different grids strategies, is controllable but must be considered also as unpredictable.

In this context, the role of energy storage/recovery system is

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fundamental. Stabilization of DC bus is the main task of this elements: store or recovery energy depending on system situation. Perfect bus stabilization is possible by means of coordinate operation of all energy storage/recovery modules (master-slave operation and communication between modules is required) but in LSG, with a dedicated internal DC bus, a friendly range of fluctuation of DC bus is possible and simplify design of all elements.

Using strategies of power extracted or injected to or from the DC bus voltage as a function of the voltage value (Droop Control), see figure 2, communications between modules is not required in order to assure a perfect equalization of all energy/storage modules assuring a perfect operation a high level of modularity in the whole system.

This study propose the use of DAB converters as energy storage/system using a easy to implement strategy of simplified Droop Control strategies, denoted as Linear Phase Droop Control (LPDC) and Cosine Phase Droop Control (CPDC). A complete study of the DAB converter in order to make compatible LPDC/CPDC strategies with operation over optimal line (not reactive energy and zero current switching in one of the inverters) has been done.

II. BASIC OPERATION OF THE DUAL-ACTIVE BRIDGE (DAB) CONVERTER

Figure 3 shows the basic and well-known [2][3] [4][5] [6] structure of a DAB converter used in different applications, in this case proposed as a modular energy storage/recovery system for a Lighting Smart Grid. It is a bidirectional converter [2] and

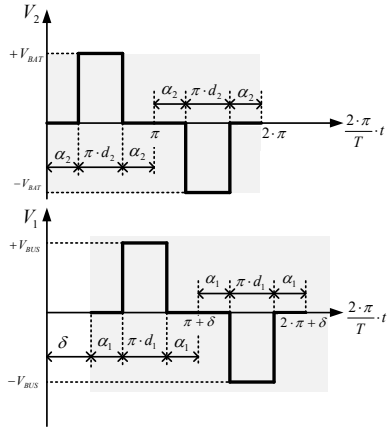

Fig. 4. Typical control waveforms (δ positive, energy storage)..

it is based in the coordinate operation of two full bridge inverters, one inductor and, optionally, one isolation transformer.

Several design strategies can be conducted in order to use this extremely flexible converter. Duty Cycles (d1 and d2) and phase shift (δ1 and δ2) of both converters can be used as control signals. δ2 is assumed as reference (δ2=0) and δ1 represents the phase of waveforms between both inverters (δ1 = δ).

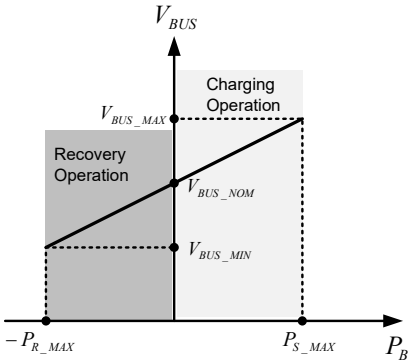

Fig. 2. Design objective of linear Power versus DC bus voltage control strategy for each Energy/Recovery module.

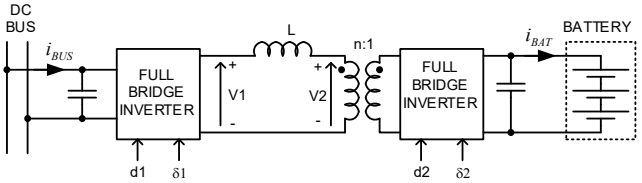

Fig. 3. Basic structure of a Dual Active-Bridge (DAB) bidirectional converter.

Typical waveforms have been included in figure 4. It is necessary to mention that d_1 and d_2 moves from 0 to 1 and phase δ moves from – 180º to +180º (Negatives values implies V_1 voltage delayed with V_2 voltage and positive values implies V_1 voltage in advance with V_2 voltage).

Different methods of analysis can be found in the literature, but in this work a Fourier analysis has been conducted in order to establish a design procedure.

The Fourier development of $V_1(t)$ is:

$$V_1(t) = \frac{4 \cdot n \cdot V_{BAT}}{\pi} \cdot \sum_{i=0}^{\infty} \frac{1}{2 \cdot i + 1} \cdot \cos\left(\frac{\pi}{2} \cdot (1 - d_1) \cdot (2 \cdot i + 1)\right) \cdot \sin\left(\frac{2 \cdot \pi}{T} \cdot (2 \cdot i + 1) \cdot t\right) \quad (1)$$

The fundamental value of V_1 voltage is obtained with i=0:

$$V_{1\_F}(t) = \frac{4 \cdot n \cdot V_{BAT}}{\pi} \cdot \cos\left(\frac{\pi}{2} \cdot (1 - d_1)\right) \cdot \sin\left(\frac{2 \cdot \pi}{T} \cdot t\right) \quad (2)$$

In the same way, de Fourier development of $V_2(t)$ is:

$$V_2(t) = \frac{4 \cdot V_{BUS}}{\pi} \cdot \sum_{i=0}^{\infty} \frac{1}{2 \cdot i + 1} \cdot \cos\left(\frac{\pi}{2} \cdot (1 - d_2) \cdot (2 \cdot i + 1)\right) \cdot \sin\left(\frac{2 \cdot \pi}{T} \cdot (2 \cdot i + 1) \cdot t + \delta \cdot \frac{\pi}{180}\right) \quad (3)$$

And similarly, the fundamental value of V_2 voltage is obtained with i=0:

$$V_{2\_F}(t) = \frac{4 \cdot V_{BUS}}{\pi} \cdot \cos\left(\frac{\pi}{2} \cdot (1 - d_2)\right) \cdot \sin\left(\frac{2 \cdot \pi}{T} \cdot t + \delta \cdot \frac{\pi}{180}\right) \quad (4)$$

Using a complex representation of each harmonic, the output of each inverter (V_1 and V_2) and the current across the inductor can be easily obtained.

$$\vec{V}_{1\_i} = \frac{4 \cdot n \cdot V_{BAT}}{\pi \cdot (2 \cdot i + 1)} \cdot \cos\left(\frac{\pi}{2} \cdot (1 - d_1) \cdot (2 \cdot i + 1)\right) \quad (5)$$

$$\vec{V}_{2\_i} = \frac{4 \cdot V_{BUS}}{\pi \cdot (2 \cdot i + 1)} \cdot \cos\left(\frac{\pi}{2} \cdot (1 - d_2) \cdot (2 \cdot i + 1)\right) \cdot \left[\cos\left(\delta \cdot \frac{\pi}{180}\right) + j \cdot \sin\left(\delta \cdot \frac{\pi}{180}\right)\right] \quad (6)$$

And

$$\vec{I}_{L\_i} = \frac{\vec{V}_{1\_i} - \vec{V}_{2\_i}}{R + j \cdot 2 \cdot \pi \cdot f \cdot (2 \cdot i + 1) \cdot L} \quad (7)$$

In the particular case of the fundamental value (i=0) these expressions are:

$$\vec{V}_1 = \frac{4 \cdot n \cdot V_{BAT}}{\pi} \cdot \cos\left(\frac{\pi}{2} \cdot (1 - d_1)\right) \quad (8)$$

And

$$\vec{V}_2 = \frac{4 \cdot V_{BUS}}{\pi} \cdot \cos\left(\frac{\pi}{2} \cdot (1 - d_2)\right) \cdot \left[\cos\left(\delta \cdot \frac{\pi}{180}\right) + j \cdot \sin\left(\delta \cdot \frac{\pi}{180}\right)\right] \quad (9)$$

And

$$\vec{I}_L = \frac{\vec{V}_1 - \vec{V}_2}{R + j \cdot 2 \cdot \pi \cdot f \cdot L} \quad (10)$$

The active power (Pi) and the reactive power (Qi) handled by the converter can be also easily obtained for each harmonic:

$$\vec{S}_i = \frac{\vec{V}_{2\_i} \cdot \vec{I}_{L\_i}}{2} = P_i + j \cdot Q_i \quad (11)$$

The expressions obtained (12) and (13) are:

$$P_i = \frac{NUM1}{R^2 + 4 \cdot \pi^2 \cdot f^2 \cdot (2 \cdot i + 1)^2 \cdot L^2}$$

with

$$NUM1 = R \cdot |V_{1\_i}| \cdot |V_{2\_i}| \cdot \cos(\delta) - R \cdot |V_{2\_i}|^2 + |V_{1\_i}| \cdot |V_{2\_i}| \cdot 2 \cdot \pi \cdot f \cdot (2 \cdot i + 1) \cdot L \cdot \sin(\delta) \quad (12)$$

And

$$Q_i = \frac{NUM2}{R^2 + 4 \cdot \pi^2 \cdot f^2 \cdot (2 \cdot i + 1)^2 \cdot L^2}$$

with

$$NUM2 = R \cdot |V_{1\_i}| \cdot |V_{2\_i}| \cdot \sin(\delta) - |V_{1\_i}| \cdot |V_{2\_i}| \cdot 2 \cdot \pi \cdot f \cdot (2 \cdot i + 1) \cdot L \cdot \cos(\delta) + 2 \cdot \pi \cdot f \cdot (2 \cdot i + 1) \cdot L \cdot |V_{2\_i}|^2 \quad (13)$$

And from these expression the total active power (P) and the total reactive power (Q) handled for the converter have been obtained (14) and (15) and represented in figures 5 and 6.

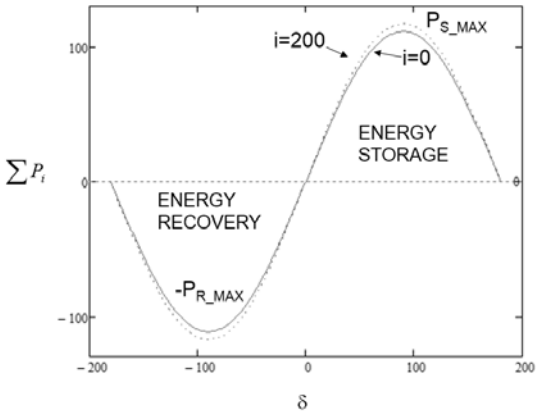

Fig. 5. *Power handled by the converter ($\sum P_i$) using only fundamental (i=0) and 200 Harmonics. (V_{BUS} = 24 V, V_{BAT} = 12 V, f = 50 KHz, n = 1, L = 10 µH and R = 1 mΩ)*

$$P = \sum_{i=0}^{\infty} P_i \quad (14) \qquad Q = \sum_{i=0}^{\infty} Q_i \quad (15)$$

It is important to emphasize that differences between design based on fundamental harmonic and complete signal is very small. As it is shown in figures 7 and 8 differences in Active Power (P) and Reactive Power (Q) really small. As it is well kwon maximum power stored (δ positive) or delivered (δ negative) it is obtained with a phase-shift of 90º (in advance or

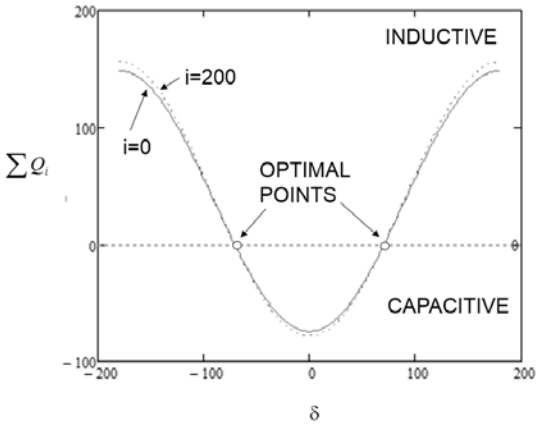

Fig. 6. *Reactive Power handled by the converter ($\sum Q_i$) using only fundamental (i=0) and 200 Harmonics. (V_{BUS} = 24 V, V_{BAT} = 12 V, f = 50 KHz n = 1, L = 10 µH and R = 1 mΩ)*

delayed).

On the other hand, the maximum Reactive Power handled by the converter occurs with phase-shift values of 0º (capacitive behavior) and 180^0 (Inductive behavior). In the figure 6, optimal points (Q=0) have been marked. Operation in this points implies an optimal design and it is the goal of this work.

The operation of the converter is graphically presented in the Figure 7. Two vectors V_1 and V_2 represent the output voltage of both inverters delayed the phase δ. Accessible region of the DAB converter is inside the circle of greater voltage (V_1 or V_2).

Energy Storage Region and Energy Delivered Region have been emphasized in the figure 7. Absolute Maximum Power Points, P_{S_MAX} and P_{R_max} , (phase ±90º) are also indicated in the figure.

The Optimal Line (Q=0 Line) divides the operation area in two regions denoted as capacitive and inductive behavior.

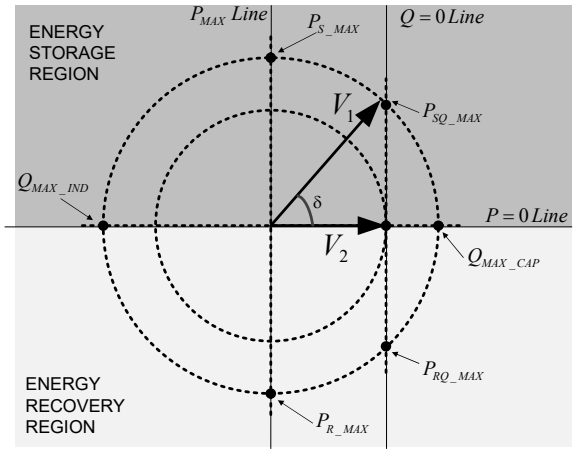

Fig. 7. *Operation regions of a DAB converter.*

Assuring operation over Optimal Line, maximum power capability in order to store or recover energy have been indicated in the figure (points P_{SQ_MAX} and P_{RQ_max}). Both points are fundamental elements in the design proposal included in this paper.

Regions are different depending on relative values of V_1 and V_2. In any case, in the context of this paper, δ positive implies V_1 in advance with V_2.

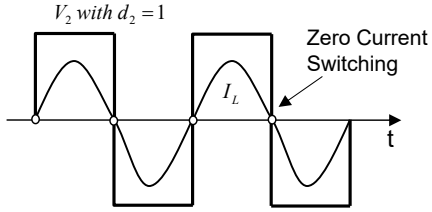

Fig. 8. *DAB operation over Q=0 line with LPDC or CPDC. Zero Current Switching (ZCS)..*

Operation over the Optimal Line between P_{SQ_MAX} and P_{RQ_max}, implies a quasi-linear relationship between Power (P) and angle (δ) and this a remarkable consideration.

Taking into account these ideas, two control strategies have been proposed (Linear Phase Droop Control – LPDC and Cosine Phase Droop Control-CPDC) in order to operate over this line.

If V_1 is greater than V_2, operation over Optimal Line implies not reactive power and Zero Current Switching (ZCS) capability in the Battery Inverter (V_2). See figure 8 for ZCS waveforms in V_1.

Furthermore, If V_2 is greater than V_1, operation over Optimal Line implies not reactive power and ZCS capability in the DC bus Inverter (V_1).

This is an additional advantage to be considered during design procedure. Depending on the control strategy proposed ZCS can be obtained in one of the inverters (p.e. in the battery inverter during energy storage an energy recovery process with LPDC) or in both inverters depending on storage or recovery energy process (p.e. in the battery inverter during energy storage process and in de DC bus inverter during energy recovery process with CPDC).

III. DESIGN STRATEGY OF DAB CONVERTER AS ENERGY/RECOVERY SYSTEM IN A LIGHTING SMART GRID

Having in mind previous consideration the main design criteria is to assure ZCS in one or in both of the inverters during the whole operation range move all the operation points in the Optimal Line.

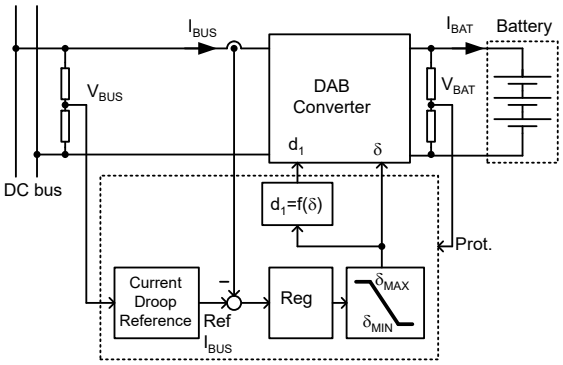

Fig. 9. *DAB control with optimal line follower, internal DC bus current regulation and current reference DC bus voltage dependent (general Current Droop Control-CDC).*

(a).- LPDC implementation (Figure 11).

With LPDC, transformer ratio n must be chosen to assure $V_1>V_2$ during all the operation region and the duty cycle of V_2 voltage has been chosen in order to assure $d_2=1$. With this LPDC, ZCS is possible in the Battery Inverter (V_2) during energy storage and also energy recovery.

LPDC assuring $V_2 > V_1$ during all operation region is also possible, assuring in this case ZCS operation in the DC Bus Inverter (V_1). Design of this option is similar to LPDC and it has not been included in this paper.

With LPDC implementation, a direct relationship between phase angle (δ) and specified duty cycle (d_1 value) in V_1 inverter

(DC bus inverter) exists in order to assure the operation over "Q=0 line", optimal line, allowing ZCS in battery inverter (V_2).

(b).- CPDC implementation (Figure 12).

With CPDC, transformer ratio n must be chosen to assure V_1=V_2 with nominal values. Then, during energy charging state V_1 is greater than V_2 (V_1>V_2) and during energy recovery state V_2 is greater than V_1 (V_2>V_1).

The phase δ is chosen as a cosine function of DC bus voltage in order to assure operation over the Optimal Line allowing operation always with duty equal 1 in both inverters (d_1 and d_2 =1).

Important advantage and simplification of MCU implementation. Using the proposed cosine function, obtained from the analysis, ZCS is achieved in battery inverter (V_2) during energy storage (V_1>V_2). Similarly, ZCS is achieved in the DC bus inverter (V_1) during energy recovery (V_2>V_1). In any case, LPDC and CPDC implies δ value has been adopted as regulation parameter.

(c) Mathematical study of LPDC and CPDC implementations.

Mathematically operation over optimal line implies:

$$\left|\vec{V}_1\right| \cdot \cos(\delta) = \left|\vec{V}_2\right| \tag{16}$$

And using fundamental approach, the condition of operation over the optimal line can be obtained:

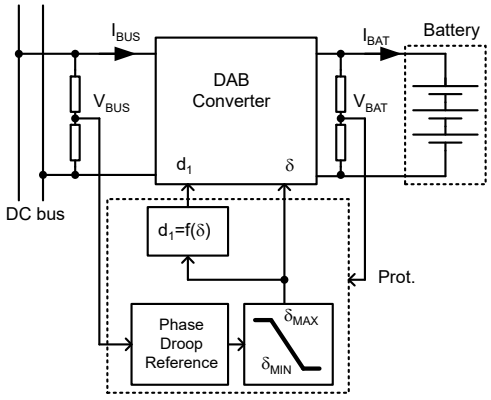

Fig. 10. *DAB control with optimal line follower and phase-shift reference DC bus voltage dependent (LPDC or CPDC).*

$$\frac{4 \cdot V_{BUS}}{\pi} \cdot \cos\left[\frac{\pi}{2} \cdot (1 - d_1)\right] \cdot \cos\left(\delta \cdot \frac{\pi}{180}\right) = \frac{4 \cdot n \cdot V_{BAT}}{\pi} \tag{17}$$

In a general situation, the task of obtain the duty cycle value (d1) from this expression is complex, and implies a complex MCU implementation of the.

Figure 9 shows a DAB control with optimal line follower, internal DC bus current regulation and current reference DC bus

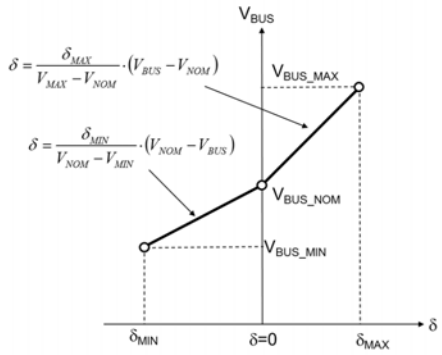

Fig. 11. *Linear implementation of LPDC.*

voltage dependent (general Current Droop Control-CDC). Behavior of this converter is excellent but the disadvantage is a complex implementation in the MCU. The advantage is the perfect control of the current extracted or injected to/from the DC bus.

As alternative to this design, figure 10, shows the proposed implementation. DAB control with optimal line follower and phase-shift reference as a function of the DC bus voltage (LPDC or CPDC).

One of the advantages of both proposed designs is, only V_{BUS} will be used to modify the phase δ (that is to say: or V_{BUS} = f(δ)) and another advantage it is not current sensing is required in order to implement the control method.
Control of the current extracted or injected from/to de DC bus

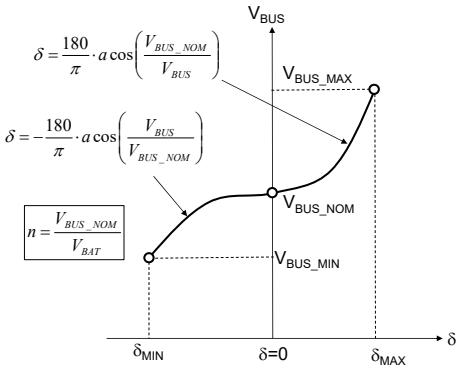

Fig. 12. *Cosine implementation of CPDC.*

is not perfect with both methods, but enough to assure a correct operation of the energy storage/deliver system and a perfect equalization of different modules connected to the bus.

With LPDC implementation estimation of duty cycle (d_1) has been obtained, see equation (18), implementation is easy and can be stored in the MCU memory as a simple table with different values depending on phase shift angle (δ).

With CPDC implementation, d_1 is always 1 in all the operation range.

$$d_1(\delta) = 1 - \frac{2}{\pi} \cdot a\cos\left(\frac{n \cdot V_{BAT}}{V_{BUS}(\delta) \cdot \cos\left(\delta \cdot \frac{\pi}{180} \right)} \right) \quad (18)$$

Figure 11 shows graphically the linear implementation of PDC control (LPDC) and figure 12 shows the sinusoidal implementation of PDC control (CPDC), with cosine function dependence between DC bus voltage (V_{BUS}) and phase δ.

IV. DESIGN EXAMPLE, EXPERIMENTAL AND SIMULATION VERIFICATION

An experimental DAB converter with both Linear Phase Droop Control (LPDC) and Cosine Phase Droop Control (CPDC) have been tested and simulated. A laboratory prototype of both implementations are now under construction and operation of the converter under test will be evaluated over a laboratory Lighting Smart Grid, using renewable sources with Maximum Point Tracking Operation (MPPT) and a LED Lighting System with maximum power of 30 W.

The main elements of the converters are:

- Inductance (L): 10 μH with Rs = 0.1 Ω
- Isolation transformer (1:1). Lm = 1 mH, Ld1 =Ld2= 0.05 uH, Rs1= Rs2=5 mΩ (LPDC implementation)
- Isolation transformer (2:1). Lm = 1 mH, Ld1 = 0.2 uH, Ld2= 0.05 uH, Rs1= 20 mΩ, Rs2=5 mΩ (CPDC implementation)
- Power Mosfet= IRSM005-301H 30A, 100 V, R_{DS} = 35 mΩ, Vd = 0.2 V, Rd = 10 mΩ
- Switching Frequency = 50 KHz (T = 20 μS). Dead Time = 0.2 μS
- V_{BAT} = 12 V (Voltage Point under test). Lithium batteries of 3.2 V/15 Ah (V_{CELL_MAX}=3.7 V and V_{CELL_MIN} = 2 V) have been used in the final laboratory prototype.
- Bus voltage: V_{BUS_MAX}=36 V, V_{BUS_NOM}=24 V, V_{BUS_MIN}=18 V.

Using these parameters the next design values have been obtained:

LPDC operation:

- δ_{MAX}= 72^0 (theoretical P_{SQ_MAX}= 111.5 W, V_{BUS} = 36 V with d_1 =1). Maximum Charging Power
- δ_{MIN}= -42^0 (theoretical P_{RQ_MAX}= 46.2 W, V_{BUS} = 18 V with d_1 =1). Maximum Recovering Power

CPDC operation (d1 and d2 always 1):

- δ_{MAX}= $48{,}2^0$ (theoretical P_{SQ_MAX}= 174.7 W, V_{BUS} = 36 V). Maximum Stored Power
- δ_{MIN}= -41.4^0 (theoretical P_{RQ_MAX}= -77.5 W, V_{BUS} = 18 V). Maximum Recovered Power

A low cost ARM-based 32-bit MCU from ST (STM32F051R8) has been used in order to implements the control. PWM control has been implemented by software using powerful capabilities of above mentioned MCU. Module IRSM005-301H from IR integrated one leg inverter (two Power MOS of 100 V and 20 A) with all drivers and allowing direct interface with the MCU using 3.3 V logic levels. Power stages can be easily implemented in a robust way using four IRSM005-301H modules (2 for each inverter).

Several Simulation Test have been done in order to validate theoretical design:

TEST 1: LPDC implementation and maximum energy storage point: V_{BUS}= 36 V, V_{BAT}=12 V (see figure 13 for waveforms) P_{BUS} = 122.4 W P_{BAT} = 101.5 W η=82.9% (theoretical value = 111.5 W)

TEST 2: LPDC implementation and maximum energy delivery point: V_{BUS}= 18 V, V_{BAT}=12 V (see figure 14 for waveforms) P_{BUS} = -39.6 W P_{BAT} = -44.0 W η=90% (theoretical value = 46.2 W)

TEST 3: LPDC implementation and point of not power handled: V_{BUS}= 24 V, V_{BAT}=12 V (see figure 15 for waveforms) P_{BUS} = -17.6 mW P_{BAT} = -0.38 W (Theoretical value =0)

TEST 4: CPDC implementation in maximum energy storage point: V_{BUS}= 36 V, V_{BAT}=12 V n=2 (see figure 16 for waveforms). P_{BUS} = 179.7 mW P_{BAT} = 159.7 W η=88.8 % (Theoretical value =174.7 W)

TEST 5: CPDC implementation in maximum energy delivery point: V_{BUS}= 18 V, V_{BAT}=12 V n=2 (see figure 17 for waveforms). P_{BUS} = -71.6 W P_{BAT} = -81.5 W η=87.8 % (Theoretical value =77.5 W)

TEST 6 : CPDC implementation: Power fluctuations again 200 Hz fluctuation in DC bus. Test V_{BUS}= 24±5 V/ 200 Hz, V_{BAT}=12 V n=2 (see figure 18 for waveforms)

TEST 7 : CPDC implementation: Power fluctuation response again 200 Hz fluctuation in Battery voltage (I). Test V_{BAT}= 12±2 V/ 200 Hz, V_{BUS}=36 V n=2 (see figure 19 for waveforms).

TEST 8 : CPDC implementation: Power fluctuation response again 200 Hz fluctuation in Battery voltage (II). Test V_{BAT}= 12±2 V/ 200 Hz, V_{BUS}=24 V n=2 (see figure 20 for waveforms).

TEST 9 : CPDC: Power fluctuation response again 200 Hz fluctuation in Battery voltage (III). Test V_{BAT}= 12±2 V/ 200 Hz, V_{BUS}=18 V n=2 (see figure 21 for waveforms).

Final prototypes will be evaluated over a laboratory Lighting Smart Grid using a renewable energy source with MPPT operation delivering to DC bus a total power of 50 W and a LED lighting system consuming a power of 30 W. ON/OFF

operation in both elements has been verified using DAB converter with Phase Droop Control (PDC).

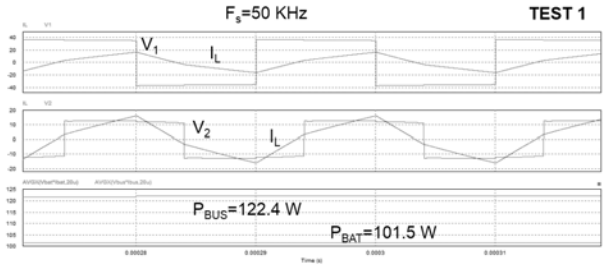

Fig. 13. *Test 1 LPDC implementation (V_{BUS}= 36 V, V_{BAT}=12 V, n=1).*

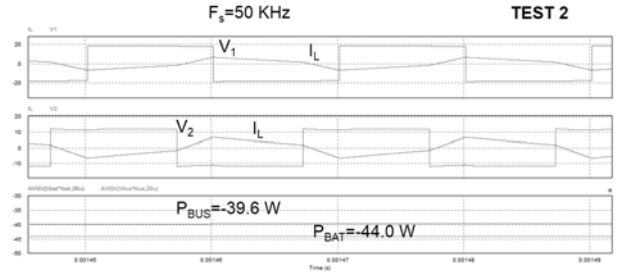

Fig. 14. *Test 2 LPDC implementation (V_{BUS}= 18 V, V_{BAT}=12 V, n=1).*

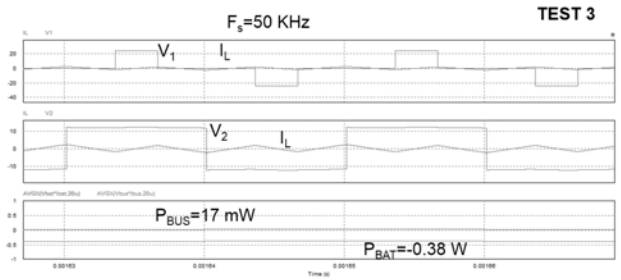

Fig. 15. *Test3 LPDC implementation (V_{BUS}= 24 V, V_{BAT}=12 V, n=1).*

V. CONCLUSIONS

Lighting Systems are suffering and important evolution with introduction of LED lighting capabilities allowing new strategies of energy savings, incorporation of renewable energy sources and optionally a bidirectional interconnection with the mains (AC grid or DC interconnection bus).

Lighting Systems are moving to Lighting Smart Grids a step by step integrating in Smart Cities strategies. In this context design of modular and efficient energy storage/recovery systems are gaining importance looking for future applications and new services.

This work evaluates the use of Dual-Active Bridge (DAB) as energy storage/recovery system thinking in the context of a Lighting Smart Grid.

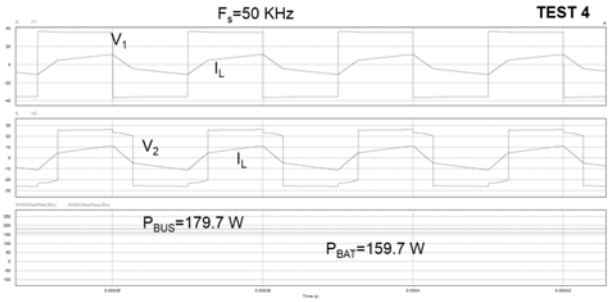

Fig. 16. *Test 4 CPDC implementation (V_{BUS}= 36 V, V_{BAT}=12 V, n=2)*

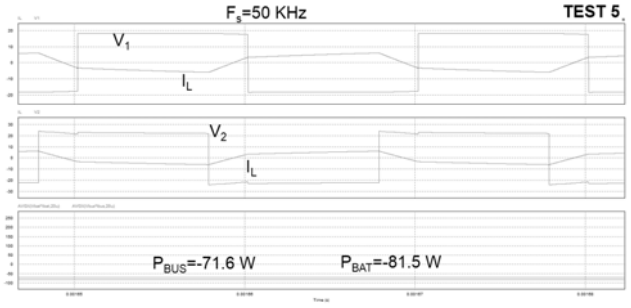

Fig. 17. *Test 5 CPDC implementation (V_{BUS}= 18 V, V_{BAT}=12 V, n=2)*

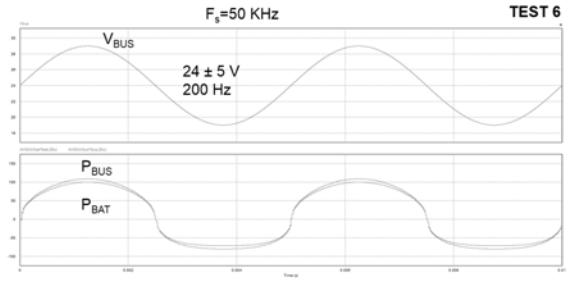

Fig. 18. *Test 6 CPDC implementation (V_{BUS}= 24±5 V/ 200 Hz, V_{BAT}=12 V, n=2)*

A complete study of this converters, design procedure in order to operate over the Optimal Line (no reactive power) and two simplified control strategies (Linear Phase Droop Control – LPDC and Cosine Phase Droop Control – LPDC) have been proposed, offering robust, modular and self-equalization performances.

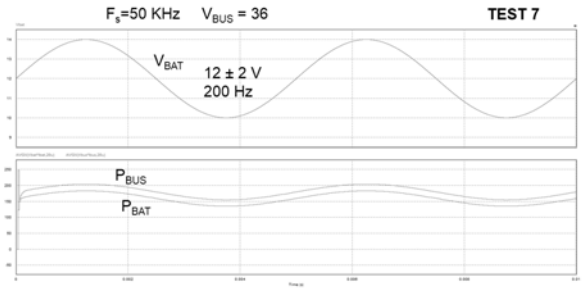

Fig. 19. *Test 7 CPDC implementation (V_{BAT}= 12±2 V/ 200 Hz, V_{BUS}=36 V, n=2)*

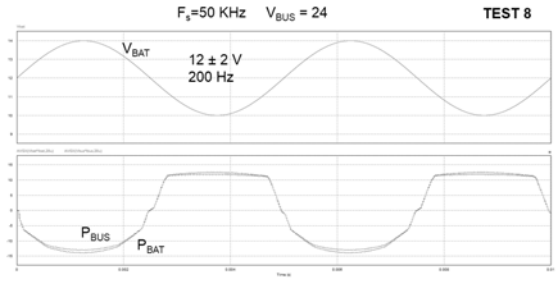

Fig. 20. *Test 8 CPDC implementation (V_{BAT}= 12±2 V/ 200 Hz, V_{BUS}=24 V, n=2)*

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