

# Small-Signal and Large-Signal Analysis of the Two-Transformer Asymmetrical Half-Bridge Converter Operating in Continuous Conduction Mode

Manuel Arias, Marcos Fernández, Diego González Lamar, Francisco Fernández Linera, Javier Sebastián

**Abstract.**—The Asymmetrical Half-Bridge converter (AHBC) has many advantages over other PWM converters. The possibility of soft switching in primary switches and reduced switching losses in the secondary ones implies that the AHBC is a suitable topology for many high-performance applications. Besides, the lack of dead times, except those needed for achieving soft switching, is a very interesting feature to implement self-driven synchronous rectification. Moreover, the small size of its output filter is also a remarkable advantage in some fields (e.g., LED lighting). On the other hand, it also has some disadvantages. One of them is the short range of the duty cycle (lower than 0.5) and the other one is the difficult regulation due to a complex transfer function. The Two-Transformer AHBC (TTAHBC) solves the first problem as it enlarges the duty cycle range making its top limit higher than 0.5. Nevertheless, the regulation of this converter is still very complex and, besides, the transfer functions of the standard AHBC are not valid for the TTAHBC. As a consequence, the small- and large-signal models have yet to be studied. In this paper, the complete small-signal and large-signal analysis of the TTAHBC operating in Continuous Conduction Mode is provided. The large-signal and small-signal models are developed taking into account the main parasitic components that affect the transient response of this converter. The validation of the resulting model is carried out by means of both, simulation and experimental results. The prototype is a 60-W TTAHBC designed for an input voltage of 400 V and an output voltage of 48 V.

**Keywords:** Asymmetrical Half Bridge, Half Bridge with Complementary Control, Small signal, large signal.

## I. INTRODUCTION

Due to its many advantages, the use of the Asymmetrical Half Bridge (AHBC) [1], [2] has expanded over many fields of application, such as lighting [3], [4], PC power supplies [5], Power Factor Correction [6], [7], telecommunication and computer server applications [8], [9] and, in general, low-to-medium power applications [10]. One of its advantages is that the voltage withstood by the primary switches is limited to the input voltage. Besides, Zero Voltage Switching (ZVS) [11]-[15] can be achieved in these switches thanks to the energy stored in the leakage inductance of the transformer and to the right selection of short dead times, strongly reducing switching losses [16]-[18]. Moreover, the achievement of ZVS and a deep analysis of the switching process [19]-[21] also reduce the voltage and current spikes in the rectifier diodes (boosting efficiency as well). The output filter of the AHBC, for applications with a narrow output voltage range, can be very small, reducing cost and size and allowing the development of topologies without electrolytic capacitor, something very important in, for instance, long-lifespan lighting applications [3], [22]-[23]. Besides, the aforementioned

dead times used in the driving signals are very short and, as a consequence, energy is transferred from input to output almost all the time, boosting the power-size ratio [24]. Finally, the AHBC is a perfect candidate for Self-Driven (SD) Synchronous Rectification (SR) technique [25] in low-output-voltage applications, boosting efficiency while the driver of the secondary MOSFETs can be strongly simplified [11], [26]-[28].

It should be mentioned that, due to its many advantages, some topologies derived from the AHBC have been also presented in literature: the AHBC based on the flyback topology [8], [28], the resonant AHBC [13], [29], the AHBC with tapped inductor [10], the AHBC with unbalanced turns ratios in the transformer [30], the two-transformer forward-flyback converter [9], or the Two-Transformer AHBC (TTAHBC) [31]-[32]. Each of them has some advantages and disadvantages in comparison to the standard AHBC (lower number of components, extended duty cycle range, low-profile magnetics, etc.).

Obviously, the AHBC also has some disadvantages. First of all, the maximum duty cycle is 0.5. Therefore, if a wide output voltage and/or input voltage range is desired, the limitation in the maximum duty cycle implies that the converter will have to work with low duty cycles under certain conditions, with the associate problems of current ripple, losses, etc. Another problem is that it is a converter difficult to control [33]-[38]. The transfer function between the output voltage and the control variable is strongly conditioned by the resonance of the magnetizing inductance with the input capacitors [34]. This resonance adds complexity to the task of designing a stable controller [37], [38] and makes virtually impossible to achieve high bandwidths. Therefore, the AHBC is normally relegated to applications with relaxed requirements regarding time response.

Regarding the stability problems and the design of the closed-loop controllers, [35]-[38] present the small-signal analysis of the standard AHBC while [33] presents the same analysis but when a voltage doubler is used. Moreover, [34] explains the advantages of including a feedforward loop in the standard AHBC. These small-signal models allow the designers to adjust the phase margin of the AHBC in close loop without instability risks (even though the controller still cannot be very fast). References [39]-[41] present the large-signal and small-signal models of the current-mode control of the standard AHBC while [30] presents the same model but with unbalanced turns ratios in the transformer. Although bandwidth can be boosted, the inner loop may lead to fast variations of the duty cycle and, as a consequence, to

large and uncontrolled currents through primary MOSFETs due to energy exchange between the input capacitors.

The problem with the maximum duty cycle can be solved by using a Two-Transformer AHBC (TTAHBC) in series-series connection as explained in [31] and [42]-[44], which is different from other configurations, such as series-parallel [45], parallel-parallel [46] or parallel-series [8] connections. In the TTAHBC with series-series connection, the proper selection of the turns ratios of each transformer allows the maximum duty cycle to be higher than 0.5 (this will be fully explained later in this paper). Nevertheless, adding the second transformer invalidates the equations obtained in [33]-[38] for the standard-AHBC small-signal analysis. Hence, obtaining the transfer functions that relates the output voltage with the control variable (duty cycle) and with the input voltage (audiosusceptibility) have yet to be studied in the TTAHBC. In this paper, the small-signal and large-signal models of this converter are presented and deeply analysed. The results show that the TTAHBC model is completely different and more complex than the model of the standard AHBC due to the interaction of both transformers.

This paper is organized as follows. A brief description of the TTAHBC is presented in section II in order to provide some background to the next sections. The small-signal analysis is explained in section III. This section also includes some useful hints in order to simplify the resulting quartic equations in the denominator of the transfer functions. Besides, the large-signal and small-signal equivalent circuits are presented in section 0 in order to ease the addition of parasitic components to the analysis. Although it is not the main purpose of the paper, a brief guideline for the design of the closed-loop controller is presented in section V, focusing on the influence of system parameters in stability. Finally, the experimental results will be provided in section VI in order to validate the theoretical models and calculations and all the conclusion will be gathered in section VII.

## II. SHORT DESCRIPTION OF THE TTAHBC. STEADY-STATE ANALYSIS

It is not the purpose of this paper to explain the full static analysis of the TTAHBC as it is already done in [31], [42]-[44]. Only a brief description of its principle of operation and its main features will be provided in order to give support to the small-signal analysis.

The schematic of the TTAHBC is shown in Fig. 1. As can be seen, the driving signals of both MOSFETs are complementary (i.e., asymmetrical), so one of the primary MOSFETs is always turned on. If the converter is operating

in Continuous Conduction Mode (CCM), diode  $D_1$  is directly biased all the time  $M_1$  is turned on while diode  $D_2$  is directly biased all the time MOSFET  $M_2$  is turned on. As a consequence, and taking into account that the volt-second balance in the magnetizing inductances of the transformers has to be maintained, the voltages of the input capacitors depend on the duty cycle:

$$V_{C1} = (1-D) \cdot V_g, \quad (1)$$

$$V_{C2} = D \cdot V_g, \quad (2)$$

where  $V_{C1}$  and  $V_{C2}$  are the voltages of the input capacitors  $C_1$  and  $C_2$ ,  $D$  is the duty cycle of MOSFET  $M_1$  and  $V_g$  is the input voltage. As can be seen, these voltages are different except when  $D=0.5$ .

The static transfer ratio can be also obtained from the volt-second balance applied to the transformers [42]:

$$V_o = V_g \cdot \frac{D \cdot (1-D)}{\frac{D}{n_1} + \frac{1-D}{n_2}}, \quad (3)$$

where  $V_o$  is the output voltage of the TTAHBC and  $n_1$  and  $n_2$  the turns ratios of the two transformers. Differentiating equation (3) it is possible to obtain the value of  $D$  that maximizes the static transfer ratio:

$$D_{\max} = \frac{\sqrt{n_1}}{\sqrt{n_1} + \sqrt{n_2}}, \quad (4)$$

and substituting (4) into (3) the value of that maximum static transfer ratio can be obtained:

$$\left. \frac{V_o}{V_g} \right|_{\max} = \frac{n_1 \cdot n_2}{(\sqrt{n_1} + \sqrt{n_2})^2}. \quad (5)$$

Fig. 2 shows the representation of equation (3) for different values of the ratio between  $n_1$  and  $n_2$  ( $X=n_1/n_2$ ). Depending on this ratio, the maximum static gain is reached for a different value of  $D_{\max}$ , which is always higher than 0.5 if  $n_1$  is higher than  $n_2$  (or equal to 0.5 when  $n_1=n_2$ ). This represents one of the main advantages of this topology. It should be noted that  $n_1$  has to be modified in order to reach the same maximum static gain for different ratios  $n_1/n_2$ . Besides, the voltage withstood by the output rectifiers can also be tailored [31], allowing a better design to be made.

## III. SMALL SIGNAL ANALYSIS

### III.1. Calculation of transfer functions: output voltage-duty cycle and output voltage-input voltage

The nomenclature followed in this paper is as follows:

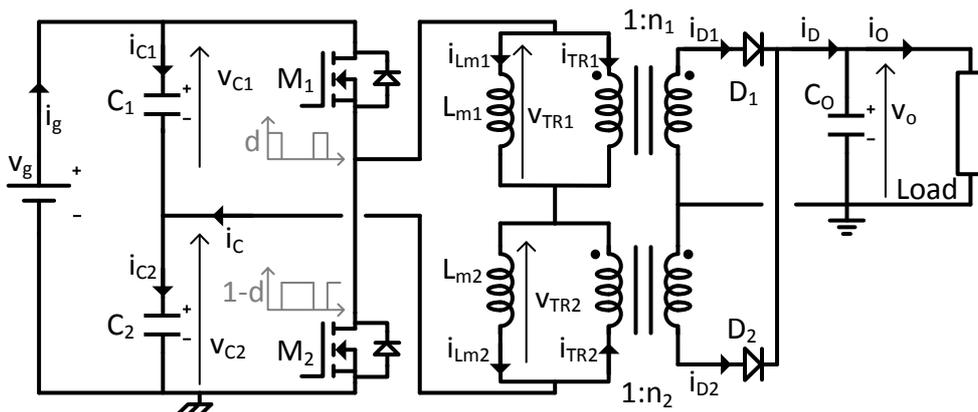


Fig. 1. Schematic of the TTAHBC

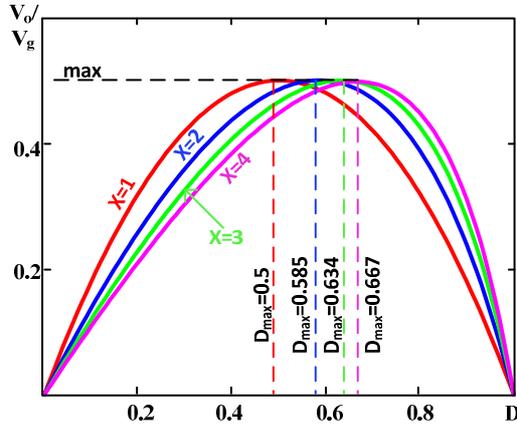


Fig. 2. Static gain for different values of  $X=n_1/n_2$ . Turns ratio  $n_1$  has been adjusted in each case in order to obtain the same maximum static gain.

- Instantaneous quantities are represented with lower-case letters and as a function of time. E.g.,  $i_{c1}(t)$ ,  $v_{TR1}(t)$ .
- Average quantities in a switching period are represented with the corresponding instantaneous quantities inside ' $\langle \dots \rangle_{T_s}$ '. E.g.,  $\langle i_{c1}(t) \rangle_{T_s}$ ,  $\langle v_{TR1}(t) \rangle_{T_s}$ .
- Steady-state values of average quantities are represented with capital letters. E.g.,  $I_{c1}$ ,  $V_{TR1}$ .
- Small-signal perturbations of the average quantities are represented with lower-case letters with  $\hat{\cdot}$ . E.g.,  $\hat{i}_{c1}$ ,  $\hat{v}_{TR1}$ .
- Therefore, any average quantity is equal to the corresponding steady-state value plus the corresponding small-signal perturbation. E.g.,  $\langle i_{c1}(t) \rangle_{T_s} = I_{c1} + \hat{i}_{c1}$ .

Besides, this analysis is made assuming the following considerations:

- The converter operates in Continuous Conduction Mode (CCM).
- All components are ideal. For the sake of simplicity, none of the parasitic components are going to be considered in this analysis. Nevertheless, as their final influence may be relevant, the small-signal and large-signal circuit models (see section 0) will include these parasitic components as a way of taking its influence into account.
- The effect of dead times is neglected. It should be highlighted that ZVS in this topology can be achieved by adding small dead times between the turning-off of one MOSFET and the turning-on of the other. These dead times are very short and, as a consequence, they do not affect the small-signal analysis substantially.

The equations used for carrying out the average techniques [47], [48] are obtained from Fig. 1. The following two equations can be obtained analysing the average voltage of the magnetizing inductances of the transformers:

$$\langle v_{TR1}(t) \rangle_{T_s} = \frac{\langle v_o(t) \rangle_{T_s}}{n_1} \langle d(t) \rangle_{T_s} - \left( \langle v_{c2}(t) \rangle_{T_s} - \frac{\langle v_o(t) \rangle_{T_s}}{n_2} \right) (1 - \langle d(t) \rangle_{T_s}), \quad (6)$$

$$\langle v_{TR2}(t) \rangle_{T_s} = -\frac{\langle v_o(t) \rangle_{T_s}}{n_2} (1 - \langle d(t) \rangle_{T_s}) + \left( \langle v_{c1}(t) \rangle_{T_s} - \frac{\langle v_o(t) \rangle_{T_s}}{n_1} \right) \langle d(t) \rangle_{T_s}, \quad (7)$$

where  $v_{TR1}(t)$  and  $v_{TR2}(t)$  are the voltages applied to the transformers. From the inductors and the capacitors of the circuit:

$$\langle i_{c1}(t) \rangle_{T_s} = C_1 \frac{d \langle v_{c1}(t) \rangle_{T_s}}{dt}, \quad (8)$$

$$\langle i_{c2}(t) \rangle_{T_s} = C_2 \frac{d \langle v_{c2}(t) \rangle_{T_s}}{dt}, \quad (9)$$

$$\langle v_{TR1}(t) \rangle_{T_s} = L_{m1} \frac{d \langle i_{Lm1}(t) \rangle_{T_s}}{dt}, \quad (10)$$

$$\langle v_{TR2}(t) \rangle_{T_s} = L_{m2} \frac{d \langle i_{Lm2}(t) \rangle_{T_s}}{dt}, \quad (11)$$

where  $i_{c1}$  and  $i_{c2}$  are the currents of the input capacitors,  $C_1$  and  $C_2$  their capacitance,  $v_{c1}$  and  $v_{c2}$  their voltages,  $L_{m1}$  and  $L_{m2}$  are the magnetizing inductances of the transformers, and  $i_{Lm1}$  and  $i_{Lm2}$  are their currents.

Applying Kirchhoff's current law and Kirchhoff's voltage law to the circuit:

$$\langle i_{c1}(t) \rangle_{T_s} + \langle i_c(t) \rangle_{T_s} = \langle i_{c2}(t) \rangle_{T_s}, \quad (12)$$

$$\langle i_c(t) \rangle_{T_s} = \langle i_{Lm1}(t) \rangle_{T_s} + \langle i_{TR1}(t) \rangle_{T_s}, \quad (13)$$

$$\langle i_c(t) \rangle_{T_s} = \langle i_{Lm2}(t) \rangle_{T_s} - \langle i_{TR2}(t) \rangle_{T_s}, \quad (14)$$

$$\langle v_g(t) \rangle_{T_s} = \langle v_{c1}(t) \rangle_{T_s} + \langle v_{c2}(t) \rangle_{T_s}, \quad (15)$$

where  $i_c$  is the current that goes to the input capacitors and  $i_{TR1}$  and  $i_{TR2}$  are the currents through the ideal transformers.

Analysing the primary and the secondary side of the ideal transformers:

$$\langle i_{TR1}(t) \rangle_{T_s} = n_1 \langle i_{D1}(t) \rangle_{T_s}, \quad (16)$$

$$\langle i_{TR2}(t) \rangle_{T_s} = n_2 \langle i_{D2}(t) \rangle_{T_s}, \quad (17)$$

where  $i_{D1}$  and  $i_{D2}$  are the currents driven by the diodes  $D_1$  and  $D_2$ .

Considering the output current as a variable of the system so that the analysis is independent from the kind of load connected to the output:

$$\langle i_D(t) \rangle_{T_s} = \left( \langle i_o(t) \rangle_{T_s} + C_o \frac{d \langle v_o(t) \rangle_{T_s}}{dt} \right), \quad (18)$$

where  $C_o$  is the capacitance of the output capacitor and  $i_o(t)$  is the output current.

Finally, two additional equations should be considered:

$$\langle i_D(t) \rangle_{T_s} = \langle i_{D1}(t) \rangle_{T_s} + \langle i_{D2}(t) \rangle_{T_s}, \quad (19)$$

$$\langle i_c(t) \rangle_{T_s} = \langle i_{Lm2}(t) \rangle_{T_s} \langle d(t) \rangle_{T_s} + \langle i_{Lm1}(t) \rangle_{T_s} (1 - \langle d(t) \rangle_{T_s}) \quad (20)$$

The last equation is valid as long as the converter operates in CCM, which is one of the aforementioned assumptions. Besides, this equation is obtained considering that, due to the way this topology works, only one of the

ideal transformers is driving current at the same time (i.e., either  $i_{TR1}$  or  $i_{TR2}$  is always equal to zero).

Perturbing equations (6)-(20) and taking Laplace transforms, the following equations can be obtained:

$$\hat{v}_{TR1} = \hat{v}_o \cdot \left[ D \cdot \left( \frac{1}{n_1} - \frac{1}{n_2} \right) + \frac{1}{n_2} \right] + \hat{d} \cdot \left[ V_o \cdot \left( \frac{1}{n_1} - \frac{1}{n_2} \right) + V_{c2} \right] - \hat{v}_{c2} \cdot (1-D), \quad (21)$$

$$\hat{v}_{TR2} = \hat{v}_o \cdot \left[ D \cdot \left( \frac{1}{n_2} - \frac{1}{n_1} \right) - \frac{1}{n_2} \right] + \hat{d} \cdot \left[ V_o \cdot \left( \frac{1}{n_2} - \frac{1}{n_1} \right) + V_{c1} \right] + \hat{v}_{c1} \cdot D, \quad (22)$$

$$\hat{i}_{c1} = s \cdot C_1 \cdot \hat{v}_{c1}, \quad (23)$$

$$\hat{i}_{c2} = s \cdot C_2 \cdot \hat{v}_{c2}, \quad (24)$$

$$\hat{v}_{TR1} = s \cdot L_{m1} \cdot \hat{i}_{Lm1}, \quad (25)$$

$$\hat{v}_{TR2} = s \cdot L_{m2} \cdot \hat{i}_{Lm2}, \quad (26)$$

$$\hat{i}_{c1} + \hat{i}_C = \hat{i}_{c2}, \quad (27)$$

$$\hat{i}_C = \hat{i}_{Lm1} + \hat{i}_{TR1}, \quad (28)$$

$$\hat{i}_C = \hat{i}_{Lm2} - \hat{i}_{TR2}, \quad (29)$$

$$\hat{v}_g = \hat{v}_{c1} + \hat{v}_{c2}, \quad (30)$$

$$\hat{i}_{TR1} = n_1 \cdot \hat{i}_{D1}, \quad (31)$$

$$\hat{i}_{TR2} = n_2 \cdot \hat{i}_{D2}, \quad (32)$$

$$\hat{i}_D = \hat{i}_O + C_O \cdot s \cdot \hat{v}_O, \quad (33)$$

$$\hat{i}_D = \hat{i}_{D1} + \hat{i}_{D2}, \quad (34)$$

$$\hat{i}_C = \hat{i}_{Lm2} \cdot D + \hat{d} \cdot I_{Lm2} + \hat{i}_{Lm1} \cdot (1-D) - \hat{d} \cdot I_{Lm1}. \quad (35)$$

With these equations, it is possible to obtain the control-to-output-voltage transfer function, the audiosusceptibility and the output impedance of the TTAHBC:

$$G_{vo\_d}(s) = \frac{\hat{v}_o}{\hat{d}} \Big|_{\substack{\hat{v}_g=0 \\ \hat{i}_O=0}} = - \frac{B_{G\_A}(s) \cdot N_{G\_A}(s) + N_{G\_B}(s) \cdot B_{G\_B}(s)}{M_{G\_A}(s) \cdot B_{G\_A}(s) + M_{G\_B}(s) \cdot B_{G\_B}(s)}, \quad (36)$$

$$G_{vo\_vg}(s) = \frac{\hat{v}_o}{\hat{v}_g} \Big|_{\substack{\hat{i}_O=0 \\ \hat{d}=0}} = \frac{B_{G\_A}(s) \cdot N_{G\_C}(s) + N_{G\_D}(s) \cdot B_{G\_B}(s)}{M_{G\_A}(s) \cdot B_{G\_A}(s) + M_{G\_B}(s) \cdot B_{G\_B}(s)}, \quad (37)$$

$$G_{vo\_io}(s) = \frac{\hat{v}_o}{\hat{i}_O} \Big|_{\substack{\hat{v}_g=0 \\ \hat{d}=0}} = - \frac{n_1 \cdot B_{G\_B}(s)}{M_{G\_A}(s) \cdot B_{G\_A}(s) + M_{G\_B}(s) \cdot B_{G\_B}(s)}, \quad (38)$$

where,

$$B_{G\_A}(s) = \left( C_t \cdot s + \frac{D}{L_{m2} \cdot s} \right) \cdot \frac{n_1}{n_2} - \left( C_t \cdot s + \frac{1-D}{L_{m1} \cdot s} \right), \quad (39)$$

$$B_{G\_B}(s) = \frac{(1-D)^2}{L_{m1} \cdot s} + \frac{D^2}{L_{m2} \cdot s} + C_t \cdot s, \quad (40)$$

$$N_{G\_A}(s) = (I_{Lm2} - I_{Lm1}) + \frac{D \cdot V_{c1}}{L_{m2} \cdot s} + \frac{(1-D) \cdot V_{c2}}{L_{m1} \cdot s} + V_o \cdot n_{d12} \cdot \left( \frac{1-D}{L_{m1} \cdot s} - \frac{D}{L_{m2} \cdot s} \right), \quad (41)$$

$$N_{G\_B}(s) = \frac{V_{c2}}{L_{m1} \cdot s} - \frac{n_1 \cdot V_{c1}}{n_2 \cdot L_{m2} \cdot s} + V_o \cdot n_{d12} \cdot \left( \frac{1}{L_{m1} \cdot s} + \frac{n_1}{n_2 \cdot L_{m2} \cdot s} \right), \quad (42)$$

$$M_{G\_A}(s) = n_{dd} \cdot \left( \frac{1-D}{L_{m1} \cdot s} - \frac{D}{L_{m2} \cdot s} \right), \quad (43)$$

$$M_{G\_B}(s) = n_1 \cdot C_O \cdot s + n_{dd} \cdot \left( \frac{1}{L_{m1} \cdot s} + \frac{1}{L_{m2} \cdot s} \cdot \frac{n_1}{n_2} \right), \quad (44)$$

$$N_{G\_C}(s) = C_2 \cdot s + \frac{(1-D)^2}{L_{m1} \cdot s}, \quad (45)$$

$$N_{G\_D}(s) = C_2 \cdot s \cdot \frac{n_2 - n_1}{n_2} + \frac{(1-D)}{L_{m1} \cdot s}. \quad (46)$$

$$n_{dd} = \frac{D}{n_1} + \frac{1-D}{n_2}, \quad (47)$$

$$n_{d12} = \frac{1}{n_1} - \frac{1}{n_2}, \quad (48)$$

$$C_t = C_1 + C_2. \quad (49)$$

$$I_{Lm2} - I_{Lm1} = \frac{n_1 \cdot n_2}{n_1 \cdot (1-D) + n_2 \cdot D} \cdot I_O. \quad (50)$$

Hence:

$$\hat{v}_o = G_{vo\_d}(s) \cdot \hat{d} + G_{vo\_vg}(s) \cdot \hat{v}_g + G_{vo\_io}(s) \cdot \hat{i}_O. \quad (51)$$

Considering that the load connected to the output will present its own transfer function,  $G_{load}(s)$ , which relates output voltage and output current:

$$\hat{v}_o = G_{vo\_d}(s) \cdot \hat{d} + G_{vo\_vg}(s) \cdot \hat{v}_g + G_{vo\_io}(s) \cdot \frac{\hat{v}_o}{G_{load}(s)}. \quad (52)$$

Therefore:

$$\hat{v}_o = \frac{G_{vo\_d}(s)}{\left( 1 - \frac{G_{vo\_io}(s)}{G_{load}(s)} \right)} \cdot \hat{d} + \frac{G_{vo\_vg}(s)}{\left( 1 - \frac{G_{vo\_io}(s)}{G_{load}(s)} \right)} \cdot \hat{v}_g. \quad (53)$$

In order to go in depth in the analysis of the TTAHBC, a pure resistive load [ $G_{load}(s)=R$ ] is going to be considered as example and the corresponding transfer functions will be obtained, using them for analysing the main parameters that contribute to the resonances that will appear in the transient

response. With equation (53), and nulling the perturbed value of  $v_g$ , it is possible to obtain the transfer function  $G_{vo\_d}(s)$  between the output voltage and the control variable (i.e., the duty cycle):

$$G_{vo\_d}(s) = \frac{\hat{v}_0}{\hat{d}} \Big|_{\hat{v}_g=0} = n_{dd} \cdot R \cdot \frac{s^3 \cdot N_A + s^2 \cdot N_B + s \cdot N_C + N_D}{s^4 \cdot M_A + s^3 \cdot M_B + s^2 \cdot M_C + s \cdot M_D + M_E}, \quad (54)$$

being,

$$N_A = L_{m1} \cdot L_{m2} \cdot C_t \cdot (I_{L_{m2}} - I_{L_{m1}}) \cdot \frac{n_{d12}}{n_{dd}}, \quad (55)$$

$$N_B = C_t \cdot [L_{m1} \cdot (V_{c1} - V_o \cdot n_{d12}) - L_{m2} \cdot (V_{c2} + V_o \cdot n_{d12})], \quad (56)$$

$$N_C = \frac{I_{L_{m2}} - I_{L_{m1}}}{n_{dd}} \left( L_{m2} \cdot \frac{1-D}{n_1} - L_{m1} \cdot \frac{D}{n_2} \right), \quad (57)$$

$$N_D = (1-D) \cdot (V_{c1} - V_o \cdot n_{d12}) - D \cdot (V_{c2} + V_o \cdot n_{d12}), \quad (58)$$

$$M_A = L_{m1} \cdot L_{m2} \cdot C_t \cdot C_o \cdot R, \quad (59)$$

$$M_B = L_{m1} \cdot L_{m2} \cdot C_t, \quad (60)$$

$$M_C = R \cdot \left[ C_o \cdot (L_{m1} \cdot D^2 + L_{m2} \cdot (1-D)^2) + L_t \cdot C_t \cdot n_{dd}^2 \right], \quad (61)$$

$$M_D = L_{m1} \cdot D^2 + L_{m2} \cdot (1-D)^2, \quad (62)$$

$$M_E = n_{dd}^2 \cdot R, \quad (63)$$

$$L_t = L_{m1} + L_{m2}, \quad (64)$$

Nulling the perturbed value of  $d$ , the transfer function  $G_{vo\_vg}(s)$  between the input and the output voltage can be obtained:

$$G_{vo\_vg}(s) = \frac{\hat{v}_0}{\hat{v}_g} \Big|_{\hat{d}=0} = n_{dd} \cdot R \cdot \frac{s^2 \cdot [L_{m1} \cdot C_2 \cdot D + L_{m2} \cdot C_1 \cdot (1-D)] + D \cdot (1-D)}{s^4 \cdot M_A + s^3 \cdot M_B + s^2 \cdot M_C + s \cdot M_D + M_E}, \quad (65)$$

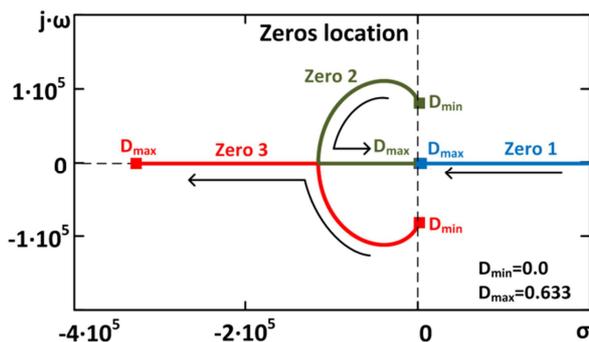
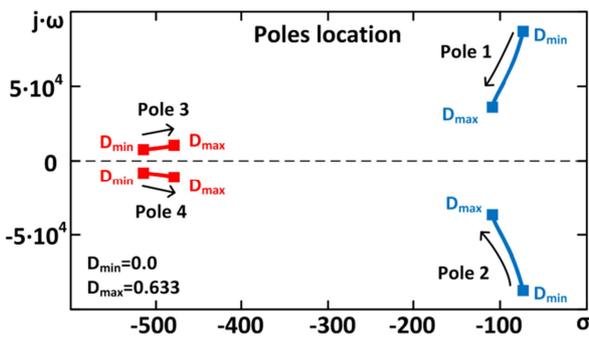


Fig. 3. Location of poles and zeros for a TTAHBC.  $L_{m1}=280 \mu\text{H}$ ,  $L_{m2}=3800 \mu\text{H}$ ,  $V_g=300 \text{V}$ ,  $C_o=6 \times 4.7 \mu\text{F}$ ,  $n_1=1.085$ ,  $n_2=0.366$ ,  $C_1=C_2=270 \text{nF}$ ,  $R=30 \Omega$

The denominator of (54) and (65) and the numerator of (54), which are fourth- and third-order equations, will be simplified in section III.3. Before, the analysis of the output voltage-duty cycle transfer function will be presented.

### III.2. Analysis of the transfer function $G_{vo\_d}(s)$

The analysis of  $G_{vo\_d}(s)$  is fundamental in order to design the TTAHBC and its closed-loop controller. The location of the poles and zeros of (54) in the complex plane  $s=\sigma+j \cdot \omega$  is shown in Fig. 3 for the whole duty cycle range (from  $D_{\min}=0$  to  $D_{\max}=0.633$  in this design example). As can be seen, the transfer function presents two pairs of complex poles and three zeros, one of them always located in the right half-plane (adding complexity when designing the closed-loop controller). Besides, this zero is always real and, for low values of  $D$ , its value is considerably higher than  $2 \cdot 10^5$  (therefore, not shown in Fig. 3). Although the precise location of poles and zeros depends not only on the value of the duty cycle, but also on other parameters ( $L_{m1}$ ,  $L_{m2}$ ,  $V_g$ , etc.), it is possible to analyse the example shown in Fig. 3 in order to explain some useful hints for the design of any TTAHBC (in the next section, the simplified expression of  $G_{vo\_d}(s)$  will allow us to precisely determine which are the main variables that determine the location of each pole and zero). The system pole-zero patterns corresponding to two specific situations of the previously mentioned example ( $D=0.2$  and  $D=0.5$ ) are presented in Fig. 4. With these patterns, it is possible to determine the bode plots of the converter (see Fig. 5) when the duty cycle is equal to 0.2 and when is equal to 0.5. In these bode plots, the resonance frequency, the peak value of the resonances, the slopes, the phase, etc. can be obtained attending to the value of  $\sigma$  and  $j \cdot \omega$  of each pole and zero.

If the duty cycle is limited to low values (see Fig. 4 when  $D=0.2$ ), the moduli (or magnitudes) of the three zeros are higher than the moduli of the four poles. Besides, poles 1 and 2 have the same modulus, whose value is higher than the one corresponding to poles 3 and 4. Therefore, the  $-40 \text{ dB/dec}$  slope introduced by poles 3 and 4 in the bode plot

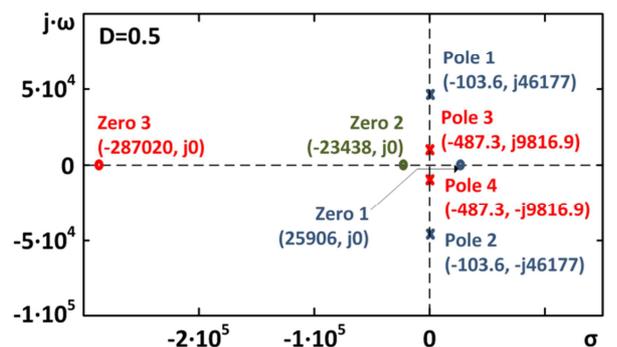
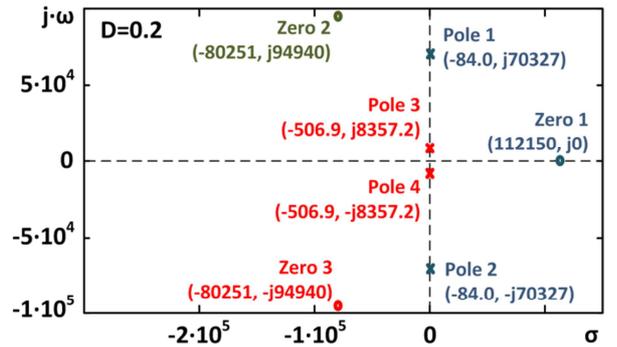


Fig. 4. System pole-zero pattern when  $D$  is equal to 0.2 (left) and to 0.5 (right).

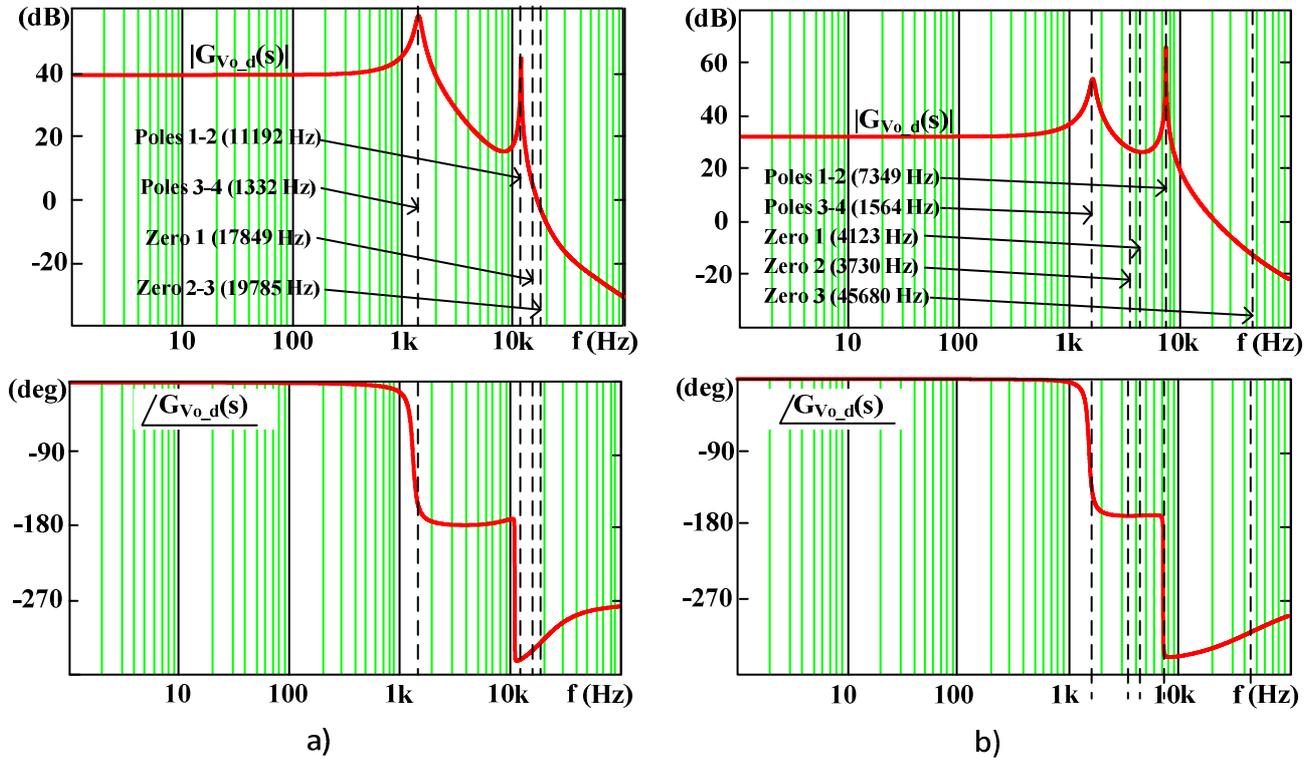


Fig. 5. Bode plots for the proposed TTAHBC (same conditions as Fig. 3). a)  $D=0.2$ ; b)  $D=0.5$ .

makes the resonance due to poles 1 and 2 reaching a lower gain (see Fig. 5a) and, as a consequence, it has a lower impact on the design of the controller and on the stability. Nevertheless, it should be noted that one of the main advantages of the topology (reaching duty cycles higher than 0.5) has been lost in this case.

When the duty cycle increases, the complex zeros become real (see Fig. 4 when  $D=0.5$ ). Besides, the moduli of zeros 1 and 2 decreases and become lower than the modulus of poles 1 and 2. Besides, the modulus of poles 3 and 4 is nearly unchanged while the modulus of poles 1 and 2 becomes smaller. As a consequence (see Fig. 5b), the  $-40$  dB/dec introduced by poles 3 and 4 is partially cancelled by the  $+40$  dB/dec slope introduced by zeros 1 and 2 (one of them located in the right half-plane). Therefore, the resonance due to poles 1 and 2 reaches a higher gain. Moreover, this resonance is located at a lower frequency and, consequently, its effect on stability is even worse. Although this situation may seem to be considerably worse than the previous one, the duty cycle is closer to  $D_{max}$ , taking advantage of an extended duty cycle range.

### III.3. Simplification of $G_{vo_d}(s)$

The analysis of (54) (i.e.,  $G_{vo_d}(s)$ ) in order to determine the influence of each parameter on stability and on the design of the regulator is not easy as has been shown in the previous section. The use of these equations for implementing an adaptive controller or an observer is not easy either due to limitations in computing power in standard microcontrollers of FPGAs. The denominator of (54) is a fourth-degree (quartic or biquadratic) equation whose solution is not easy to obtain by analytical methods (i.e., Ferrari's solution). In (65), the transfer function also presents the same four poles and, as a consequence, the same problem. Due to the topology of the standard AHBC, with just one transformer and one output inductor, it was possible to divide the denominator into two second-order equations, one defined by the output filter and the other one defined by the input capacitors and the magnetizing

inductance of the transformer. Therefore, it was possible to obtain the poles by analytical methods and analyse all the possible situations [37]. Nevertheless, in the case of the TTAHBC, this is not possible. During  $D \cdot T$ , energy is stored in one of the magnetizing inductances ( $L_{m2}$ ) and, at the same time, the other one ( $L_{m1}$ ) transfers its energy to the output. During  $(1-D) \cdot T$ , the first inductance ( $L_{m2}$ ) is the one to transfer energy to the output while the second one ( $L_{m1}$ ) stores energy (i.e., they can be considered as the "false transformer" of a Flyback). Therefore, it is not possible to analytically split the denominator because the magnetizing and demagnetizing processes of one transformer affect the other.

Nevertheless, the denominator of (54) and (65) can be strongly simplified by non-analytical methods paying attention to the relevance of each addend (e.g.,  $M_A \cdot s^4$  or  $M_C \cdot S^2$ ) around the frequency of each double pole. As a consequence, the denominator of (54) and (65) can be rewritten as:

$$\text{Den}(s) \Big|_{\text{poles 1-2}} = s^4 \cdot L_{m1} \cdot L_{m2} \cdot C_t \cdot C_o \cdot R + s^2 \cdot R \cdot [C_o \cdot L_D + L_t \cdot C_t \cdot n_{dd}^2], \quad (66)$$

for frequencies around the frequency of the first double pole, at which the terms in  $s^3$ ,  $s^1$  and  $s^0$  can be neglected. Around the frequency of the second double pole, the terms in  $s^4$ ,  $s^3$  and  $s^1$  can be disregarded and, therefore:

$$\text{Den}(s) \Big|_{\text{poles 3-4}} = s^2 \cdot R \cdot (L_t \cdot C_t \cdot n_{dd}^2 + C_o \cdot L_D) + R \cdot n_{dd}^2 \quad (67)$$

where  $L_D$  is:

$$L_D = L_{m1} \cdot D^2 + L_{m2} \cdot (1-D)^2 \quad (68)$$

The accuracy of this simplification will be shown later. As can be seen, the denominator is now presented as two independent equations which can be easily solved. Therefore, poles can be easily obtained from (66) and (67), which can be used also in adaptive controllers and observers:

$$s_{\text{Poles}_{1-2}} = \pm j \sqrt{\frac{L_t \cdot C_t \cdot n_{dd}^2 + C_0 \cdot L_D}{L_{m1} \cdot L_{m2} \cdot C_0 \cdot C_t}}, \quad (69)$$

$$s_{\text{Poles}_{3-4}} = \pm j \sqrt{\frac{n_{dd}^2}{L_t \cdot C_t \cdot n_{dd}^2 + C_0 \cdot L_D}}. \quad (70)$$

Each of these equations provides a pair of the four poles that equations (54) and (65) present. Besides, this result can be even more simplified attending to the quotient:

$$K_s = \frac{L_t \cdot C_t \cdot n_{dd}^2}{C_0 \cdot L_D} \quad (71)$$

If  $K_s \ll 1$ , equations (69) and (70) can be rewritten as:

$$s_{\text{Poles}_{1-2}} = \pm j \sqrt{\frac{L_D}{L_{m1} \cdot L_{m2} \cdot C_t}}, \quad (72)$$

$$s_{\text{Poles}_{3-4}} = \pm j \sqrt{\frac{n_{dd}^2}{C_0 \cdot L_D}}. \quad (73)$$

On the other hand, when  $K_s \gg 1$ , equations (69) and (70) are rewritten as:

$$s_{\text{Poles}_{1-2}} = \pm j \sqrt{\frac{L_t \cdot n_{dd}^2}{L_{m1} \cdot L_{m2} \cdot C_0}}, \quad (74)$$

$$s_{\text{Poles}_{3-4}} = \pm j \sqrt{\frac{1}{L_t \cdot C_t}}. \quad (75)$$

Although equations for both cases are provided (i.e.,  $K_s \gg 1$  and  $K_s \ll 1$ ), it should be mentioned that standard designs of a TTAHBC normally imply a value of  $K_s$  lower than 1 (see Annex I). Therefore, many times (72) and (73) may be used in order to ease the calculation of the poles. Paying attention to these equations, it is possible to summarize the following:

- The TTAHBC always presents complex poles. As a consequence, the bode plots of  $G_{vo_d}(s)$  and  $G_{vo_{vi}}(s)$  present two resonances located at frequencies that can be easily calculated with (72) and (73).
- One pair of complex poles is due to the resonance between  $L_{m1}$  and  $L_{m2}$  with the input capacitance  $C_t$ .
- The other pair of complex poles is due to the resonance between the magnetizing inductance of the transformers and the output capacitor.
- The location of the poles is not affected by the output load.
- The location of the poles, on the other hand, is affected by the duty cycle  $D$ . Nevertheless, this influence is very slight in comparison to the influence of  $D$  in the location of the zeros, as can be seen in Fig. 3, Fig. 4 and Fig. 5. Poles 3-4 are nearly unaffected while poles 1-2 change their location, although they are always located at a frequency higher than poles 3-4. On the other hand, zeros 1 and 2 move from a frequency higher than poles 1-2 to a frequency located between the two pair of complex poles. Zero 3 moves from a frequency close to the complex pole 1-2 to a frequency even higher.

Regarding numerators, the one of equation (65) is a simple second-order equation that does not need simplification. Nevertheless, the numerator of equation (54)

is a third-order equation which can be simplified by means of a method similar to the one used for obtaining equations (66) and (67). At frequencies around zeros 2 and 3, the terms in  $s^3$  and  $s^1$  can be disregarded:

$$\begin{aligned} \text{Num}(s)|_{\text{zeros}_{2-3}} &= \\ &= s^2 \cdot C_t \cdot [L_{m1} \cdot (V_{c1} - V_o \cdot n_{d12}) - L_{m2} \cdot (V_{c2} + V_o \cdot n_{d12})] + \\ &+ (1-D) \cdot (V_{c1} - V_o \cdot n_{d12}) - D \cdot (V_{c2} + V_o \cdot n_{d12}) \end{aligned} \quad (76)$$

In the same way, the terms in  $s^1$  and  $s^0$  can be disregarded at frequencies around the zero located in the right half plane

$$\begin{aligned} \text{Num}(s)|_{\text{zero}_{1}} &= s^3 \cdot L_{m1} \cdot L_{m2} \cdot C_t \cdot (I_{m2} - I_{m1}) \cdot \frac{n_{d12}}{n_{dd}} + \\ &+ s^2 \cdot C_t \cdot [L_{m1} \cdot (V_{c1} - V_o \cdot n_{d12}) - L_{m2} \cdot (V_{c2} + V_o \cdot n_{d12})] \end{aligned} \quad (77)$$

Therefore:

$$s_{\text{Zeros}_{2-3}} = \pm j \sqrt{\frac{(1-D) \cdot (V_{c1} - V_o \cdot n_{d12}) - D \cdot (V_{c2} + V_o \cdot n_{d12})}{C_t \cdot [L_{m1} \cdot (V_{c1} - V_o \cdot n_{d12}) - L_{m2} \cdot (V_{c2} + V_o \cdot n_{d12})]}} \quad (78)$$

$$s_{\text{Zero}_{1}} = \frac{L_{m2} \cdot (V_{c2} + V_o \cdot n_{d12}) - L_{m1} \cdot (V_{c1} - V_o \cdot n_{d12})}{L_{m1} \cdot L_{m2} \cdot \frac{n_{d12}}{n_{dd}} \cdot \frac{n_1 \cdot n_2}{n_1 \cdot (1-D) + n_2 \cdot D}} \cdot I_o \quad (79)$$

It should be taken into account that these equations do not depend on  $K_s$ . As can be seen:

- $s_{\text{Zero}_{1}}$ , which is the one located in the right half-plane, does not depend on either the input capacitor ( $C_t$ ) or the filter capacitor ( $C_0$ ), as occurs in any Boost or Flyback converter.
- $s_{\text{Zeros}_{2-3}}$  does not depend on the output capacitor but only on the input capacitors (apart from the magnetizing inductances of the transformers).

In order to analyse the accuracy of the simplified equations, Table 1 shows the location of poles and zeros according to (54), (72) and (73). In the first four examples, the output capacitor  $C_0$  is lower or the input capacitors ( $C_1$  and  $C_2$ ) are higher than the values resulting from a standard design. These four examples can be then considered as the worst possible situation for the validity of the simplified equations as  $K_s$  is not significantly lower than one. It can be seen that the approximation provided by the simplified equations is still accurate (the error is always lower than 10%). In the fifth example, the value of  $C_0$  is higher in comparison to the second example and, as a consequence,  $K_s$  is considerably lower than one, obtaining a higher degree of accuracy in the calculation of the poles frequency.

It should be mentioned that the Bode plots shown in Fig. 5 are obtained by using equation (54) and, therefore, without considering the effect of the parasitic components, which tend to attenuate the effects of the resonances. Hence, using this equation, or the simplified ones, for designing the compensator adds a security factor from the stability point of view, but also implies a non-real situation which tends to drastically reduce the attainable bandwidth. Therefore, before suggesting a possible guideline for the design of the compensator, closer-to-real transfer functions will be provided in the next section as they take into account the main parasitic components that affect the TTAHBC: the parasitic resistors of the transformers and the  $R_{\text{DS(on)}}$  of the MOSFETs.

Table 1. Poles and zeros location for different designs with the complete equations and with the simplified ones.

Design	$K_s$	$f_{\text{Poles}}$ (Hz) equation (54)	$f_{\text{Poles}}$ (Hz) equations (72) (73)	Error $f_{\text{poles}}$ (%)	$f_{\text{Zeros}}$ (Hz) equation (54)	$f_{\text{Zeros}}$ (Hz) equations (78) (79)	Error $f_{\text{zeros}}$ (%)
$V_o=48\text{ V}$ , $P=60\text{ W}$ , $V_g=300\text{ V}$ $L_{m1}=280\text{ }\mu\text{H}$ , $L_{m2}=3800\text{ }\mu\text{H}$ , $C_o=6\times 4.7\text{ }\mu\text{F}$ , $n_1=1.085$ , $n_2=0.366$ , $C_1=C_2=270\text{ nF}$ , $D=0.5$	0.256	1564 1564 7349 7349	1714 1714 6706 6706	9.5 9.5 8.7 8.7	3730 4123 3939 45680	3939 3939 45390	5.6 4.4 0.6
$V_o=600\text{ V}$ , $P=60\text{ W}$ , $V_g=300\text{ V}$ $L_{m1}=280\text{ }\mu\text{H}$ , $L_{m2}=3800\text{ }\mu\text{H}$ , $C_o=0.20\text{ }\mu\text{F}$ , $n_1=13.51$ , $n_2=4.5$ , $C_1=C_2=270\text{ nF}$ , $D=0.5$	0.237	1515 1515 7301 7301	1649 1649 6706 6706	8.8 8.8 8.1 8.1	3830 4118 58480	3981 3981 58190	3.9 3.3 0.5
$V_o=48\text{ V}$ , $P=300\text{ W}$ , $V_g=300\text{ V}$ $L_{m1}=250\text{ }\mu\text{H}$ , $L_{m2}=1000\text{ }\mu\text{H}$ , $C_o=6\times 22\text{ }\mu\text{F}$ , $n_1=1.085$ , $n_2=0.366$ , $C_1=C_2=1500\text{ nF}$ , $D=0.5$	0.303	1346 1346 3456 3456	1432 1432 3249 3249	6.3 6.3 6.0 6.0	5750 5750 4167	5660 5660 4301	1.5 1.5 3.2
$V_o=600\text{ V}$ , $P=300\text{ W}$ , $V_g=300\text{ V}$ $L_{m1}=250\text{ }\mu\text{H}$ , $L_{m2}=1000\text{ }\mu\text{H}$ , $C_o=1\text{ }\mu\text{F}$ , $n_1=13.51$ , $n_2=4.5$ , $C_1=C_2=1500\text{ nF}$ , $D=0.5$	0.263	1265 1265 3425 3425	1334 1334 3249 3249	5.5 5.5 5.1 5.1	5784 5784 4230	5821 5821 4176	0.6 0.6 1.3
$V_o=600\text{ V}$ , $P=60\text{ W}$ , $V_g=300\text{ V}$ $L_{m1}=280\text{ }\mu\text{H}$ , $L_{m2}=3800\text{ }\mu\text{H}$ , $C_o=1\text{ }\mu\text{F}$ , $n_1=13.51$ , $n_2=4.5$ , $C_1=C_2=270\text{ nF}$ , $D=0.5$	0.047	725 725 6824 6824	737 737 6706 6706	1.6 1.6 1.7 1.7	3830 4118 58480	3981 3981 58190	3.9 3.3 0.5

#### IV. AVERAGE LARGE-SIGNAL AND SMALL-SIGNAL EQUIVALENT CIRCUITS.

Due to the principle of operation explained in section II, it is possible to define the two circuits (see Fig. 6) that define the TTAHBC during D·T and during (1-D)·T. With these two circuits, it is possible to obtain the average large-signal and small-signal equivalent circuits of the TTAHBC, which are shown in Fig. 7 and Fig. 8 respectively. As has been said, the main advantage of these circuits is that it is very easy to include parasitic components and analyse their effect on the dynamics of the system. The series resistors of the transformers and the  $R_{\text{DS(on)}}$  of the MOSFETs have been included ( $R_{m1}$  and  $R_{m2}$ ) as they are the more relevant parasitic components of the proposed design. Nevertheless, others could be added, such as the parasitic resistor and parasitic inductance of the capacitors.

The analysis of the circuit shown in Fig. 8 leads to the following transfer functions:

$$G_{\text{vo\_d}}(s) = \frac{1}{n_{\text{dd}}} \frac{N_{\text{p\_A}}(s) \cdot B_{\text{p\_A}}(s) - B_{\text{p\_B}}(s) \cdot N_{\text{p\_B}}(s)}{M_{\text{p\_A}}(s) \cdot B_{\text{p\_A}}(s) + B_{\text{p\_B}}(s) \cdot M_{\text{p\_B}}(s)}, \quad (80)$$

$$G_{\text{vo\_vg}}(s) = \frac{1}{n_{\text{dd}}} \frac{N_{\text{p\_C}} \cdot B_{\text{p\_A}}(s) - B_{\text{p\_C}}(s) \cdot N_{\text{p\_D}}(s)}{M_{\text{p\_C}}(s) \cdot B_{\text{p\_A}}(s) + B_{\text{p\_C}}(s) \cdot M_{\text{p\_D}}(s)}, \quad (81)$$

where,

$$N_{\text{p\_A}}(s) = V_{\text{p\_B}}(s) - Z_{m2}(s) \cdot I_{\text{p\_C}} \cdot (1-D), \quad (82)$$

$$B_{\text{p\_A}}(s) = 1 - D + s \cdot Z_{m1}(s) \cdot C_t, \quad (83)$$

$$B_{\text{p\_B}}(s) = D + s \cdot Z_{m2}(s) \cdot C_t, \quad (84)$$

$$N_{\text{p\_B}}(s) = V_{\text{p\_A}}(s) + D \cdot I_{\text{p\_C}} \cdot Z_{m1}(s), \quad (85)$$

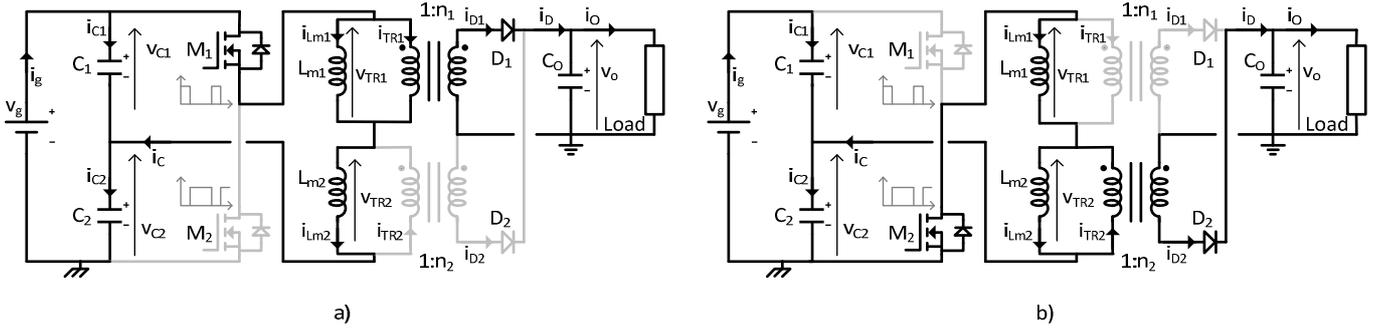


Fig. 6. Operational stages of the TTAHBC that lead to the small- and large signal models; a) during D and b) during 1-D.

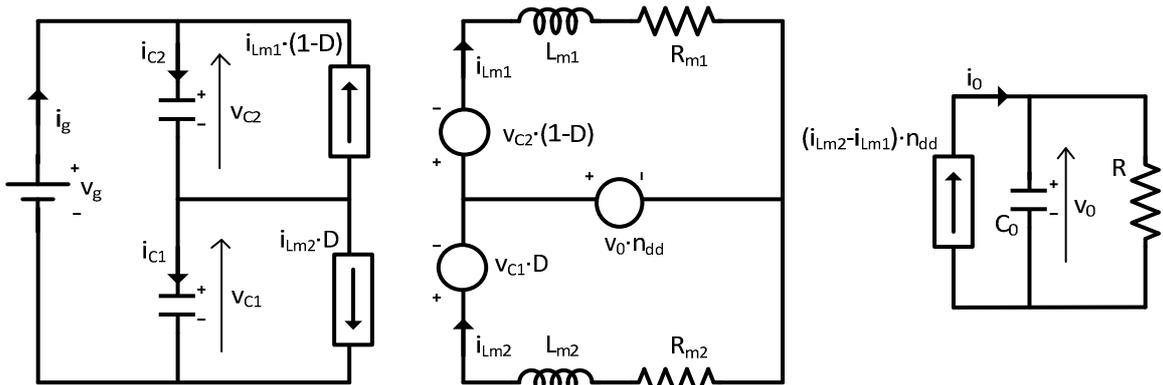


Fig. 7. Average large-signal model of the TTAHBC with the most-relevant parasitic components.

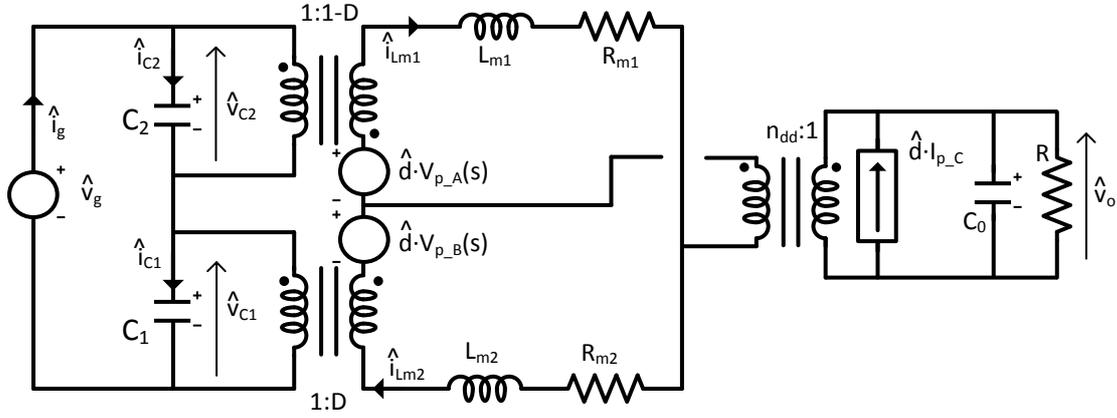


Fig. 8. Small-signal model of the ATHBTT with the most-relevant parasitic components.

$$M_{p\_A}(s) = \frac{Z_p(s) + Z_{m2}(s) \cdot (1-D)}{Z_p(s)} \quad (86)$$

$$M_{p\_B}(s) = \frac{Z_p(s) + Z_{m1}(s) \cdot D}{Z_p(s)} \quad (87)$$

$$N_{p\_C} = D \cdot (1-D) \quad (88)$$

$$B_{p\_C}(s) = Z_{m1} \cdot D - Z_{m2} \cdot (1-D) \quad (89)$$

$$N_{p\_D}(s) = s \cdot C_1 \cdot (1-D) \quad (90)$$

$$M_{p\_C}(s) = \frac{Z_p(s) + Z_{m2}(s) \cdot (1-D)}{Z_p(s)} \quad (91)$$

$$M_{p\_D}(s) = \frac{D \cdot (1-D) - s \cdot Z_p(s) \cdot C_1}{Z_p(s)} \quad (92)$$

$$Z_{m1}(s) = s \cdot L_{m1} + R_{m1} \quad (93)$$

$$Z_{m2}(s) = s \cdot L_{m2} + R_{m2} \quad (94)$$

$$Z(s) = \frac{R}{1 + s \cdot C_0 \cdot R} \quad (95)$$

$$V_{p\_A}(s) = V_g \cdot D + V_o \cdot n_{12} - \frac{I_{Lm1} \cdot Z_{m1}(s)}{1-D} \quad (96)$$

$$V_{p\_B}(s) = V_g \cdot (1-D) - V_o \cdot n_{12} + \frac{I_{Lm2} \cdot Z_{m2}(s)}{D} \quad (97)$$

$$I_{p\_C} = (I_{Lm2} - I_{Lm1}) \cdot n_{12} - \left( \frac{I_{Lm1}}{1-D} + \frac{I_{Lm2}}{D} \right) \cdot n_{dd} \quad (98)$$

$$R_{m\_1} = (R_{TR\_1} + R_{TR\_2} + R_{DSON\_2}) \cdot (1-D) \quad (99)$$

$$R_{m\_2} = (R_{TR\_1} + R_{TR\_2} + R_{DSON\_1}) \cdot D \quad (100)$$

where  $R_{TR\_1}$  and  $R_{TR\_2}$  are the series resistance of the transformers (referred to their primary side) and  $R_{DSON\_1}$  and  $R_{DSON\_2}$  are the parasitic resistance of the primary MOSFETs. It should be highlighted that due to the principle of operation of the TTAHBC,  $R_{DSON\_1}$  is included in the equation that defines  $R_{m\_2}$  and vice versa. Normally, dead times are very short and they can be disregarded in the small-signal analysis. If they have to be taken into consideration, they can be modeled as loss-free resistors that should be included in series with  $R_{m\_1}$  and  $R_{m\_2}$ . It should be said that the value of these resistors is not easy to calculate and is out of the scope of this paper. Besides, dead times are typically negligible in comparison to switching period.

The comparison of both transfer functions, with and without parasitic components, is shown in Fig. 9. As can be seen, the frequency location of poles and zeros is not affected but the peak value of the resonances is attenuated.

The validation of the proposed models and transfer functions is carried out by both, simulation and experimental results. The latter are shown in section VI. In this section, the simulation results obtained using PSim® software will be discussed. In these results, the transient response of the simulated real TTAHBC (i.e., switching model) is going to be compared with the one obtained with the average large-signal model. In both models, the parasitic components have been included. The TTAHBC that is going to be tested is designed for an input voltage of 400 V. The nominal output voltage is around 48 V. The turns ratios of both transformers

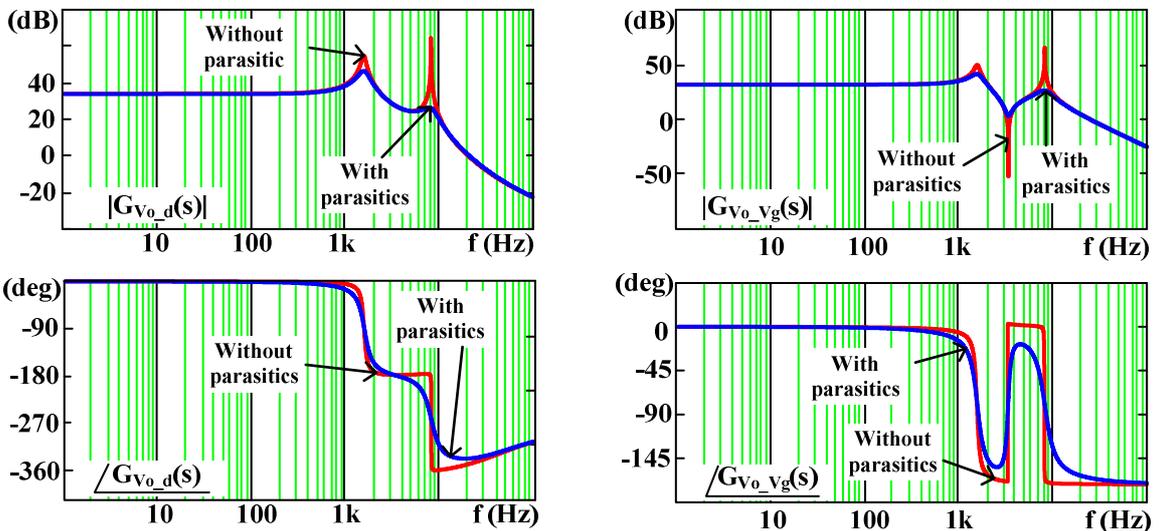


Fig. 9. Comparison between the two models, with and without parasitic components (same conditions as Fig. 3 and  $D=0.5$ ).

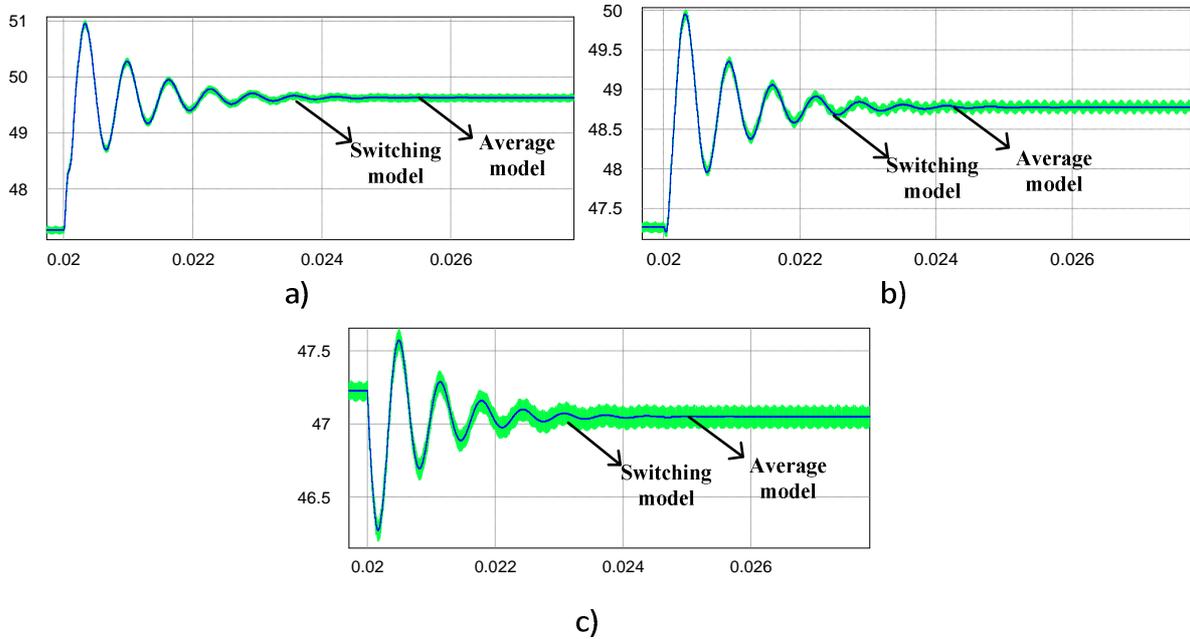


Fig. 10. Comparison of the transient responses of the simulated real model and the simulated average model for a) a 5% input voltage step; b) 5% duty cycle step; and c) 5% load step. The three simulations are carried out considering parasitic components.

are 1.085 and 0.366 and  $D_{\max}$  is equal to 0.633. The magnetizing inductances of the transformers are 280  $\mu\text{H}$  and 3800  $\mu\text{H}$ . The input capacitors have a capacitance of 270 nF and the output capacitor has a capacitance of  $6 \times 4.7 \mu\text{F}$ . The switching frequency is 100 kHz.

As can be seen in Fig. 10, the accuracy obtained for a duty cycle step, an input-voltage step and a load step (obviously, the three of them in open-loop) is high, even when the parasitic components are taken into account in both models.

## V. DESIGN OF THE CLOSED-LOOP CONTROLLER. USEFUL HINTS.

The main purpose of this paper is providing the TTAHBC small-signal analysis so it can be directly used in any project in which the TTAHBC is going to be used and its close-loop controller has to be designed. Providing a full design guideline of a specific or optimum closed-loop controller is out of the scope of this paper due to the large variety of controllers and its specific target performance depending on the final application. Nevertheless, it is possible to provide some general useful hints paying attention to the small-signal analysis of the TTAHBC, so it can be seen the influence of the parameters of the TTAHBC in stability.

The TTAHBC presents a bode plot with two resonances (as shown in Fig. 5 and Fig. 9). Therefore, a type-3 regulator (three poles, one of them in the origin, and two zeros) may be a suitable option if the maximum bandwidth has to be obtained [37] (however, this is not always possible and that is the reason for not proposing a specific design guideline). When designing any regulator, the following hints should be taken into account (see Fig. 11, where  $H(s)$  is the transfer function for the controller and the corresponding sensor of the output voltage):

- The two zeros of the regulator should be placed at frequencies around the first complex pole of the TTAHBC (see (62), (72) or (74)). In this way, the  $180^\circ$  phase lag of this double pole is compensated by the phase boost introduced by the two zeros. The key point is taking into account that this poles location is nearly not

affected by variations in the duty cycle, as has been mentioned before. Hence, the location of the zeros is straightforward.

- The two poles of the controller are normally placed at the lowest of the following frequencies:
  - The frequency of the second resonance of the TTAHBC.
  - The frequency of the zeros of the controller plus one decade.
  - In both cases, the main purpose is obtaining the maximum advantage of the phase boost introduced by the two zeros of the controller. In the first case, this is achieved by not introducing a phase lag until the second resonance is reached (which introduces a  $-180^\circ$  phase lag that limits the maximum attainable bandwidth). In the second case, by letting the phase boost introduced by the zeros of the controller reaching its maximum value (i.e.,  $+180^\circ$ ). It should be taken into account that, in many designs, the difference between the frequency of the first resonance (poles 3-4) and the frequency of the second one (poles 1-2) is always lower than one decade. Therefore, the two poles of the controller should be located close to the second resonance. Besides, the location of the zeros may imply a small modification of the location of the two poles of the controller in order to obtain optimum results.
- The zero located in the right-half plane should be taken into account as the bandwidth of the control loop should be always lower than the frequency at which this zero is located.
- The gain is adjusted in order to have the desired bandwidth under stability conditions. Here, the complex transfer function of the TTAHBC does not lead to any specific hint or recommendation.

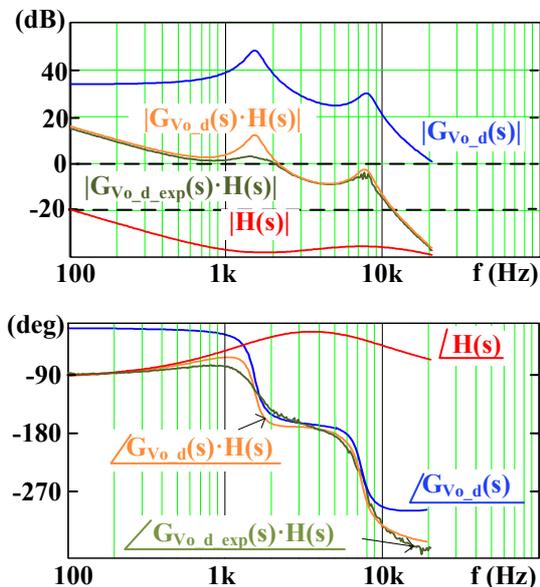


Fig. 11. Bode plot of  $G_{v_o,d}(s)$ , the compensator  $H(s)$  and  $G_{v_o,d}(s) \cdot H(s)$ .

To sum up, when designing the closed-loop controller, designers should take into account the following:

- Poles location in the TTAHBC bode plot is nearly not affected by the load.
- Both resonances are normally close to each other (lower than one decade).
- The influence of the zeros should be considered.
- The influence of the zero located in the right-half plane is especially important as it limits the maximum bandwidth attainable by the control loop.

Actually, the use of a type-1 compensator may be also necessary even when using the model including parasitic components. The reason can be found in Fig. 11. As can be seen, the phase margin is  $45^\circ$  approximately. This leads to a stable and valid design. Nevertheless, due to the second resonance (double pole) and the zeros, when the phase is equal to  $-180^\circ$ , the gain is lower than 0 dB (i.e., theoretically stable) but is close to this value. Depending on the requirements, this may imply a non-valid design for industrial purposes. Hence, a more conservative (i.e., with smaller bandwidth but larger gain margin) design may be necessary, making the type-1 compensator as useful as the type-3 one. Finally, Fig. 11 also includes the Bode plot  $G_{v_o,d,exp}(s) \cdot H(s)$ , which is the loop gain of the prototype presented in the next section when the proposed controller is used.

## VI. EXPERIMENTAL RESULTS

A prototype has been built and tested in order to analyse the accuracy of the proposed model (Fig. 12). The



Fig. 12. Photo of the 60-W prototype,

prototype is a 60-W TTAHBC with a nominal input voltage of 400 V and a nominal output voltage of 48 V. Table 2 shows the other characteristics of the prototype.

Table 2. Prototype summary.

Design parameters	Value
$V_{in}$	400 V
$V_O$	48 V
$V_O$ ripple	4%
$P_{out}$	60 W
Switching frequency	100 kHz
Transformer 1	Value
Core	ETD34
$n_1$	1.085
$R_{TR,1}$	0.3 $\Omega$
Leakage inductance	3 $\mu$ H
Magnetizing inductance ( $L_{m1}$ )	305 $\mu$ H
Transformer 2	Value
Core	ETD34
$n_2$	0.366
$R_{TR,2}$	1 $\Omega$
Leakage inductance	6 $\mu$ H
Magnetizing inductance ( $L_{m2}$ )	3460 $\mu$ H
Semiconductors	Value
MOSFETs	STP12N65
Diodes	MBRS3200T3G (Schottky)
Capacitors	Value
$C_1$	270 nF (MKP)
$C_2$	270 nF (MKP)
$C_O$	6×4.7 $\mu$ F (MKP) (in parallel)

The comparison between the experimental results and those predicted by the average large-signal model are shown in Fig. 13. As can be seen, the accuracy is high and, more important, the parasitic components included in the model proposed in section 0 have proven to be the most relevant ones in order to achieve a high degree of accuracy. It should be taken into account that in the duty cycle step and the load step, there is a small previous transitory caused by the contact bounce in the mechanical switches used to generate the steps. These contact bounces could even be modelled as an additional load or duty-cycle step. Besides, it should be highlighted that, in certain TTAHBC designs, if the dead times introduced in order to achieve ZVS are too long, it might be necessary to add an additional loss-free resistor in order to take into account and to model the effect of these dead times, as explained in [49]. In broad outline, its purpose is taking into consideration the output voltage reduction caused by these dead times, bearing in mind that they do not generate losses.

Finally, Fig. 14 shows the comparison of the Bode plot obtained from the prototype using a HP 3589A spectrum analyser with the Bode plot obtained using the equations presented in section III (small-signal model) and the equations presented in section 0 [small-signal model (with parasitic components)]. As can be seen, the resonant frequencies are perfectly fitted. Moreover, both sets of equations (equations of section III and equations of section 0) have been independently obtained and, as consequence, the fact that they fit helps to validate the proposed models. It should be noted that there is a small difference in the gain of the first resonance between the small-signal model and the experimental results. Nevertheless, this difference is completely cancelled when the parasitic resistance of MOSFETs and transformers are considered. Finally, the Bode plots of  $G_{v_o,v_i}(s)$  and  $G_{v_o,i_o}(s)$  are presented in Annex II.

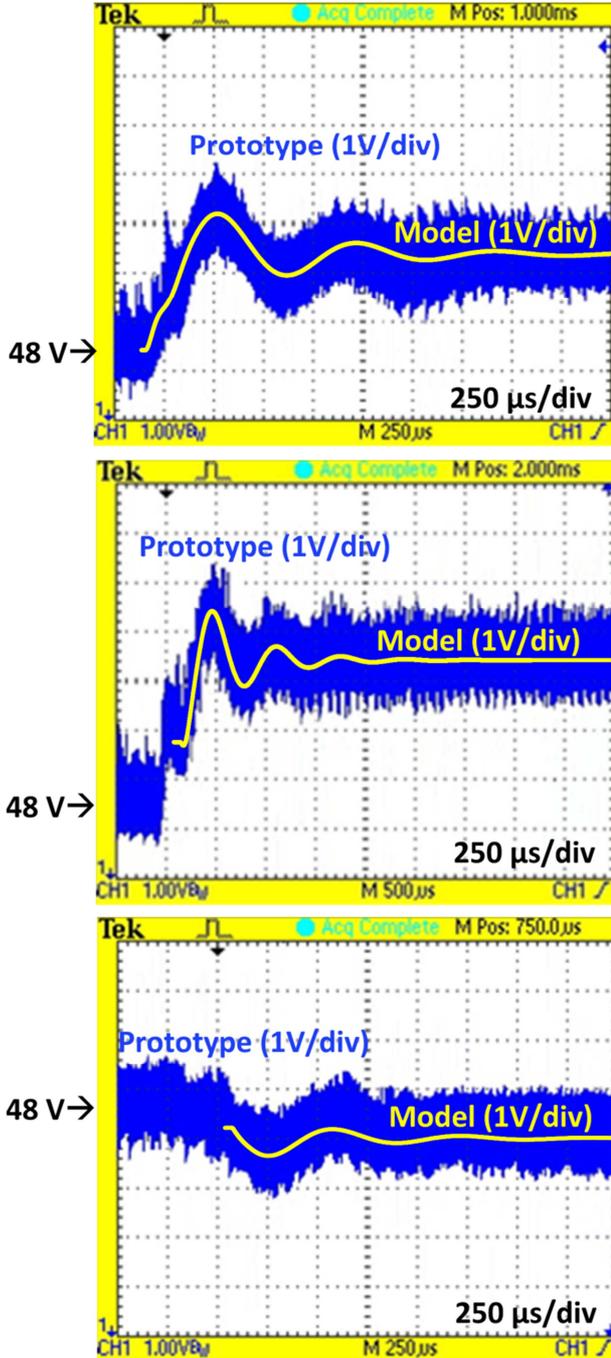


Fig. 13. Comparison between the experimental prototype and the proposed model for a) input-voltage step, b) duty cycle step and c) load step. In the three snapshots, the 48 V level is highlighted.

## VII. CONCLUSIONS

The TTAHBC allows the duty cycle range to be wider, this being the big difference in comparison to the standard AHBC. Nevertheless, it still has a complex transfer function that needs to be wisely analysed in order to develop successful designs. In fact, the transfer functions of the TTAHBC are more complex than the transfer functions of the standard AHBC due to the impossibility of easily separate the effect of the magnetizing inductance of each transformer (i.e., their operation is interrelated).

The small-signal analysis of the TTAHBC shows that it presents four poles (two resonances). The quartic equation that leads to these four poles can be simplified as explained in this paper in order to obtain two simpler equations. These equations show that one pair of poles is due to the resonance between the magnetizing inductances of the transformers and the input capacitors. The other pair of poles is due to the

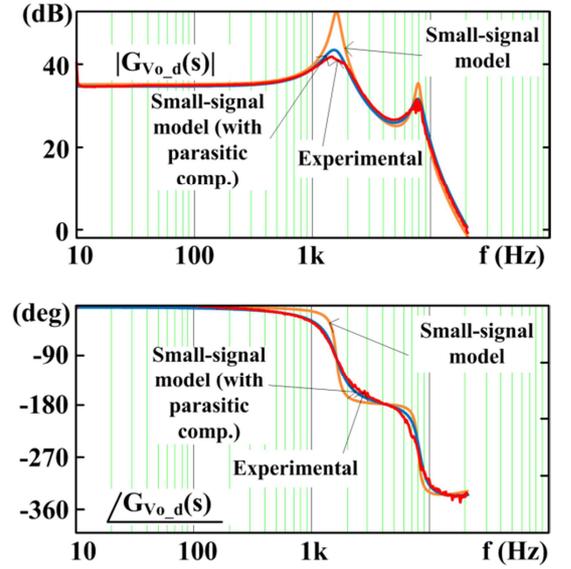


Fig. 14. Comparison of the Bodes obtained with the prototype and the small-signal model proposed in the paper.

resonance between the same inductances and the output capacitor. These equations also show that the influence of the duty cycle in the location of the poles is low and that the influence of the load can be neglected. Regarding the zeros, the TTAHBC presents three zeros, one of them located in the right half-plane and independent from the input and output capacitors, duty cycle and load. The other two zeros are independent from the output capacitor and the load, but they still depend on the input capacitor and the duty cycle. Obviously, all the zeros depend on the magnetizing inductances of the transformers.

The design of the closed-loop controller of the TTAHBC is as complex as in the standard AHBC. The use of complex controllers is mandatory in order to overcome the inherent problem of having two resonances (close to each other) and a zero in the right half-plane. Obviously, it is possible to use a simple controller if increasing the bandwidth is not a strong requirement. Besides, the model that includes parasitic components allows a more precise design to be obtained (i.e., higher bandwidth).

Finally, it should be mentioned that all the theoretical results has been validated by means of simulation and, also, by means of a 60-W prototype.

## ANNEX I

For understanding why  $K_s$  is usually, but not always, lower than 1, it has to be taken into account that the necessary capacitor for keeping the voltage ripple under a desired limit is as follows:

$$C = \frac{P}{2 \cdot 2 \cdot \pi \cdot f \cdot V^2 \cdot R_{pp}} \quad (101)$$

where  $P$  is the power,  $V$  is the voltage of the capacitor,  $R_{pp}$  is the desired ripple in the voltage and  $f$  is the frequency of the ripple.

Considering a 100% efficiency, the input power and the output power are equal. Therefore:

$$\frac{C_t}{C_o} = \frac{V_o^2 \cdot R_{pp_o}}{V_g^2 \cdot R_{pp_t}} \quad (102)$$

Admitting that the desired ripple in the input capacitors is equal to the ripple in the output capacitor (which is a very conservative approach, as will be explained later):

$$\frac{C_t}{C_o} = \frac{V_o^2}{V_g^2} \quad (103)$$

Besides, the static gain transfer function of the TTAHBC leads to the following equation (see (3)):

$$\frac{V_o}{V_g} = \frac{D \cdot (1-D)}{n_{dd}} \quad (104)$$

Also,  $K_s$  can be expressed as:

$$K_s = \frac{L_t \cdot C_t}{C_o \cdot L_D} = \frac{(L_{m1} + L_{m2}) \cdot C_t \cdot n_{dd}^2}{C_o \cdot (L_{m1} \cdot D^2 + L_{m2} \cdot (1-D)^2)} \quad (105)$$

Considering (103) and (104), (105) can be rewritten as:

$$K_s = \frac{(L_{m1} + L_{m2}) \cdot n_{dd}^2 \cdot D^2 \cdot (1-D)^2}{(L_{m1} \cdot D^2 + L_{m2} \cdot (1-D)^2) \cdot n_{dd}^2} = \frac{L_{m1} \cdot D^2 \cdot (1-D)^2 + L_{m2} \cdot D^2 \cdot (1-D)^2}{L_{m1} \cdot D^2 + L_{m2} \cdot (1-D)^2} \quad (106)$$

Paying attention to the different addends of (106), the following inequations can be obtained:

$$L_{m1} \cdot D^2 > L_{m1} \cdot D^2 \cdot (1-D)^2 \quad (107)$$

$$L_{m2} \cdot (1-D)^2 > L_{m2} \cdot D^2 \cdot (1-D)^2 \quad (108)$$

Adding inequations (107) and (108):

$$L_{m1} \cdot D^2 + L_{m2} \cdot (1-D)^2 > L_{m1} \cdot D^2 \cdot (1-D)^2 + L_{m2} \cdot D^2 \cdot (1-D)^2 \quad (109)$$

This inequation shows that the denominator of (106) is always higher than its numerator. Therefore, it can be concluded that:

$$K_s < 1 \quad (110)$$

Obviously, some particular designs may require higher values of  $C_t$  and lower values of  $C_o$ , leading to designs in which  $K_s$  is close to or is even higher than unity. In such a case, the equations without the simplification, or even the simplified ones for the case  $K_s > 1$  may be used. Nevertheless, it should be said that increasing the value of  $C_1$  and  $C_2$  above the necessary value has an important drawback. As can be seen from equations (1) and (2), any variation in the duty cycle implies that the input capacitors has to change their voltage in order to maintain the volt-second balance in the transformers. As a consequence, energy is transferred from one capacitor to the other through the MOSFETs and the magnetizing inductances. If their capacitance is too high, the amount of energy is also too high and the current driven by the MOSFETs may become excessive, breaking them down. Therefore, in standard designs, the relative ripple in the input capacitors is higher than in the output one, reducing the ratio  $C_t/C_o$  [see equation (102)]. This reduction leads to low values of  $K_s$ .

## ANNEX II

In section VI, the  $G_{V_o,d}(s)$  Bodes obtained with the prototype and the small-signal model were compared. Due to the input voltage range, the Spectrum Analyzer could not be used for obtaining the Bode of the audiosusceptibility ( $G_{V_o,vi}(s)$ ) as any failure may lead to damage in the measurement equipment. Therefore, the output voltage was reduced to 100 V and the output voltage to 12 V (while keeping the output current with a value of around 1 A) in order to obtain the abovementioned Bode plot while observing the laboratory rules regarding safety operation of

its equipment. In these new conditions, the magnetizing inductances were reduced to 150 and 900  $\mu$ H. The other parameters (switching frequency, capacitances, etc.) were not modified.

The comparison of the experimental results with the ones obtained with the small-signal model is presented in Fig. 15. As can be seen, the accuracy is very high. Moreover, this also implies that the proposed model has been tested in two different conditions.

Finally, the output impedance was also obtained from the experimental prototype and compared with the one obtained with the small-signal model (see Fig. 16).

## ACKNOWLEDGMENTS

This work has been supported by Spanish Government under projects RUE-10-CSD2009-00046 FEDER Funds and MICINN10-DPI2010-21110-C02-01.

## REFERENCES

- [1] P. Imbertson and N. Mohan, "Asymmetrical Duty Cycle Permits Zero Switching Loss in PWM Circuits with No Conduction Loss Penalty," *Industry Applications, IEEE Transaction on*, vol. 29, p. 121, January 1993.
- [2] J. A. Cobos, O. Garcia, J. Sebastian, J. Uceda, and F. Aldana, "Optimized Synchronous Rectification Stage for Low Output Voltage (3.3 V) DC/DC Conversion," presented at *the Power Electronics Specialists*

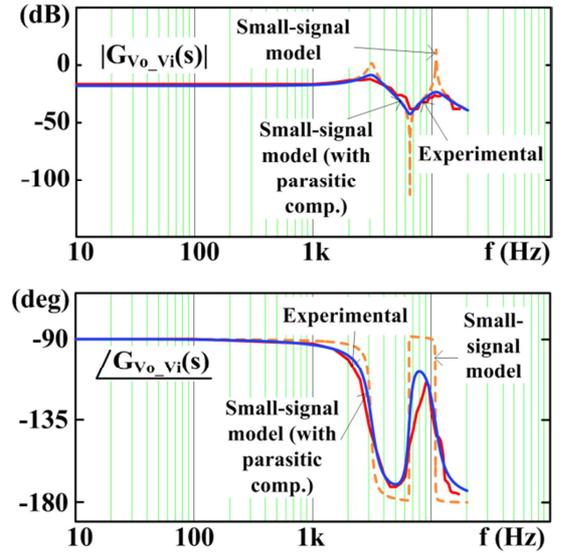


Fig. 15. Comparison of the Bodes ( $G_{V_o,vi}(s)$ ) obtained with the prototype and the small-signal model proposed in the paper.

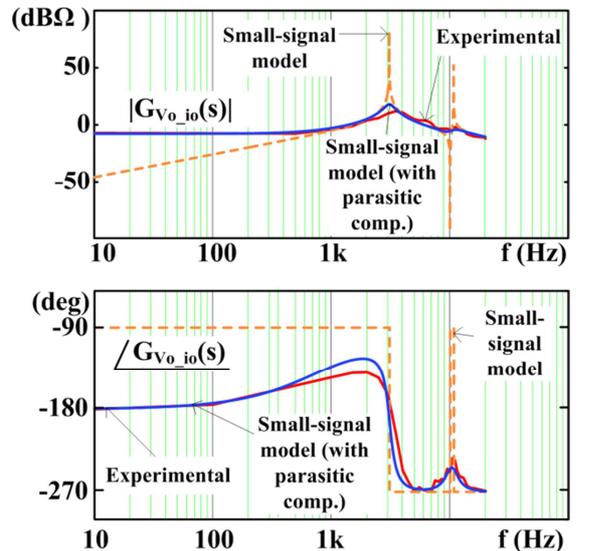


Fig. 16. Comparison of the Bodes ( $G_{V_o,io}(s)$ ) obtained with the prototype and the small-signal model proposed in the paper.

Conference, 1994. PESC '94 Record., 25th Annual IEEE, Taipei (Taiwan), 1994.

[3] M. Arias, D. G. Lamar, F. F. Linera, D. Balocco, A. A. Diallo, and J. Sebastian, "Design of a Soft-Switching Asymmetrical Half-Bridge Converter as Second Stage of an LED Driver for Street Lighting Application," *Power Electronics, IEEE Transactions on*, vol. 27, pp. 1608-1621, 2012.

[4] M. Arias, M. Fernandez, D. G. Lamar, D. Balocco, A. Aguisa Diallo, and J. Sebastian, "High-Efficiency Asymmetrical Half-Bridge Converter Without Electrolytic Capacitor for Low-Output-Voltage AC-DC LED Drivers," *Power Electronics, IEEE Transactions on*, vol. 28, pp. 2539-2550, 2013.

[5] K. Jae-Kuk, L. Sung Sae, O. Won-Sik, K. Jung-Eun, M. Gun-Woo, G. Chang-Hyun, and C. Ja-Ryong, "Start-up inrush current reduction technique of asymmetrical half-bridge DC/DC converter for PC power supply," in *Power Electronics, 2007. ICPE '07. 7th International Conference on*, 2007, pp. 243-245.

[6] B. Lin and C. Chao, "Soft Switching Converter with Two Series Half-Bridge Legs to Reduce Voltage Stress of Active Switches," *Industrial Electronics, IEEE Transactions on*, vol. PP, pp. 1-1, 2012.

[7] S. Korotkov, V. Meleshin, R. Miftakhutdinov, A. Nemchinov, and S. Fraidlin, "Integrated AC/DC converter with high power factor," in *Applied Power Electronics Conference and Exposition, 1998. APEC '98. Conference Proceedings 1998., Thirteenth Annual, 1998*, pp. 434-440 vol.1.

[8] H. Kim, J. Jung, and J. Baek, "Analysis and Design of a Multi-output Converter using Asymmetrical PWM Half-bridge Flyback Converter Employing a Parallel-series Transformer," *Industrial Electronics, IEEE Transactions on*, vol. PP, pp. 1-1, 2012.

[9] K. Yonghan, C. Byungcho, and L. Wonseok, "Analysis and design of a forward-flyback converter employing two transformers," in *Power Electronics Specialists Conference, 2001. PESC. 2001 IEEE 32nd Annual, 2001*, pp. 357-362 vol. 1.

[10] Y. H. Leu and C. L. Chen, "Improved asymmetrical half-bridge converter using a tapped output inductor filter," *Electric Power Applications, IEE Proceedings*, vol. 150, pp. 417-424, 2003.

[11] O. Garcia, J. A. Cobos, J. Uceda, and J. Sebastian, "Zero voltage switching in the PWM half bridge topology with complementary control and synchronous rectification," in *Power Electronics Specialists Conference, 1995. PESC '95 Record., 26th Annual IEEE, 1995*, pp. 286-291 vol.1.

[12] L. Bor-Ren, C. Huann-Keng, T. Chao-Hsien, and C. Kao-Cheng, "Analysis and Implementation of an asymmetrical half-bridge converter," in *Power Electronics and Drives Systems, 2005. PEDS 2005. International Conference on*, 2005, pp. 407-412.

[13] R. Oruganti, H. Phua Chee, J. T. K. Guan, and C. Liew Ah, "Soft-switched DC/DC converter with PWM control," *Power Electronics, IEEE Transactions on*, vol. 13, pp. 102-114, 1998.

[14] X. Xu, A. M. Khambadkone, T. M. Leong, and R. Oruganti, "A 1-MHz Zero-Voltage-Switching Asymmetrical Half-Bridge DC/DC Converter: Analysis and Design," *Power Electronics, IEEE Transactions on*, vol. 21, pp. 105-113, 2006.

[15] R. C. Beltrame, J. R. R. Zientarski, M. L. da Silva Martins, J. R. Pinheiro, and H. L. Hey, "Simplified Zero-Voltage-Transition Circuits Applied to Bidirectional Poles: Concept and Synthesis Methodology," *Power Electronics, IEEE Transactions on*, vol. 26, pp. 1765-1776, 2011.

[16] Mishima, T.; Nakaoka, M.; , "Practical Evaluations of a ZVS-PWM DC-DC Converter With Secondary-Side Phase-Shifting Active Rectifier," *Power Electronics, IEEE Transactions on*, vol.26, no.12, pp.3896-3907, Dec. 2011.

[17] C. D. Townsend, T. J. Summers, J. Vodden, A. J. Watson, R. E. Betz, and J. C. Clare, "Optimization of Switching Losses and Capacitor Voltage Ripple Using Model Predictive Control of a Cascaded H-Bridge Multilevel StatCom," *Power Electronics, IEEE Transactions on*, vol. 28, pp. 3077-3087, 2013.

[18] L. Il-Oun, C. Shin-Young, and M. Gun-Woo, "Interleaved Buck Converter Having Low Switching Losses and Improved Step-Down Conversion Ratio," *Power Electronics, IEEE Transactions on*, vol. 27, pp. 3664-3675, 2012.

[19] F. Jiangtao, H. Yuequan, C. Wei, and W. Chau-Chun, "ZVS analysis of asymmetrical half-bridge converter," in *Power Electronics Specialists Conference, 2001. PESC. 2001 IEEE 32nd Annual, 2001*, pp. 243-247 vol. 1

[20] M. Arias, D. G. Lamar, A. Vazquez, J. Sebastian, D. Balocco, and A. Diallo, "Analysis of the switching process in the Asymmetrical Half-Bridge converter for street led-lighting applications," in *Applied Power Electronics Conference and Exposition (APEC), 2012 Twenty-Seventh Annual IEEE, 2012*, pp. 1210-1217.

[21] T. Tolle and T. Duerbaum, "Modelling of ZVS transitions in asymmetrical half-bridge PWM converters," in *Power Electronics Specialists Conference, 2001. PESC. 2001 IEEE 32nd Annual, 2001*, pp. 308-313 vol. 1.

[22] M. Arias, A. Vázquez, and J. Sebastián, "An Overview of the AC-DC and DC-DC Converters for LED Lighting Applications," *Automatika – Journal for Control, Measurement, Electronics, Computing and Communication*, vol. 53, p. 17, 2012.

[23] Z. Fanghua, N. Jianjun, and Y. Yijie, "High Power Factor AC-DC LED Driver With Film Capacitors," *Power Electronics, IEEE Transactions on*, vol. 28, pp. 4831-4840, 2013.

[24] I. D. Jitaru, "Education Seminar S.1.: Trends in soft switching topologies," presented at the *Applied Power Electronics Conference, APEC, Orlando (FL), 2012*.

[25] Zhiliang Zhang; Meyer, E.; Yan-Fei Liu; Sen, P.C.; , "A Nonisolated ZVS Self-Driven Current Tripler Topology for Low-Voltage and High-Current Applications," *Power Electronics, IEEE Transactions on*, vol.26, no.2, pp.512-522, Feb. 2011

[26] G. Y. Jeong, "High efficiency asymmetrical half-bridge converter using a self-driven synchronous rectifier," *Power Electronics, IET*, vol. 1, pp. 62-71, 2008.

[27] F. Weiyi, F. C. Lee, P. Mattavelli, and H. Daocheng, "A Universal Adaptive Driving Scheme for Synchronous Rectification in LLC Resonant Converters," *Power Electronics, IEEE Transactions on*, vol. 27, pp. 3775-3781, 2012.

[28] L. Bor-Ren, Y. Cheng-Chang, and D. Wang, "Analysis, design and implementation of an asymmetrical half-bridge converter," in *Industrial Technology, 2005. ICIT 2005. IEEE International Conference on*, 2005, pp. 1209-1214.

[29] P. K. Jain, A. St-Martin, and G. Edwards, "Asymmetrical pulse-width-modulated resonant DC/DC converter topologies," *Power Electronics, IEEE Transactions on*, vol. 11, pp. 413-422, 1996.

[30] W. Eberle, H. Yongtao, L. Yan-Fei, and Y. Sheng, "An overall study of the asymmetrical half-bridge with unbalanced transformer turns under current mode control," in *Applied Power Electronics Conference and Exposition, 2004. APEC '04. Nineteenth Annual IEEE, 2004*, pp. 1083-1089 vol.2.

[31] L. Yi-Hsin, C. Tsou-Min, and C. Chern-Lin, "Analysis and design of the two-transformer asymmetrical half-bridge converter," in *Industrial Electronics Society, 2005. IECON 2005. 31st Annual Conference of IEEE, 2005*, p. 6 pp.

[32] B. R. Lin and T. Chao-Hsien, "Analysis of Parallel-Connected Asymmetrical Soft-Switching Converter," *Industrial Electronics, IEEE Transactions on*, vol. 54, pp. 1642-1653, 2007.

[33] S. Abedinpour, R. Liu, G. Fasullo, and K. Shenai, "Small-signal analysis of a new asymmetrical half-bridge DC-DC converter," in *Power Electronics Specialists Conference, 2000. PESC 00. 2000 IEEE 31st Annual, 2000*, pp. 843-847 vol.2.

[34] F. F. Linera, J. Sebastian, J. Diaz, and F. Nuno, "A novel feedforward loop implementation for the half-bridge complementary-control converter," in *Applied Power Electronics Conference and Exposition, 1998. APEC '98. Conference Proceedings 1998., Thirteenth Annual, 1998*, pp. 363-368 vol.1.

[35] J. Sebastian, J. A. Cobos, O. Garcia, and J. Uceda, "An overall study of the half-bridge complementary-control DC-to-DC converter," in *Power Electronics Specialists Conference, 1995. PESC '95 Record., 26th Annual IEEE, 1995*, pp. 1229-1235 vol.2.

[36] S. Korotkov, V. Meleshin, A. Nemchinov, and S. Fraidlin, "Small-signal modeling of soft-switched asymmetrical half-bridge DC/DC converter," in *Applied Power Electronics Conference and Exposition, 1995. APEC '95. Conference Proceedings 1995., Tenth Annual, 1995*, pp. 707-711 vol.2.

[37] B. Choi, W. Lim, B. Sanghyun, and C. Seungwon, "Small-signal analysis and control design of asymmetrical half-bridge DC-DC converters," *Industrial Electronics, IEEE Transactions on*, vol. 53, pp. 511-520, 2006.

[38] X. Xinyu, A. M. Khambadkone, and R. Oruganti, "An asymmetrical half bridge DC-DC converter: close loop design in frequency domain," in *Power Electronics Specialists Conference, 2004. PESC 04. 2004 IEEE 35th Annual, 2004*, pp. 1642-1647 Vol.2.

[39] C. Byungcho and L. Wonseok, "Current-mode control to enhance closed-loop performance of asymmetrical half-bridge DC-DC converters," *Electric Power Applications, IEE Proceedings*, vol. 152, pp. 416-422, 2005.

[40] E. Wilson, L. Yan-Fei, and P. C. Sen, "A Simple Large Signal Model for Isolated DC-DC Converters," in *Electrical and Computer*

*Engineering, 2006. CCECE '06. Canadian Conference on*, 2006, pp. 883-886.

[41] C. Byungcho, L. Wonseok, C. Seungwon, and S. Jian, "Comparative Performance Evaluation of Current-Mode Control Schemes Adapted to Asymmetrically Driven Bridge-Type Pulsewidth Modulated DC-to-DC Converters," *Industrial Electronics, IEEE Transactions on*, vol. 55, pp. 2033-2042, 2008.

[42] L. Yi-Hsin and C. Chern-Lin, "Analysis and design of two-transformer asymmetrical half-bridge converter," in *Power Electronics Specialists Conference, 2002. pesc 02. 2002 IEEE 33rd Annual*, 2002, pp. 943-948 vol.2.

[43] L. Krupskiy, V. Meleshin, and A. Nemchinov, "Unified model of the asymmetrical half-bridge converter for three important topological variations," in *Telecommunication Energy Conference, 1999. INTELEC '99. The 21st International*, 1999, p. 8 pp.

[44] R. Miftakhutdinov, A. Nemchinov, V. Meleshin, and S. Fraidlin, "Modified asymmetrical ZVS half-bridge DC-DC converter," in *Applied Power Electronics Conference and Exposition, 1999. APEC '99. Fourteenth Annual*, 1999, pp. 567-574 vol.1.

[45] L. Bor-Ren, H. Chien-Lan, and T. Chao-Hsien, "Analysis and Design of Half-Bridge Converter with Two Current Doubler Rectifiers," in *Industrial Electronics and Applications, 2006 1ST IEEE Conference on*, 2006, pp. 1-6.

[46] B. R. Lin, H. K. Chiang, J. J. Chen, J. J. Cheng, and C. Y. Cheng, "Implementation of an interleaved ZVS forward converter," in *Power Electronics and Drive Systems, 2009. PEDS 2009. International Conference on*, 2009, pp. 854-859.

[47] G. W. Wester and R. D. Middlebrook, "Low-Frequency Characterization of Switched DC-to-DC Converters," presented at the *IEEE Power Processing and Electronics Specialists Conference*, Atlantic City, NJ, 1972.

[48] R. D. Middlebrook and S. Cuk, "A general Unified Approach to Modelling Switching-Converter Power Stages," presented at the *Power Electronics Specialists Conference. PESC 1976*, Cleveland, OH, 1976.

[49] Polivka, W. M.; Chetty, P. R. K.; Middlebrook, R. D. "State-space average modelling of converters with parasitics and storage-time modulation", *PESC '80; Power Electronics Specialists Conference*, Atlanta, Ga., June 16-20, 1980.