Modular converters analysis and design for the standardization of the power bus in satellites

Abraham López[1], Manuel Arias[1], Pablo F. Miaja[1], José A. Villarejo[2], Theyllor H. Oliveira[1] and Arturo Fernández[3]
[1] Universidad de Oviedo, Electronic Power Supply Systems Group (e-mail: lopezabraham@uniovi.es)
Campus Universitario de Viesques, 33204 Gijón, Spain
[2] Universidad Politécnica de Cartagena, Cartagena, Spain
[3] Electrical Power Management Section European Space Agency (ESA), Noordwijk, Netherlands

***Abstract*: The power subsystem role in a satellite is to generate, store and distribute the electrical power to all the satellite subsystems. The energy is obtained from a solar array when solar energy is available and from a battery otherwise. Whilst the voltage levels in the electrical power bus are standardized to certain values, the voltage of the solar array is not. Therefore, all the converters in the power subsystem have to be redesigned for every new mission, increasing costs and development times. This work presents one possible approach to promote standardization at converter level in the power subsystem, minimizing, this way, the redesign for every new mission. The use of a modular DC transformer (DCX) or electronic transformer (ET) with straightforward interconnection capability (i.e. automatic voltage and power sharing) will be presented as a possible solution to keep the design of all the converters of the power subsystem unchanged between missions. The validation of this design has been carried out using a modular prototype for an input and output voltages of 56 V and 28 V respectively, for a rated power of 200 W (per module) and for a switching frequency of 400 kHz.**

***Keywords*: standardization, reliability, satellites, power subsystem, electronic transformer.**

I. INTRODUCTION

A schematic of the power subsystem of a spacecraft, using a regulated bus architecture, is represented in Fig. 1. The main building blocks (BBs) of the power subsystem are the Solar Array Regulator (SAR), the Battery Charge Regulator (BCR) and the Battery Discharge Regulator (BDR) [1]. The SAR is the one which extracts energy form the solar array (SA), while the BCR and the BDR work injecting energy to the batteries or extracting it from them, depending on the power balance between the solar array and the loads. These BBs are based on DC/DC converters with different power and voltage specifications. All of them are connected to the main power bus, making that only one of them takes the control of the power bus at a time, becoming the master. The distribution system (also shown in Fig. 1) conducts the bus voltage to the rest of the subsystems of the satellite and provides them with an overcurrent protection plus ON/OFF capabilities through the use of a latching current limiter (LCL) circuit [2]. Each of the subsystems will adapt the bus voltage to its necessities by means of their own DC/DC converters form the secondary power system. Since the specifications of each converter are different, the usual solution is to implement different topologies for each one. In the case of the SAR and the BCR, buck or superbuck converters are the typical choice, while the BDR uses a Weinberg [3] or a superboost [4] topology.

In the regulated bus architecture the voltage level of the main power bus will depend on the power requirements [1]. For power levels lower than 1.5 kW, the bus is designed to operate at 28 V. Between 1.5 and 8 kW, 50 V are selected. Power demands more than 8 kW are supplied through 100 V or 120 V buses. An important issue is the lack of a strong standardization in the power subsystem. While voltage levels at the power bus are partially fixed, the power range is quite large (for the 50 V buses the power range is about 6.5 kW). Nonetheless, this problem is strongly aggravated in the SAR. Solar arrays are designed and built ad-hoc [1], adjusting their geometry and electrical connections between solar cells to the geometry, size, and some other requirements of the satellite. As a result, the output voltage of the SA does not follow any standard. All of this makes the BBs (specially the SAR) prone to be design nearly from scratch for every new mission.

This lack strong standardization confronts with the current paradigm, where the use of satellites is increasing widely [5] and the time for project development is getting shorter. This forces the necessity of gradually introducing standardization and reusability as a key factor in the design and construction of satellites [6]. To avoid the redesign of the SAR for every new mission due to the solar array variability, one option is designing the SAR with a large input voltage range. The price to pay would be an inefficient and bulky design. Another option is based on the design of SAR modules that can be connected in series at the input, sharing this way the SA voltage. It would be then necessary a control stage capable of achieving a good power and input voltage sharing, while at the same time, controlling the SA point of operation. If this option is taken, it would lead to an optimized SAR design valid for every new mission (including the EMI filter). The main drawback could be the complexity in the control stage, with many alternatives based on a central control or a master-slave structure, having a great impact in reliability.

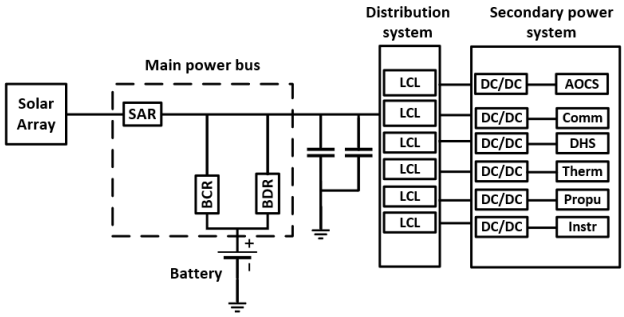

Fig. 1. Regulated power bus system on a satellite

The alternative explored in this paper for achieving a SAR standardization is based on using an intermediate stage between the SA and the SAR, as shown in Fig. 2. This allows to split the tasks and optimized each stage for just one task.

The proposed intermediate stage task is adapting the SA output voltage range (i.e. SA I-V curve) to be inside of the input voltage range of the fixed-design SAR, which is still responsible for performing the maximum power point tracking (MPPT) or controlling the bus voltage, depending on the operating conditions. This intermediate stage will be based on an electronic transformer (ET). To avoid the whole redesign of the ET in each mission due to the SA variability, it will be formed by fixed-design modules with a fixed static gain (based on DC transformers, DCX). Their series and/or parallel connections at their input will determine the ET voltage gain and power. Thanks to the selected DCX topology, these series/parallel connections can be achieved without using a central control, but just a simple common clock signal.

This paper is organized as follows. In Section II, a description of the ET concept based on the interconnection of DCXs is given. Section III will be based on the description of the selected topology to implement the DCX modules. Section IV presents the experimental results regarding the use of DCX modules and finally, conclusions are drawn in Section V.

II. DESCRIPTION OF THE CONCEPT

The interconnection of several smaller converters in series and/or parallel to achieve different transformation ratios and power scalability is not new [7]. In this work the voltage adaptation provided by the ET is achieved by serially connecting several standard modules at their inputs (see Fig. 3) while keeping all their outputs in parallel, as well as by wisely choosing a common static gain (G_v) value to all of them. These common static gain and common output voltage assure that the input voltage of all modules is equal, leading to a perfect sharing of the SA voltage among modules. As can be deduced from (1), the number of the DCX modules in series (m_s) allows to adapt the overall gain of the ET (G_{vTE}) and the final value of the output voltage:

$$V_o = V_{in} \cdot G_v = \frac{V_{SA}}{m\_s} \cdot G_v = V_{SA} \cdot G_{v\_TE} \quad (1)$$

where V_o and V_{in} are the average output and input voltage of each module and V_{SA} is the SA output voltage. The voltage level V_o is common to all the DCX modules and, consequently, is the output voltage of the ET, while V_{SA} is the input voltage level. Once the voltage range adaptation is achieved by selecting the appropriate m_s and G_v values, the resulting scheme can be repeated and parallelized m_p times to reach power scalability.

This method implies and additional stage in between the SA and the SAR. Hence, the topology chosen for the DCX modules needs to have high efficiency, and to provide fast SA emulation at their output. On the other hand, with this approach, the design of these modules, as well as the design of the SAR, is fixed, improving mission development times and converter reliability.

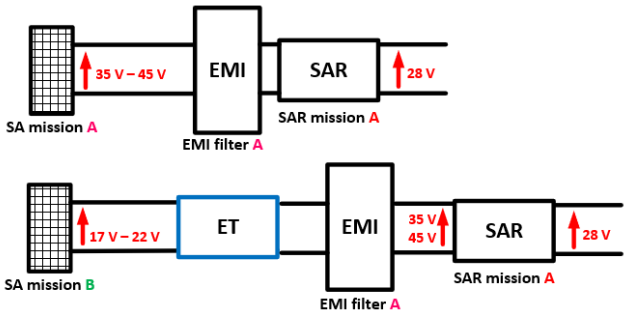

Fig. 2. Example of the reutilization of the SAR block for two different space missions

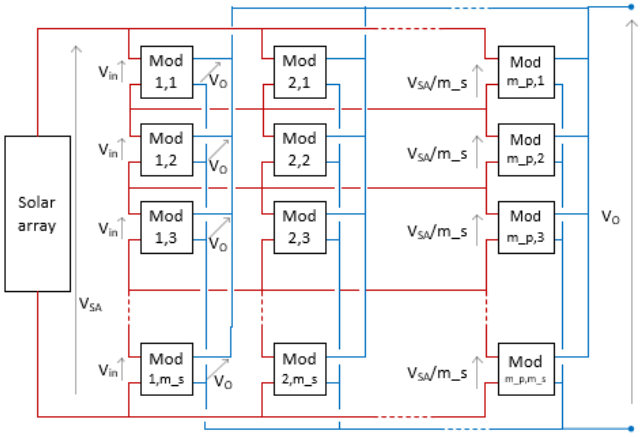

Fig. 3. Schematic of the proposed voltage adaptation through modular connection of standard fixed-gain modules

III. THE DCX MODULE IN THE ELECTRONIC TRANSFORMER

Considering the information in Section II, the four conditions for the DCX topology are: high efficiency, fast SA emulation, OFF line gain definition and stable static gain. The concept of DCX [8] suits the conditions imposed to the DCX modules. The proposed resonant topology is presented in Fig. 4.a), and the basic concept has already been introduced in [8]. For the sake of clarity, a summary of its operation will be introduced here along with the series/parallel connection and its working behaviour without a central control stage.

A. *Description of the DCX selected topology*

The topology consists in a resonant full bridge converter operating with fixed duty cycle and fixed switching frequency. In the secondary side, a center-tap rectifier (including Or-ing diode) is implemented. In each half switching period, the resonance takes place between the leakage inductance of the transformer (L_{lki}) and the output capacitor (C_O). If L_{lki}, Co and f_{sw} are conveniently selected, current will start and end at zero level at any load condition, leading to the waveforms shown in Fig. 4.b) and ensuring ZCS in secondary diodes. It is worth to mention that this figure includes periods in which the resonance has finished but the new half switching period has not started yet (T_{wait}). If magnetizing current is conveniently adjusted, ZVS is reached on primary MOSFETs even at no load situation. All of this leads to a very high efficiency.

This topology presents a fixed static voltage gain only dependent on the turn ratio ‘n’ of the magnetic transformer:

$$V_o = V_{in} \cdot n \quad (2)$$

This is the main advantage of the topology for this application in comparison to other options, such as DCXs based on the LLC resonant converter [9], whose static gain is dependent not only on the switching frequency, but also on the parameters of its resonant tank. This dependence forces the necessity of specific controls to ensure power and voltage sharing when tolerances are considered. On the other hand, the turns ratio of a transformer is a fixed value independent from tolerances or control signal variability. This makes the equalization of input voltages between series or parallel-connected modules straightforward.

Any control action induced by the SAR in the ET output voltage would be automatically and proportionally transferred to their input (i.e. to the SA). Therefore, from the SAR point of view, the output of the ET behaves as the SA, but with a different I-V curve.

Finally, the use of a reduced set of predesigned transformers provides a fast way to adapt the static gain of the converter in an easy way during assembly stage (i.e. off-line) without compromising standardization.

The resonant current and the output voltage can be expressed as:

$$V_o(t) = (V_{in} \cdot n) - I_o \cdot \sqrt{\frac{L_{LKi}}{C_O}} \cdot sin(\omega_i \cdot t) + [V_O(0) - V_{in} \cdot n] \cdot \cos(\omega_i \cdot t) \quad (3)$$

$$I_{LKi}(t) = I_o \cdot [1 - cos(\omega_i \cdot t)] + \frac{(V_{in} \cdot n) - V_O(0)}{\sqrt{\frac{L_{LKi}}{C_O}}} \cdot sin(\omega_i \cdot t) \quad (4)$$

$$\omega_i = \frac{1}{\sqrt{L_{LKi} \cdot C_O}} \quad (5)$$

where $v_o(t)$ is the output voltage, V_{in} the input voltage, 'n' the turn ratio of the magnetic transformer, I_o is the output current, L_{lki} is the leakage inductance of the winding i (as well as the resonant inductance), C_o is the output capacitance (which is also the resonant capacitance), $v_o(0)$ is the output voltage at the beginning of each resonance, $I_{lk\_i}(t)$ is the resonant current through leakage inductance 'i'. It should be considered that the time 't' restarts in zero for each resonant period (i.e. for each half switching period of the topology, $T_{sw}/2$). The magnetizing inductance does not play any role in the resonant tank. This aspect alleviates the design constraints of the transformer and makes easier the integration of the resonant inductance and the transformer in a single core. The magnetizing inductance is only tied to the condition of reaching ZVS under any load condition, so its value can be wisely adjusted.

The output capacitor is the resonant capacitor as well. This reduces the number of components, but it may also increase the output voltage ripple. In general, this is a drawback that makes this topology unsuitable for many applications.

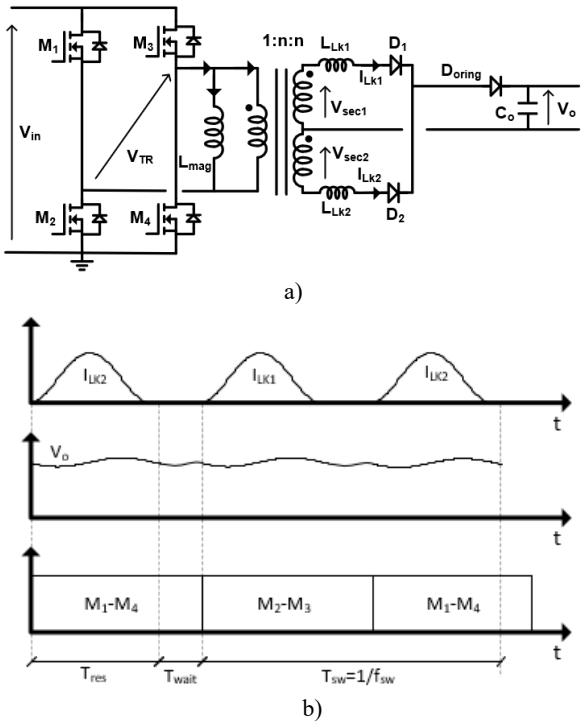

Fig. 4.a) Schematic of the DCX module; b) Main waveforms of the DCX module

Nonetheless, in this one, this drawback can be neglected as it is an intermediate stage. This high frequency ripple (at the switching frequency of the DCX module) can be easily filtered by the input filter of the SAR, which is designed to comply with EMI requirements and is mandatory. This EMI filter will be usually designed to considerably reject all the components at the SAR switching frequency. Assuming a ET switching frequency higher than the SAR switching frequency, the voltage ripple that the ET will introduce will be vastly attenuated. This implies that the high frequency voltage ripple introduced by the SAR will not propagate into the main bus. Moreover, as this input filter behaves as a high impedance at the ET resonant frequency, it decouples the ET output from the SAR input, so the resonant frequency of the ET remains unchanged. The control system of the SAR is designed to be compliant with this filter and thus any action taken by the SAR towards the SA can be considered as not delayed by the ET.

B. Modular operation

In this section, it will be explained how different DCX modules sharing only a clock signal (synchronization signal) can reach automatic input-voltage and power sharing without a centralized or master-slave control. It will be done using a straightforward circuital analysis.

For the sake of simplicity, this analysis assumes equal values of L_{lk} for both windings ($L_{lk} = L_{lk1} = L_{lk2}$), and of L_{lk} and C_o for all modules. The key point is that standardization of the SAR implies that a single value for its nominal input voltage is desired. Therefore, there is no need to connect the output ports of the DCX modules in series to adapt the overall output voltage. Their outputs can be designed for this unique SAR

input voltage and connected in parallel for power scalability. This common output voltage to all the modules leads to equal input voltages between all the modules, as can be derived from 0, whether they are connected in series or parallel. Consequently:

$$V_{SA} = \sum_{j=1}^{m\_s} V_{in_{i,j}} = \sum_{j=1}^{m\_s} \frac{V_o}{n} = \frac{V_o}{n} \cdot m\_s \quad (6)$$

$$V_{in_{i,j}} = \frac{V_{SA}}{m\_s} \quad (7)$$

where $Vin_{i,j.}$ is the input voltage of module i, j in Fig. 3.

Therefore, the ($m_s \cdot m_p$) DCX modules can be represented as in Fig. 5.a), where the square-pulse voltage sources represent the voltage at the secondary side of the transformers with a given time (T_{wait}) in which zero voltage is applied to the transformer. It is important to note that all of them, given 0, have the same amplitude. Assuming a clock signal synchronizing the local controllers of all modules, the phase of all the square-pulse voltage sources is the same. Consequently, the voltage at the switching nodes ($SN_{i,j}$) is equal for every module in every instant, so they are electrically equivalent, and the system can be represented as in Fig. 5. b), where all the resonant tanks are connected in parallel. Thus, the output voltage of this equivalent circuit is:

$$V_o(t) = (V_{in} \cdot n) - I_o' \cdot \sqrt{\frac{L_{LKi}}{C_O \cdot (m_s \cdot m_p)^2}} \cdot sin(\omega' \cdot t) + [V_O(0) - V_{in} \cdot n] \cdot \cos(\omega' \cdot t) \quad (8)$$

being,

$$\omega' = \sqrt{\frac{1}{L_{LK} \cdot C_O}} = \omega \quad (9) \qquad I_o' = I_o \cdot (m_s \cdot m_p) \quad (10)$$

The pulsation is equal for every single resonant tank and for the equivalent one (see (5) and (9)). Replacing (9) and (10) in (8):

$$I_{LKi}(t) = \frac{1}{L_{LK}} \cdot \int_0^{\frac{2\cdot\pi}{\omega}} [V_{in} \cdot n - V_o(t)] \cdot dt = I_o \cdot [1 - cos(\omega_i \cdot t)] + \frac{(V_{in} \cdot n) - V_O(0)}{\sqrt{\frac{L_{LKi}}{C_O}}} \cdot sin(\omega_i \cdot t) \quad (11)$$

As can be seen from (4) and (11), all the resonant currents are equal and are not affected by the number of modules or by the array configuration (bear in mind the assumption of no tolerances in the resonant inductors). This means that, given the common output voltage, accurate power sharing between all the modules can be achieved without any kind of dedicated or complex sharing control, just with a clock signal that synchronizes all the primary full bridges. Considering the intended application, where very short distances can be expected between modules (or even connection by means of a backplane), delays or any other problem related to the transmission of this clock signal are minor, can be easily overcome, and do not affect the performance of the proposed system.

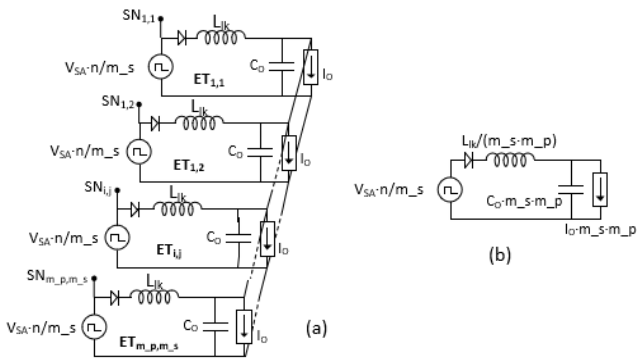

Fig. 5. a) Equivalent circuit for the ET-based array with several DCX modules; b) Simplified equivalent circuit derived from a)

Thanks to the control of the modular operation, it is possible to overcome the effect of drifts dur to tolerances and aging in the resonant components (C_{eq} and L_{eq}). As soon as tolerances appear, the ZCS conditions in the diodes can be lost. With this topology it is possible to establish the value of the final L_{eq} and C_{eq} values, considering tolerances. Therefore, it is possible to calculate the maximum and the minimum values for the resonant frequency, and finally, achieve an expression for the maximum resonant time (T_{res_max}), which ensures that the resonant process is not restarted for any drift due to aging or tolerance in the resonant components. This way, the ZCS condition in not lost in the diodes, making that the efficiency in the DCX topology is not going to be affected. This analysis is not straightforward in the traditional DCX topologies.

IV. EXPERIMENTAL RESULTS

This section is structured in three parts. On the first part experimental results for a single DCX module are shown. On the second part, DCX modules are connected in Input-Parallel Output-Parallel (IPOP) or Input-Series Output-Parallel (ISOP) configurations. Finally, a connection between a solar array simulator and an ET has been performed in order to proof that a SAR would see the SA curves scaled by the ET.

A. Experimental results for a single DCX module

Four prototypes of DCX modules (two different layouts) have been designed and built according to the schematic in Fig. 4. Its mains characteristics are listed in Table I. The semiconductors listed are the equivalents of the space-qualified one, with the same characteristics. A photograph of one of the prototypes is shown in Fig. 6, where MOSFETs are highlighted in green and diodes in red. Fig. 7 shows the drain-source voltage in M_4 primary transistor (V_{DSM4}), the resonant currents through the rectifier diodes (I_{LK}), and the output voltage (V_O) considering the EMI input filter of the SAR. This way, it is possible to reduce the voltage ripple, without affecting the resonant current behavior. Fig. 8 shows a detail of the transition in the M_4 MOSFET. As can be seen, ZVS can be reached in primary switches and ZCS in secondary ones. Therefore, the efficiency of each module is very high, as shown in Fig. 9, reaching 97 % at the rated power and around 96 % at half the rated power.

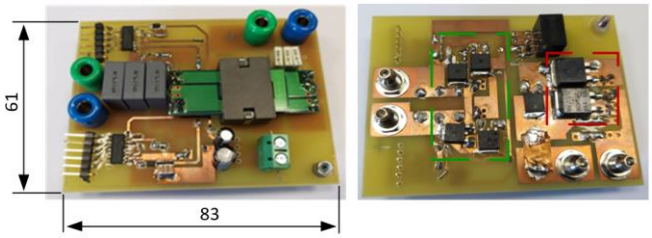

Fig. 6. Prototype of one DCX module

Table I. Main specifications of the ET designed

Input voltage (V_{in})	56 V
Output voltage (V_O)	28 V
Rated power (P_O)	200 W
Switching frequency (f_{SW})	400 kHz
Clock Source	Altera 10M50DAF484C7G
Leakage inductance (L_{LK})	65 nH
Output capacitor (C_O)	0.3 µF
MOS (M_1, M_2, M_3 and M_4)	PSMN063-150D
Rectifier diodes (D_1, D_2)	NRVBB60H100CTT4G
Magnetic core	EIR22/6/16
Magnetic material	N97
Drivers	IR2110 / SI8238BB
Turns	4:2

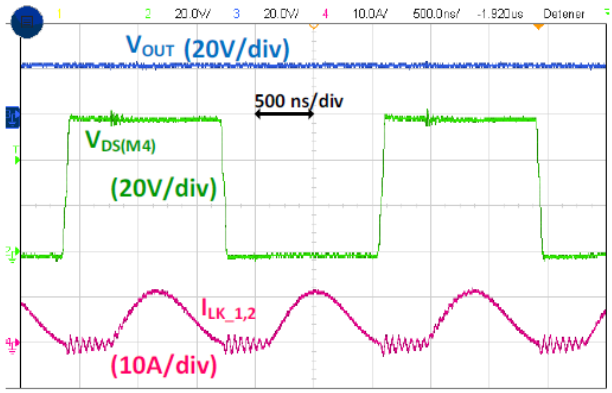

Fig. 7. V_{DS} (M_4), V_O and $I_{LK\_1,2}$ through the diodes, using the EMI SAR input filter

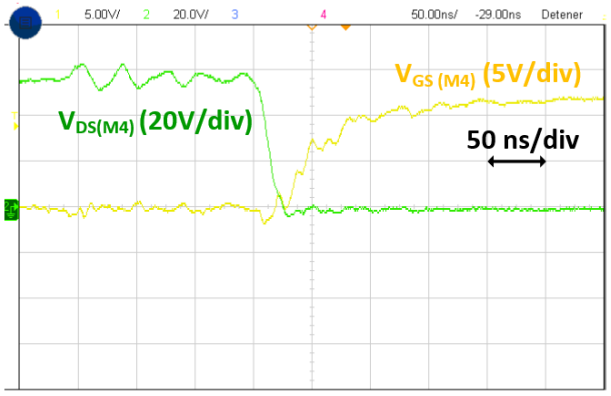

Fig. 8. ZVS achievement on primary switches

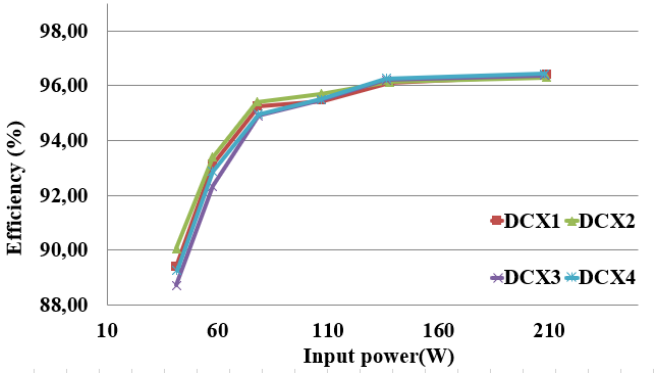

Fig. 9. Efficiency comparison between DCX modules

B. Experimental results using several DCX modules

By combining several DCX modules it is possible to increase the voltage and power levels manage form the whole system. For example, with four modules using IPOP and ISOP configurations it is possible to build a system whose nominal input voltage is twice (i.e. 112 V) the rated voltage of one module (i.e. 56 V) while the output voltage is still equal to 28 V. At the same time, the rated power of the whole system (i.e. 800 W) is four times the rated power of a single DCX module (i.e. 200 W). Fig. 10 shows the combination of four modules using IPOP and ISOP configurations. Sub 1 and Sub 2 blocks represent the IPOP combination of a pair of modules, while both blocks are serialized at their input. Fig. 11 shows the input voltages in both subsystems (close to 56 V) and the output voltage (V_O) of the whole system (28 V). As can be seen, the input voltage is perfectly shared among the modules connected in series with the simple control proposed. Fig. 12 represents the resonant currents through the rectifying diodes in the four modules (I_{DCX1}-I_{DCX4}).

The matrix structure in Fig. 3 allows reliability. This way, thanks to the input parallel connection between DCXs in the same row, and to the series connection between inputs in the same column, when a DCX module fails, it is possible to force the input and output ports to behave as an open circuit, making that the module will be disconnected while the whole ET structure is maintained. The matrix structure allows the current and voltage distribution (i.e. power distribution) between the DCX alive modules, without affecting the normal working behavior of the ET.

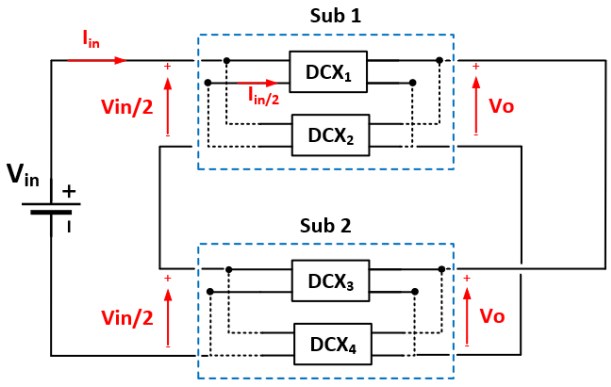

Fig. 10. Schematic of two subsystems of DCX modules in IPOP configuration, connected in ISOP

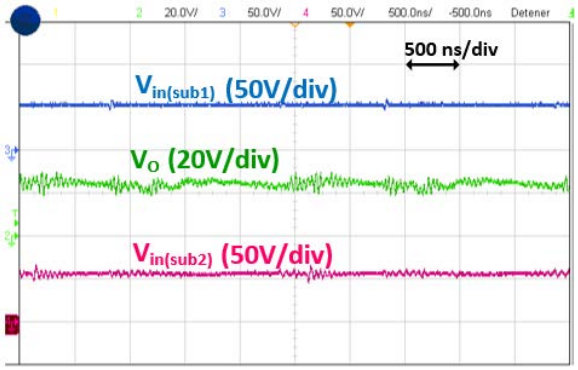

Fig. 11. Input voltages for sub1 and sub2 with the whole system output voltage (V_O)

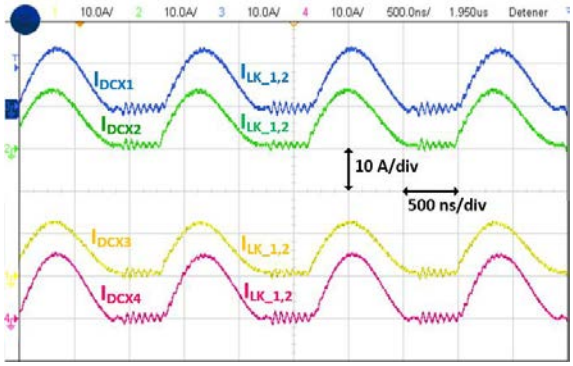

Fig. 12. Currents through the rectifier diodes in the four DCX modules. The shared power per module is nearly 200 W

C. *Solar array simulation using the ET*

This section shows the behavior of the ET system when it is connected to a solar array emulator. In this case a E4360 from *Keysight* [10] has been used, in order to emulate the solar array behaviour, analysing how its I-V curve is adapted, due to the presence of the ET system, to certain values which fixed with the ones stablished by the SAR. In this case, a solar array with an open circuit voltage (V_{OC}) of 56 V, a short circuit current (I_{SC}) of 2 A, a maxim power point voltage (V_{MP}) of 53 V, and a maximum power current (I_{MP}) of 1.7 A has been simulated. Fig. 13 shows its I-V curve along with the I-V curve of the ET output. As can be seen, the output of the ET behaves as a SA scaled to the emulated SA by a factor of 2 (defined by the DCX modules).

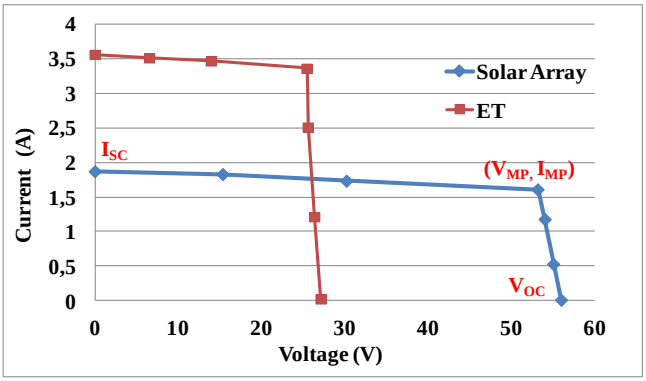

Fig. 13. I-V curves for the solar array and the ET system

V. CONCLUSIONS

This work presents a converter that behaves as a I-V curve adapter for satellite solar panels, allowing to keep the design of the SAR and its control unaltered through different missions. The purpose is adapting the design and construction of satellites to the present trend in aerospace field, in which shorter time to launch are required. The proposed converter, defined as Electronic Transformer (ET), is based on the matrix connection of fixed-design DCX modules based on an isolated resonant topology. Adaptation of the solar panel voltage is achieved by series connection of modules at the input while power scalability is achieved by parallel connection.

Given that the output voltage must be adapted to a fixed voltage (defined by the standardized, fixed-design SAR), all the modules are connected in parallel at the output, leading to a combination of ISOP and IPOP connections. The topology of the module is based on an isolated resonant topology whose static gain is fixed and only dependent on the turn ratio of its transformer. This allows the modules to perfectly share the power and the input voltage, even when in ISOP configuration, without a specific or complex control apart from a simple common clock signal (synchronization signal). The overall efficiency is very high, being especially high at full load (around 97 %). This is relevant as heat evacuation is a main concern in satellite designs and the proposed converter does not compromise the thermal subsystem of the satellite.

ACKNOWLEDGEMENTS

This work has been carried out by funding from the Spanish government through the PID2021-127707OB-C21 project, and the PRE2019-088425 grant. In the same way, this work has been supported by the Principality of Asturias and FICYT under the SV-PA-21-AYUD/2021/51931 project.

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