Design of a high performance VLC-LED driver for Visible Light Communication based on the split of the power

Daniel G. Aller, Diego G. Lamar, Manuel Arias, Pablo F. Miaja and Javier Sebastián.
Electrical, Electronic, Computers and Systems Engineering Department,
University of Oviedo, Gijón 33204, Spain.

***Abstract*—This work proposes a VLC-LED driver for Visible Light Communication (VLC) based on two converters, a high frequency buck dc-dc converter and a low frequency boost dc-dc converter, connected in series regarding the LED load. A VLC system needs to fulfill two different tasks: biasing the LED and generating the communication signal. This two task have typically different power requirement, the bias power is 3/4, while the communication power is 1/4 of the total power. And the requirements of both are different: the communication signal requires a high frequency and a fast output response, while the biasing control requires a converter with slow output response. The proposed topology takes advantages of the differences between the two tasks and reaches high efficiency and high communication performance by means of splitting the power between the two converters. A high frequency buck dc-dc converter generates the communication signal, while the low frequency boost dc-dc converter is in charge of biasing the LEDs. This technique allows to process most of the DC biasing power by the low frequency converter (reaching high efficiency) and keeping the high frequency converter delivering the communication power (reaching high communication performance). As experimental results, the proposed VLC-LED driver is build and validated by reproducing a 64-QAM with a bit rate up to 1.5 Mbps, reaching a 91.5% of overall efficiency.**

I. Introduction

The present wireless technologies are mostly based on the Radio Frequency (RF) spectrum, with omnipresent technologies such as WiFi, Bluetooth, 5G, etc. The current growth of new wirelessly connected devices is leading to a more strictly regulation and a high congestion of the RF spectrum [1]. In order to mitigate the congestion or to find alternatives to the RF spectrum, researchers and industry have been heading towards finding new technologies or solutions as substitutes or supplements to the RF spectrum.

One of the most promising solutions is Visible Light Communication (VLC) [2]. By taking advantage of the widespread of LED based Solid-State Lighting (SSL), VLC uses the inherent LED capability of fast changes of its emitted light, which makes the LED a suitable to work as a wireless transmitter. VLC is proposed as an alternative for RF spectrum where the light is already present or where RF is not a viable option due to strict regulations (such as hospitals, airplanes, etc.) [3]–[5].

Figure 1 depicts the behaviour of an LED and its control in a VLC system. Two tasks are needed in a VLC system: the bias task and the communication task.

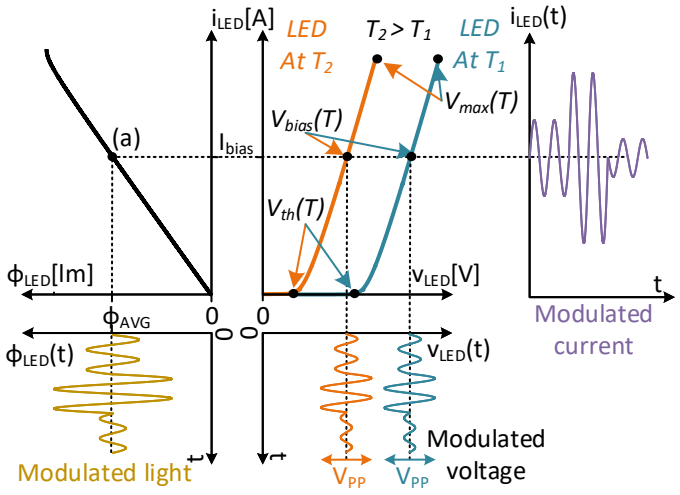

Fig. 1. Temperature shift on the LED curves.

This work was supported in part by European Regional Development Fund grants, in part by the Spanish Government under projects MINECO-17-DPI2016-75760-R, MINECO-20-PID2019-110483RB-I00 and MCIU-19-RTI2018-099682-A-I00, and in part by the Principality of Asturias under project IDI/2018/000179 and scholarship BP17-91.

Email: garciaadaniel@uniovi.es

The bias task generates a constant voltage across the LEDs, controlling the average current through the LEDs, and then the light emitted by the LEDs. As depicted in Fig. 1, for a specific emitted light flux ϕ_{avg} and average current I_{bias}, the voltage $V_{bias}(T)$ depends on the temperature T of the LED due to the temperature shift. Being $T_2 > T_1$, when the LED goes from a lower temperature T_1 to a higher temperature T_2, the necessary $V_{bias}(T)$ decreases for the same current I_{bias}. This undesired effect leads to the need of a control system over the LEDs. Without a proper control to counteract this effect, the communication performance is affected [6]. In order to counteract the temperature shift, the driver has to control the average current in order to always be working on the middle of the linear region of the LED, which also maximizes the range for the communication signal V_{pp}. The working range V_{pp} is defined as the linear part of the voltage-current relation, between the threshold voltage $V_{th}(T)$ and the maximum voltage $V_{max}(T)$. The communication task is in charge of generating the communication signal within the working range V_{pp}. As it is depicted in Fig. 1, the slope of the curve and the maximum LED current are kept unmodified regardless the temperature, meaning that the working range is also unchanged. Providing that the communication signal is lower than V_{pp} and the bias task works properly delivering I_{bias}, the distortion on the emitted light is minimized [6].

The most common VLC-LED transmitter topology is based on using a regular LED driver for the bias task connected with an amplifier (i.e. class A or B) for the communication task [7]–[9] using a bias-T circuit. Even though they achieve high bit rates, the main drawback of this proposal is the power efficiency. For example, the maximum efficiency of a class A and B amplifiers is 50% and 78% respectively (when a constant amplitude signal is delivered), but when a more complex amplitude modulated signal is used, the efficiency drops significantly [10].

Other way to implement a VLC transmitter is to modify the traditional LED driving stage by integrating the communication task, becoming VLC-LED driver. High frequency and fast response DC-DC converters have been proposed as a very promising alternative to linear amplifiers, reaching higher efficiencies (around 90%) and providing high bit rate communication [11]–[13]. The main drawback of this proposal comes from the fact that the converter is processing both bias and communication power at high frequency, increasing the total power losses. In a VLC system roughly 3/4 of the power comes from bias and 1/4 from communication. The bias task controls the current to adapt it according to the slow temperature effects over the LED, this means that there is no need for the converter to have a fast response and therefore not to have a high switching frequency. Thus, one way to further improve the efficiency is by splitting the power in the converters of which they are part of the VLC-LED driver [14], [15]. The idea consists in making two specialized converters working together: a low frequency converter and a high frequency and fast response converter. The low frequency is in charge of delivering the bias power (most of the power of the system) and then maintaining the illumination at the desired level.On the other hand, the high frequency and fast response converter is in charge of delivering a limited part of the power (mostly only the communication power). In [14] two buck dc-dc converters are used with their outputs connected in series regarding the LED load: one low frequency converter for the bias task and a high frequency converter for the communication signal. Although the solution achieves high efficiency and communication capability, the main drawbacks of this solution are the need of two different input voltages, one for each converter, and one higher than the threshold voltage of the LED load. In [15] the drawback of the need of two different input voltages is solved by using two buck dc-dc converters in a TIBuck configuration, although the need of an input voltage higher than the maximum voltage over the LED (due to the use of only buck dc-dc converters) could not be suitable for battery powered VLC applications.

In this paper, a VLC-LED driver for VLC based on a low frequency boost dc-dc converter and a high frequency buck dc-dc converter is presented. Both converters share the same input voltage and are connected in series regarding the LED load. The proposed topology reaches high efficiency and high communication performance by means of splitting the power between the two converters, where the low frequency boost dc-dc converter is in charge of controlling the bias of the LEDs, while the high frequency buck dc-dc converter generates the communication signal. This technique allows to process most of the bias power by the low frequency converter (reaching high efficiency) and keeping the high frequency converter delivering the communication power (reaching high communication performance). This configuration follows the same principle as other split of the power proposals for VLC but without the need of two input voltages [14] nor a single input voltage mandatorily higher than the maximum LED voltage [15].

As experimental results, a VLC-LED driver is built and the proposal is validated by reproducing a 64-QAM with a bit rate up to 1.5 Mbps, reaching a 91.5% of overall efficiency.

II. Use of the series buck-boost LED-driver for VLC

The block diagram of the proposed topology is shown in Fig. 2 and an example for the waveforms are shown in Fig. 3. Both converters are connected to the same input voltage V_{in} and their outputs are connected in series regarding the LED string load. The string load is comprised of n LEDs. The boost dc-dc converter is in charge of generating a DC voltages v_{boost}, while the buck dc-dc converter generates the communication signal v_{buck}, as shown in the block diagram in the Fig. 2.

A. Operating principle

In order to make the n LEDs string work within the linear region, the LED voltage v_{LED} has to be between the threshold voltage $nV_{th}(T)$ and the maximum voltage $nV_{max}(T)$, where $V_{th}(T)$ and $V_{max}(T)$ are the threshold and maximum voltage of a single LED, and $nV_{bias}(T)$ is the voltage in the middle of the linear region of the LED string. For the sake of simplicity, the LED working range is defined according to the middle point of the linear region $nV_{bias}(T)$. The peak to peak maximum amplitude allowed for the communication signal nv_{pp} is as follows:

$$\begin{aligned} nV_{max}(T) &= nV_{bias}(T) + nv_{pp}/2 \\ nV_{th}(T) &= nV_{bias}(T) - nv_{pp}/2. \end{aligned} \tag{1}$$

An effect worth to mention is that while $V_{th}(T)$, $V_{bias}(T)$ and $V_{max}(T)$ change according to the temperature T of the LED, the peak to peak value v_{pp} is independent. By controlling the $nV_{bias}(T)$ according to the temperature, the LED string is kept working in its linear region regardless the temperature shift. According to Fig. 2, the voltage across the LEDs is

$$v_{LED}(T) = v_{boost}(T) - v_{buck} \tag{2}$$

It is useful to keep in mind that $v_{boost}(T)$ only has DC component $V_{boost}(T)$ (the voltage ripple is negligible) and v_{buck} has DC and AC contributions represented by its DC component V_{buck} and its AC component Δv_{buck}.

The idea is to keep the average voltage of $v_{LED}(T)$, $avg(v_{LED}(T))$ equal to $nV_{bias}(T)$. It is important to notice that the average voltage over the LEDs, avg(v_{LED}) = $nV_{bias}(T)$ depends only on the DC component, giving

$$avg(v_{LED}(T)) = V_{boost}(T) - V_{buck} = nV_{bias}(T). \tag{3}$$

Equation (3) shows that the biasing point can be either controlled by the average value of the boost or the buck dc-dc converter. But due to the fact that the control of the temperature drift is implemented by means of the boost dc-dc converter, it is only the boost dc-dc converter voltage $v_{boost}(T)$ which has temperature dependency. On the contrary, the AC voltage is controlled only by the buck dc-dc converter as follows

$$nv_{pp}/2 = \Delta v_{buck}, \tag{4}$$

and because there is no temperature dependency on the working range v_{pp}, the buck dc-dc converter does not need any control according to the temperature shift of the LED. This means that v_{buck} could vary from 0 to nv_{pp}, generating the whole working range available on the LEDs. Moreover, the average value V_{buck} is then $nv_{pp}/2$, as shown in Fig. 3.

As a summary, according to (3), the temperature control can be implemented on the boost dc-dc converter throughout $v_{boost}(T)$, working in closed loop. This allows the buck dc-dc converter to work in open loop, by keeping V_{buck} constant, and by means of Δv_{buck}, the converter generates the communication signal. Since the signal that it generates only depends on nv_{pp}, and this is independent from the temperature, the converter will be always within the linear region of the LED string.

Other important consideration is the power flow between the two converters. As shown in Fig. 2, the boost dc-dc converter drains an input current i_{boost} from the input voltage V_{in} while the buck converter injects a current i_{buck}. The input current i_{in} can be written as

$$i_{in} = i_{boost} - i_{buck}. \tag{5}$$

The boost dc-dc converter injects power to the LED string, delivering an output voltage v_{boost} and an output current i_{LED}. The output power of the boost dc-dc converter P_{boost} can be written as

$$P_{boost} = i_{LED} v_{boost}. \tag{6}$$

Part of this power is processed by the LED string P_{LED}, whose power can be written as

$$P_{LED} = i_{LED} v_{LED} = i_{LED}(v_{boost} - v_{buck}). \tag{7}$$

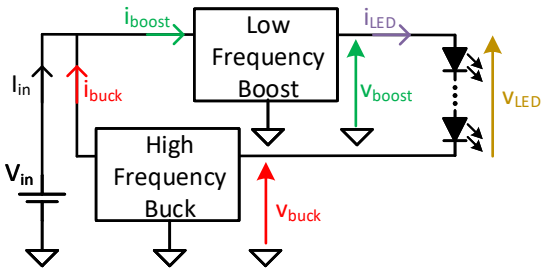

Fig. 2. Block diagram of the proposed VLC-LED driver.

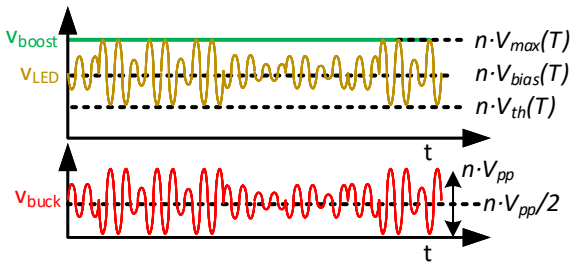

Fig. 3. Working example of the proposed VLC-LED driver waveforms.

The remaining power is reprocessed back by the buck dc-dc converter, draining P_{buck}

$$P_{buck} = i_{LED} v_{buck} \tag{8}$$

and delivering i_{buck} back to the input.

B. Design factors

One important advantage is that the input voltage is shared for both converters, allowing the simplification of the previous stages of the VLC-LED driver in comparison with other topologies based on the same principle of splitting the power with more than one input voltage [14]. Also, the input voltage V_{in} can be lower than the threshold voltage of the LED string, allowing this solution to work from low voltages, such as battery powered circuits, in contrast to solutions based only on the buck dc-dc converter [14], [15].

The selection of the V_{in} plays an important role on the design. The voltage v_{buck} is generated by a buck dc-dc converter from V_{in}, meaning that V_{in} has to be equal or higher than nv_{pp}. $v_{boost}(T)$ is generated by a boost dc-dc converter also from V_{in}, meaning that V_{in} has to be equal or lower than the maximum LED voltage $V_{max}(T)$. The two design constrains can be written together as

$$nv_{pp} \leq V_{in} \leq V_{max}(T). \tag{9}$$

One important design aspect has to be taken into account due to the temperature dependency of the upper limit. V_{in} has to be designed giving enough room due to the temperature shift, which moves the maximum LED voltage $V_{max}(T)$ to lower values as the temperature rises.

The selection of V_{in} also plays an important role regarding the power losses. Due to the high switching frequency of the buck dc-dc converter and the relatively low power of the typical lighting applications, the switching losses of the buck dc-dc converter can be considered the principal source of losses in this system. This losses have a direct dependency regarding the input voltage V_{in} [16]. The higher V_{in}, the higher the switching losses in the buck dc-dc converter. This means that in order to minimize the power losses, V_{in} has to be selected closer to nv_{pp} in inequation (9).

Other important consideration and advantage is the higher duty cycle resolution of the high frequency buck dc-dc converter, which especially important when a complex communication signal is used. Assuming that the resolution of the duty cycle that controls the high frequency switches Q_{1bu} and Q_{2bu} is limited, the whole duty cycle range is used and the overall resolution is increased by choosing a V_{in} higher and closer to nv_{pp}. As an example, if nv_{pp} = 10 V and $V_{in} = nv_{pp}$, the duty cycle varies from 0 to 1 in order to reproduce the whole signal. On the other hand, if the input voltage is twice the LEDs working range $V_{in} = 2nv_{pp}$, the duty cycle varies from 0.5 to 1, halving the resolution. This means that in order to maximize the duty resolution, V_{in} has to also be selected closer to nv_{pp} in inequation (9).

One main key of the design process is the frequency selection of both converters. The higher the frequency of the buck dc-dc converter, the higher the bandwidth of the VLC signal but the lower the efficiency. In the case of the boost dc-dc converter, the lower the switching frequency, the higher the efficiency but the size of the converter would be excessively big.

The interaction between both converters has to be taken into account regarding the loop control and the communication performance, meaning that the distance between switching frequencies and the filtering action has to be designed properly.

III. Experimental Results

As experimental results, an VLC-LED driver for VLC is built. It is based on a low frequency boost and a high frequency buck dc-dc converters sharing the same input voltage and connected in series regarding the LED load.

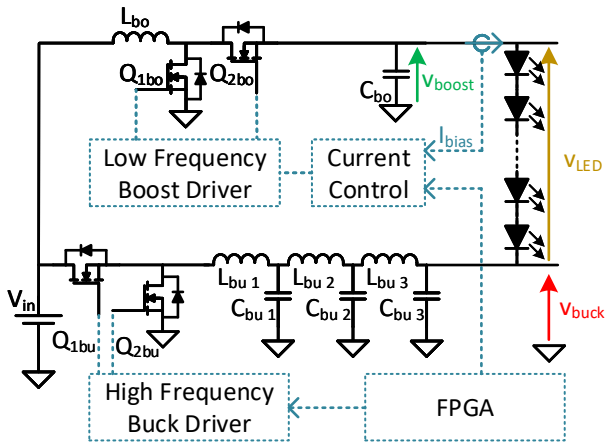

Fig. 4. Circuit of the proposed VLC-LED driver.

The load is a string of 8 HB-LEDs *XLamp MX-3* [17], with and output power around 8 W. The current and voltage necessary for the string can be obtained from the datasheet of the LED *XLamp MX-3* used [17]. A string of 8 HB-LEDs *XLamp MX-3* has a maximum voltage of 32 V (4 V for a single LED) and a current of 0.25 A in the middle of the linear region. The working range is nv_{pp} = 8 V (1 V for a single LED). The input voltage used is V_{in} = nv_{pp} = 8 V following (9).

The average current through the LEDs is kept at 0.25 A (in the middle of the lineal region) and the overall efficiency achieved is 91.5%. The efficiency is measured by comparing the DC input power with the RMS output power (taking into account biasing and communication power) on the LED string.

A. Boost dc-dc converter design

The low frequency boost dc-dc converter is designed to work as a traditional LED driver with a switching frequency of 100 kHz, working in closed loop. It is in charge of increasing the dc output voltage up to the maximum voltage allowed across the LED, and it also implements the bias current loop control of the LED string. Due to the low dynamic behavior of the temperature shift on the LEDs, there is no need for the converter to have a fast output dynamic response. Regarding the switching frequency, a trade-off has to be defined: increasing the switching frequency allows to reduce the reactive elements of the converter (especially interesting in low size applications) but it increases the power losses and the effect of the switching noise over the communication (if this noise lays within the communication band). This noise is produced by the output voltage ripple on the output boost capacitor C_{bo}. Using (10), the boost output ripple is limited to a maximum of 2% of the output boost voltage. The final values of the reactive elements of this converter are shown in Table I.

$$C_{bo} = \frac{\Delta Q}{2\Delta v_{boost}} = \frac{I_{bias} D_{bo} T_{bo}}{2\Delta v_{boost}} \tag{10}$$

In this equation, ΔQ is the total charge of the capacitor, Δv_{boost} is the amplitude of the voltage ripple, I_{bias} is the output boost current. D_{bo} and T_{bo} are the duty cycle and the time period of the boost dc-dc converter.

Ir order for the boost dc-dc converter to control the I_{bias} current, a current control is implemented. The current is measured by means of an isolated current shunt connected in series with the LED string. The current control includes a low pass filter which eliminates the communication components in the LED current and a PI controller. Regarding the PI controller, no new considerations have to be taken into account in this implementation and a standard current controller for LED can be used. Both the PWM modulation and the current control are implemented in a FPGA *Nexys A7*.

For the rest of the component selection, the dual MOSFET *CSD88539* is used for Q_{1bo} and Q_{2bo}, For the driving stage, a half bridge driver *ISL6700* is used. The complete list of components are summarized in Table I.

B. Communication scheme design

The converter reproduces a 64-QAM modulation, with a carrier frequency f_{sig} of 1 MHz. The symbol period is equal of four signal periods, achieving a maximum bit rate of 1.5 Mbps. In order to avoid any switching noise coming from the boost dc-dc converter, the signal frequency is selected a decade higher than the boost switching frequency.

C. High frequency and fast response buck dc-dc converter design

The high frequency buck dc-dc converter is in charge of generating the communication signal previously mentioned. This converter works in open loop and includes a high order output filter to achieve high bandwidth and fast response. In order to properly reproduce a communication signal by means of a buck dc-dc converter, the inequation

$$f_{sig} < f_{cut} < f_{bu} \tag{11}$$

regarding the carrier frequency f_{sig}, the cut-off frequency of the filter f_{cut} and the buck switching frequency f_{bu} has to be applied. The exact relation between the frequencies an the order and attenuation of the filter

TABLE I
CIRCUIT COMPONENTS OF THE VLC-LED DRIVER

Q_{1bo} and Q_{2bo}	Boost driver	L_{bo}	C_{bo}	Q_{1bu} and Q_{2bu}	D_{1bu} and D_{2bu}	Buck drivers	LEDs
CSD88539	*ISL6700*	71 μH	9 μF	*PD84010-E*	*UPS115UE3*	*EL7155CSZ*	*XLamp MX-3*

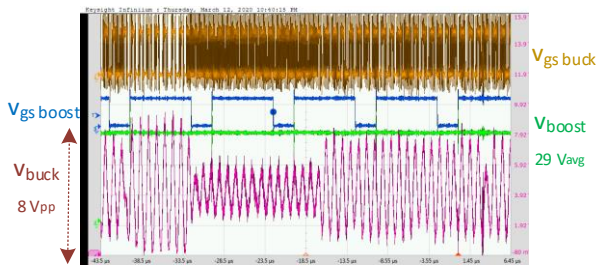

Fig. 5. Gate signal of the buck and boost dc-dc converters v_{gsbuck} and $v_{gsboost}$, output voltage of the buck converter v_{buck} and output voltage of the boost v_{boost} during normal operation.

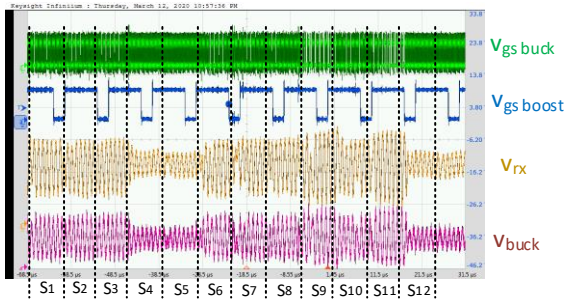

Fig. 6. Gate signals of the buck and boost dc-dc converters v_{gsbuck} and $v_{gsboost}$, output voltage of the buck converter v_{buck} and the voltage of the optical receiver v_{rx} during a transmission.

is analyzed in [18]. Following this analysis, the output filter used in a 6th low-pass filter with a cutoff frequency f_{cut} of 2.5 MHz. The reactive components of the filter are shown in Table II. The switching frequency f_{bu} used is 10 MHz.

TABLE II
REACTIVE COMPONENT VALUES OF THE 6TH ORDER OUTPUT FILTER OF THE HIGH FREQUENCY BUCK DC-DC CONVERTER.

L_{bu1}	C_{bu1}	L_{bu2}	C_{bu2}	L_{bu3}	C_{bu3}
$1.7\mu H$	$9.9nF$	$2.2\mu H$	$9.9nF$	$1.9\mu H$	$5.72nF$

Due to the high switching frequency, two RF high frequency mosfets *PD84010-E* are used for Q_{1bu} and Q_{2bu} in parallel with two high speed Schottky diodes *UPS115UE3*. For the driving stage two high speed drivers *EL7155CSZ* are used. The generation of the PWM signals for the converter and the communication signal is implemented in a FPGA *Nexys A7*. The complete list of components are summarized in Table I.

D. Experimental results

Figure 5 shows some of the most representative waveforms of the dc-dc converters. The signals $v_{gsboost}$ and v_{gsbuck} are the gate to source signals of the boost and buck dc-dc converters respectively. The difference in frequency between this two signals is notorious, $v_{gsboost}$ is a 100 kHz PWM signal and v_{gsbuck} is a 10 MHz PWM signal. The signals v_{boost} and v_{buck} are the output voltage of the boost and buck dc-dc converter respectively. As shown, the output voltage of the boost dc-dc converter is kept constant (and with low ripple) and the current loop control varies the duty cycle of the signal $v_{gsboost}$ in order to keep the average output current constant through the LEDs, at the design level of 0.25 A. Without considering any temperature shift over the LED, v_{boost} should be 32 V, which is the maximum LED voltage of the 8 LED string used. After a few minutes, when the LED temperature is stabilized, the current control loop of the boost dc-dc converter reduces v_{boost} to 25 V, a 21% lower.

The buck dc-dc converter works in open loop and reproducing the communication signal. It can be seen the variation of the duty cycle in v_{gsbuck}, and the effect over the output voltage v_{buck}. The peak to peak voltage of v_{buck} is 7.5 V, closer to the maximum working range of the 8 LED string, which is 8 V. The output buck filter is able to filter the high switching frequency of the converter and allows the communication signal to pass through. The correct design of this filter must take into account the correct reproduction of the sine carrier frequency of the modulation and the correct change in phase and amplitude between symbols.

In order to focus the analysis on the communication task of the converter, a longer period of time is shown in the Fig. 6. In order to test the communication performance, the communication signal generated by the buck dc-dc converter v_{buck} and the light emitted by the LEDs are measured during the transmission of 12

different symbols. In order to properly measure the light, a *Thorlabs PDA10A-EC* [19] high bandwidth optical receiver is used and placed in front of the LED string, giving an output voltage v_{rx} proportional to the light. By comparing both signals v_{buck} and v_{rx} it can be seen that the converter is able to properly reproduce the communication signal without distortion. The distortion could happen due to the temperature shift on the LEDs by making the LED working outside its linear region. By comparing the v_{buck} and its received light signal v_{rx}, it can be concluded that this undesired effect is avoided due to the correct current loop control.

In terms of efficiency, the experimental results were gathered using *34461A Digital Multimeterers* and show an efficiency of 91.5% reproducing a 64-QAM digital modulation, with a bit rate of 1.5 Mbps

IV. Conclusions

As conclusions, the proposed VLC-LED driver for VLC is able to reach high efficiency and high communication performance by means of splitting the power between two different converters. The design is based on two converters connected to the same input voltage and with their outputs connected in series regarding the LED load. A low frequency boost dc-dc converter working in closed loop is in charge of delivering most of the power and controlling the bias of the LEDs. On the other hand, a open loop and fast response buck dc-dc converter is in charge of generating the communication signal. As advantages, the proposal shows a high efficiency, high communication capability, input voltage flexibility and improved duty resolution. The overall power efficiency is improved by means of splitting the power between two converters where the communication signal is delivered by the high frequency converter and the bias power is processed by the low frequency boost. Other advantage is the flexibility regarding the input voltage. In contrast with other topologies based only on buck converters, the input voltage can be lower than the threshold voltage of the LED string. Other effect of a lower input voltages is the increase of the duty resolution in the high frequency buck dc-dc converter. The experimental results show an efficiency of 91.5% reproducing a 64-QAM digital modulation, with a bit rate of 1.5 Mbps.

References

[1] Cisco Systems. *Cisco Annual Internet Report - Cisco Annual Internet Report (2018–2023) White Paper*. en. URL: https://www.cisco.com/c/en/us/solutions/collateral/executive-perspectives/annual-internet-report/white-paper-c11-741490.html (visited on 2020-09-12).

[2] "IEEE Standard for Local and metropolitan area networks–Part 15.7: Short-Range Optical Wireless Communications". In: *IEEE Std 802.15.7-2018 (Revision of IEEE Std 802.15.7-2011)* (Apr. 2019). Conference Name: IEEE Std 802.15.7-2018 (Revision of IEEE Std 802.15.7-2011), pp. 1–407. DOI: 10.1109/IEEESTD.2019.8697198.

[3] Luiz Eduardo Mendes Matheus, Alex Borges Vieira, Luiz F. M. Vieira, et al. "Visible Light Communication: Concepts, Applications and Challenges". In: *IEEE Communications Surveys Tutorials* 21.4 (2019). Conference Name: IEEE Communications Surveys Tutorials, pp. 3204–3237. ISSN: 1553-877X. DOI: 10.1109/COMST.2019.2913348.

[4] Saeed Ur Rehman, Shakir Ullah, Peter Han Joo Chong, et al. "Visible Light Communication: A System Perspective—Overview and Challenges". en. In: *Sensors* 19.5 (Jan. 2019). Number: 5 Publisher: Multidisciplinary Digital Publishing Institute, p. 1153. DOI: 10.3390/s19051153. URL: https://www.mdpi.com/1424-8220/19/5/1153 (visited on 2020-08-28).

[5] Dilukshan Karunatilaka, Fahad Zafar, Vineetha Kalavally, et al. "LED Based Indoor Visible Light Communications: State of the Art". In: *IEEE Communications Surveys Tutorials* 17.3 (2015). Conference Name: IEEE Communications Surveys Tutorials, pp. 1649–1678. ISSN: 1553-877X. DOI: 10.1109/COMST.2015.2417576.

[6] Raed Mesleh, Hany Elgala, and Thomas D. C. Little. "On the performance degradation of optical wireless OFDM communication systems due to changes in the LED junction temperature". In: *ICT 2013*. May 2013, pp. 1–5. DOI: 10.1109/IC.2013.6632141.

[7] A. M. Khalid, G. Cossu, R. Corsini, et al. "1-Gb/s Transmission Over a Phosphorescent White LED by Using Rate-Adaptive Discrete Multitone Modulation". In: *IEEE Photonics Journal* 4.5 (Oct. 2012). Conference Name: IEEE Photonics Journal, pp. 1465–1473. ISSN: 1943-0655. DOI: 10.1109/JPHOT.2012.2210397.

[8] Xingxing Huang, Jianyang Shi, Jiehui Li, et al. "A Gb/s VLC Transmission Using Hardware Preequalization Circuit". In: *IEEE Photonics Technology Letters* 27.18 (Sept. 2015). Conference Name: IEEE Photonics Technology Letters, pp. 1915–1918. ISSN: 1941-0174. DOI: 10.1109/LPT.2015.2445781.

[9] Hyunchae Chun, Sujan Rajbhandari, Grahame Faulkner, et al. "LED Based Wavelength Division Multiplexed 10 Gb/s Visible Light Communications". In: *Journal of Lightwave Technology* 34.13 (July 2016). Conference Name: Journal of Lightwave Technology, pp. 3047–3052. ISSN: 1558-2213. DOI: 10.1109/JLT.2016.2554145.

[10] Marian K. Kazimierczuk. *RF Power Amplifiers*. en. John Wiley & Sons, Ltd, 2014. ISBN: 978-1-118-84437-3.

[11] Juan Rodríguez, Diego G. Lamar, Daniel G. Aller, et al. "Efficient Visible Light Communication Transmitters Based on Switching-Mode dc-dc Converters". en. In: *Sensors* 18.4 (Apr. 2018). Number: 4 Publisher: Multidisciplinary Digital Publishing Institute, p. 1127. DOI: 10.3390/s18041127. URL: https://www.mdpi.com/1424-8220/18/4/1127 (visited on 2020-08-30).

[12] Felipe Loose, Lucas Teixeira, Renan R. Duarte, et al. "On the Use of the Intrinsic Ripple of a Buck Converter for Visible Light Communication in LED Drivers". In: *IEEE Journal of Emerging and Selected Topics in Power Electronics* 6.3 (Sept. 2018). Conference Name: IEEE Journal of Emerging and Selected Topics in Power Electronics, pp. 1235–1245. ISSN: 2168-6785. DOI: 10.1109/JESTPE.2018.2843280.

[13] Javier Sebastián, Diego G. Lamar, Daniel G. Aller, et al. "On the Role of Power Electronics in Visible Light Communication". In: *IEEE Journal of Emerging and Selected Topics in Power Electronics* 6.3 (Sept. 2018). Conference Name: IEEE Journal of Emerging and Selected Topics in Power Electronics, pp. 1210–1223. ISSN: 2168-6785. DOI: 10.1109/JESTPE.2018.2830878.

[14] Juan Rodríguez, Diego G. Lamar, Pablo F. Miaja, et al. "Power-Efficient VLC Transmitter Based on Pulse-Width Modulated DC–DC Converters and the Split of the Power". In: *IEEE Transactions on Power Electronics* 34.2 (Feb. 2019). Conference Name: IEEE Transactions on Power Electronics, pp. 1726–1743. ISSN: 1941-0107. DOI: 10.1109/TPEL.2018.2830881.

[15] Daniel G. Aller, Diego G. Lamar, Manuel Arias, et al. "Design of a Two Input Buck converter (TIBuck) for a Visible Light Communication LED driver based on splitting the power". In: *2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*. ISSN: 2470-6647. Mar. 2020, pp. 1309–1314. DOI: 10.1109/APEC39645.2020.9124254.

[16] Marian K. Kazimierczuk. *Pulse-Width Modulated DC–DC Power Converters*. en-us. John Wiley & Sons, Ltd, 2015. ISBN: 978-1-119-00959-7. (Visited on 2020-09-25).

[17] Cree Components. *XLamp MX-3 LEDs — Cree Components*. URL: https://www.cree.com/led-components/products/xlamp-leds-discrete/xlamp-mx-3 (visited on 2020-09-24).

[18] Javier Sebastián, Pablo Fernández-Miaja, Alberto Rodríguez, et al. "Analysis and Design of the Output Filter for Buck Envelope Amplifiers". In: *IEEE Transactions on Power Electronics* 29.1 (Jan. 2014). Conference Name: IEEE Transactions on Power Electronics, pp. 213–233. ISSN: 1941-0107. DOI: 10.1109/TPEL.2013.2248752.

[19] Thorlabs. *PDA10A-EC Si Fixed Gain Detector, 200-1100 nm, 150 MHz BW*. URL: https://www.thorlabs.com/thorproduct.cfm?partnumber=PDA10A-EC (visited on 2020-09-24).