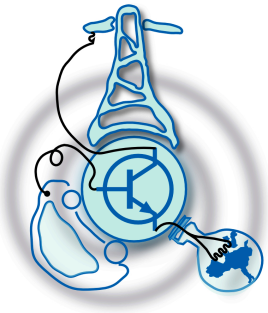
Comparative Analysis between Three Level NPC Inverter and Dual Inverter Motor Drives for SPM Synchronous Machines

by
Anuradha Sampath Mudalige



Submitted to the Department of Electrical Engineering, Electronics, Computers and Systems
in partial fulfillment of the requirements for the degree of
Erasmus Mundus Joint Master Degree in Sustainable Transportation and Electrical Power Systems
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Abstract

Permanent Magnet Synchronous Machines (PMSM) have gained increasing interest in industrial applications. Selection of the best motor drive topology for an application is a decision that involves consideration of various factors. In this research, a comprehensive comparative analysis is conducted between a Three Level Neutral Point Clamped (NPC) inverter based motor drive and a dual inverter based motor drive for Surface Permanent Magnet Synchronous Machines (SPMSM).

Control systems and modulation schemes for the two drive topologies are designed considering a SPMSM available within the facilities of the Power Electronics, Machines and Control Group (PEMC) of the University of Nottingham (UoN). Comparative analysis is conducted via mathematical modelling of the drive topologies and through a series of simulations in Matlab/Simulink for control implementations in conjunction with PLECS Blockset for thermal modelling of power electronic elements. Finally, feasibility of the two drive control philosophies are experimented by coding the controllers in C and implementing them in a laboratory experimental setup.

Keywords:

SPMSM, three level NPC, dual-inverter motor drive, uCube, Matlab, Simulink, PLECS Blockset, thermal modelling, C

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I wish to express my indebtedness to my beloved parents and brother for the moral support, encouragement and guidance extended in many ways at all stages of my life.

Last but not least, I would like to thank all the people and colleagues I met from around the world for providing a good company for two years of postgraduate studies across three countries in Europe.

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Acronyms

AC	Alternating Current.
ADC	Analog to Digital Conversion.
BDCM	Brushless DC Motor.
EACEA	The Education, Audiovisual and Culture Executive Agency of the European Union.
EMJMD STEPS	Erasmus Mundus Joint Master Degree in Sustainable Transportation and Electrical Power Systems.
EV	Electric Vehicle.
FOC	Field Oriented Control.
FPGA	Field Programmable Gate Array.
HEV	Hybrid Electric Vehicle.
IM	Induction Motor.
ISR	Interrupt Servive Routine.
NPC	Neutral Point Clamped.
NTV	Nearest Three Vectors.

OEW	Open-End Winding.
OEW-PMSM	Open-End Winding Permanent Magnet Synchronous Machine.
PEMC	Power Electronics, Machines and Control Group.
PL	Programmable Logic.
PM	Permanent Magnet.
PMSM	Permanent Magnet Synchronous Machine.
PS	Processing System.
PWM	Pulse Width Modulation.
SHEPWM	Selected Harmonic Elimination PWM.
SoC	System on Chip.
SPM	Surface Permanent Magnet.
SPMSM	Surface Permanent Magnet Synchronous Machine.
SPWM	Sinusoidal Pulse Width Modulation.
SPWMTHI	SPWM with Third Harmonic Injection.
SVPWM	Space Vector PWM.
UoN	University of Nottingham.
XSDK	Xilinx Software Development Kit.
ZSC	Zero Sequence Current.

Nomenclature

$\bar{\varphi_s}$, φ_{sd}, φ_{sq} Stator flux vector and its d,q components

$\bar{i_s}$, i_{sd}, i_{sq} Stator current vector and its d,q components

$\bar{V_A}$, V_{Ad}, V_{Aq} Inverter A voltage vector and its d,q, components

$\bar{V_B}$, V_{Bd}, V_{Bq} Inverter B voltage vector and its d,q, components

$\bar{v_s}$,v_{sd},v_{sq} stator voltage vector and its d,q components

ω shaft speed in electrical rad/s

E_A DC link voltage of the three level NPC inverter , DC link voltage of the inverter A of dual inverter drive

$I_{s,max}$ Maximum allowable stator current of the machine

L_d, L_q d,q axix stator inductance

L_s Stator inductance

p number of pole pairs

R_s Stator resistance

T Electro-mechanocal torque

$V_{A,max}$ Maximum limit of three level NPC inerter voltage vector, Maximum limit of inverter A voltage vector

$V_{B,max}$ Maximum limit of inverter B voltage vector

$V_{B,par}$ Component of the inverter B voltage vector parallel to stator current vector

$V_{B,quad}$ Component of the inverter B voltage vector orthogonal to stator current vector

Inverter A Inverter connected with the power supply in dual inverter drive with floating capacitor bridge

Inverter B Inverter associated with the floating capacitor in dual inverter drive with floating capacitor bridge

Chapter 1

Introduction

1.1 Background

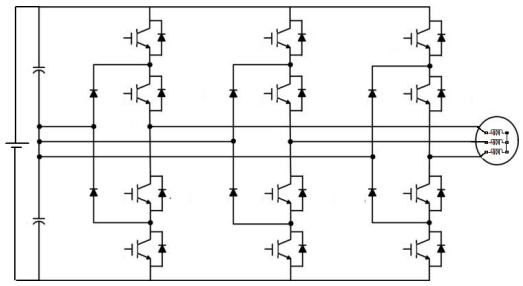
Many desirable features offered by Permanent Magnet Synchronous Machine (PMSM)s such as high torque density and better efficiency of the machine design, have made them a popular choice in industrial applications. Overall performance of the motor drive application, however, not only depends on the electrical machine, but also on associated control system and most importantly on the motor drive topology that feeds the machine. Therefore, selection of the best motor drive topology for a given industrial application involving a PMSM is an important engineering decision to be made.

In this research, performance of two motor drive topologies are comparatively assessed for their suitability in PMSM applications, exclusively focusing on Surface Permanent Magnet Synchronous Machine (SPMSM)s that find widespread industrial applications.

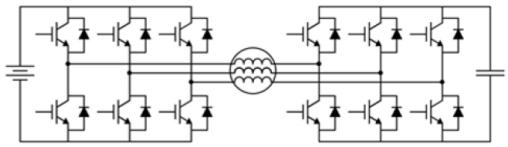
1.2 Motivation and Research Objectives

Main objective of this research is to comparatively analyse the performance of a SPMSM motor drive based on a three level Neutral Point Clamped (NPC) inverter

against a dual inverter drive with a floating capacitor bridge whose power electronics arrangements are shown in Figure 1-1a and 1-1b respectively.



(a) Three level NPC inverter drive



(b) Dual inverter drive with a floating capacitor

Figure 1-1: Schematic diagram of the power electronic arrangements of the drive topologies

First topology is essentially based on classical PMSM motor control architecture, however, instead of a two level inverter, this drive employs a three level NPC inverter to feed the machine.

The second drive topology considered in this research is based on a comparatively novel control philosophy for electrical machines. In this case, it consists of two, standard two-level inverters feeding the machine in its Open-End Winding (OEW) configuration with a floating capacitor associated with one of the inverters. This topology is one of the three dual inverter drive topologies that have gained extensive interest in academia in recent history.

A performance analysis between these two drive topologies is particularly interesting due to three reasons. Firstly, as clearly identifiable in the Figure 1-1, both drive topologies consist of equal number of power electronic switching devices. Secondly, dual inverter drives are generally assumed to generate multi-level stator voltage waveforms comparable to a multi-level inverter drives, which makes it worth investigating the performance of such a dual inverter drive against a three level inverter drive. Thirdly, even though there are many studies in literature that attempt to make comparisons between classical motor drives based on two level and three level inverters (such as [12]) or between different dual inverter drive topologies (such as [38]), no study in the literature has made an effort to compare the two drive topologies that

are the subject of this research.

Performance of the two drive topologies are to be assessed considering their applicability for a low power SPMSM prototype available within the facilities of the Power Electronics, Machines and Control Group (PEMC) of the University of Nottingham (UoN). Specifications of this SPMSM have been presented in Table 1.1 [29]

Parameter	Value
Pole number $2p$	6
PM material	NdFeB
PM remanence flux density B_{ref}	1.24T
PM relative permeability μ_r	1.031
Power rating	1.5kW
Peak value of the current I_{rated}	13A
Rated speed $\omega_{m,rated}$	3000rpm
Torque constant k_T	0.128 Nm/A
Line to line voltage constant k_v	15.5 V/krpm
Outer stator diameter	95 mm
Inner stator diameter	49.5 mm
Axial length	90 mm
Airgap length	1 mm
Magnets thickness	4 mm
Stator inductance L_d, L_q	1.35 mH
Stator resistance R_s	0.8434 Ω

Table 1.1: SPMSM Parameters

1.3 Research approach and organization of the thesis

Research was commenced with a literature review on the broader context of the research theme and state of the art developments in PMSM motor drive topologies. Most significant findings of this review are briefed in **Chapter 2** of this thesis.

Thereafter, the mathematical model of a PMSM was investigated, and its ex-

tended version for OEW configuration of a PMSM was derived and implemented in Simulink. Details of this implementation have been presented in **Chapter 3**

It was followed by the development of modulation schemes (based on Space Vector Modulation strategy) for two level and three level NPC inverters which are the fundamental power electronic systems involved in studied PMSM drive topologies. Work carried out in this respect are presented in **Chapter 4**

Control systems for three level and dual inverter motor drives are presented in **Chapter 5** and **Chapter 6** respectively.

Laboratory experiments carried out to implement the control systems associated with the two drive topologies are explained in **Chapter 7**.

Results of the comparative analysis conducted on two SPMSM motor drive topologies are presented in **Chapter 8**.

Thesis ends with its **Chapter 9** that dedicates to present conclusions of the research and proposals for possible future work.

1.4 Tools used in the research

Simulation studies related to control implementations in this research were conducted in **Simulink®**(version 9.2) graphical programming environment by **MathWorks**, in conjunction with **MATLAB®** multi-paradigm numerical computing environment and its proprietary programming language.

PLECS Blockset(version 4.1.8), a popular tool of choice for high speed simulations of power electronic systems[1] by **Plexim**, was used to conduct thermal modelling of the designed motor drive systems. PLECS Blockset facilitates seamless

integration with MATLAB®/Simulink®.

Laboratory experiments related to this work were based on a SPMSM prototype available within the facilities of PEMC of the UoN. Control systems were implemented in ***uCube***[16], a custom made control platform developed at the University of Nottingham. **C programming language** (with occasional use of **C++**) was used to program the ***uCube*** with the aid of **Xilinx Software Development Kit (XSDK)** (version 2017.4)

Chapter 2

State of the Art

This chapter presents a brief review on applications of PMSMs and state of the art motor drive topologies. It also contains a review on state of the art inverter modulation schemes that formed the basis for rational selection of modulation strategies for the drive topologies in subsequent design steps.

2.1 Applications of Synchronous Machines

Synchronous machines are well known for their widespread applications as synchronous generators in AC power grids. However, their applications are not just limited to generating mode. Many desirable features of synchronous machines, specifically, those of PMSMs such as higher power density, higher torque density [6], higher efficiency and lesser heating [34] have made them a popular choice for industrial applications including Electric Vehicle (EV) applications.

A common classification of electric motors used in industrial applications is shown in Figure 2-1. Some research has indicated that Permanent Magnet (PM) motor drives, including PMSMs and Brushless DC Motor (BDCM)s could become serious competitors to the Induction Motor (IM)s due to their overall better efficiency indicators, effective use of reluctance torque, lesser losses and compact motor size [26],[33]. In PMSMs, power losses are mainly associated with the stator whereas the rotor offers

an almost loss-free design [8]

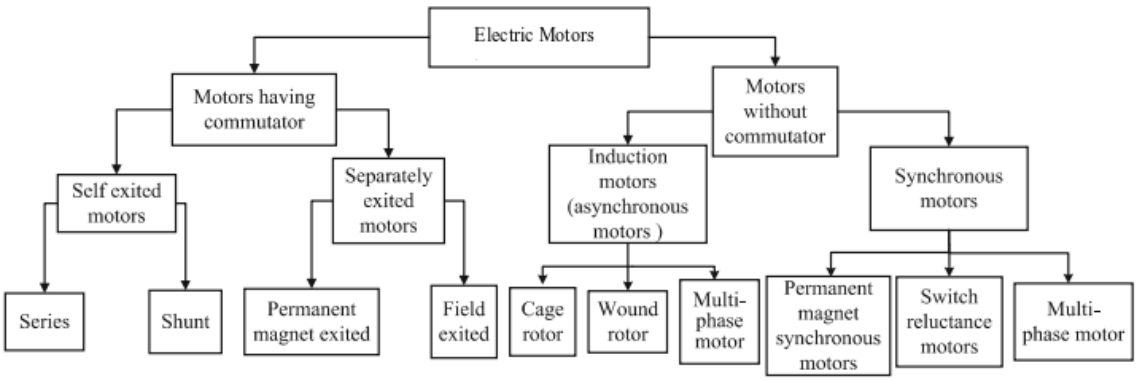


Figure 2-1: Classification of motors used in industrial applications [34]

The electric motor represents one of the key components for EVs. In such an application, the motor used for the drive train is desirable to have a high torque and power density, a high starting torque, a wide speed range, a high intermittent overload capability and a reasonable price ([11], [41], [43], [20]). In such a context, PMSMs are becoming more attractive due to their inherent features that fulfil these expectations.[14] Moreover, the fact that a relatively low-power PMSM can provide sufficient power for the drive train of a medium sized car, thus minimizing the requirement for expensive permanent magnets, has made PMSMs a popular choice for Hybrid Electric Vehicle (HEV)s. Some good examples are Toyota Prius and Honda Insight HEVs which are both equipped with PMSMs [40], [10].

SPMSMs, the specific type of PMSM focused in this research, offer additional benefits such as simplified manufacturing process, robustness and lower cost due to their solid rotor core design. However, one of the drawbacks of SPMSMs is their limited speed range compared to rest of the PMSM types, but research on dual inverter drive topologies have shown that this drawback can be effectively resolved by employing dual inverter motor drives in OEW configuration of the machine. [6]

2.2 PMSM drive topologies

Motor drive topologies, in general, can be divided into two major classes namely single inverter based drives and dual inverter based drives. Single inverter drive topology can be considered as the most common and classical motor drive topology in industrial applications. Dual inverter based motor drives are emerging nowadays as a promising alternative for conventional motor drives.

There has been much research investigating applicability of dual inverter drive topologies for different types of electrical machines. In [13], [19] and [24] authors have presented their findings on applying dual inverter drive topology for IM applications. [27] proposes a novel power circuit topology for IM dual inverter drive topologies, in which a rectifier-inverter is embedded within a conventional two-level inverter. Author in [31] has extensively studied the applicability of dual inverter drive topologies for PMSMs. Reference [25] discusses applicability of dual inverter drive topologies for Synchronous Reluctance Machines and proposes a speed control system based on one of the dual inverter drive topologies.

2.2.1 Single inverter drive topologies

Single inverter drives, controlled based on Field Oriented Control (FOC) philosophy, and fed by two level voltage source inverters have been the most common motor drive in majority of the applications involving PMSMs and IMs. Applications of multi level inverters such as three level NPC inverters can also be found in motor drive applications. In [12], the authors have presented an extensive comparative analysis between two level and three-level inverter drives for EV applications.

2.2.2 Dual inverter drives with separate voltage sources

Power electronics arrangement of this drive topology has been shown in Figure 2-2. It is evident that the two two-level inverters that feed the machine in its OEW configurations have their own DC power supplies in this topology.

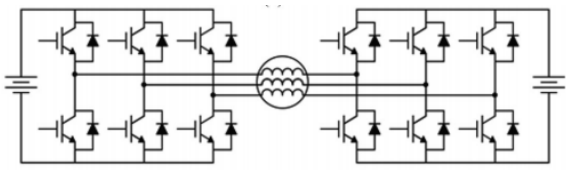


Figure 2-2: Schematic of dual inverter drive topology with separate voltage sources

Presence of separate DC power supplies facilitates maximization of the output voltage vector on the machine's stator produced by the drive while avoiding the common mode impedance. Some of the key advantages of this topology are no generation of common mode (zero sequence) currents in the motor winding and best DC bus voltage utilization. However, the fact that the drive requires two separate DC power sources, renders it more expensive and less practical in an industrial application. Requirement for separate DC voltage sources may be obtained by means of isolated voltage transformers or with completely independent battery packs. Specially, in terms of EV applications, having two separate batteries on board is not convenient for obvious reasons such as weight and cost. [29]

Authors in [18],[21] and [17] have proved one of the distinct features of this dual inverter topology, i.e. the capability to regulate the load power sharing between the two power sources within a switching period. This allows the control system to adjust the power flow between two DC power sources and manage their state of charge in an effective manner.

2.2.3 Dual inverter drives with a common voltage source

Inverter and power source arrangement of a typical dual inverter drive with a common voltage source is shown in Figure 2-3.

The obvious advantages of employing a single DC power source for the drive are reduced cost, minimal weight and overall simplicity of the the drive system. This has made it to attract the attention of the research community and there are many studies such as [29] that exclusively studies applicability of this topology for industrial

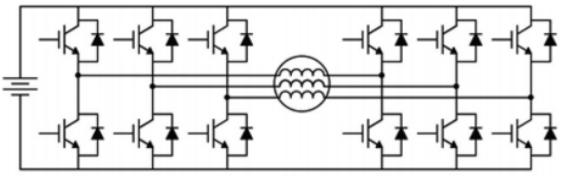


Figure 2-3: Schematic of dual inverter drive topology with common voltage source

applications.

However, one of the critical flaws of this design is the zero-sequence current loop it allows in the system leading to flow of Zero Sequence Current (ZSC)s. Authors in [42] and [35] have researched extensively to investigate root causes for the presence of ZSC in this drive topology. The author in [29] has investigated the possibility to eliminate the presence of ZSC in high speed PMSM applications involving this drive topology.

2.2.4 Dual inverter drives with a single voltage source and a floating capacitor

The third dual inverter drive topology, the one with a single voltage source with a floating capacitor bridge is the drive topology that will be focused in this research. Schematic representation of this drive topology was already presented in Chapter 1. The control philosophy of this drive topology can be found in Chapter 6.

One of the key advantages of this drive topology is the absence of ZSC flow in the system in contrary to the dual inverter drive topology with a common DC power source. In EV applications, it is a common practice to employ a DC-DC converter before the inverter that feeds the electrical motor to have a voltage boost [29]. This drive topology can serve the same purpose of voltage boost with additional benefits such as increased speed range of the machine. In [22] authors have also shown the possibility to increase the constant torque region of the machine by employing this drive topology.

2.3 Selection of modulation strategies for the drives

This section summarises the results of the literature review conducted in order to select suitable modulation strategies for the drive systems that are analysed in this research.

Modulation strategies can be classified into two main classes viz. fundamental switching frequency modulation schemes and high frequency Pulse Width Modulation (PWM) schemes[36]. Former class of modulation schemes are simple to implement and less resource intensive in terms of required processing power, and result in low switching losses due to limited number of switching events per cycle of fundamental frequency. However, they suffer with high level of harmonics in the current waveform, that needs be filtered by bulky and uneconomical low-pass filters[7].

Contrary to fundamental frequency modulation schemes, high frequency PWM schemes allow the designer to optimize the harmonic content in the waveforms [7]. For an application such as a motor drive considered in this study, less harmonics in resulting stator current waveforms, in turn result in reduced torque ripples and minimal losses in the machine.

There are many possible PWM schemes proposed in literature. Some of the most common are Sinusoidal Pulse Width Modulation (SPWM), SPWM with Third Harmonic Injection (SPWMTHI), Selected Harmonic Elimination PWM (SHEPWM) and Space Vector PWM (SVPWM) [7][36].

SPWM technique is probably the most commonly used scheme and is simple to implement. SVPWM schems, in contrary, are computation intensive, and somewhat complicated in implementation, yet can be treated as the best among all the PWM techniques [7] in terms of utilization of DC link[30] (DC link utilization for SPWM is restricted to $V_{DC}/2$ whereas SVPWM schemes can utilize the DC link up to $V_{DC}/\sqrt{3}$),

current ripples and ease of adaptation for multi level inverter topologies. Therefore, modulation schemes for both two level and three level NPC inverters used in the motor drives developed in this study are designed based on corresponding SVPWM schemes.

Chapter 3

Mathematical Model for OEW-PMSM

This chapter explains the mathematical model of an Open-End Winding Permanent Magnet Synchronous Machine (OEW-PMSM) that will be used in subsequent studies related to the dual inverter motor drive. Chapter commences by explaining the mathematical model of a conventional PMSM and will be followed by presenting its extension to OEW configuration. At the end of the chapter, there is a section explaining the work carried out to implement this mathematical model in Simulink.

3.1 Mathematical model of a conventional PMSM

Fig. 3-1 shows the schematic diagram of a conventional PMSM driven by a single inverter drive system, in terms of space vectors, under the assumption that d axis is aligned with the PM excitation field. Mathematical model for the machine in dq0 reference frame can be expressed in terms of equations 3.1 - 3.5 ([6],[29])

$$v_{sd} = R_s i_{sd} - \omega \varphi_{sq} + \frac{d\varphi_{sd}}{dt} \tag{3.1}$$

$$v_{sq} = R_s i_{sq} + \omega \varphi_{sd} + \frac{d\varphi_{sq}}{dt} \tag{3.2}$$

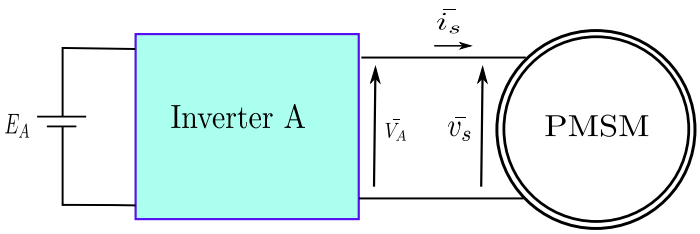


Figure 3-1: Schematic diagram of a conventional PMSM fed by a single inverter system, represented in terms of space vectors

$$\varphi_{sd} = L_d i_{sd} + \varphi_e \tag{3.3}$$

$$\varphi_{sq} = L_q i_{sq} \tag{3.4}$$

$$T = \frac{3}{2} p[\varphi_e i_{sq} + i_{sd} i_{sq}(L_d - L_q)] \tag{3.5}$$

where v_{sd} and v_{sq} are the d-q components of the stator voltage vector $\bar{v_s}$, φ_{sd} and φ_{sq} are the d-q components of the stator flux vector $\bar{\varphi_s}$ and T is the electromechanical torque generated by the machine. i_{sd} and i_{sq} represent the d-q components of the stator current vector $\bar{i_s}$. d,q stator inductances, stator resistance and permanent magnet flux are given by L_d,L_q, R_s and φ_e respectively.

With reference to Fig. 3-1, relationship between machine's stator voltage vector $\bar{v_s}$ and the inverter output voltage vector $\bar{V_A}$ in this drive system is given by equation 3.6

$$v_s = \bar{V_A} \tag{3.6}$$

3.2 Extension of the mathematical model to OEW machine configuration

In OEW configuration of a PMSM, one can access either ends of the three phase stator windings. This allows us to design a drive system that involves two inverters (Inverter

A and Inverter B) feeding machine. Schematic diagram of such a dual inverter drive system has been shown in Fig. 3-2 in terms of space vectors.

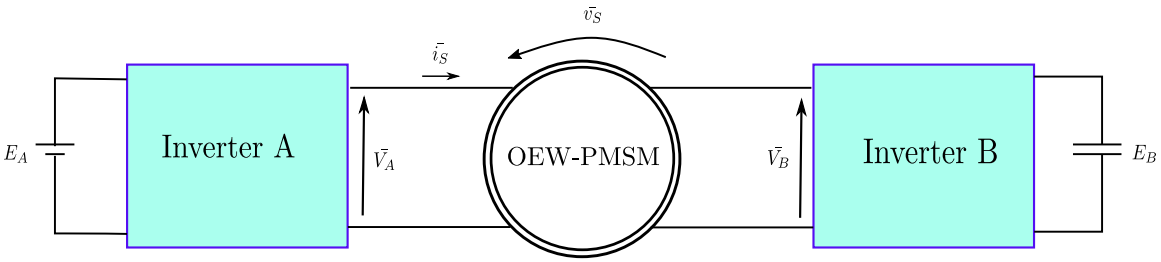


Figure 3-2: Schematic diagram of a OEW-PMSM fed by a dual inverter system, represented in terms of space vectors

With reference to Fig. 3-2, it can be noted that machine's stator voltage vector $\bar{v_s}$ is now given by equation 3.7

$$v_s = \bar{V_A} - \bar{V_B} \tag{3.7}$$

where $\bar{V_A}$ and $\bar{V_B}$ are the output voltage vectors of inverter A and inverter B respectively. By expressing voltage vectors in terms of d,q components, equation 3.7 can be rewritten as given by equation 3.8 and components can be further decomposed as given by 3.9 and 3.10

$$v_{sd} + jv_{sq} = (V_{Ad} + jV_{Aq}) - (V_{Bd} + jV_{Bq}) \tag{3.8}$$

$$v_{sd} = V_{Ad} - V_{Bd} \tag{3.9}$$

$$v_{sq} = V_{Aq} - V_{Bq} \tag{3.10}$$

This additional consideration on stator voltage vector $\bar{v_s}$ allows us to express the mathematical model for an OEW-PMSM in terms of same equations 3.1 - 3.5 used to describe a conventional PMSM.

3.3 Implementation of OEW-PMSM mathematical model

Even though simulation models for a conventional PMSM are readily available in commonly used simulation platforms such as Matlab/Simulink and PLECS, no built in models are available that facilitate simulation requirements involving open end winding configuration of PMSMs. Therefore, the mathematical model for an OEW-PMSM expressed in d-q reference frame was implemented in Matlab/Simulink.

Figure 3-3 shows the masked view of implemented OEW-PMSM model and its block parameters dialog box. The model was designed to accept d,q components of inverter A and inverter B voltage vectors (VAd,VAq,VBd,VBq) and shaft speed (wm_rad/s) as inputs and to return d,q components of stator current (Id,Iq), electromechanical torque generated by the machine (Te) and electrical angular position of the rotor (the) as outputs. Block parameters dialog box allows one to specify the parameters of the machine under consideration.

Implemented model under mask is shown in Figure 3-4. Model equations have been implemented mainly with the aid of RL branches, controlled voltage sources, a Matlab function block to perform additional calculations and an integrator block to calculate rotor's electrical angular position. This model can be used to simulate either a conventional PMSM or a PMSM in its OEW configuration. In former case, one has to feed zero for the Inverter B voltage inputs (VBd,VBq).

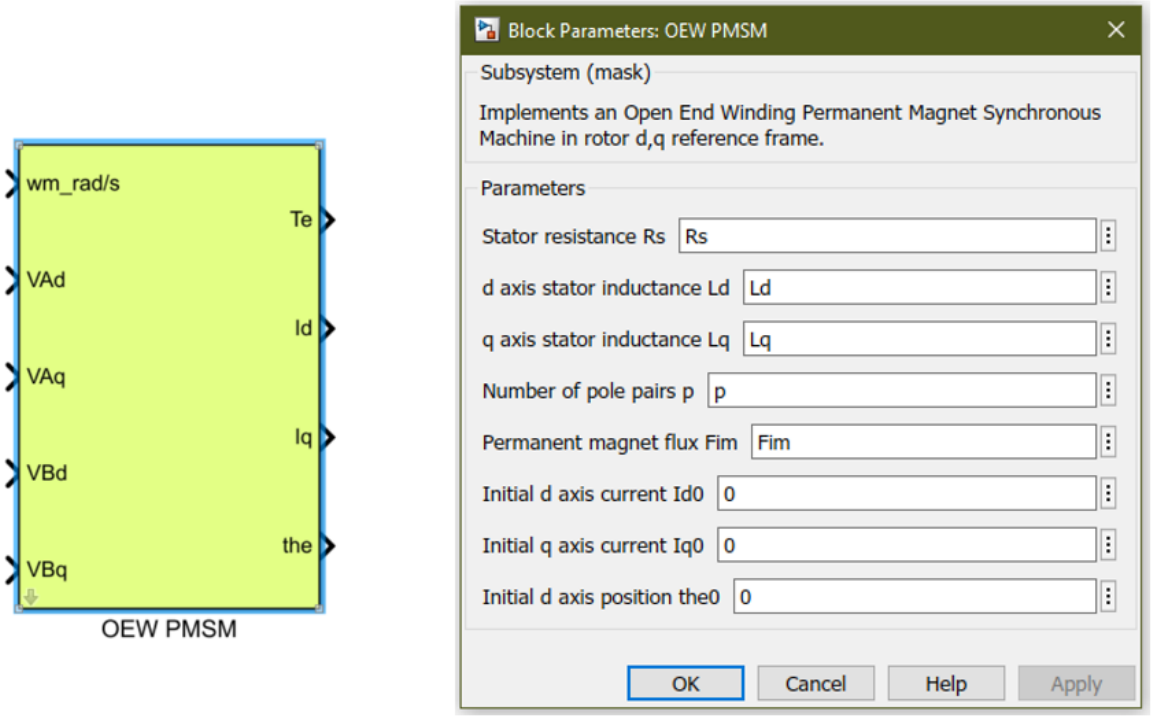


Figure 3-3: Implemented OEW-PMSM Simulink model and its block parameters dialog

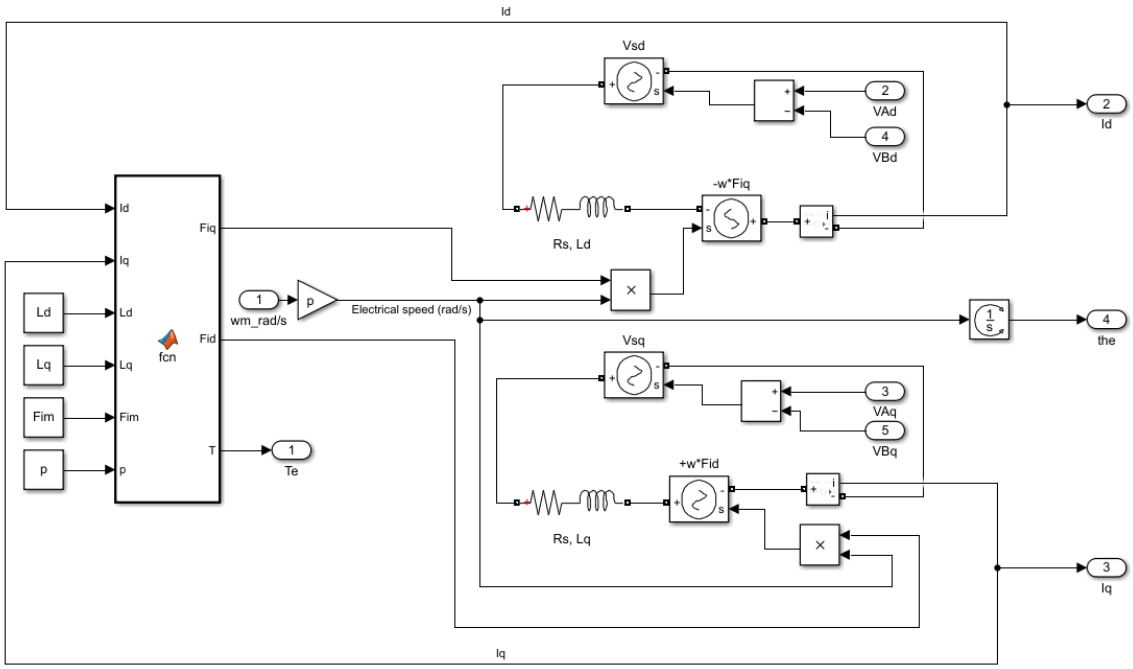


Figure 3-4: Masked view of the implemented OEW-PMSM model

Chapter 4

Development of Modulation Schemes

As already outlined in this thesis, dual inverter drive topology analyzed in this study is composed of two, two-level inverters. Performance of the dual inverter drive topology is to be compared against a single inverter motor drive based on a three level NPC inverter. Therefore, it is necessary to select and implement appropriate modulation schemes for two level and three level NPC inverter systems.

Modulation schemes provided by Matlab/Simulink and PLECS simulation platforms, were found incapable to cater the simulation requirements under this analysis. Specially, the modulation scheme provided by PLECS software for the three level NPC inverter was found to loose control over DC link voltage balancing under unbalanced and transient conditions. Therefore, modulation schemes for both two level and three level inverter topologies were carefully selected and implemented in Simulink as an initial step of the motor drive design process.

4.1 Implementation of SVPWM scheme for two level inverter

Schematic diagram of a typical two level inverter is shown in Figure 4-1. Switches of the inverter, at a given instant, can be either ON or OFF (denoted as 1 and 0 respectively in subsequent notations). However, in order to avoid a short circuit on the DC link, upper and lower switches in the same leg must always operate in complimentary states. This implies that there are only eight possible switching combinations for the inverter that can be written as **OOO, POO, PPO, OPO, OPP,OOP,POP,PPP** by adopting the convention specified in Table 4.1(three letters in this notation refer to the switching state of a,b,c legs of the inverter, stated in sequential order).

Switching state	Switch status, Phase x = a,b,c	
	S_{x1}	S_{x2}
P	1	0
O	0	1

Table 4.1: Two level inverter switching states convention

Space vector representation of these voltage vectors (in $\alpha - \beta$ reference frame) is shown in Figure 4-2. Vectors corresponding to switching states **OOO** and **PPP** are zero in magnitude. Magnitude of the remaining vectors can be shown to be equal to $\frac{2}{3}V_{DC}$ [36]

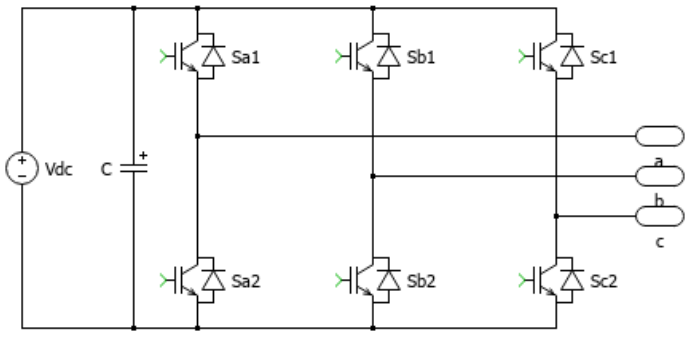


Figure 4-1: Schematic representation of a typical two level inverter

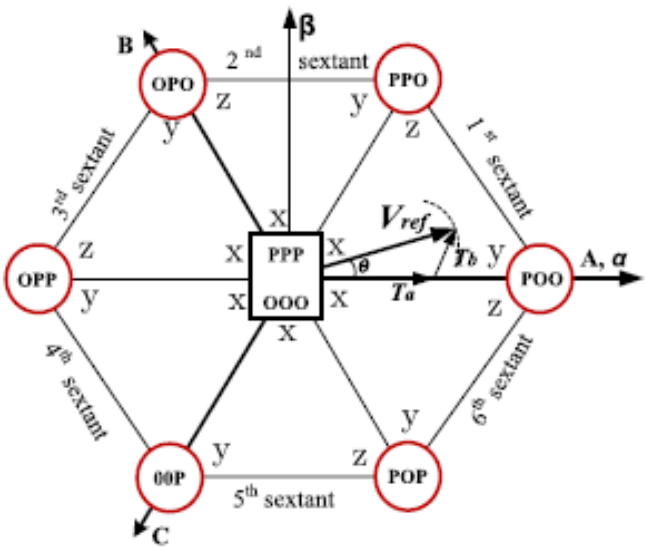


Figure 4-2: Space-vector diagram for a two-level inverter

4.1.1 Operating principle

In order to generate required voltage waveform out of the inverter using SVPWM principle, firstly, it is necessary to locate the reference voltage vector within the space vector diagram and identify the Nearest Three Vectors (NTV)s surrounding it. Reference vector can then be represented as a vector sum of the NTVs together with appropriate switching times for each of the NTV during a given switching period.

4.1.2 Main steps

Implemented SVPWM scheme can be described as a process consisting of three main steps viz. identification of NTVs, NTV duty cycle calculation and determination of switching states.

1. **Identification of Nearest Three Vectors**

Requested a,b,c voltage references are first converted to $\alpha - \beta$ stationary reference

frame using the Clarke transform given by equation 4.1[36].

$$\begin{pmatrix} V_\alpha \\ V_\beta \end{pmatrix} = \begin{pmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{pmatrix} \begin{pmatrix} V_a \\ V_b \\ V_c \end{pmatrix} \tag{4.1}$$

Having calculated α, β components , magnitude and phase of the reference voltage vector $\bar{V}_{ref}$ can easily be obtained. With these information $\bar{V}_{ref}$ can be written as,

$$\bar{V}_{ref} = \sqrt{V_\alpha^2 + V_\beta^2} \angle \tan^{-1} \frac{V_\beta}{V_\alpha} \tag{4.2}$$

Information on magnitude and angle can be used to exactly locate $\bar{V}_{ref}$ within the space vector diagram.

2. **Calculation of dwelling times**

Assuming that NTVs corresponding to $\bar{V}_{ref}$ located on the space vector diagram are v_x,v_y and v_z, reference voltage vector can be synthesized by means of appropriate combinations of the NTVs as given by equation 4.3

$$V_{ref}.T_s = v_x.T_x + v_y.T_y + v_z.T_z \tag{4.3}$$

where T_s is the switching period of the inverter(inverse of the switching frequency). T_x, T_y and T_z refer to the dwelling times for each of the NTV during a switching period. Dwelling time for the three NTVs should add up to the switching period and can be expressed as,

$$T_s = T_x + T_y + T_z \tag{4.4}$$

By considering above relationships and geometric relationships of vector representation in the space vector diagram, following general expressions were derived for dwelling times. x,y,z vectors that correspond to this notation have been indicated for

each of the sector in the space vector diagram.

$$T_x = a\sin(S\frac{\pi}{3} - \theta) \tag{4.5}$$

$$T_y = a\sin(\theta - (S-1)\frac{\pi}{3}) \tag{4.6}$$

$$T_z = T_s - (T_x + T_y) \tag{4.7}$$

where S is the sector number$(1, 2..., 6)$ within which $\bar{V}_{ref}$ is located in. a is defined as the modulation index and θ is the angle of the $\bar{V}_{ref}$ given by following expressions. V_{DC} refers to the DC link voltage of the inverter.

$$a = \sqrt{3}\frac{\sqrt{V_\alpha^2 + V_\beta^2}}{V_{DC}} \tag{4.8}$$

$$\theta = \tan^{-1}\frac{V_\beta}{V_\alpha} \tag{4.9}$$

3. **Determination of switching states.**

Implemented modulator divides a switching period into seven segments of duration $\frac{T_x}{4}$, $\frac{T_y}{2}$, $\frac{T_z}{2}$, $\frac{T_x}{2}$, $\frac{T_z}{2}$, $\frac{T_y}{2}$ and $\frac{T_x}{4}$. If the reference vector is located in the first sector, for each segment of time, it sequentially assigns the states OOO - POO - PPO - PPP - PPO - POO - OOO. Switching state assignment algorithm for all the cases is given in Appendix B under Figure B-1

4.1.3 Implementation of the modulation scheme in Simulink

Figure 4-3 shows the two level SVPWM modulator subsystem implemented in Simulink. Modulator receives α,β components of the reference voltage vector $\bar{V}_{ref}$ and DC link voltage of the inverter as inputs. It includes an additional port that accepts a trigger that is used to synchronize the modulator with the intended switching frequency of

the inverter. Modulator outputs the gate pulses that can be used drive a two level inverter.

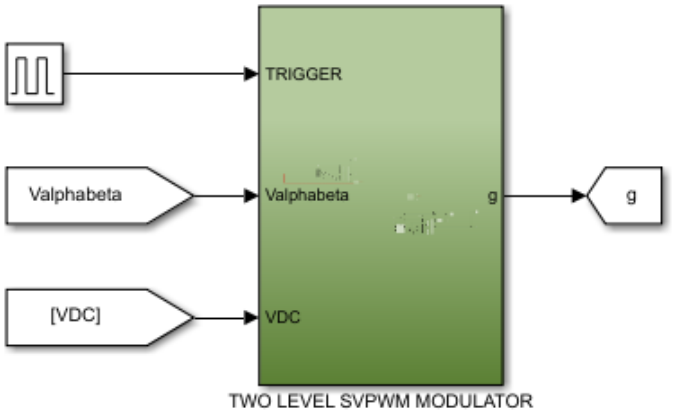


Figure 4-3: Space Vector Pulse Width Modulator for two level inverter implemented in Simulink

First level internal view of of the modulator subsystem in shown in Figure 4-4.

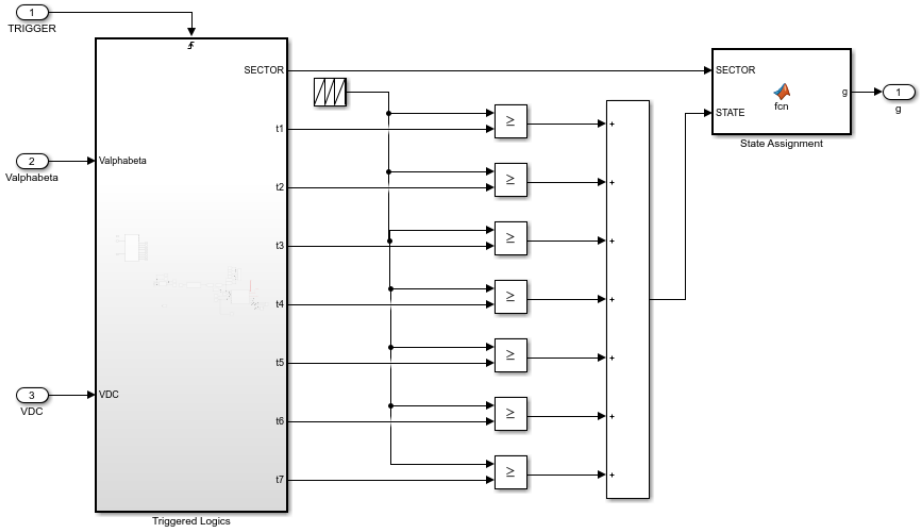


Figure 4-4: First level internal view of the two level Space Vector Pulse Width Modulator

Logical implementations in this level can be divided in to two categories, namely triggered logics and continuous logics. Triggered logics are executed once at the beginning of each switching period and are responsible for sector determination of the

reference voltage vector and dwelling time calculations. Triggered logics block returns information related to seven time segments and sector of the reference voltage vector. These information are passed to comparison logics and "State assignment" Matlab script that are collectively responsible for generating the gate pulses. Triggered logics have also been implemented in the form of a Matlab script, and are not shown in this discussion in order to maintain conciseness of the thesis.

4.2 Implementation of SVPWM scheme for three level NPC inverter

Schematic representation of a typical three level NPC inverter is shown in Figure. 4-5. This topology consists of four power electronic switches and two clamping diodes in each leg, whose connection points are connected to the common connection point of the two DC link capacitors.

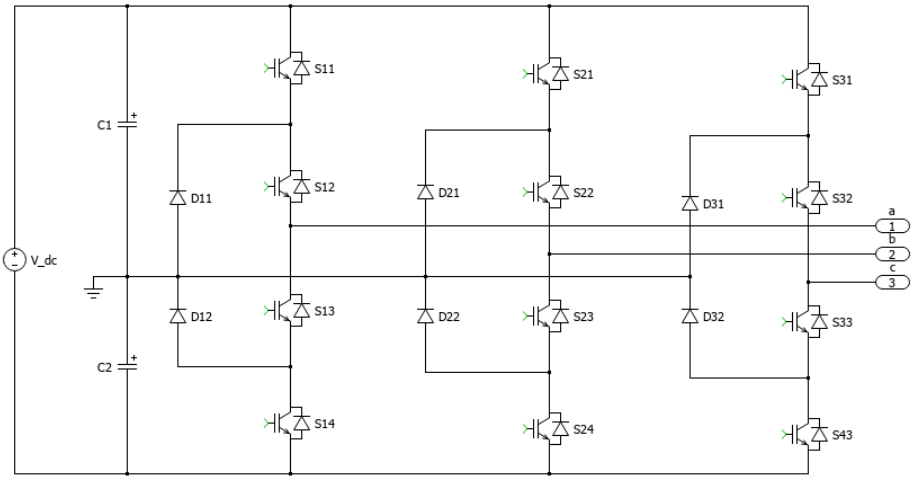


Figure 4-5: Schematic representation of a typical three level NPC inverter

Convention adopted in denoting the switching states is shown in Table 4.2. There are three possible switching states for each leg. Consequently, it results in 27 switching state combinations. Voltage vectors generated by the inverter at these switching states are shown in Figure 4-6 in the form of a space vector diagram. Table 4.3 tabulates the magnitude of each of the vectors, classifying them as null, small, medium

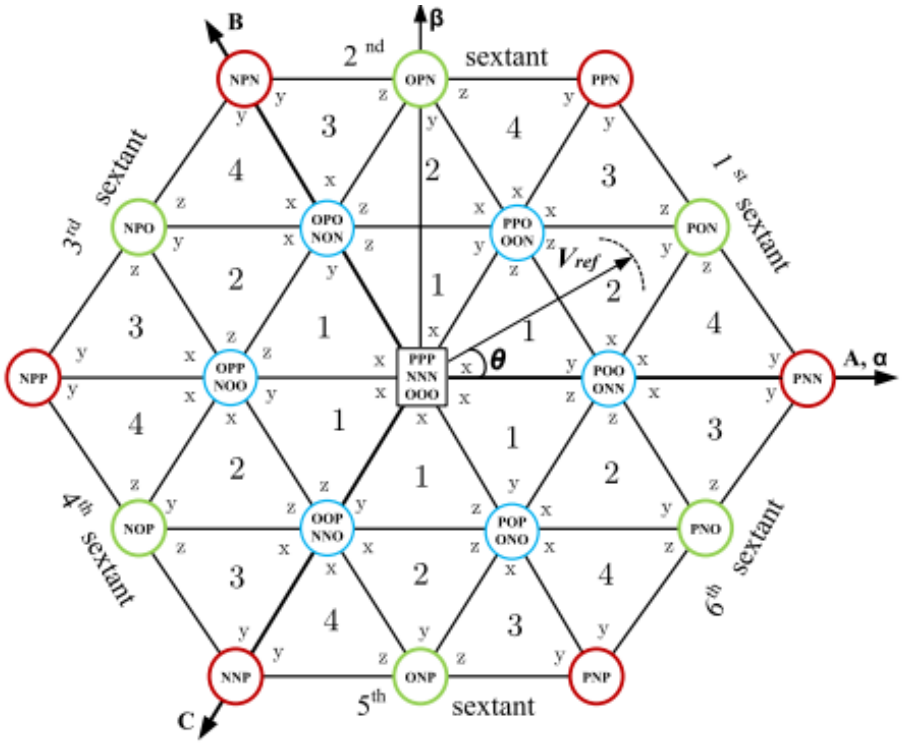


Figure 4-6: Space-vector diagram for three-level NPC inverter

and large vectors.

It is possible to identify that there exist more than one switching state resulting in identical voltage vectors in the space vector diagram, which will be called as "redundant vectors" in subsequent discussion, whose existence serves a useful function in maintaining voltage balance of the two DC link capacitors.

Switching state	Status of the switches, Phase x(a,b,c)			
	S_{x1}	S_{x2}	S_{x3}	S_{x4}
P	1	1	0	0
O	0	1	1	0
N	0	0	1	1

Table 4.2: Three level NPC inverter switching states convention

Switching vector combination	Voltage level
PPP,NNN,OOO	0 (Null vectors)
PPO,OON,POO,ONN,POP,ONO, OOP,NNO,OPP,NOO,OPO,NON	$V_{dc}/3$ (Small vectors)
PON,OPN,NPO,NOP,ONP,PNO	$V_{dc0/\sqrt{3}}$ (Medium vectors)
PNN,PPN,NPN,NPP,NNP,PNP	$2V_{dc}/3$ (Large vectors)

Table 4.3: Three level NPC inverter different switching combinations

4.2.1 Operating principle

Basic concept behind SVPWM strategy on any multi-level inverter, remains unchanged to that applicable for a two level inverter. Similar to the two level SVPWM scheme, it involves identifying NTVs for the reference voltage vector and synthesizing it by means of appropriate NTV and dwelling time combinations.

DC link voltage balancing

DC link voltage balancing is an important concern in multi-level inverters. For a three level NPC inverter, it can be shown that different voltage vectors affect differently on capacitor voltage balancing problem. Figure 4-7 indicates the effect of each of the voltage vectors in sector 1 of the space vector diagram on capacitor voltage balancing.

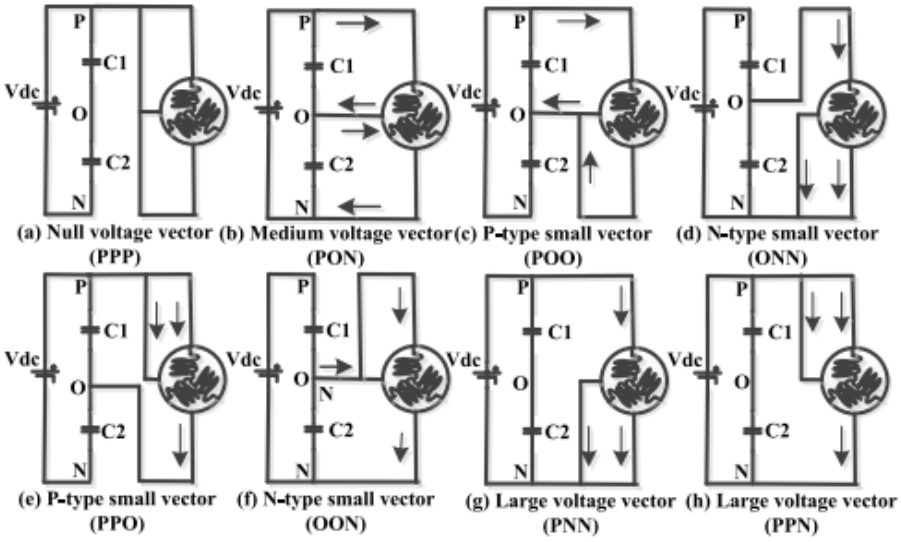


Figure 4-7: Effects of different voltage vectors on DC-link capacitor voltage

Null (a) and large voltage vectors (g and h) have no effect on the dc-link voltage balancing as they are not connected to the neutral point of the inverter. Therefore, only the small voltage (c, d, e, and f) and medium voltage (b) vectors are mainly responsible for the balancing problem. [12]. In the implemented modulation scheme, this phenomenon is appropriately utilized to select redundant voltage vectors in order to maintain the capacitor voltage balance of the inverter.

4.2.2 Main steps

1. **Identification of Nearest Three Vectors**

As clearly identifiable in the given space vector diagram for a three level NPC inverter, each of the six sectors consists of four triangular regions, which will be referred to as "sub-sectors" in subsequent text. (Sub-sectors are numbered 1 to 4 in the given space vector diagram). Therefore, identifying the NTVs at a given point of operation requires a slightly advanced computation methodology compared to the case of two level SVPWM sector identification. In order to facilitate a generalised approach for sub-sector identification, and subsequent NTV determination process, a generalized reference-vector coordinates $V_{\alpha}^{'}$ and $V_{\beta}^{'}$ are defined[23] as given by following equations.

$$V_{\alpha}^{'} = |\bar{V}_{ref}| \cos[\theta - (S-1)\frac{\pi}{3}] \tag{4.10}$$

$$V_{\beta}^{'} = |\bar{V}_{ref}| \sin[\theta - (S-1)\frac{\pi}{3}] \tag{4.11}$$

Equations follow same notations adopted in the discussion for two level SVPWM scheme. With this treatment, and based on simple geometric relationships on the space vector diagram, logic for sub-sector identification can be formulated as given by following equations;

$$\text{if} \quad V_\alpha' < \frac{V_{dc}}{3} - \frac{\sqrt{3}}{3}.V_\beta' \quad \text{then, Sub-sector} = 1 \tag{4.12}$$

$$\text{else if} \quad V_\alpha' > \frac{V_{dc}}{3} + \frac{\sqrt{3}}{3}.V_\beta' \quad \text{then Sub-sector} = 4 \tag{4.13}$$

$$\text{else if} \quad V_\beta' < \frac{\sqrt{3}V_{dc}}{6} \quad \text{then Sub-sector} = 2 \tag{4.14}$$

$$\text{else} \quad \text{Sub-sector} = 3 \tag{4.15}$$

2. **Calculation of dwelling times**

Once the NTVs of the reference voltage vector are identified, dwelling times for each of the vector is calculated based on the generalized set of equations given in Table 4.4. x,y,z vectors that correspond to this notation have been indicated for each of the sub-sector in the space vector diagram.

	T_x	T_y	T_z
Sub-sector 1	$1 - 2a\sin[\theta - (S-2)\frac{\pi}{3}]$	$2a\sin(S\frac{\pi}{3} - \theta)$	$2a\sin[\theta - (S-1)\frac{\pi}{3}]$
Sub-sector 2	$1 - 2a\sin[\theta - (S-1)\frac{\pi}{3}]$	$-1 + 2a\sin[\theta - (S-2)\frac{\pi}{3}]$	$1 - 2a\sin(S\frac{\pi}{3} - \theta)$
Sub-sector 3	$2 - 2a\sin[\theta - (S-2)\frac{\pi}{3}]$	$-1 + 2a\sin[\theta - (S-1)\frac{\pi}{3}]$	$2a\sin(S\frac{\pi}{3} - \theta)$
Sub-sector 4	$2 - 2a\sin[\theta - (S-2)\frac{\pi}{3}]$	$-1 + 2a\sin(S\frac{\pi}{3} - \theta)$	$2a\sin[\theta - (S-1)\frac{\pi}{3}]$

Table 4.4: Formulas for NTV dwelling time calculations

3. **Determination of switching states**

Switching state assignment step in implemented modulator is based on the algorithm presented in [12]. It takes into account the voltage of the upper and lower capacitors of the DC link at the beginning of each switching period to assign the switching states in order to maintain neutral point voltage balance. Adopted state assignment algorithm is given in Appendix A.

4.2.3 Implementation of the modulation scheme in Simulink

The modulator subsystem implemented in Simulink is shown in Figure 4-8. Figure 4-9 shows the first level internal view of the modulator.

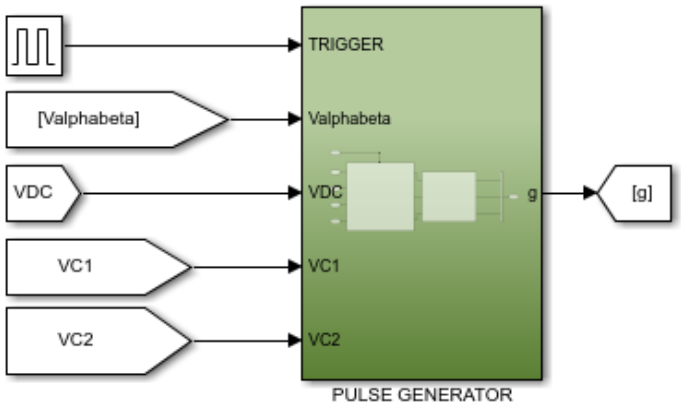


Figure 4-8: Space Vector Pulse Width Modulator for three level NPC inverter implemented in Simulink

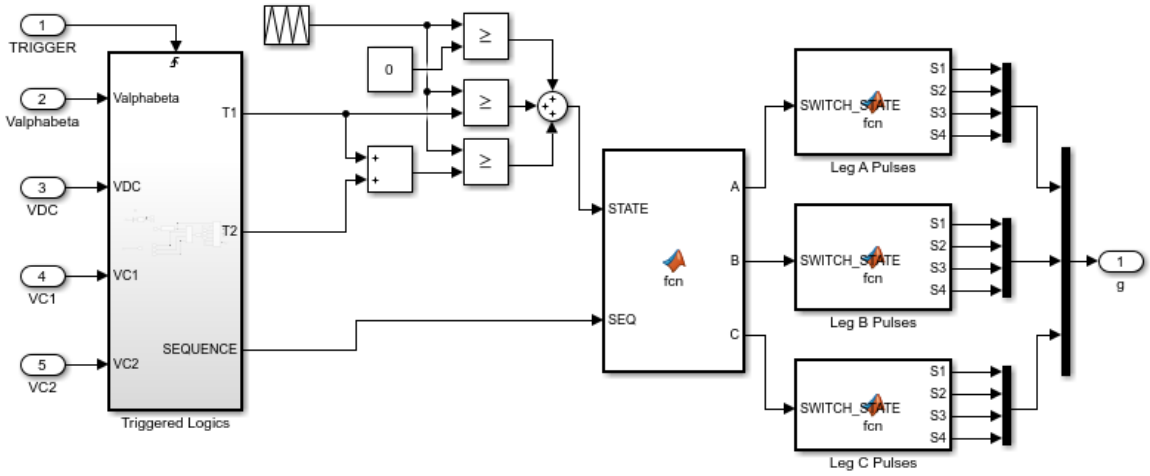


Figure 4-9: First level internal view of the three level Space Vector Pulse Width Modulator

Implementation has adopted a similar paradigm to that of the two level SVPWM modulator implementation. However, as evident in the figure, the modulator now accepts instantaneous voltages of DC link capacitors as additional inputs in order to use them as inputs for subsequent switching state assignment logics.

4.3 THD analysis of two level and three level NPC inverter voltage waveforms

A Total Harmonic Distortion(THD) analysis of phase-to-phase voltage waveforms generated by two level and three level inverters triggered by implemented modulators was conducted. Voltage and current waveforms of the two inverters with the modulation index varying from 0 to 1 is shown in Figure 4-10. Variation of THD of the phase to phase voltages with varying modulation indices under two inverters is shown in Figure 4-11.

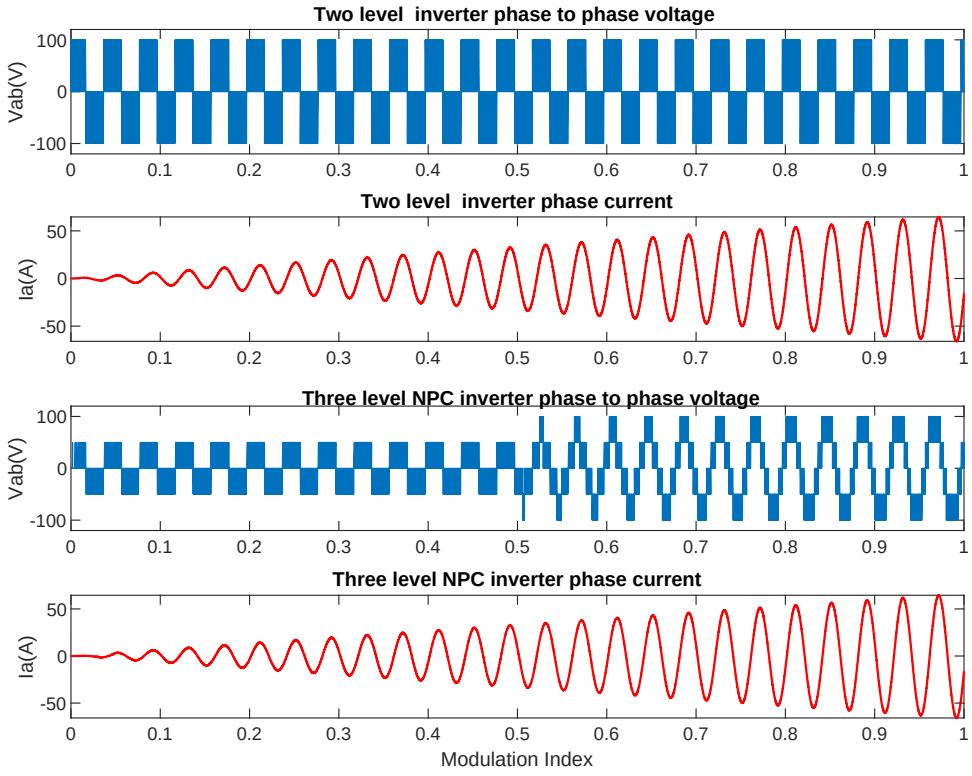


Figure 4-10: Phase-to-phase voltages and phase currents with two inverters

It is evident that three level inverter performs well with respect to THD in generated voltage waveform, except at very low modulation indices where it effectively acts as a two level inverter.

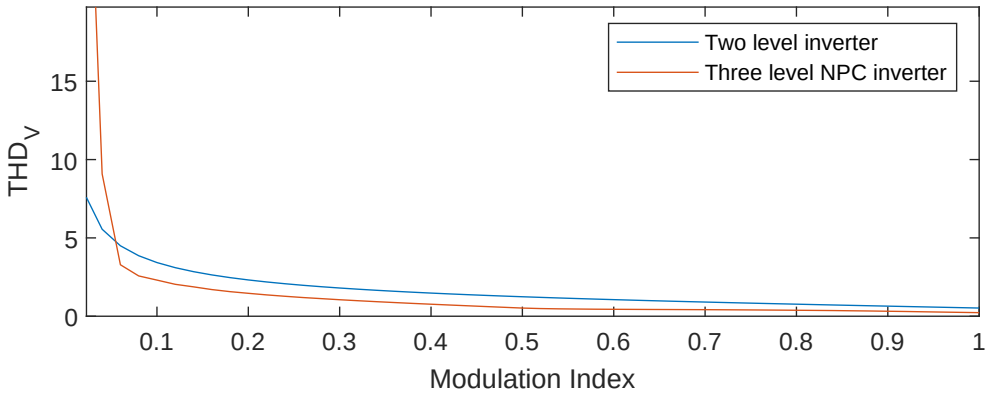


Figure 4-11: THD of phase-to-phase voltage waveforms

Chapter 5

Control System for Three Level NPC Inverter Drive

This chapter explains the speed control system applicable for the three level inverter drive. It is based on classical Field Oriented Control (FOC) scheme used to control SPMSMs. FOC system in this context assumes that the d axis is aligned on the direction of permanent magnet flux of the rotor.

5.1 Design specifications

Parameters of the SPMSM given in Table 1.1 were used to design the three level NPC inverter based speed control system. DC link voltage of the three level NPC inverter (E_A) was considered as 80V.

5.1.1 Voltage and current constraints

Operating limits of the speed control system are constrained by voltage and current limits offered by the machine and the inverter.

Maximum permissible current $I_{s,max}$ which can be the nominal thermal current of he machine at steady state or the the nominal current of inverters in transient overload conditions, limits the torque capability of the motor drive.[6] In this design,

$I_{s,max}$ is taken as $13A$ which is the rated current of the machine. Therefore steady state stator current vector $\bar{i_s}$ has to be limited within its maximum limit as given by equation 5.1

$$|\bar{i_s}| \leq I_{s,max} \tag{5.1}$$

Above the based speed, machine behaviour is also constrained by the available DC link voltage of the inverter, i.e,

$$|\bar{V_A}| \leq V_{A,max} \tag{5.2}$$

where V_{max} is the maximum voltage that can be generated by the three level NPC inverter, which depends on the modulation strategy. In this study, the inverter is based on SVPWM. Therefore, maximum voltage that can be generated in the linear operating range is:

$$V_{A,max} = \frac{E_A}{\sqrt{3}} \tag{5.3}$$

5.2 Control scheme

Control scheme adopted in this design for driving the SPMSM shown in Fig.5-1.

It consists of inner control loops that are responsible for controlling d,q components of stator current and outer control loops that generate corresponding current references.

5.2.1 Inner control loops

PI regulators (a) and (b) in inner control loops are responsible for controlling stator currents. Inputs to these two controllers are respective current errors and they output $V^*_{d,ref}$, $V^*_{q,ref}$ components of voltage reference for the inverter ($\bar{V}^*_{ref}$). Feed-forward

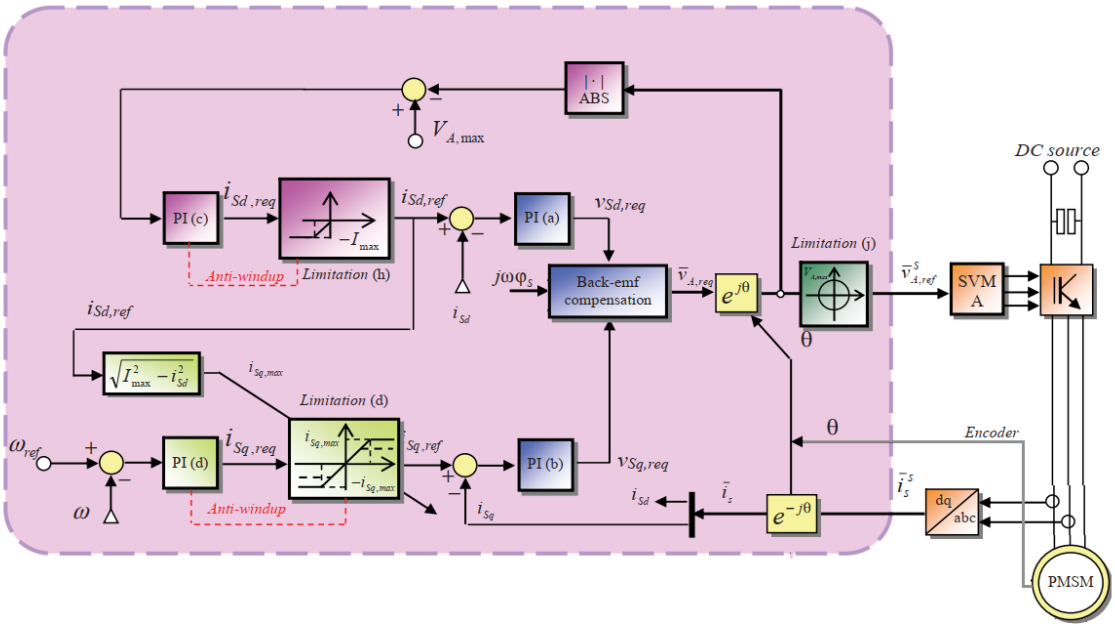


Figure 5-1: Speed control system for the SPMSM based on a three level NPC inverter drive

terms resulting from back-emf terms are added to the output of these controllers in order to improve transient performance of the control system.

$\bar{V}^*_{ref}$ is limited to $V_{A,max}$ within the d-q control axis system by employing a saturation logic and voltage reference $\bar{V}^s{*}_{ref}$ is sent as an input to the modulation scheme of the inverter to generate requested reference voltage at machine's stator terminals.

By neglecting the terms $-\omega\varphi_{sq}$ and $\omega\varphi_{sd}$ in equation 3.1 and 3.2 respectively and considering the fact that $L_d = L_q = L_s$ for our machine, one can observe that Laplace transform on equations results in identical plant transfer functions for both id and iq in a control perspective. Common plant transfer function applicable for both PI regulators (a) and (b) can be written as given in equation 5.4

$$P_i(S) = \frac{i_s(S)}{v_(S)} = \frac{1}{R_s + SL_s} \tag{5.4}$$

Regulators were tuned by considering the closed loop transfer function involving a PI controller with a natural frequency(ω_n) of 200Hz and a damping factor ζ 0.75 for the closed loop current response.

5.2.2 Outer control loops

PI controller (c) generates the reference for d axis current component $i_{sd}*$. Input to the controller is the difference between $V_{A,max}$ and magnitude of V^*_{ref}. Output of the regulator is limited between $I_{s,max}$ and 0. Saturation feedback is used as an input to the regulator to avoid integrator wind-up.

PI regulator (d) takes care of issuing reference for the q component of stator current $i_{sq}*$. It receives speed error $(\omega^*_m - \omega_m)$ as the input. Output of the regulator is limited between $\pm I_{q,avail}$ that is given by,

$$\pm I_{q,avail} = \sqrt{I^2_{s,max} - i^2_{sd}*} \tag{5.5}$$

Saturation feedback is employed as an input to the controller in order to avoid overshoots in th speed response due to integrator wind-up.

PI control parameters for the speed regulator in this design were obtained by considering a natural frequency (ω_n) of 6Hz and a damping factor ζ 0.70

5.2.3 Concept of Maximum Torque Per Amp - (MTPA) for SPMSM

Mathematical expression for the electromagnetic torque generated by a PMSM was already introduced in Chapter 3 under equation 3.5. The first term in the equation $(\varphi_e i_{sq})$ is termed as magnet alignment torque and the second term that is proportional to $(L_d - L_q)$ is termed as reluctance torque. [37] SPMPMs are characterized by equal values for L_d and L_q. Therefore, for the case of a SPMSM, equation 3.5 can be simplified and rewritten as given by equation 5.6.

$$T = \frac{3}{2} p(\varphi_e i_{sq}) \tag{5.6}$$

This implies that maximum torque per unit of stator current is generated when d component of stator current is maintained at zero as long as the machine does not require

flux weakening control in order to maintain stator voltage vector below permissible maximum limit.

Chapter 6

Control System for Dual Inverter Drive with a Floating Capacitor Bridge

This chapter explains the control system adopted for the control of the dual inverter drive with a floating capacitor bridge. It is based on the control scheme published in [6].

6.1 Design specifications

The control system explained in this chapter will be implemented for the SPMSM whose specifications are given in Table 1.1. Figure 6-1 shows how two level inverters, (inverter A and inverter B) are interfaced with the SPMSM in its open end winding configuration.

In Figure 6-1, DC link voltages of inverter A and inverter B have been denoted by E_A and E_B respectively. $\bar{v}_A$, $\bar{v}_B$ and $\bar{v}_S$ indicate voltage vectors of inverter A, inverter B and the stator of the SPMSM respectively. $\bar{i}_s$ represents the stator current vector. Table 6.1 tabulates the values for fixed E_A, upper limit considered for E_B and capacitance(C) of the DC link capacitor associated with the inverter B.

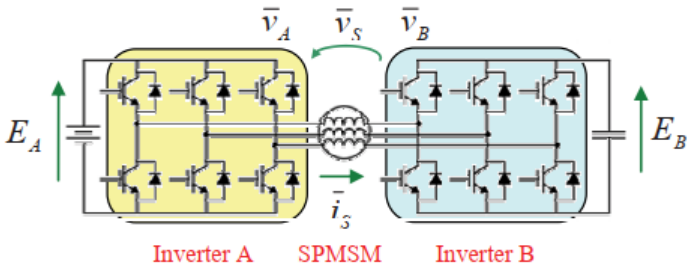


Figure 6-1: Schematic diagram of the OEW-SPMSM fed by inverter A and inverter B with a floating capacitor

Parameter Symbol	Value
E_A	$80V$
$E_{B,max}$	$160V$
C	$160\mu F$

Table 6.1: Dual inverter drive design specifications

6.1.1 Voltage and current constraints

Maximum stator current $I_{s,max}$ has to be limited to 13A similar to the case of single inverter based motor drive. Control system must also ensure that the voltage requests commanded to inverter A and inverter B are within their maximum limits.i.e.

$$|\bar{V}_A| \leq V_{A,max} \text{ and } |\bar{V}_B| \leq V_{B,max} \tag{6.1}$$

Upper limits for voltages can be stated as in equation 6.2 considering the SVPWM scheme adopted for the inverters in this design.

$$V_{A,max} = \frac{E_A}{\sqrt{(3)}} \text{ and } V_{B,max} = \frac{E_B}{\sqrt{(3)}} \tag{6.2}$$

6.2 Control Scheme

Overall control scheme for the OEW-PMSM fed by the dual inverter system is shown in Figure 6-2. It consists of two sub control systems. Subsystem in pink background deals with the control of inverter A whereas that in light blue background is responsible for controlling inverter B, which involves the floating capacitor.

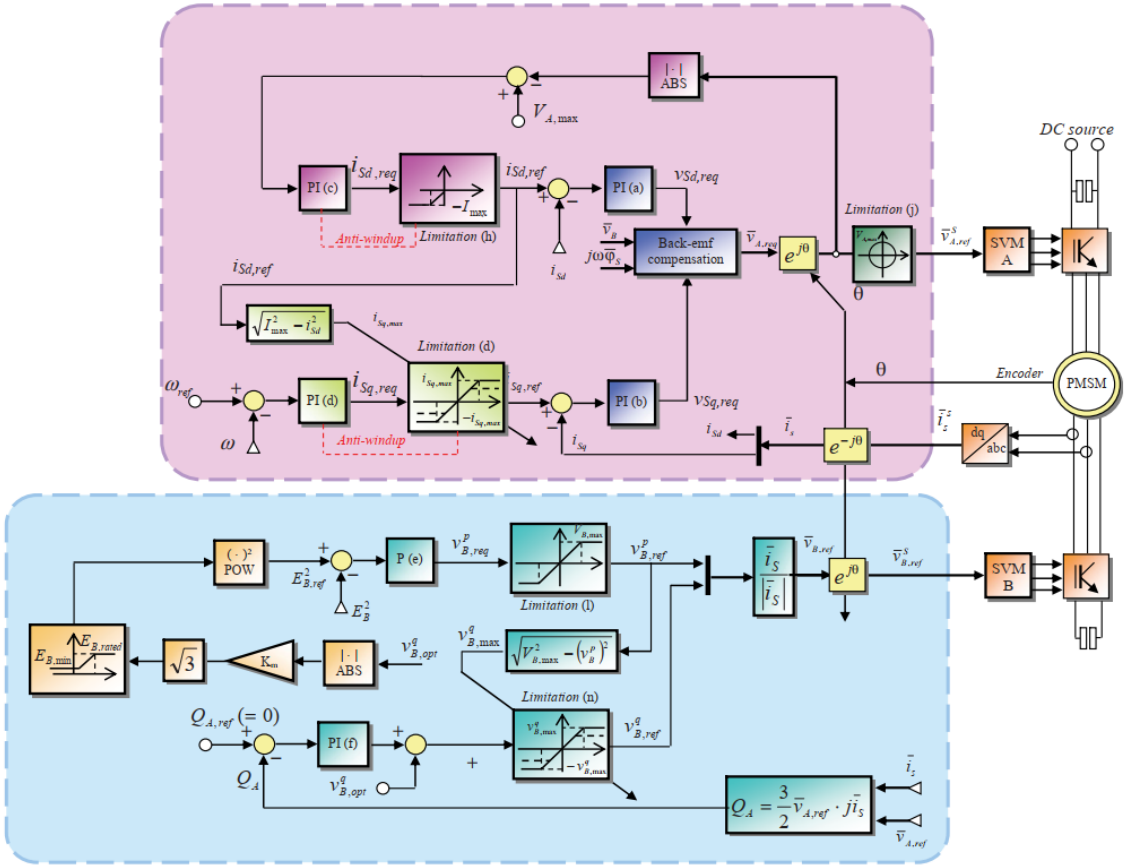


Figure 6-2: Block diagram of the control scheme for the OEW-PMSM fed by the dual inverter system.

6.2.1 Control of inverter A

Purpose of the controls implemented for the inverter A that is connected to the external power supply from which the system receives real power, can be considered to be very much similar to the objectives of the FOC system implemented for the inverter in the case of a single inverter based motor drive. Main objective of this sub-control system is to control the speed of the machine at the set-point commanded by the user via control of stator currents.

Relationship between voltage vectors

With reference to Figure 6-1 and based on Kirchhoff's voltage law, relationship between voltage vectors of the inverters and that of the machine can be written as in equation 6.3

$$\bar{v_s} = \bar{v_A} - \bar{v_B} \tag{6.3}$$

This relationship implies the ability to boost the stator voltage of the machine by appropriate manipulation of inverter A and B voltage vectors. This is one of the key benefits of the dual inverter topology over the single inverter drive design considered in previous chapter.

In a control point of view for the inverter A, equation 6.3 indicates that, by adding inverter B voltage vector $\bar{v_B}$ as a compensation term at the end of the current controllers' control action, it is possible to maintain plant equations for the d,q current control of the inverter A unchanged compared to the single inverter based control system investigated in previous chapter. With this modification, same control parameters calculated for current, speed and flux controllers in single inverter based drive design can be used for the controllers associated with inverter A of the dual inverter drive.

Control of flux, speed and stator current

As indicated in the pink area of the control system shown in Figure 6-2, control scheme for inverter A involves PI controllers (a) and (b) in the inner control loops for controlling d,q components of stator currents and associated outer PI controllers (c) and (d) that generate corresponding current references. Apart from the additional $\bar{v_B}$ compensation added after the control action of PI controllers (a) and (b), overall architecture of the control system and design considerations are similar to the case of the control system design presented in previous chapter. Notations similar to the control system for single inverter drive given in Figure 5-1 have been adopted in this figure considering the ease of cross reference between the two cases for the reader.

6.2.2 Control of inverter B

Control systems implemented for inverter B serves two purposes. Firstly, it involves controls for controlling the DC link voltage of the floating capacitor of inverter B (E_B). E_B can either be maintained at a fixed reference value of $E_{B,max}$ at the expense of increased switching losses associated with the inverter B or it can be varied depending on operating point of the machine in an attempt to minimize the losses associated wih the inverter B. Control system adopted in this study is based on the latter option where DC link voltage reference will be varied depending on the operating point of the machine.

Secondly, it attempts to compensate reactive power of the inverter A by injecting or absorbing reactive power from the system. This function allows the inverter A to maximize transferable active power to the PMSM in compliance with the voltage and current constraints of the drive.

Selection of control reference frame

Contrary to the inverter A controls, controls for the inverter B are implemented in a reference frame synchronous with the stator current space vector $\bar{i_s}$. As outlined in subsequent sections, mathematical formulations based on such a reference frame facilitate development of independent control loops for inverter B for reactive power control and floating capacitor voltage control.

Principle of floating capacitor voltage control

In a reference frame synchronous to the stator current vector, output voltage vector of inverter B, can be expressed as in equation 6.4,

$$\bar{v_B} = (v_{B,par} + jv_{B,quad})\frac{\bar{i_s}}{|\bar{i_s}|} \tag{6.4}$$

where $v_{B,par}$ and $v_{B,quad}$ respectively, are the parallel and orthogonal components of $\bar{v_B}$ with respect to $\bar{i_s}$

By neglecting losses of the inverter B, instantaneous active power exchanged by

the inverter B should be equal to the rate of change of electromagnetic energy stored in the floating capacitor C. This relationship can be mathematically expressed by equation 6.5

$$\frac{d}{dt}(\frac{1}{2}CE_B^2) = \frac{3}{2}\bar{i_s}.\bar{v_B} \tag{6.5}$$

"." in this context refers to the dot product meaning the sum of the products of corresponding d and q components of the first and second vector.

Now, in a reference frame synchronous to $\bar{i_s}$, one can deduce that equation 6.6 can be rewritten as given by following equation

$$\frac{d}{dt}(\frac{1}{2}CE_B^2) = \frac{3}{2}|\bar{i_s}|v_{B,par} \tag{6.6}$$

This leads to an interesting observation that the electromagnetic energy stored in the floating capacitor (and its voltage) is completely independent of $v_{B,quad}$ and depends solely on the parallel component $v_{B,par}$ with respect to $\bar{i_s}$. Furthermore, it implies that $v_{B,par}$ should be zero in steady state operation of the drive.

Principle of reactive power control

Expression for the reactive power injected by the inverter A (Q_A), can be expressed as in equation 6.7, where Q_S and Q_B denote reactive power of the PMSM and the inverter B respectively.

$$Q_A = \frac{3}{2}v_A.(j\bar{i_s}) = Q_S + Q_B \tag{6.7}$$

This implies the possibility to nullify the reactive power of inverter A by appropriately injecting or absorbing reactive power via inverter B. Combining equations 3.1 and 3.2 at steady state and by neglecting voltage drop due to stator resistance, equation 6.7 can be re-written as:

$$Q_A = \frac{3}{2}(j\omega\bar{\varphi_s}).(j\bar{i_s}) + \frac{3}{2}\bar{V_B}.(j\bar{i_s}) \tag{6.8}$$

Equating 6.8 to zero and considering 6.4, following expression can be obtained for the orthogonal component $v_{B,quad}$

$$v_{B,quad} = -\frac{\omega\bar{\varphi}_s.\bar{i_s}}{|\bar{i_s}|} \tag{6.9}$$

This mathematical expression which indicates the condition for zero reactive power injection by the inverter A, is completely independent of $v_{B,par}$ and solely depends on $v_{B,quad}$, the orthogonal component of inverter B voltage vector with respect to stator current vector $\bar{i_s}$. In a control point of view, this result confirms feasibility of controlling the reactive power of inverter A by controlling $v_{B,quad}$ of inverter B.

Control of floating capacitor voltage

In the control system shown in Figure 6-2, reference for E_B is given by the equation,

$$E_{B,ref} = \sqrt{3}k_m|v_{B,quad,opt}| \tag{6.10}$$

where $|v_{B,quad,opt}|$ is the optimum value for $v_{B,quad}$ to nullify reactive power of inverter A computed based on equation 6.9. k_m is the transient voltage margin, a constant greater than 1 incorporated in order to provide sufficient voltage margin for drive operation considering the transient voltage terms in equation 6.5. In this driver implementation, a value of 1.35 was used for k_m. Reference calculated by equation 6.10 is limited within minimum and maximum values for E_B tabulated in Table 6.1. A proportional controller (indicated as (e)) with a proportional gain of 0.001 is used in this driver design. Output of the regulator $v_{B,par,req}$ is limited within the maximum limit $V_{B,max}$ given by equation 6.2 based on instantaneous value of E_B. Reference for $v_{B,par}$ after applying saturation logics has been denoted as $v_{B,par,ref}$ in Figure 6-2.

Control of reactive power

Reactive power computer computes instantaneous reactive power delivery Q_A by the inverter A. This is compared against the reactive power reference $Q_{A,ref}$ (which is maintained at zero for our control purpose). Reactive power regulator (indicated

by (f)) in the control system accepts reactive power error as the input and outputs $v_{B,quad,req}$ as the output. $v_{B,quad,opt}$ is added to this output as a feed-forward term in order to improve the dynamic performance of the control system. $v_{B,quad,req}$ is limited within the maximum limit given by following equation.

$$v_{B,quad,max} = \sqrt{V_{B,max}^2 - (v_{B,par})^2} \tag{6.11}$$

In this control design, priority for utilization of floating capacitor voltage E_B is given to the voltage regulator rather than to the reactive power regulator. References calculated in stator current reference frame are finally transformed into corresponding references expressed in common d-q reference frame before they are being fed as inputs to the modulator for inverter B.

Chapter 7

Laboratory Experiments

This chapter presents the work carried out in implementing the single inverter based and dual inverter based speed control system designs presented in Chapter 5 and 6 respectively. Chapter contains explanations on the experimental setup, control software development and sequential implementation steps of the respective control systems along with experimental results acquired for different test cases.

7.1 Experimental setup

Experimental setup used in this series of experiments is shown in Fig.7-1. Main components of the setup are OEW-SPMSM, controller, inverter stack, DC power source for the inverter stack, DC power supply for secondary systems in the inverter stack, computer and oscilloscope. In Figure 7-1, these components have been numbered from 1 to 7 in sequential order.

OEW-SPMSM

A closer view of the OEW-SPMSM for which the control systems have been designed, is shown in Fig.7-2a. Specifications of this low power OEW-SPMSM were already presented in Table 1.1. This prototype allows access to either ends of the three phase stator windings, therefore it is possible to configure it either in open end winding configuration or in conventional configuration where the stator windings are connected

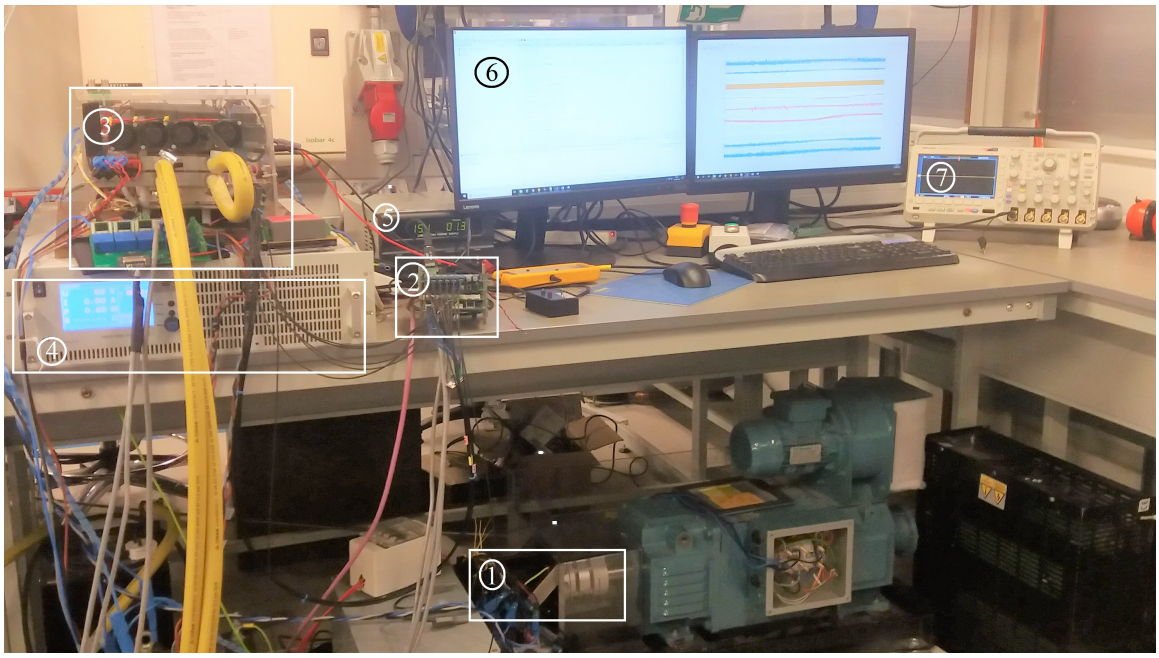


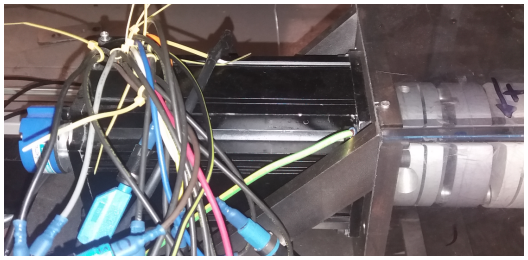
Figure 7-1: Experimental setup

in star.

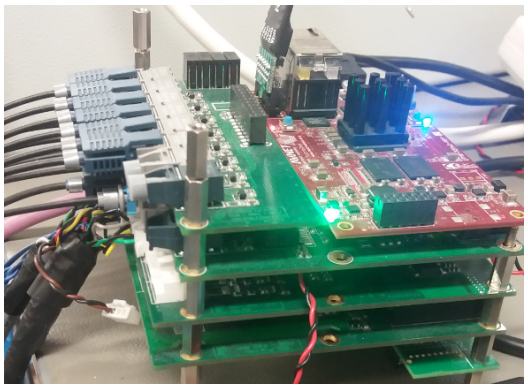
Controller

Fig. 7-2b shows a closer view of the control platform. It is a custom made, research oriented control board developed at the UoN named *uCube*. The control platform is based on off-the-shelf Microzed board from Avnet which is a low cost development board based on Xilinx Zynq-7000 All Programmable System on Chip (SoC)[2]. The Zynq is a heterogeneous SoC that consists of a dual-core ARM CortexA9 based Processing System (PS) and a Field Programmable Gate Array (FPGA) Programmable Logic (PL) in a single device. Detailed explanations on the design of the control platform and its software architecture can be found in [16]

Gate signal commands from the control platform are communicated to the inverter gate driver system via optical fibre links. Analogue-to-Digital Converters expansion board of the *uCube* receives current and voltage measurements from the inverter stack through wired sensor connections.



(a) SPMSM prototype



(b) uCube control platform

Figure 7-2: Closer views of the SPMSM and uCube

Inverter stack

Inverter stack (numbered 3 in Figure 7-1) contains three inverter modules. All of them are standard two-level three phase inverter modules with associated capacitor banks. Module 0 is based on SiC IGBTs whereas Module 1 and 2 are based on Si IGBTs. The stack also contains associated gate driver systems, liquid and air cooling systems, voltage and current sensing and signal conditioning circuitry.

DC power supplies

Controlled voltage source (numbered 4 in Figure 7-1) is used as the power source for the inverter modules. DC power supply numbered 5 in the same figure is operated at 15V to energize the gate driver system, air cooling system and associated sensing circuitry in the inverter stack.

Computer

Computer is connected to the *uCube* via two communication links. One of them is used to program the controller while the other is used to issue commands to the *uCube* in run-time and to acquire data written to data buffers of the *uCube*

Control software in this implementation were programmed in C programming language using Xilinx Software Development Kit (XSDK) (version 2017.4) [3]. Commands to the *uCube* are issued through Matlab console with the aid of custom made

Matlab functions developed as a part of the *uCube* control platform development process.

7.2 Implementation of single inverter based speed control system

The single inverter based speed control system in this study is designed to be operated with a three level NPC inverter. However, at the time of experiments, the three level NPC inverter within the facilities of PEMC was unavailable for this series of experiments. Therefore the speed control system was implemented employing standard two level SiC IGBT module in the inverter stack considering the fact that inverter topology has little impact on testing the speed control system. Secondary access terminals of three phase windings of the SPMSM were connected in star in order to convert it into a conventional SPMSM for this series of experiments.

7.2.1 Control software development

The field oriented vector controller design presented in Chapter 5 needs to be programmed in C programming language in order to implement within the *uCube* control platform. Therefore, the controller design initially implemented in Simulink (using Simulink block elements) for simulation purposes was re-implemented in C programming language. Effectiveness of developed C code was verified in Simulink by replacing previously implemented control system with the the control system implemented in **C** programming language. Simulink block ***S-Function*** with an associated **C++** script was used to interface developed C code with the remaining system (i.e. power electronics and the machine)

Code structure

Developed C code consists of following files. Code files have been excluded in this report considering the space limitations.

- **constant_defs.h**

This header file defines all the constants used in the controller including, but not limited to, machine parameters, controller gains and inverter switching frequencies.

- **StructComponents.h**

C language structures for holding *abc*, $dq0$ and $\alpha\beta0$ components of currents and voltages are introduced in this header file

- **clark_park_transforms.c and clark_park_transforms.h**

This c file with its associated header file introduces functions for calculating Clark, Park transformations and their respective inverse transformations.

- **FOC.c and FOC.h**

Vector control system is mainly implemented within the file FOC.c. It contains two main functions, one for initializing the controller and the other to perform control actions. The function that is responsible for controlling the machine receives stator currents, rotor speed, DC link voltage of the inverter and speed reference as inputs and outputs *abc* voltage references for the two level inverter.

7.2.2 Implementation procedure

This section explains the steps involved in implementing the control system.

Initial system settings

As the first step in control implementation, settings associated with the *uCube* control platform were declared within the project created in XSDK. Some of the main settings are as following;
Switching frequency of the inverter was set to 10kHz and *uCube* Interrupt Servive Routine (ISR) that reads sensor signals and calls the vector control function was set to operate at twice the inverter switching frequency.
As a protection measure, a trip threshold of 15A was introduced for stator currents allowing a sufficient margin for transient current overshoots (note that the rated current of the machine is 13A). This setting immediately terminates inverter switching operations in case of a fault current detection in the system exceeding the trip threshold.

Integration of developed C code to the XSDK project

C code files developed and verified for satisfactory operation were then appropriately integrated to the XSDK project. This step also involved declarations involving communications (commands from Matlab console and acquisitions) between the *uCube* and the controller.

Introduction of signal adaptation statements

C statements to convert ADC readings of stator currents, DC link voltage and rotor position feedback signal into their real world values were introduced based on corresponding current and voltage sensor calibration data.

Field orientation error correction of the stator position feedback

In order to properly implement a motor drive system for a PMSM based on field oriented vector control philosophy, it is important that the positions feedback from the encoder is properly adjusted for field orientation. In the case of a PMSM, this implies that electrical angle given by the position feedback must be read as 0 when d

axis of the stator $dq0$ system is aligned with the excitation field of rotor permanent magnet field. Any value read other than zero can be termed as a field orientation error. Following steps were followed in an attempt to obtain an estimation of the field orientation error of the encoder position feedback.

Firstly, rotor electrical angle position sent to the control system was overridden to zero. Thereafter, while allowing the rotor to move freely, *uCube* was commanded to establish a finite d axis current (5A) and zero q axis current in the stator. This makes the rotor field to magnetically align with the d axis of the stator current. Non zero value read for the electrical angle given by the encoder in this configuration was acquired and this was used to correct the field orientation error of the position feedback.

Implementation of current control loops

As outlined in Chapter 5, designed vector control system consists of inner stator current control loops and outer control loops that generate current references. Current control loops were implemented first, by disabling outer control loops and manually commanding the d,q current references. This step also involved attempts to fine-tune controller gains.

Both d and q current controllers were tested for satisfactory tuning. Response of i_d controller for a step reference change from 0A to 8A has been shown in Figure 7-3. Similar response was observed for the q axis current control for a step reference change.

Implementation of speed control loop

After verifying satisfactory performance of the current controllers, speed control loop was implemented so that it will generate reference for i_q. In this step, reference for i_d was manually commanded to zero. PI parameters of the speed controller were tuned to obtain a satisfactory and stable system performance.

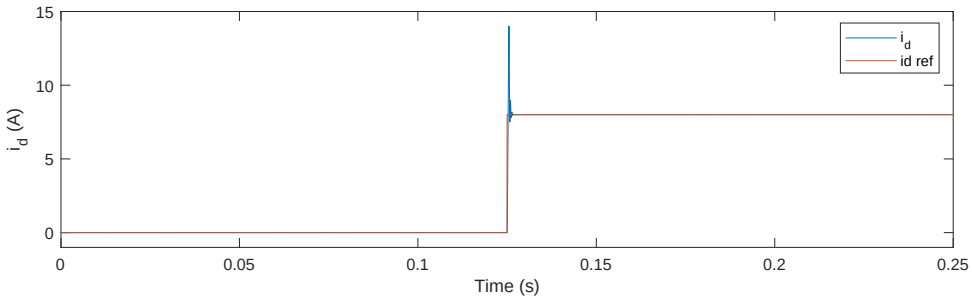


Figure 7-3: d axis current response for a step reference change

Implementation of flux weakening control loop

As the final step, flux weakening controller was implemented in order to generate reference for i_d. Gains of the controller were tuned in order to obtain a satisfactory performance of the machine in its operation within the flux weakening region.

7.2.3 Experimental results

Operation of the complete speed control system was tested for the entire speed range extending to flux weakening region. DC link voltage of the inverter was maintained at 80V in these tests.

Operation below flux weakening region

Figure 7-4 shows the response of the control system for a step speed reference change from 0 to 500rpm. The machine operates below flux weakening region under this loading condition at 500rpm, therefore id_{ref} remains at zero during the entire period, as anticipated. It can be observed how reference changes for i_q attempts to track the speed reference. abc stator currents have also been shown in the figure. Variation of DC link voltage under transient conditions corresponds to the transient power flows in the system and agrees with theoretical expectations.

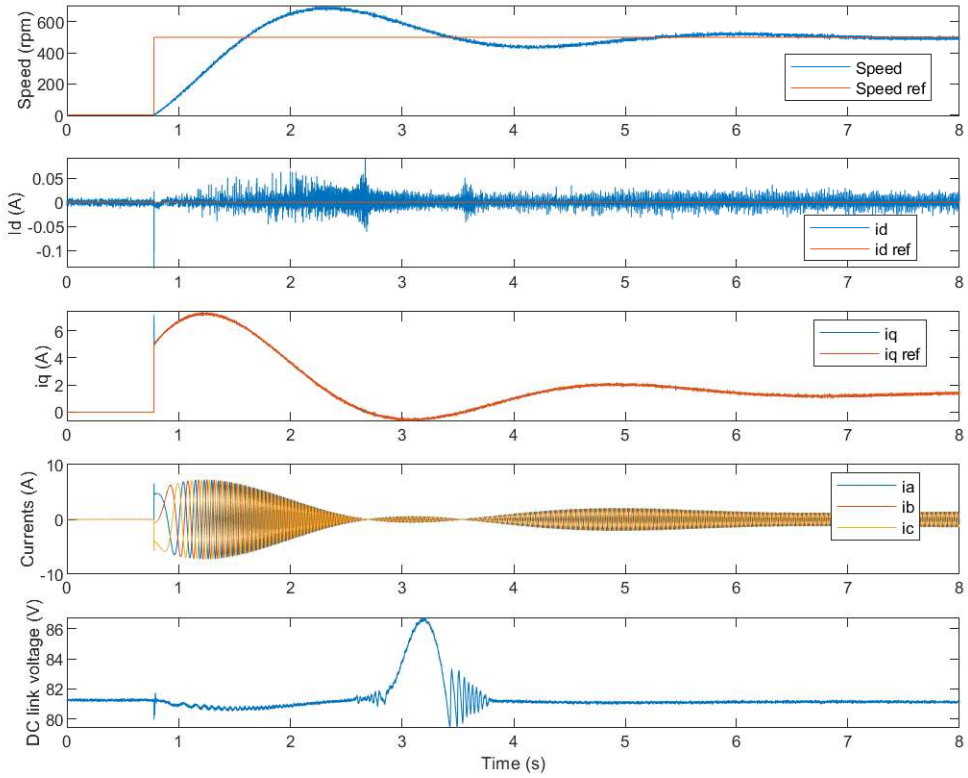


Figure 7-4: Performance of the control system for a step reference change in speed below flux weakening region

Operation in the flux weakening region

Figure 7-5 shows the response of the control system for a step reference change from 1500rpm to 1600rpm. At 1600rpm, machine has entered its flux weakening region with a steady state iq_{ref} of -3.7A in order to maintain stator terminal voltage within permissible limit.

Maximum speed range

Based on steady state iq current value, external load torque associated with the machine was estimated to be 0.58Nm (using equation 5.6). This corresponds to a theoretical maximum speed of approximately 2000rpm for the machine under these operating conditions. However, the maximum speed achievable with the implemented

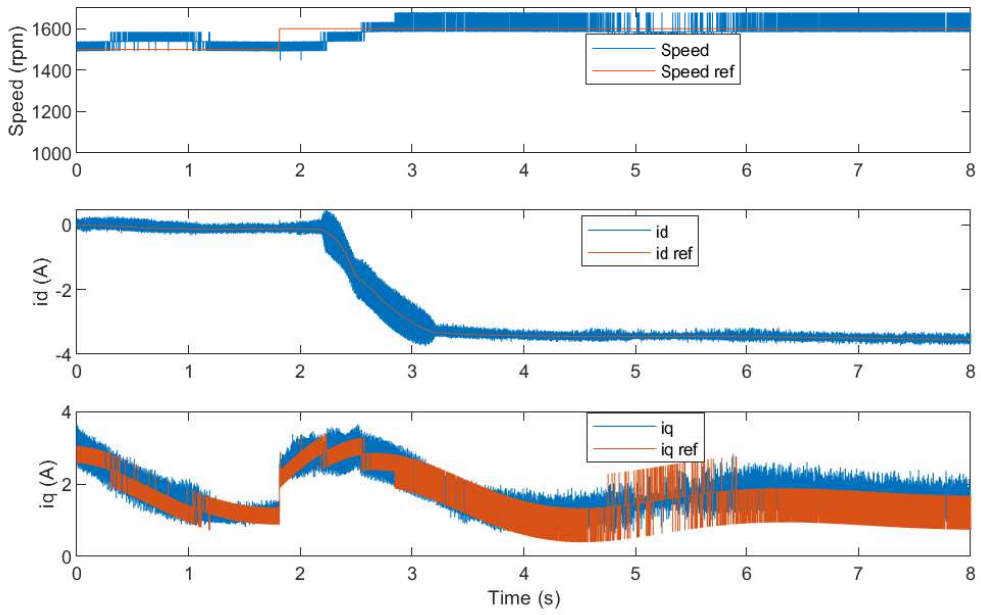


Figure 7-5: Performance of the control system for a step reference change in speed into the flux weakening region

control system was 1900rpm, a value which is sufficiently close to theoretically expected limit. Minor disagreement can be thought as a result of possible discrepancies in estimations for machine parameters from their actual values or possible measurement errors.

7.3 Implementation of dual inverter based speed control system with a floating capacitor bridge

Purpose of this series of experiments is to investigate the feasibility of implementing the dual inverter based speed control system with a floating capacitor bridge whose control philosophy was presented in Chapter 6. The SPMSM was reconfigured to its OEW configuration for these experiments. Module 0 of the inverter stack (two level SiC IGBT inverter module) was used as the inverter involving the floating capacitor (i.e inverter B) and Module 3 of the inverter stack (two level Si IGBT) was used as

the inverter A of the dual inverter system.

7.3.1 Control software development

Vector control system for the dual inverter drive can be thought as an extension of the vector controller implemented for the single inverter based motor drive. Controls for inverter A are essentially the same for this case, except additional feed-forward terms that account for inverter B voltage vectors. Controls for inverter B, in contrary to those of inverter A, are implemented in a reference frame synchronized with the stator current vector. C code for the control of the dual inverter system was developed, tested and verified adopting the same procedure outlined in section 7.2.1.

Code structure

The C code consists of all the files outlined in section 7.2.1. An additional file named **complexMath.c** along with its header file was developed and included to the code structure in order to implement the complex number arithmetic (that are related to reference frame transformations in the control system) in a less memory intensive manner.
Control system is mainly implemented within the file **FOC.c**. The core function of this code that performs the control operations related to inverter A and B is given in Appendix C

7.3.2 Implementation procedure

Initial system settings

Switching frequencies for both inverter A and B were set to 10kHz. In addition to safety trip thresholds for currents, a new trip threshold of 200V was introduced for inverter B capacitor voltage, since it is now dynamically controlled by the control system.

Verifying the operation of inverter A controls

First, the proper operation of current, speed and flux controllers associated with the inverter A was tested while using the inverter B to make a star connection in the SPMSM.

Implementation of floating capacitor bridge voltage control loop

Thereafter, the capacitor voltage regulator associated with the inverter B was enabled and tested for its proper operation. Response of the regulator at different operating points of the machine was observed and controller was tuned considering overall stability of the system.

Implementation of reactive power controller

As the final step, reactive power control loop associated with the inverter B was enabled and tuned for stable operation.

7.3.3 Experimental results

Voltage regulator transients

Response of the voltage regulator for a step capacitor voltage reference change from 20V to 160 is shown in Figure 7-6. Notice the change of $V_{B,par}$ that attempts to track the voltage reference. $V_{B,par}$ reference operates at its saturation limits at initial stages, while attempting to raise the capacitor voltage towards the reference.

Reactive power controller transients

In order to demonstrate the ability of the reactive power controller to compensate for inverter A reactive power via injection of reactive power though inverter B, following test was performed.

Speed of the machine was raised to 1600rpm while keeping the reactive power controller disabled. At this speed, machine operates in flux weakening region where

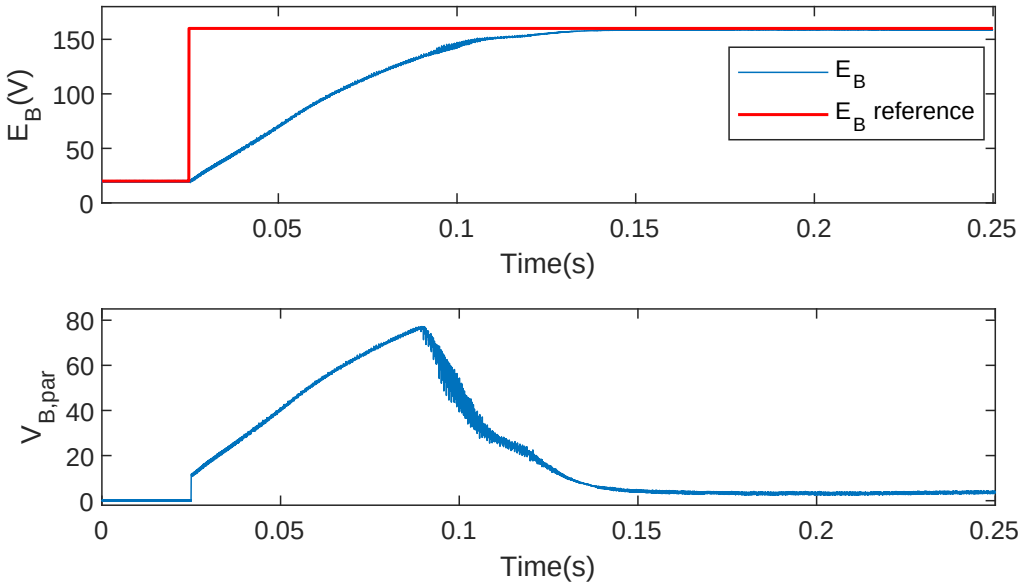


Figure 7-6: Performance of the voltage regulator for a step voltage reference change from 20V to 160V

inverter A has to inject approximately 500VAr of reactive power. At 0.025s, the reactive power controller was enabled and inverter A reactive power flow was observed. Results of this test is shown in Figure 7-7. It clearly indicates the ability of the inverter B to compensate for inverter A reactive power which is restored to the reference of 0VAr when the controller is active. Change in $V_{B,quad}$ under transients has also been shown in the same figure.

It is clearly evident that the controls for inverter B can successfully maintain a given capacitor voltage reference for inverter B and nullify the inverter A reactive power by adjusting the reactive power injection of inverter B.

7.4 Implementation of dual inverter drive with a common voltage source

Even though not directly related to the topology under consideration in this research, it is worth mentioning the following result obtained for the dual inverter drive topol-

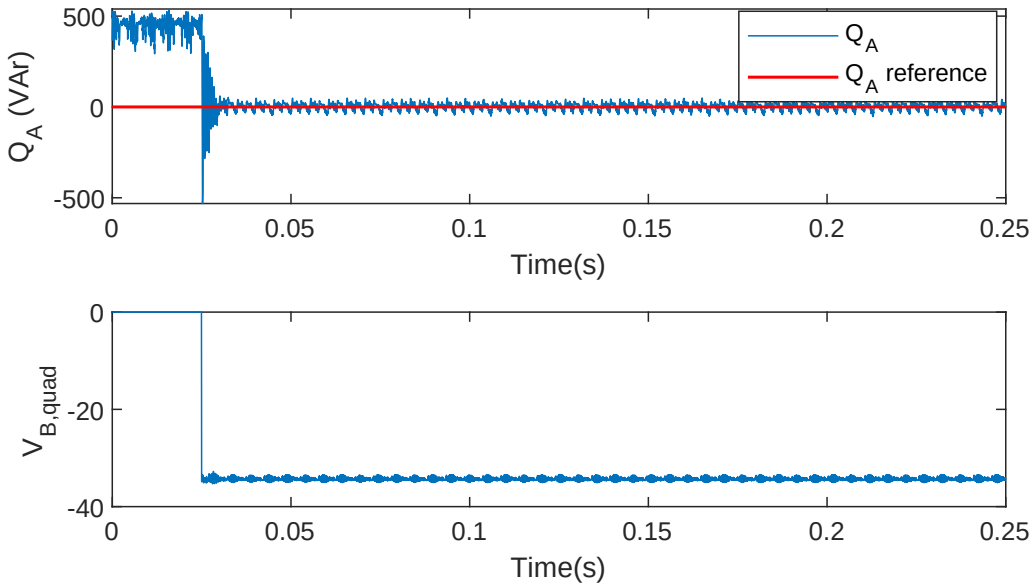


Figure 7-7: Performance of the reactive power controller

ogy with a shared DC link. As already outlined in Chapter 2, this configuration significantly reduces the cost of the motor drive. However, ZSC flow in the system is a serious flaw of this design, which demands sophisticated mechanisms to eliminate its presence.

7.4.1 Experimental procedure

DC links of the two IGBT modules in the inverter stack were configured to be parallel and were excited with 40V from the power supply. Control system implemented for the dual inverter drive with a floating capacitor bridge was used for this test excluding the voltage regulator. Speed and flux regulators were also disabled for simplicity and references for i_d and i_q were manually commanded to 0A and 1A respectively. Phase currents and the ZSC flow in the system were observed.

7.4.2 Experimental results

Phase currents and ZSC flow (I_0) in the system at this condition is shown in Figure 7-8. Note that phase currents are way away from their sinusoidal expectation, with a large ZSC component flowing in the system.

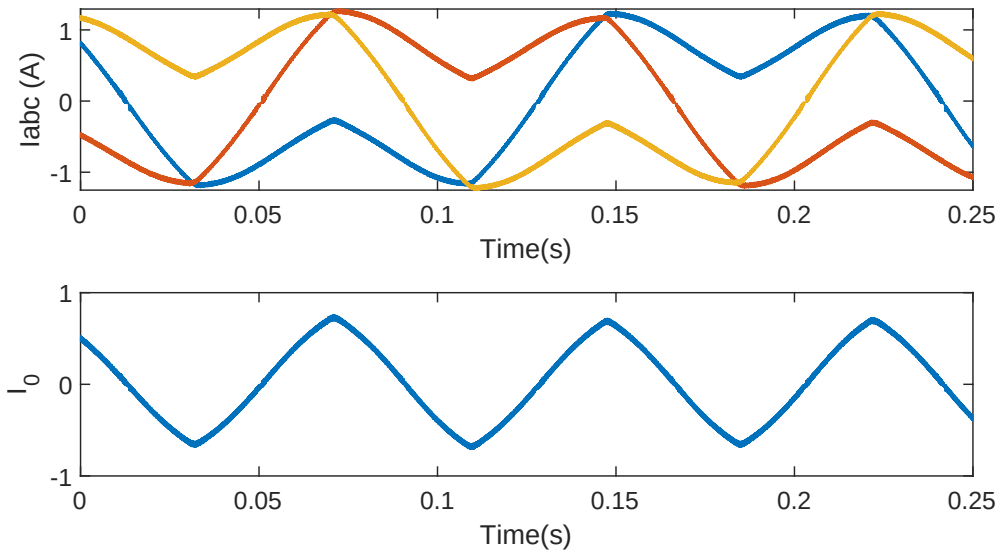


Figure 7-8: Zero-Sequence Current flow in dual inverter drive with shared DC links.

Chapter 8

Comparison of Drive Topologies

This chapter presents the results of the comparative analysis conducted on two drive topologies 5 and 6 respectively. Analysis presented in this chapter is based on the SPMSM whose specifications can be found in Table 1.1.

8.1 Speed range of the machine, limits of deliverable torque and mechanical power

The objective of this analysis is to investigate the maximum speed, the limit of electromechanical torque and mechanical power achievable by the machine under two drive topologies.

One possible approach to obtain the operating limits of a motor drive is to transform all the constraints (i.e current limit of the machine and voltage limits offered by the inverters) that limit the operating rage of the machine into a set of inequalities representing the admissible domain of stator currents in d-q reference via mathematical manipulations. This is a popular approach found in literature such as [6], [25] and [37] applied for different types of electrical machines.

8.1.1 Analysis based on admissible domain of stator currents

- **Three level NPC inverter drive**

For the three level NPC inverter motor drive, the constrains that limit the operating range of the machine are the stator current and inverter voltage constraint.

Current constraint can be written as,

$$\sqrt{i_{s,d}^2 + i_{s,q}^2} \leq I_{s,max} \tag{8.1}$$

This condition results in a circle in the d-q plane centred at the origin with a radius of $I_{s,max}$ which is 13A for the machine under consideration.

Voltage constraint can be written as,

$$\sqrt{v_{s,d}^2 + v_{s,q}^2} \leq V_{max} \tag{8.2}$$

where V_{max} is the maximum voltage that can be generated by the inverter. This relationship can be transformed into a corresponding limiting condition in d-q current plane by substituting for $v_{s,d}$ and $v_{s,q}$ from equation 3.1 and 3.2 , considering steady state operation of the machine (thus neglecting derivative terms) and disregarding the stator resistance. This leads to following inequality,

$$\left(\frac{|V_{max}|}{\omega L_s}\right)^2 \leq \left(i_{s,d} + \frac{\varphi_e}{L}\right)^2 + i_{s,q}^2 \tag{8.3}$$

In a geometric point of view, this represents a circle with a radius of $\frac{|V_{max}|}{\omega L_s}$ centred at$(-\frac{\varphi_e}{L_s}, 0)$ in d-q current plane.

- **Dual inverter drive with a floating capacitor bridge**

For the case of dual inverter drive, there are three constraints to be considered, viz. stator current constraint and voltage constraints of inverter A and inverter B.

Current constraint given by equation 8.1 remains unchanged since it is a limitation governed by the machine's thermal limit. Voltage constraints can be stated as,

$$\sqrt{v_{A,d}^2 + v_{A,q}^2} \leq V_{A,max} \tag{8.4}$$

$$\sqrt{v_{B,d}^2 + v_{B,q}^2} \leq V_{B,max} \tag{8.5}$$

These limitations can be transformed into limiting conditions expressed in d-q current plane under similar assumptions made for the case of single inverter drive. The expressions thus obtained are given in 8.6 and 8.7 respectively. [6]

$$\varphi_e \left| \frac{i_{sq}}{\bar{i_s}} \right| \leq \frac{V_{A,max}}{|\omega|} \tag{8.6}$$

$$\left| L_s |i_{s,q}| + \varphi_e \frac{i_{s,d}}{|\bar{i_s}|} \right| \leq \frac{V_{B,max}}{|\omega|} \tag{8.7}$$

Inequality 8.7 can be further rearranged as given in 8.8. In a geometric point of view, it represents a trajectory of a limaçon in d-q current plane.

$$\left[i_{s,d}^2 + i_{s,q}^2 - \left(-\frac{\varphi_e}{L_s} \right) i_{s,d}) \right]^2 \leq \left(\frac{V_{B,max}}{\omega L_s} \right) (i_{s,d}^2 + i_{s,q}^2) \tag{8.8}$$

The admissible domain of the stator current vector, resulting from above above formulations for single inverter drive and dual inverter drive at two speed levels of the machine (1800rpm and 2500rpm) are shown in Figure 8-1.

For the single inverter drive, admissible current vectors are those delimited by the circle with constant radius $I_{s,max}$ and the circle resulting from inverter voltage constraint given by 8.3. For the dual inverter drive, admissible current vectors are those within the regions bounded by the current limit and inverter A and B voltage constraints given by 8.6 and 8.8.

As clearly observable in the figure, the curves do change depending on the speed of the machine and so do the admissible domains of stator currents. Maximum torque that can be generated at a given speed can be obtained by finding the maximum value of i_q permissible subjected to constraints in the current plane.

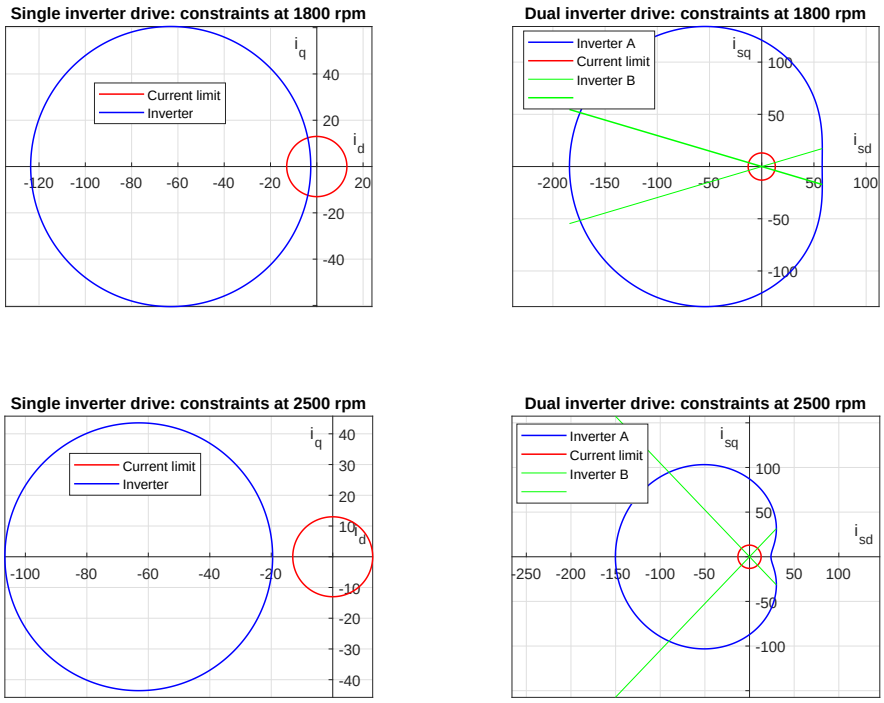


Figure 8-1: Representation of voltage and current constraints for single and dual inverter drives at 1800rpm and 2500rpm

It is worth noting that, at 2500rpm, the constraints in current plane drawn for the single inverter drive do not intersect each other. This corresponds to an infeasible operating point for the single inverter drive. Contrary to single inverter drive, we can observe the existence of a common area bounded by three limiting conditions for the dual inverter drive even at 2500rpm, which clearly demonstrates its ability to reach higher speeds compared to single inverter drive.

8.1.2 Analysis by formulating a maximization problem

Two algorithms have been proposed in this work in order to obtain the operating limits of the drive systems. These algorithms are based on modelling the drive systems and governing constraints as constrained multi-variable torque maximization problems.

Proposed algorithms are represented in the form of flow charts in Figure 8-2 and 8-3. These formulations are based on accurate complete system models without any simplified assumptions such as zero stator resistance. In fact, for the low power SPMSM that is considered in this discussion, negligence of stator resistance was found to result in significant errors in the estimations.

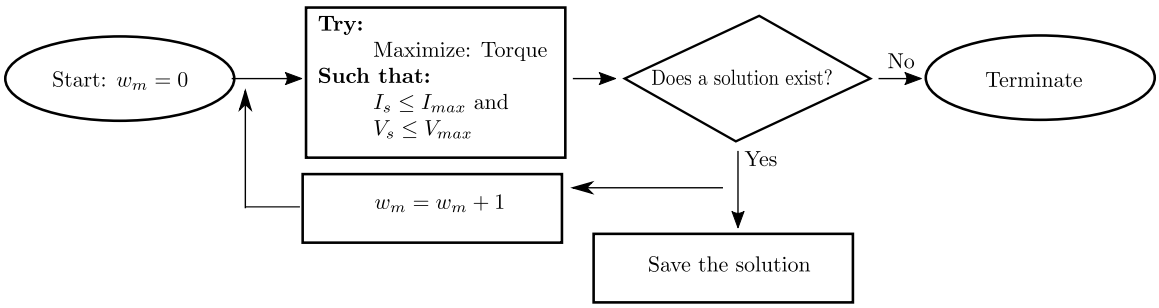


Figure 8-2: Proposed algorithm for obtaining operating limits of the single inverter drive

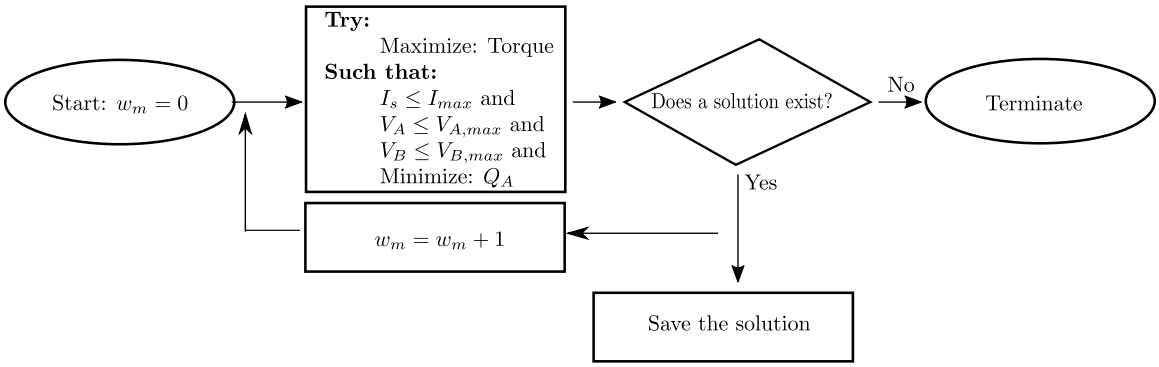


Figure 8-3: Proposed algorithm for obtaining operating limits of the dual inverter drive

For each drive, the system involving the PMSM and the inverters are modelled as a system of equations suitable for solving as a torque maximization problem at a given speed of the machine. Maximization problems for two drive systems are implemented using the ***fmincon*** non-linear programming solver in Matlab [4].[1] and are repetitively executed at incremental shaft speeds to obtain the operating points of the

[1]Note that Matlab based *fmincon* non-linear programming solver is in fact designed to find the

machine and the drive system. Exit-flag of the solver is used to identify the convergence state of the system, and the repetitive process for finding the operating points is terminated when the solver can no longer find a solution for the system of equations.

Limits of torque and mechanical output power deliverable by the machine under each of the drive topologies were obtained by using the above algorithm. Plot of the results are shown in Figure 8-4.

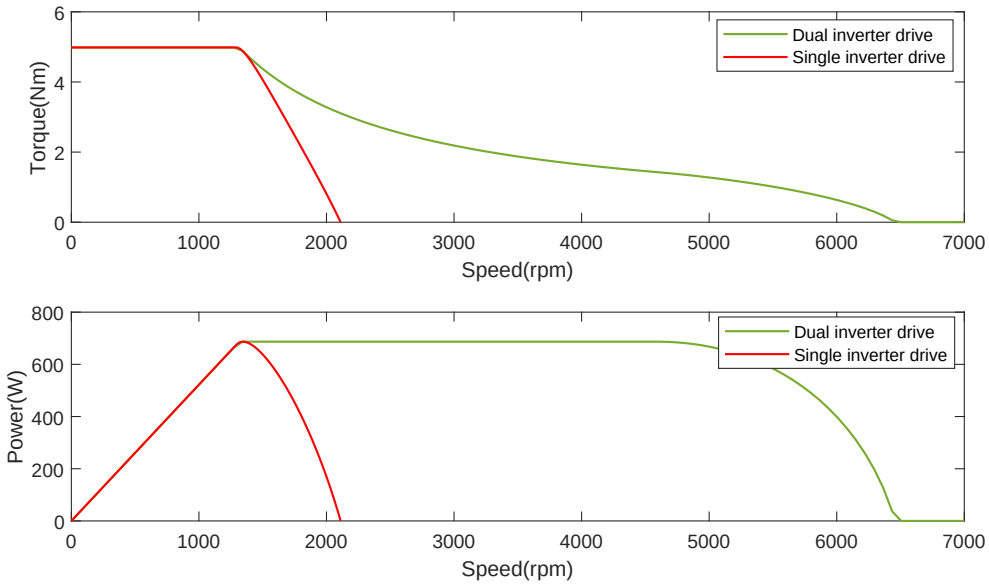


Figure 8-4: Torque and mechanical power limits for single inverter and dual inverter drives

We can clearly identify a substantial, threefold improvement in maximum speed range of the machine when driven by the dual inverter drive. This result agrees with the mathematical expression proposed in [6] for maximum speed ratios of the two drive topologies where it mathematically shows that ,

$$\frac{\omega_{max,DI}}{\omega_{max,SI}} = \frac{V_{B,max}}{V_{A,max}} + 1 \tag{8.9}$$

minimum of a constrained non-linear multi-variable function, therefore the problem was programmatically formulated to minimize the negative value of torque that is equivalent to maximizing the torque at a given speed reference.

where $\omega_{max,DI}$ and $\omega_{max,SI}$ respectively, refers to the maximum speed achievable by dual inverter and single inverter drive systems.

The maximum torque and the mechanical power deliverable by the machine has remained unchanged under both drive topologies, yet, we can identify that there is a considerable improvement in the constant power operating region of the machine in the case of the dual inverter drive.

8.2 Main inverter active and reactive power delivery

It is interesting to investigate the active and reactive power delivered by the inverter connected to the power supply and its power factor over feasible operating ranges. These information were also extracted by executing the algorithm explained in previous section. Results of this analysis are graphically presented in Figure 8-5.

- **Active power**

One can observe that the active power delivered by the main inverter (for both drive topologies) closely follow their corresponding graphs for mechanical power output by the machine, yet with an offset corresponding to resistive losses associated with the machine.

- **Reactive power**

Behaviour of the reactive power injected by the main inverter over the speed range, and power factor are quite different among the two drive topologies. As identifiable in the figure, inverter of the single inverter drive has to always inject or absorb reactive power in its operating range. And, most importantly when the machine operates in the flux weakening region its reactive power delivery exponentially increases with increasing speed and its power factor drops to a significantly low value.

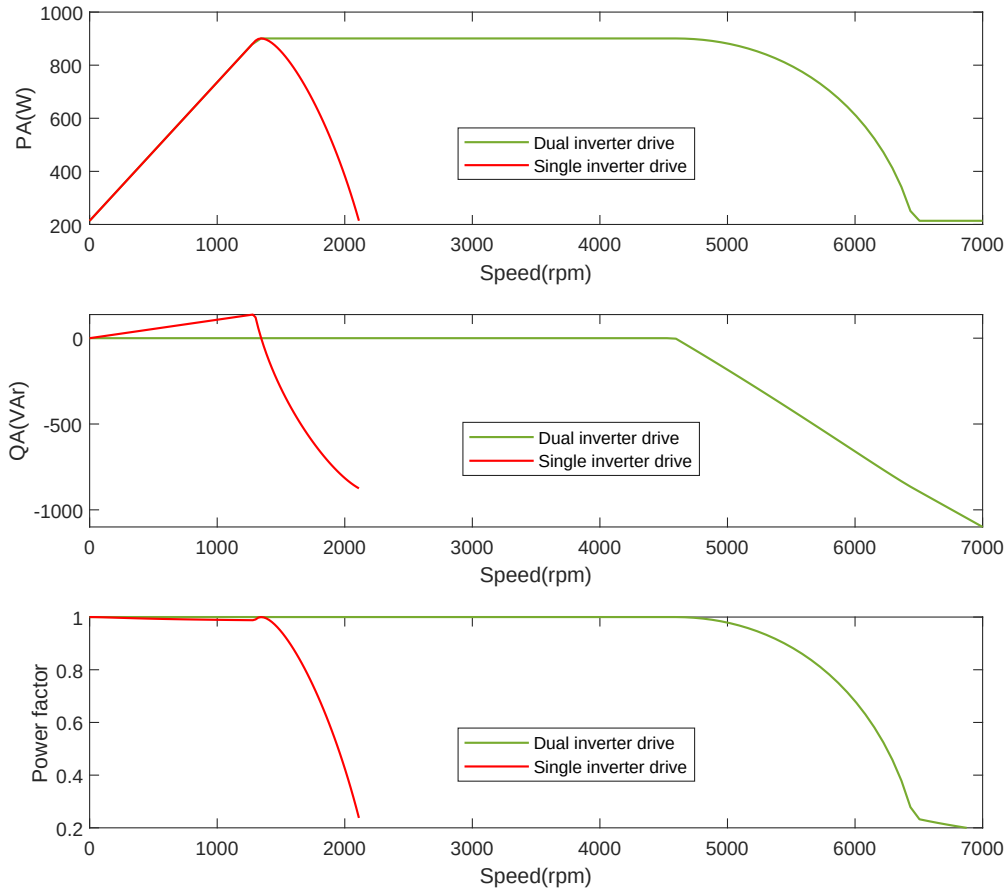


Figure 8-5: Main inverter active-reactive power delivery and power factor

In contrast, we can notice that the main inverter of the dual inverter drive (inverter A) operates at unity power factor during most of its operating range with zero reactive power delivery. This is a result of the reactive power compensation provided by the inverter B which is the main reason for extended speed range of the dual inverter drive. At higher speeds, however, the reactive power compensation capability of the inverter B gets limited by its DC link voltage limit and the inverter A has to inevitably inject reactive power to further increase the speed of operation, therefore lowering its power factor.

8.3 THD of stator current

8.3.1 Overview

THD of the stator current is an important aspect to consider in a motor drive application. Main causes for stator current harmonics are inverter switching, inverter non-linearities and spatial harmonics of the machine [28]. High switching frequencies generally result in lower THD in stator currents [15]. Furthermore, technological advancements in power electronic devices such such as SiC power devices allow high frequency switching [15] for motor drive applications. However, selection of an optimal switching frequency for a motor drive application is a multi-variable optimization problem that must also address the effects of switching frequency on losses associated with the machine end the motor drive. Such a study conducted on a SPMSM can be found in [32].

Lower level of THD in stator currents result in reduced magnetic saturation in the stator, reduced losses in the machine and low ripple in the torque generated by the machine. Even though harmonic currents have little effect on the average torque, it badly affects the torque ripples in the machine [39]. Therefore, it is interesting to investigate how THD of stator currents vary under two drive topologies.

The main objective of this study is to compare the single inverter motor drive based on the three level NPC inverter against the dual inverter drive. However, it is interesting to observe how stator current THD changes between a single inverter drive based on a two level inverter and dual inverter drive, noting the fact that dual inverter drive is made up of two, two-level inverters.

8.3.2 Simulation procedure

Investigation was carried out at three torque levels viz. 1.5Nm, 3.0Nm and 4.5Nm with the aim of having an overall view of the THD behaviour over the entire oper-

ating range of the drives. (The maximum torque limit of this SPMSM is 4.9Nm). Simulations were run in Simulink, for the three drive topologies in speed steps of 100rpm up-to maximum possible speed at respective torque level under each of the drive topologies. Stator current waveforms were obtained, all at electrical steady state and at a switching frequency of 10kHz. Waveforms were recorded and THD of stator currents were obtained using FFT tool in Simulink.

8.3.3 Simulation results and analysis

Results of this analysis are graphically shown in Figure 8-6

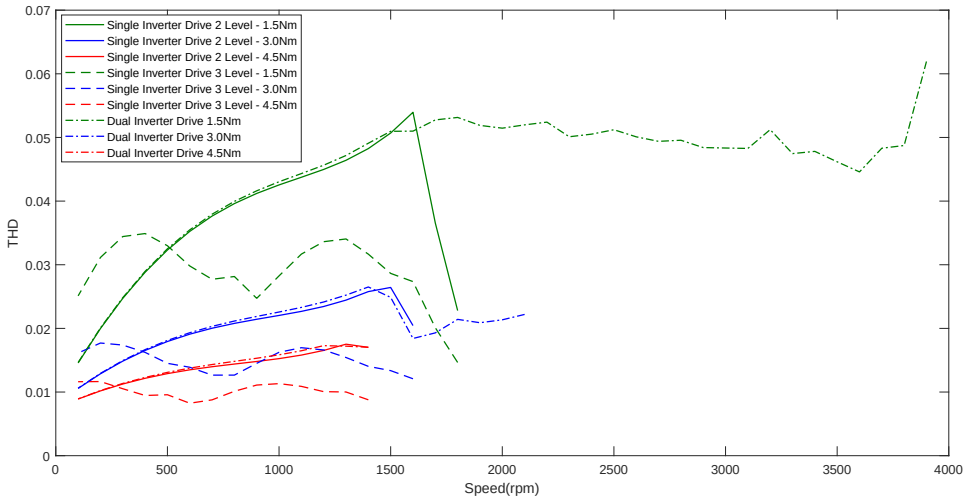


Figure 8-6: THD of stator current

These results can be better visualized by representing them in THD contour maps. THD contour maps generated for three level NPC inverter drive and the dual inverter drive are shown in Figure 8-7 . A differential THD contour map, that indicates the difference in THD of the two drives for their common operating range has also been included in the same figure.

In general, for all drive topologies, higher torque levels result in lesser THD in stator current. This can be explained by considering the results obtained for voltage harmonics produced by the two level and three level NPC inverters shown in Figure

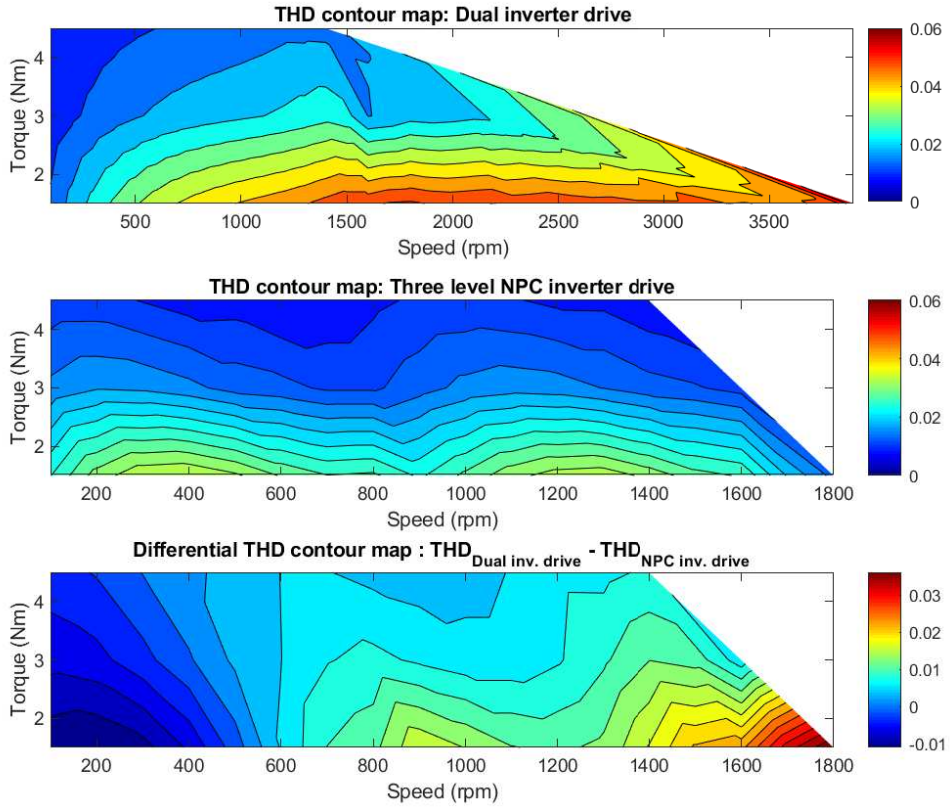


Figure 8-7: THD of stator current: contour map representation

4-11. It was identified that both inverters produce lesser voltage harmonics at higher modulation indices. Therefore, it is logical to expect lesser harmonics in stator current at higher torque levels, since the inverters have to operate at high modulation indices at the same speed of the machine but at higher torque levels.

At any given torque level, the drive based on three level NPC inverter is found to exhibit the best performance in terms of stator current THD, except at low speeds. This is again explainable with reference to the results presented in the same Figure 4-11, where it was observed that a three level NPC inverter, indeed, produces higher voltage harmonics at lower modulation indices compared to a two level inverter.

Another observation is that THD of stator currents produced by the dual inverter drive is slightly higher compared to that of the drive based on a single two-level

inverter. In [38], authors have investigated this effect in a different approach where they have explained it as a result of the fact that output voltage vectors of the two inverters in dual inverter drive are orthogonal to each other at steady state.

8.4 Efficiency analysis

This section presents the efficiency analysis conducted on two drive topologies.

8.4.1 Overview

Increased demand for energy efficient appliances has in turn resulted in increased research interest in all fields of engineering to optimize the designs in both functional and efficiency aspects. In industrial applications involving electrical machines, efficiency of the overall system not only depends on the electrical machine itself, but also on the associated motor drive. There has been much research addressing energy efficiency of electrical machines in the recent past. [8] and [14] are two such studies that exclusively focus on energy efficiency of PMSMs.

8.4.2 Losses in the system and definition for efficiency

Switching losses and conduction losses are the main losses associated with a power electronic system. Losses due to leakage currents, which are technically termed as blocking losses are insignificantly negligible and can be safely neglected in a practical efficiency assessment[5]. Switching losses can be further classified as turn on losses and turn off losses.

Dual inverter drive consists of 12 power electronic switches in total, six each for inverter A and B. Three level NPC inverter drive consists of 12 power electronic switches and additional 6 clamping diodes which incur losses in its operation.

Efficiency of the drive systems in this analysis is defined as the ratio of output power ($P_{out,drive}$) from the drive to the input power (P_{in}) given by equation 8.10

$$\eta = \frac{P_{out,drive}}{P_{in}} = \frac{P_{in} + Losses}{P_{in}} = 1 - \frac{P_{sw} + P_{cond}}{P_{DC}} \tag{8.10}$$

where input power to the drive system P_{in} is equal to the power delivered by the DC link P_{DC}. P_{cond} and P_{sw} respectively, refer to the sum of conduction losses and switching losses of all the power electronic elements involved in the drive.

8.4.3 Thermal modelling of the motor drives

Efficiency of the motor drives were assessed by modelling the power electronic elements of the drive systems in PLECS blockset. PLECS is a powerful software package that facilitates electrical, thermal, magnetic and mechanical modelling and simulation of dynamic systems. Its thermal modelling capabilities are employed in this study in conjunction with Matlab/Simulink. Control systems of the motor drives including modulation schemes were implemented in Simulink while PLECS was used to thermally model the system involving power electronics and the machine. Simulation models created in PLECS for the dual inverter drive and three level NPC inverter drive are shown in Figure 8-8 and 8-9 respectively.

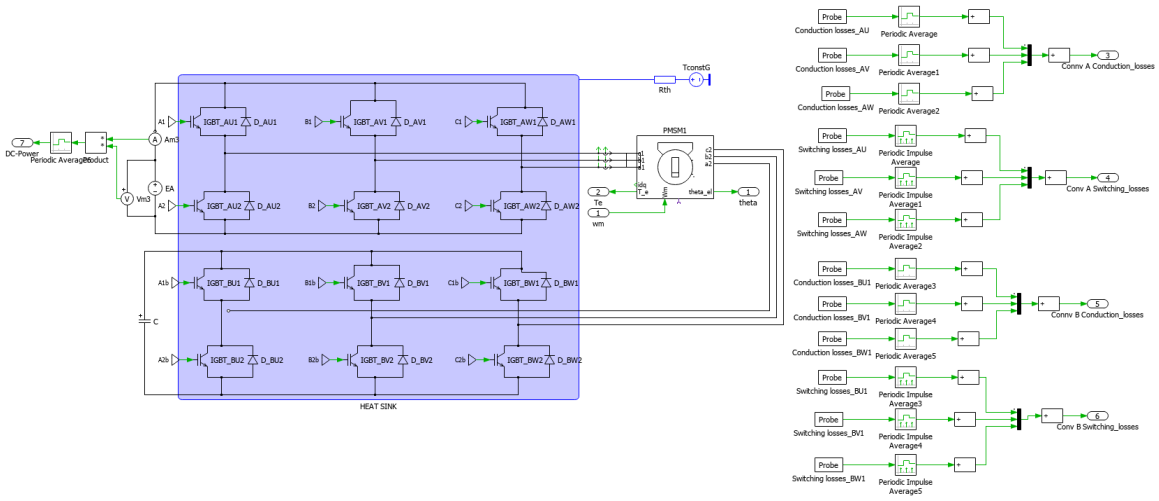


Figure 8-8: PLECS thermal model for dual inverter drive

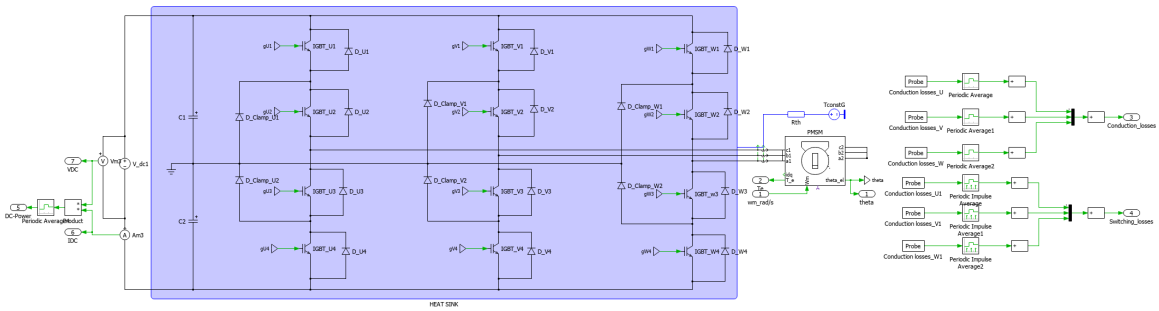


Figure 8-9: PLECS thermal model for three level NPC inverter drive

In order to explain the thermal modelling process in PLECS, it is important to explain the concept of *heat sink* and the techniques involved in estimation of conduction and switching losses.

Heat sink

Heat sink component of PLECS thermal library represents an idealized heat sink that absorbs the thermal losses dissipated by the components within its boundaries. In figures 8-8 and 8-9 heat sinks can be identified as transparent (light blue) boxes. A heat sink defines an isotherm environment and propagates its temperature to the components which it encloses. [5].

Calculation of conduction losses

Conduction losses in PLECS are calculated simply as the product of the device current and the device voltage. Device current is an online measurement variable in simulation time. Voltage across the device is assessed in PLECS by using the *thermal description* of the device that can be specified either as a function or a 2D look-up table. In this analysis, thermal descriptions of the selected devices were uploaded for loss calculations. 2D look-up table that is used for conduction loss calculation of IGBTs in three level NPC inverter drive is shown in Figure 8-10

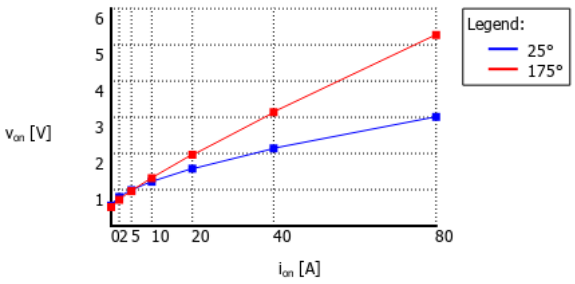


Figure 8-10: 2D look-up table for conduction loss calculation

Calculation of switching losses

PLECS adopts an efficient technique for calculation of switching losses where it uses thermal description of the device that specifies the energy dissipated in a switching event as a function of blocking voltage v_{block}, device junction temperature T_{junc} and the on state current i_{on} of the device as 3D look-up tables. 3D look-up tables specified as part of the thermal descriptions of three level NPC inverter drive IGBTs for calculation of turn-on and turn-off losses are shown in Figures 8-11a and 8-11b respectively. Loss functions can be mathematically represented as;

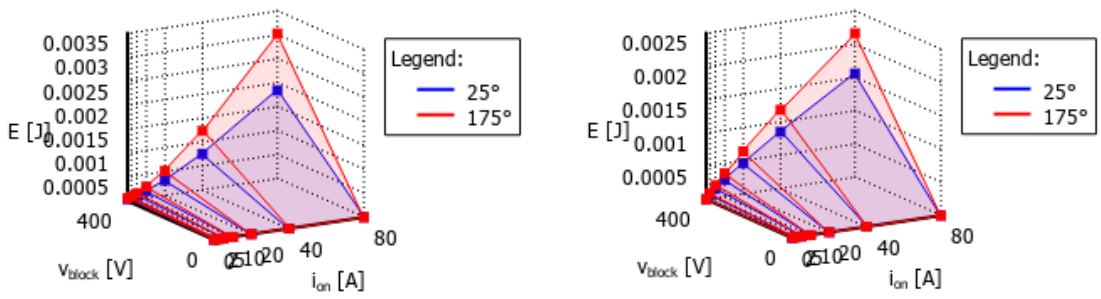
$$E_{on} = f(v_{block}, i_{on}, T_{junc}) \tag{8.11}$$

$$E_{off} = f(v_{block}, i_{on}, T_{junc}) \tag{8.12}$$

where E_{on} and E_{off} respectively refer to the losses associated with a switching on and off event of a given device.

Thermal and electrical stability concerns

Losses of the power semiconductor devices depend on the junction temperature. Therefore, in order to make sure that the measurements represent a realistic estimation of steady state losses, they have to be measured when the system is stable in both electrical and thermal viewpoints. Thermal stability of the system is assessed by monitoring the heat sink temperature and allowing it sufficient time to stabilize at its steady state value. Inverters of both topologies were operated at a switching



(a) 3D look-up table for turn-on loss calculation

(b) 3D lookup table for turn-off loss calculation

Figure 8-11: 3D look-up table for switching loss calculation

frequency of 10kHz in this analysis.

8.4.4 Simulation results and analysis

Plot of efficiency of the two drive topologies, assessed at three torque levels of operation viz. 1.5Nm, 3.0Nm and 4.5Nm is shown in Figure 8-12

A better visualization of drive efficiencies for their entire operating ranges can be

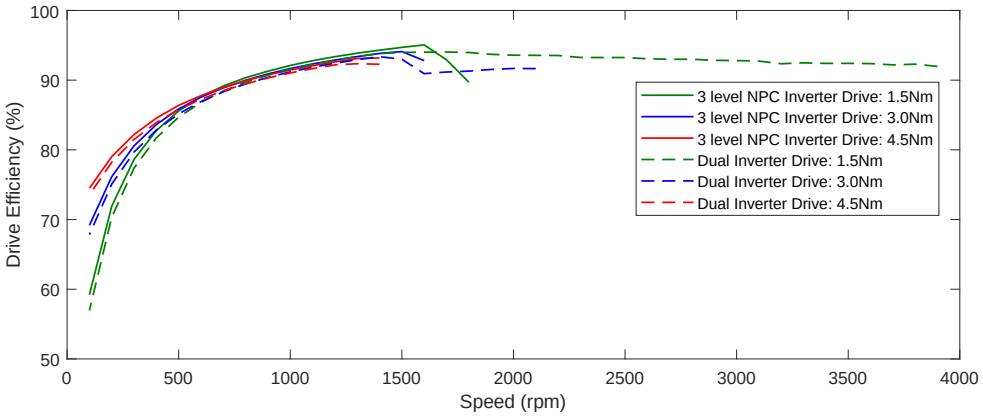


Figure 8-12: Efficiency of the two drive topologies assessed at three torque levels

obtained by representing the results in terms of efficiency maps. Efficiency maps for the two drive typologies are shown in Figure 8-13. A differential efficiency map has also been included in the same figure, which indicates the difference between the efficiencies of the dual inverter drive and the three level NPC inverter drive during their

common operating regions.

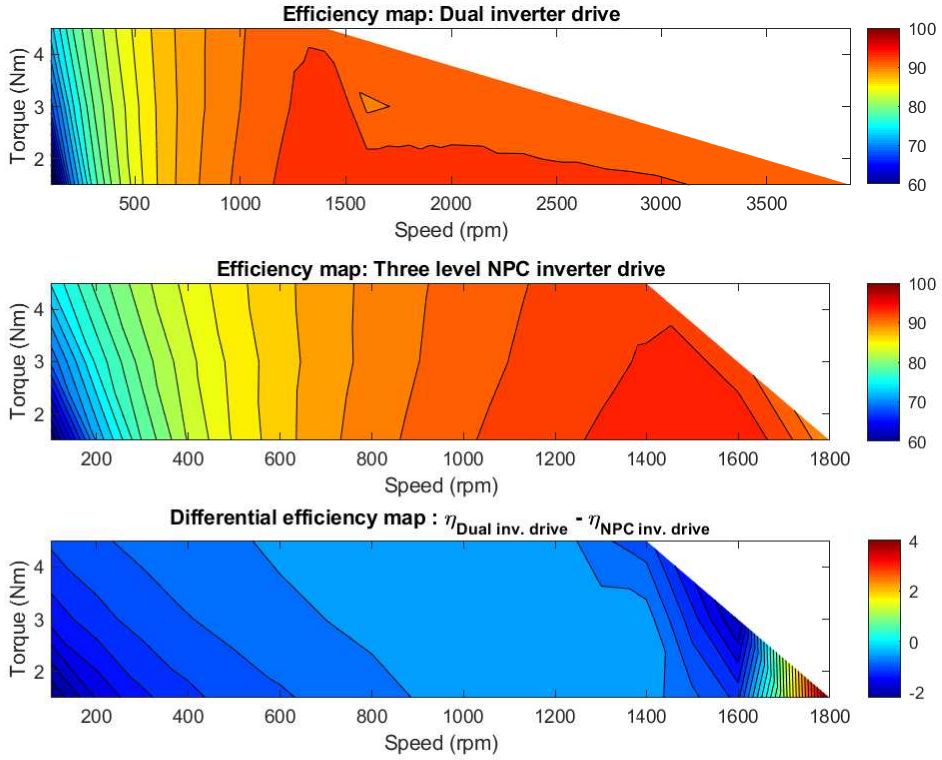


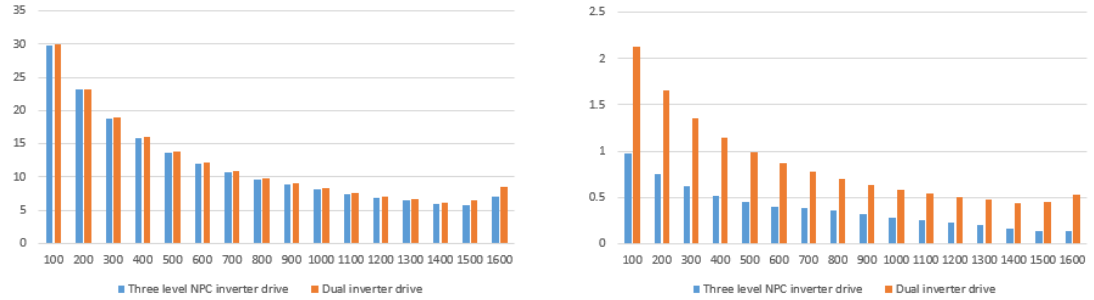
Figure 8-13: Efficiency maps

A. Observations

A common observation regarding the efficiency of both drive topologies is that they offer better efficiencies at higher torque-speed operating points. With reference to the differential efficiency map, it can also be observed that the drive based on NPC inverter is more efficient compared to its counterpart during most of their common operating points.

B. Split of losses between two drive topologies

It is worth investigating as to why the three level NPC inverter drive offers better performance in terms of efficiency. In order to understand this, the losses were spit



(a) Conduction losses as a percentage of input power

(b) Switching losses as a percentage of input power

Figure 8-14: Split of drive losses at 3.0Nm load torque

into conduction and switching loss components and were plotted as a percentage of input power at each of the operating points. Results of this split of losses obtained when the machine drives a load of 3.0Nm is shown in Figure 8-14.

1. **Conduction losses**

The split of conduction losses shown in Figure 8-14a indicates that, both drive topologies incur almost similar conduction losses. A careful observation, however, indicates that conduction losses of the three level NPC inverter drive are marginally less in all the operating points.

The comparability of conduction the losses under two drive topologies can be understood by considering the number of active devices contributing to conduction at a given moment of time. Through an analysis of conduction paths in two level and three level NPC inverters, it can be shown that, despite the NPC inverter contains a higher number of devices, both drive topologies will have equal number of power electronic devices (6 each) contributing for conduction at a given point of time. Conducting devices can either be IGBTs or diodes depending on the power factor of the load current.

2. **Switching losses**

Split of switching losses shown in Figure 8-14b indicates that the three level NPC inverter incurs substantially low switching losses at all the operating points. Being a

multi-level inverter, the devices of the three level NPC inverter experience exactly a half of the blocking voltage experienced by the devices of the inverter A of the dual inverter drive. Variable DC link control scheme adopted for the control of inverter B of the dual inverter drive can reduce the switching losses of it at lower speeds. However, floating capacitor voltage reference takes higher values at high speeds, therefore, dual inverter drive is likely to incur even more losses at higher speeds.

C. Split of losses between the Inverter A and Inverter B of dual inverter drive

For the completeness of this analysis, it is worth examining the split of losses between the Inverter A and Inverter B of the dual inverter drive.

1. **Conduction losses**

Split of losses between two inverters of the dual inverter drive as it drives a load of 3.0Nm at different speeds, is shown in Figure 8-15. The direct relationship between the losses and the stator current is clearly evident. An important observation is that, at all operating points, the inverter B incurs more losses, even though the current flow is identical for both inverters. The reactive power compensation function of the inverter B forces it to operate at zero power factor whereas the inverter A can operate at unity power factor for most of the operating points, leading to such a difference in losses even though current flows in two inverters are essentially identical in magnitude.

1. **Switching losses**

Split of switching losses between the two inverters and DC link voltages at each of the operating points are shown in Figure 8-16.

It clearly shows the effectiveness of variable DC link voltage control of inverter B on reducing its losses at lower speeds.

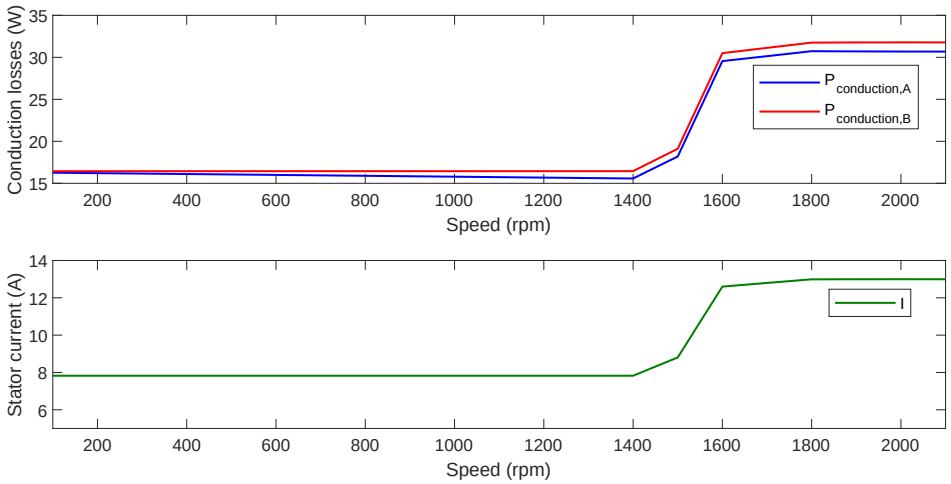


Figure 8-15: Dual inverter drive: split of conduction losses

8.5 Fault tolerant capability

Fault tolerant capability of the drive system is a significant consideration in safety critical applications [38]. This refers to the ability of the drive to continue its operation in the event of a possible failure in certain elements within the system.

The dual inverter drive with a floating capacitor bridge exhibits appreciable fault tolerant capability for faults involving inverter B. In case of failure of the floating capacitor or, one or more switches in the inverter B, there are certain combinations of switches that can be used to establish a star connection in the stator windings of the PMSM. This allows the drive to sustain the fault and continue to feed the machine though inverter A. Ability of the inverter B to make the stator star connection and maintaining continuity of operation of the machine through inverter A by suitably incorporating changes to the control system was experimentally validated in one of the laboratory experiments.

However, failure of any of the DC link capacitors or switching devices demands a drive based on a three level NPC inverter to cease its operation with immediate effect. There are certain three level NPC inverter topologies which are fault tolerant

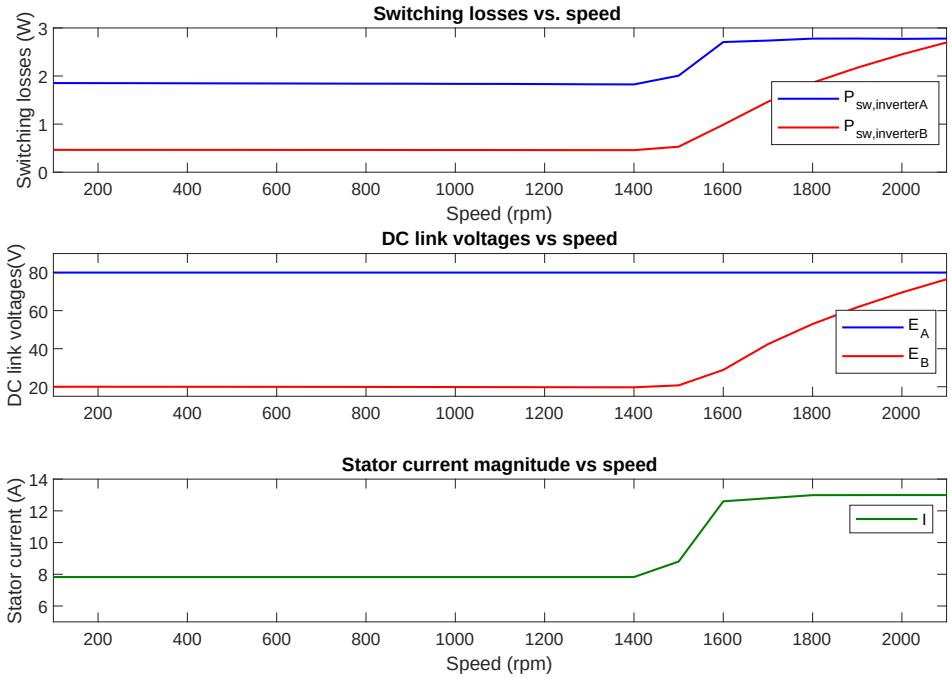


Figure 8-16: Dual inverter drive: split of switching losses

such as the one proposed in [9], but all of them come at extra power electronic devices added up, increasing the overall cost and complexity of such a motor drive.

Chapter 9

Conclusions and Future Work

9.1 Conclusions

A comprehensive performance evaluation between a three level NPC inverter based motor drive and a dual inverter motor drive with a floating capacitor bridge for SPMSM applications was conducted in this work. Analysis conducted via mathematical, thermal and electrical modelling of the two drive systems and simulation work as well as laboratory experiments to implement the control systems associated with the respective drive topologies, lead to interesting conclusions regarding the performance of the two drive topologies.

- The dual inverter drive with a floating capacitor bridge was found to be able to appreciably increase the constant power operating range of the machine and consequently the speed range by several times compared to a single inverter drive depending on the choice of floating capacitor voltage. Two algorithms were proposed to obtain the speed range of the machine under two drive topologies which were found to deliver comparable (and more accurate) results compared to simplified formulations available in literature.

- The drive based on three level NPC inverter was found to outperform the dual inverter drive with a floating capacitor bridge in terms of stator current THD in most of the operating points, obviously due to multi-level operation of such

a drive. Furthermore, performance of the dual inverter drive with a floating capacitor bridge, in this respect, was found even inferior (marginally) to that of a two level inverter drive due to additional constraints that prevent the inverters to exploit space vectors in an effective manner to produce multi-level voltage waveforms.

- Results of the efficiency analysis shows that, a drive based on three level NPC inverter offers a more efficient design compared to its counterpart despite the high number of power electronic elements in such an inverter.

- Dual inverter drive with a floating capacitor bridge presents a fault tolerant design with no additional complexity, a feature that is not supported by a drive based on a three level NPC inverter.

- As well experienced in experimental work, even though implementation of a single inverter drive is a straightforward task, maintaining stability of the controls of a dual inverter drive with floating capacitor bridge, specially at high speeds, is a complex task and requires advanced analysis techniques to tune the controllers.

9.2 Future work

The following list of future work was identified as promising possibilities for improvements to the work carried out in this research.

- The dual inverter drive with a floating capacitor bridge investigated in this research was found to exhibit considerably inferior performance in terms of THD indicators, despite the better performance expected from dual inverter drives in this respect. The control philosophy adopted in the study and those discussed in literature are based on independent modulators acting upon two inverters of the drive. It will be an interesting study to investigate the possibility to design a global modulator to issue coordinated switching commands for the

two inverters in the view of improving waveform quality whilst adhering to orthogonality constraint of the inverters' voltage vectors in steady state.

- Fault tolerant capability of a dual inverter drive with a floating capacitor bridge was much evident in experimental work, and its feasibility was examined through simple tests. However, fault tolerant capability improvements to this topology is a promising branch of study that can be focused in a future work.

- The performance of the speed control systems for single inverter and dual inverter drives implemented within laboratory experiments can be improved by employing advanced speed estimation techniques and by adopting a control theory based in-depth analysis to calculate the gains of the controllers.

- Simulation results obtained for three level NPC inverter drive can be experimentally validated and the effectiveness of implemented SVPWM modulation scheme can be tested in a future work.

Appendix A

Tables

Sector	Sub-sector	DC link status	Switching sequence
1	1	$V_{DC1} > V_{DC2}$	OOO-POO-PPO-POO-OOO
		$V_{DC2} > V_{DC1}$	NNN-ONN-OON-ONN-NNN
	2	$V_{DC1} > V_{DC2}$	POO-PPO-PON-PPO-POO
		$V_{DC2} > V_{DC1}$	ONN-OON-PON-OON-ONN
	3	$V_{DC1} > V_{DC2}$	POO-PON-PNN-PON-POO
		$V_{DC2} > V_{DC1}$	ONN-PNN-PON-PNN-ONN
	4	$V_{DC1} > V_{DC2}$	PPO-PPN-PON-PPN-PPO
		$V_{DC2} > V_{DC1}$	OON-PON-PPN-PON-OON
2	1	$V_{DC1} > V_{DC2}$	OOO-OPO-PPO-OPO-OOO
		$V_{DC2} > V_{DC1}$	NNN-NON-OON-NON-NNN
	2	$V_{DC1} > V_{DC2}$	PPO-OPO-OPN-OPO-PPO
		$V_{DC2} > V_{DC1}$	OON-NON-OPN-NON-OON
	3	$V_{DC1} > V_{DC2}$	PPO-PPN-OPN-PPN-PPO
		$V_{DC2} > V_{DC1}$	OON-OPN-PPN-OPN-OON
	4	$V_{DC1} > V_{DC2}$	OPO-OPN-NPN-OPN-OPO
		$V_{DC2} > V_{DC1}$	NON-NPN-OPN-NPN-NON
3	1	$V_{DC1} > V_{DC2}$	OOO-OPO-OPP-OPO-OOO
		$V_{DC2} > V_{DC1}$	NNN-NON-NOO-NON-NNN
	2	$V_{DC1} > V_{DC2}$	OPP-OPO-NPO-OPO-NOO
		$V_{DC2} > V_{DC1}$	NOO-NPO-NON-NPO-NOO
	3	$V_{DC1} > V_{DC2}$	OPO-NPO-NPN-NPO-OPO
		$V_{DC2} > V_{DC1}$	NON-NPN-NPO-NPN-NON
	4	$V_{DC1} > V_{DC2}$	OPP-NPP-NPO-NPP-OPP
		$V_{DC2} > V_{DC1}$	NOO-NPO-NPP-NPO-NOO
4	1	$V_{DC1} > V_{DC2}$	OOO-OOP-OPP-OOP-OOO
		$V_{DC2} > V_{DC1}$	NNN-NNO-NOO-NNO-NNN
	2	$V_{DC1} > V_{DC2}$	OOP-OPP-NOP-OPP-OOP
		$V_{DC2} > V_{DC1}$	NNO-NOO-NOP-NOO-NNO
	3	$V_{DC1} > V_{DC2}$	OPP-NPP-NOP-NPP-OPP
		$V_{DC2} > V_{DC1}$	NOO-NOP-NPP-NOP-NOO
	4	$V_{DC1} > V_{DC2}$	OOP-NOP-NNP-NOP-OOP
		$V_{DC2} > V_{DC1}$	NNO-NNP-NOP-NP-NNO
5	1	$V_{DC1} > V_{DC2}$	OOO-OOP-POP-OOP-OOO
		$V_{DC2} > V_{DC1}$	NNN-NNO-ONO-NNO-NNN
	2	$V_{DC1} > V_{DC2}$	OOP-POP-ONP-POP-OOP
		$V_{DC2} > V_{DC1}$	NNO-ONO-ONP-ONO-NNO
	3	$V_{DC1} > V_{DC2}$	OOP-ONP-NNP-ONP-OOP
		$V_{DC2} > V_{DC1}$	NNO-NNP-ONP-NNP-NNO
	4	$V_{DC1} > V_{DC2}$	POP-PNP-ONP-PNP-POP
		$V_{DC2} > V_{DC1}$	ONO-ONP-PNP-ONP-ONO
6	1	$V_{DC1} > V_{DC2}$	OOP-POO-POP-POO-OOP
		$V_{DC2} > V_{DC1}$	NNN-ONN-ONO-ONN-NNN
	2	$V_{DC1} > V_{DC2}$	POP-POO-PNO-POO-POP
		$V_{DC2} > V_{DC1}$	ONO-ONN-PNO-ONN-ONO
	3	$V_{DC1} > V_{DC2}$	POP-PNP-PNO-PNP-POP
		$V_{DC2} > V_{DC1}$	ONO-PNO-PNP-PNO-ONO
	4	$V_{DC1} > V_{DC2}$	POO-PNO-PNN-PNO-POO
		$V_{DC2} > V_{DC1}$	ONN-PNN-PNO-PNN-ONN

Table A.1: Three level NPC inverter SVPWM switching sequences

Appendix B

Figures

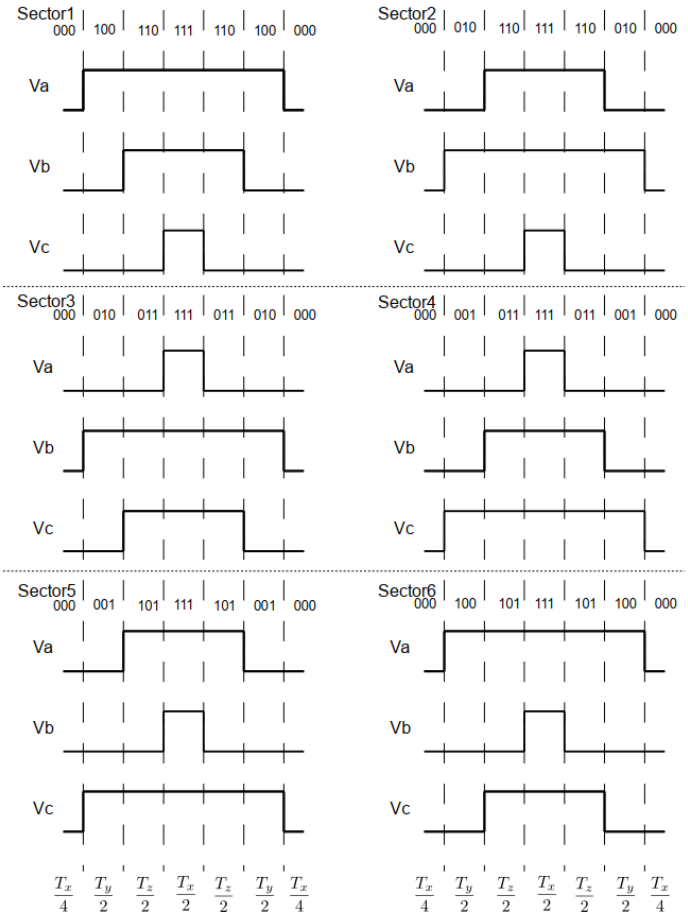


Figure B-1: Sequence of switching states for two level inverter SVPWM

Appendix C

Programming

C.1 C code for dual inverter drive vector controller

```
1  void FOC(struct ABC *iabc_in, float thEl, struct DQ0 *idq0_Ref, float wm_ref, float wm
       ,float EB, struct DQ0 *idq0_out, struct ABC *o_Vabc_RefA,struct ABC *o_Vabc_RefB )
2  {
3      float coseno, seno;
4      struct AB0 iab0; //alph beta components of stator current
5      struct DQ0 idq0;  //dq components  of stator current
6      struct DQ0 Vdq0_RefA; //dq components of vrefA
7      struct AB0 Vab0_RefA; //alpha beta components of vrefA
8      struct AB0 Vab0_RefA_sat; //alpha beta components of vrefA saturated
9      struct DQ0 Vdq0_RefA_sat; //d q components of VrefA saturated
10     struct ABC Vabc_RefA; //a b c components of vrefA
11     float  V_Ref_phase, V_Ref_sat, Valfa_sat, Vbeta_sat,wm_e;
12     struct ABC Vabc_Ref_B;  //abc components of inverter B reference
13     struct AB0 Vab0_Ref_B;  //alpha beta components of inverter B reference
14     struct DQ0 Vdq0_Ref_B;  //d q components of inverter B reference
15     float Iqavail;
16
17     cos_sin(thEl, &coseno, &seno);
18     clark_transform(iabc_in, &iab0);   //i_abc -> i_ab0
19     Rot(&iab0, coseno, seno, &idq0);   //i_ab0 -> i_dq0
20     *idq0_out = idq0;
21     ///==============INVERTER A CONTROLS ====================///
22     //Outer control loops (speed control and flux weakening)
23     //-------------------------------------------------------
24     //compute errors
25     wm_Err = wm_ref - wm; //speed error
26     VErr = Vlim - V_Ref_module;   //voltage magnitude error
```

```
    //update integral state
    wm_Int = wm_Int + TS*wm_Err;
    VErr_Int =VErr_Int + TS*VErr;
    //PI control law
    idq0_Ref->d = Ki_fw * VErr_Int;
    idq0_Ref->q = Ki_speed*wm_Int+ + Kp_speed*wm_Err;
    //saturation and integrator anti-windup
    if((idq0_Ref->d > 0) || (idq0_Ref->d < -Ilim)){
        VErr_Int =VErr_Int - TS*VErr; //anti-windup
        if((idq0_Ref->d > 0)) idq0_Ref->d = 0;
        else idq0_Ref->d = -Ilim;
    }
    Iqavail = sqrt(Ilim*Ilim - idq0_Ref->d * idq0_Ref->d);
    if(fabs(idq0_Ref->q) >Iqavail){
        wm_Int = wm_Int - TS*wm_Err; //anti windup
        if(idq0_Ref->q > 0) idq0_Ref->q = Iqavail;
        else  idq0_Ref->q = -Iqavail;
    }
    //Inner control loop(current control)
    //-----------------------------------
    //compute errors
    Id_err = idq0_Ref->d - idq0.d;
    Iq_err = idq0_Ref->q - idq0.q;
    //update integral state
    Id_Int = Id_Int + Id_err*TS;
    Iq_Int = Iq_Int + Iq_err*TS;
    //PI control law
    Vdq0_Ref.d = KI_d_fb*Id_Int + K_d_fb*Id_err;
    Vdq0_Ref.q = KI_q_fb*Iq_Int + K_q_fb*Iq_err;
    Vdq0_Ref.zero = 0;
    //coupling terms
    wm_e = wm*P*(C_2PI/60.0);  //electrical shaft speed in rad/s
    Vdq0_RefA.d = Vdq0_Ref.d - wm_e*(idq0.q) * Lq + VBdref;;    //back emf  + inverter
         B voltage feedforward
    Vdq0_RefA.q = Vdq0_Ref.q + wm_e*(idq0.d) * Ld + wm_e * PH + VBqref;  //back emf +
        nverter B voltage feedforward
    //transformations and output voltage saturation
    Rot_Inv(&Vdq0_RefA, coseno, seno, &Vab0_RefA); //
    V_Ref_module = sqrt(Vab0_ref.alpha*Vab0_ref.alpha + Vab0_ref.beta*Vab0_ref.beta);
    V_Ref_phase = atan2(Vab0_ref.beta, Vab0_ref.alpha);
    if (V_Ref_module >= Vlim) V_Ref_sat = Vlim;
    else V_Ref_sat = V_Ref_module;
    Vab0_ref_sat.alpha = V_Ref_sat * cos(V_Ref_phase);
    Vab0_ref_sat.beta  = V_Ref_sat * sin(V_Ref_phase);
    Vab0_ref_sat.zero  = 0;
```

```
70      clark_inv_transform(&Vab0_ref_sat, &Vabc_ref);
71      *o_Vabc_RefA = Vabc_ref;
72
73      ///==============INVERTER B CONTROLS ====================///
74      //Inverter B controls are implemented in a reference frame aligned with startor
            current vector
75      //Floating cap. control loop
76      //--------------------------
77      Is_module = sqrt(idq0.d*idq0.d + idq0.q*idq0.q); //stator current magnitude
78      Fluxd = Ld*idq0.d + PH;  //rotor flux d component
79      Fluxq = Lq*idq0.q; //rotor flux q component
80
81      VBlim = EB/SQRT3;  //limit for inverter B voltage vectors (SVPWM)
82      if(VBlim == 0 ) VBlim = 2;
83
84      //calculate optimum valus for VBquad_opt
85      if(Is_module < 0.1)  VBquad_opt = 0;
86      else VBquad_opt = -wm_e* (Fluxd*idq0.d + Fluxq*idq0.q)/Is_module ;
87      //determine EB reference
88      EB_reference = fabs(VBquad_opt)* CAP_V_MARGIN* SQRT3;
89      //rerefence saturation
90      if(EB_reference > EB_MAX) EB_reference = EB_MAX;
91      else if(EB_reference < EB_MIN ) EB_reference = EB_MIN;
92
93      EBsq_Err = EB_reference*EB_reference - EB*EB;
94      //proportional control law
95      VBpar_req = P_CAP*EBsq_Err;
96      //saturation
97      VBpar_sat = VBpar_req;
98      if(VBpar_req > VBlim) VBpar_sat = VBlim;
99      else if(VBpar_req < -VBlim) VBpar_sat = -VBlim;
100
101     VBavail = sqrt(VBlim*VBlim - VBpar_sat*VBpar_sat );
102
103     // Reactive power control loop
104     //----------------------------
105     //caculate inverter A reactive power
106     Rot(&Vab0_ref_sat, coseno, seno, &Vdq0_ref_sat);  //alpha beta --> d q
107     QA = -Vdq0_ref_sat.d*idq0.q + Vdq0_ref_sat.q*idq0.d;
108     //compute reactive power error
109     QA_Err = QA_reference - QA;
110     //update integral state
111     QA_Int = QA_Int  + TS* QA_Err;
112     //PI control law
113     VBquad_req = KI_RP * QA_Int + KP_RP * QA_Err;
```

```
114     VBquad_req +=  VBquad_opt; //feedforward from optimal value calculation
115     //saturation and integrator anti-windup
116     VBquad_sat = VBquad_req;
117 
118     if(VBquad_req > VBavail ||  VBquad_req < -VBavail){
119         QA_Int = QA_Int   - TS* QA_Err; //integrator anti-windup
120         if(VBquad_req > VBavail)  VBquad_sat = VBavail;
121         else VBquad_sat = -VBavail;
122     }
123     //cordinate transformation
124     unitvec(idq0.d, idq0.q, &IsU_real, &IsU_imag);  //returns the components of staotr
            current unit vector
125     complex_product(VBpar_sat, VBquad_sat, IsU_real, IsU_imag, &VBdref, &VBqref); //
            returns d q components of VBref after cordinate transformation
126 
127     Vdq0_ref_B.d = VBdref;
128     Vdq0_ref_B.q = VBqref;
129     Vdq0_ref_B.zero = 0;
130 
131     Rot_Inv(&Vdq0_ref_B ,coseno, seno, &Vab0_ref_B); //dq --> alpha beta
132     clark_inv_transform(&Vab0_ref_B, &Vabc_ref_B); //alha beta --> a b c
133     *o_Vabc_RefB = Vabc_ref_B;
134 }
```

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