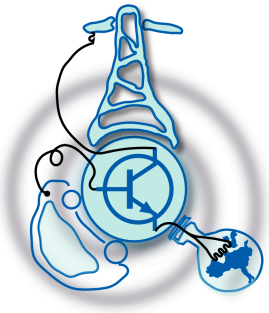
# Design of the test bench using controlled permanent magnet machine as a load for inverter testing

by
Aleksandra Stanojevic



Submitted to the Department of Electrical Engineering, Electronics, Computers and Systems
in partial fulfillment of the requirements for the degree of
Erasmus Mundus Master Course in Sustainable Transportation and Electrical Power Systems
at the
UNIVERSIDAD DE OVIEDO
September 2019

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## Abstract

In this thesis is developed and analyzed the control of speed of permanent magnet machine fed up from back-to-back PWM three-phase converter supplied from the grid, as part of the project of a testbench for testing the commercial inverter. Methodology to the derivation of the control of the system, including control of the speed of the permanent magnet machine and maintaining the stable voltage reference on DC link capacitor, is explained. The obtained control strategy is simulated in *Simulink* simulation tool of *Matlab* software package. Thesis is also covering several aspects of the hardware design of the application, such as sizing of the components of the power stage (machine, DC link capacitor, filters), design of the hardware interface between power stage and digital signal processor and control implementation in DSP written in *C* code. An experimental test of the control of the output of the three-phase IGBT module generated from DSP is performed for the sake of validation of the design of the PCB interface and the configuration of DSP.

Thesis Supervisor: Jorge Garcia Garcia
Title: Associate Professor

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# Acknowledgments

Doing an internship in “ Electronica y Comunicaciones Noroeste ”, in Ferrol, was a great experience in a professional and personal level. During the development of the thesis project, I had the opportunity to cooperate with the great staff of the company. I would express especial gratitude to the Roberto Pena, Jose Castro, Antonio Trabado and my mentor, Dario Otero, for sharing knowledge and the hands-on advice from their extensive engineering experience. Above all, as this was my first working experience in the industry, they made me feel like a part of the company and environment. With their guidance and support, I gained valuable engineering skills. My exceptional gratitude and admires are addressed to my supervisor from The University of Oviedo, Jorge Garcia. I appreciate all the effort, support and time invested in my project during the development. At last, as important for me was the support and help of my friends and family, which encouraged me to work, focus on task and finalize the thesis in the best way.

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# List of symbols

## Active rectifier

| | |
|---|---|
| $E_m$ | the amplitude of grid voltage |
| $e_a$ | phase grid voltage-phase A |
| $e_b$ | phase grid voltage-phase B |
| $e_c$ | phase grid voltage-phase C |
| $e_d$ | d component of the grid voltage vector |
| $e_q$ | q component of the grid voltage vector |
| $u_{ab}$ | phase-to-phase voltage on the input of grid side converter-between phase A and B |
| $u_{bc}$ | phase-to-phase voltage on the input of grid side converter-between phase B and C |
| $u_{ca}$ | phase-to-phase voltage on the input of grid side converter-between phase C and A |
| $u_{dc}$ | DC link voltage |
| $u_a$ | phase voltage on the input of grid side converter-phase A |
| $u_b$ | phase voltage on the input of grid side converter-phase B |
| $u_c$ | phase voltage on the input of grid side converter-phase C |
| $i_{ra}$ | phase current input to the grid side converter-phase A |
| $i_{rb}$ | phase current input to the grid side converter-phase B |
| $i_{rc}$ | phase current input to the grid side converter-phase C |

$i_{rd}$ d component of the vector of input current to the grid side converter

$i_{rd}$ d component of the vector of input current to the grid side converter

$I_o$ DC load current of the active rectifier

## Permanent magnet machine

$u_{sa}$ phase voltage on the permanent magnet machine input terminal-phase A

$u_{sb}$ phase voltage on the permanent magnet machine input terminal-phase B

$u_{sc}$ phase voltage on the permanent magnet machine input terminal-phase C

$u_{sd}$ d component of the permanent magnet voltage vector

$u_{sq}$ q component of the permanent magnet voltage vector

$i_{ma}$ phase current input to the permanent magnet machine-phase A

$i_{mb}$ phase current input to the permanent magnet machine -phase B

$i_{mc}$ phase current input to the permanent magnet machine -phase C

$i_{md}$ d component of the permanent magnet current vector

$i_{mq}$ q component of the permanent magnet current vector

$\Psi_{PM}$ permanent magnet flux

$\Psi_a$ flux in phase A of the permanent magnet machine

$\Psi_b$ flux in phase B of the permanent magnet machine

$\Psi_c$ flux in phase C of the permanent magnet machine

$\Psi_d$ d component of the flux vector of permanent magnet machine

$\Psi_q$ q component of the flux vector of permanent magnet machine

$R_s$ stator resistance

| | |
|---|---|
| $L_d$ | d component of the stator inductance |
| $L_q$ | q component of the stator inductance |
| $P_n$ | rated power |
| $T_e$ | electromagnetic torque |
| $T_m$ | load torque |
| $J$ | moment of inertia of permanent magnet machine |
| $B$ | friction damping factor |
| $\omega$ | mechanical rotor speed in rad/s |
| $\omega_e$ | electrical speed in rad/s |

# List of abreviations

| | |
|---|---|
| ADC | Analog-to-Digital conversion |
| AC | alternate current |
| DC | direct current |
| DSP | digital signal processor |
| PCB | printed circuit board |
| PM | permanent magnet |
| PWM | pulse width modulation |
| VOC | voltage oriented control |
| FOC | field oriented control |
| DTC | direct torque control |

# Chapter 1

# Introduction

The increase of electrical energy consumption due to the constant growth of the population is one of the major concerns. The consequences of rising emissions on climate change are already present. That is why saving electrical energy is one of the priorities in research and development of the technologies. The significant part of electrical energy is consumed by motors in the industrial applications, converting electrical to mechanical energy. The revolution in increasing energy efficiency of such application is brought by the implementation of variable frequency drives empowering AC machines. With the emerging semiconductor technologies for commercial use, the applications based on variable frequency drives are replacing traditional applications and improving controllability, performance and energy efficiency of the applications.

With improved performance and controllability of the AC motors driven from variable frequency drives, there is a wider range of functionalities and possibilities that can be implemented in various applications.

This thesis is studying control design and hardware implementation of drive application controlling the speed of permanent magnet machine, as part of the industrial project of Testbench for testing industrial inverters.

## 1.1 The application topology and characteristics

Considering the aforementioned advantages of using VFDs, the topology of a test-bench for industrial inverters is developed as presented with the block diagram on Figure 1-1. The inverter under test is driving induction machine, which is mechanically coupled to the permanent magnet machine. The load of the inverter is regulated by controlling the bspeed of the permanent magnet machine mechanically coupled to than induction motor, the control system which is the subject of this thesis. The system discussed in this thesis is a shaded part on Figure 1-1.

The permanent magnet machine is fed from a back-to-back PWM converter connected to the grid. Both the grid side converter and machine side converter stages are three-phase full-bridge IGBT converters. Discussing the three-phase rectifier topologies, the author in [1] points out that this specific topology is widely used for motor drives due to its characteristics, also particularly important for this application. The induction machine will operate as a motor and permanent magnet machine as a generator and regenerate energy back to the grid. Thus, the possibility of controlled IGBT converters to act both as active rectifier and inverter is essential and will enable the system to work in all four quadrants. Speed control of the permanent magnet machine is performed by controlling the switching of the machine side converter and stable DC link voltage reference is provided by control of the grid side converter.

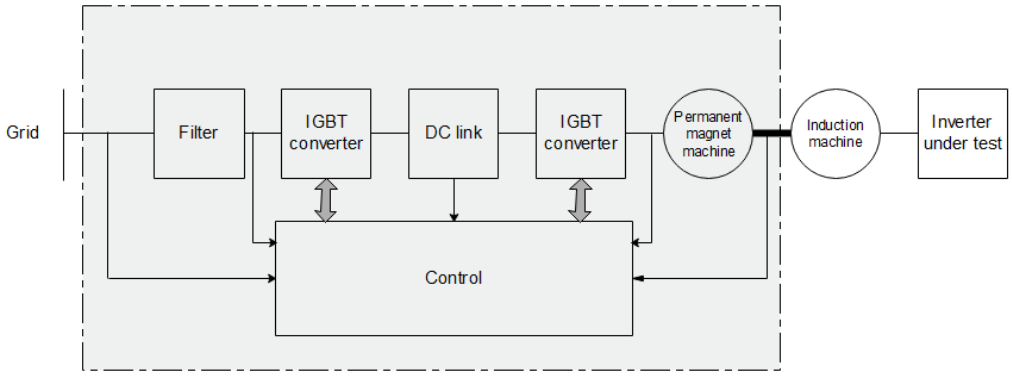


Figure 1-1: Block diagram of the application

## 1.2 Thesis objectives

The aim of the project is the development of a laboratory benchmark based on Permanent Magnet Machines, able to test different commercial AC drives at various operating conditions. The description of the target setup is based on a back-to-back IBGT converter, controlled from a digital signal processor, which interfaces the three-phase permanent magnet machine to the three-phase grid.

For achieving the main goal of a project following objectives are defined:

- Design of the power setup, which includes sizing of the filters and machine.
- Analysis and modeling of the power converter topology
- Analysis and modeling of the permanent magnet machine
- Design of the closed loop control.
- Validation through simulations.
- Design of the control interface, including hardware required for measuring the input variables and PCB design.
- Implementation and testing of the control of PCB.
- Assembling the laboratory setup.
- Experimental validation

## 1.3 Organization of the thesis

The content of the master thesis is based on analysis of the design and implementation of the described application, and results of experimental work. Following previously defined objectives, the thesis structure is organized in the following chapters:

- Chapter 1.

Chapter one contains an introduction, underlying the benefits of using variable frequency drives. Moreover, it describes the structure of the application which is the subject of the thesis and its features. It points out the general approach to the control of the system, based on which design will be developed. Taking that into account, the objectives for developing thesis work are set.

- Chapter 2.

The second chapter will give a brief review of technologies and techniques to be used in the application. This chapter will provide the theoretical background needed to understand and design the control system. This includes main power elements as permanent magnet machine and power converter, and development of their dynamic models.

- Chapter 3.

Based on dynamic model equations developed in the previous chapter, the third chapter will explain the vector control strategy and approach to the derivation of parameters for the proposed design.

- Chapter 4.

Forth chapter will be dedicated to the hardware and software design of system implementation, meeting constraints of the real system. The first part will discuss the design of the power stage, which includes all main elements that are subject to control as PM machine, filters and DC link, but also transducers which are the link and provide feedback to control. The second part will explain the role and design of the PCB interface between the power stage and control software. Lastly, software implementation of the control strategy in DSP will be described.

- Chapter 5.

The fifth chapter will contain the simulation results of the system, following the control design described in Chapter 3. In general, it will comment on results obtained

from simulating the two topologies. The first is control of a three-phase active rectifier with elements designed according to real system requirements and second is simulation of whole system topology with resized elements adapted to sample motor from the Simulink database.

- Chapter 6.

The results of the experimental validation of the design explained in Chapter 4 will be presented in Chapter 6. It will compare obtained results with expected ones and give a review on the validation process and corrections made along the way.

- Chapter 7.

Finally, Chapter 7 will summarize achieved results and contribution of the project. Moreover, it will propose ideas to improve efficiency, functionality, performance out of the defined scope of the project.

# Chapter 2

# Analysis and modeling of system

## 2.1 Power conversion stage

Discovering of semiconductor devices led to research and development of different converter topologies for various applications. Classification and analysis of different power topologies is discussed in [9] and [10]. Among all types of three-phase rectifiers (diode rectifier, thyristor-based rectifier and self-commutated) only self-commutated or fully-controlled converters (name used depending on literature) are able to transfer power in both directions (AC to DC or DC to AC) and also control power factor [10]. That is the reason for the fully-controlled converters being the most common choice for machine drives. As the name is suggesting, the full controllability of this family of converter is possible due to its capability of gate turn-on, as well as gate turn-off of the switch using switchable semiconductors. The most commonly used fully-controlled converters are employing DC link stage. Depending on DC link there are two types of fully-controlled converters, voltage source converters, and current source converters. Voltage source converters employ capacitive DC link and current source converters inductive. [10]

High-frequency switching, which is widely used nowadays, is achieved with fully controlled converters using PWM switching methods. The basic principle of PWM and different PWM techniques that can be applied are explained in [10].

One of the most used topology for machine drives is **three-phase back-to-back**

**IGBT converter** shown on Figure 2-1. Two 3-phase IGBT converters are connected by DC link capacitor which ensures stable and smooth DC link voltage. Transformer have the functions of filtering harmonics and isolation. Control of the DC link voltage is performed by controlling switching of grid side converter and control of machine by switching of machine side converter.

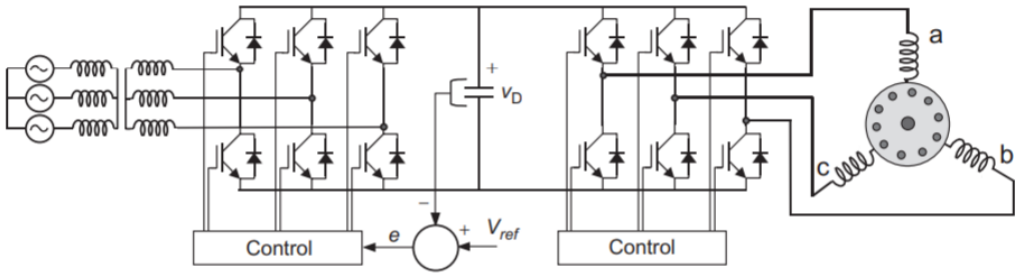


Figure 2-1: Typical application of three-phase back-to-back IGBT converter for machine drives [1]

The following sections will discuss the development of a model of active rectifier (inverter, based on which control strategy will be designed for the specific application.

### 2.1.1 Dynamic model of two-level three-phase active rectifier in abc reference frame

This section separates the analysis of the grid side converter operation for being able to develop its dynamic model. The system observed is shown in Figure 2-2, where the load is a machine side converter connected to the permanent magnet machine. The dynamic model of active rectifier presented in this section is proposed by authors in [3, 11, 12].

Under assumptions that switching power losses are neglected (IGBTs are considered ideal switches) and, input voltage to converter is equal to reference voltage provided by control, switching model from Figure 2-2 can be replaced by average model on Figure 2-3. Ideal current source is modeling load of active rectifier.

Input voltages to the active rectifier from the grid are defined by Equations 2.1 for the three-phase balanced system. All voltages and currents are also functions of

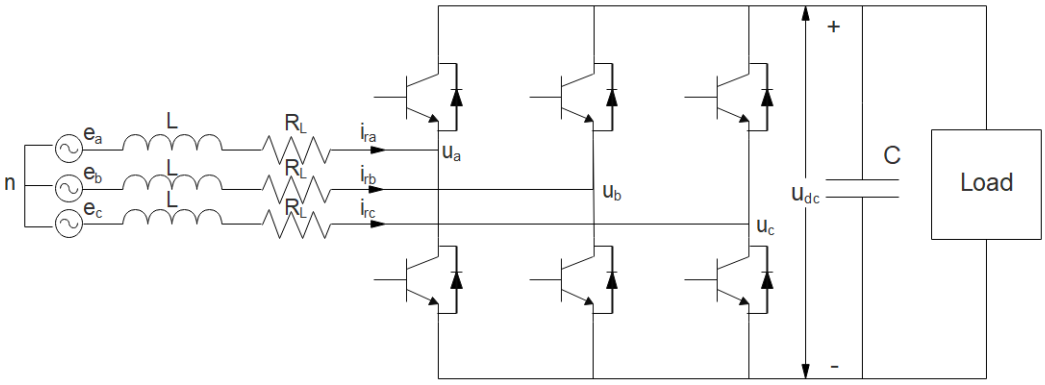


Figure 2-2: Operation of three-phase IGBT converter

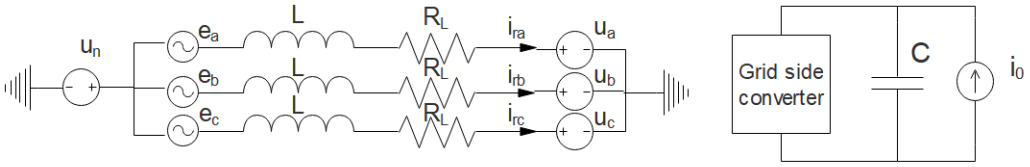


Figure 2-3: Average model of active rectifier

time which will be omitted in following derivations for simplicity.

$$
\begin{aligned}
e_a &= E_m \cos \omega t \\
e_b &= E_m \cos \left(\omega t - \frac{2\pi}{3}\right) \\
e_c &= E_m \cos \left(\omega t + \frac{2\pi}{3}\right)
\end{aligned}
\tag{2.1}
$$

Equations 2.2 of the active rectifier line voltages are modelling switching behavior of the active rectifier, where $s_i$ for each leg is taking value 0 or 1.

$$
\begin{aligned}
u_{ab} &= (s_a - s_b) u_{dc} \\
u_{bc} &= (s_b - s_c) u_{dc} \\
u_{ca} &= (s_c - s_a) u_{dc}
\end{aligned}
\tag{2.2}
$$

Based on discussion from [9] voltage of isolated neutral point with respect to ground is equal to average value of phase input converter voltages. Thus, phase input voltages can be described with equations 2.3 where $f_a$, $f_b$, $f_c$ are variables which are function of $s_a$, $s_b$, $s_c$ as given in Equations 2.4

$$\begin{aligned} u_a &= f_a u_{dc} \\ u_b &= f_b u_{dc} \\ u_c &= f_c u_{dc} \end{aligned} \tag{2.3}$$

$$\begin{aligned} f_a &= s_a - \frac{1}{3}(s_a + s_b + s_c) \\ f_b &= s_b - \frac{1}{3}(s_a + s_b + s_c) \\ f_c &= s_c - \frac{1}{3}(s_a + s_b + s_c) \end{aligned} \tag{2.4}$$

Dynamic behaviour of active rectifier will be described with set of voltage equations and power balance. Based on model on Figure 2-3 Equations 2.5 are derived. Moreover, Equation 2.6 is defining DC link side states.

$$\begin{vmatrix} e_a \\ e_b \\ e_c \end{vmatrix} = R_L \begin{vmatrix} i_{ra} \\ i_{rb} \\ i_{rc} \end{vmatrix} + L\frac{d}{dt} \begin{vmatrix} i_{ra} \\ i_{rb} \\ i_{rc} \end{vmatrix} + \begin{vmatrix} u_a \\ u_b \\ u_c \end{vmatrix} \tag{2.5}$$

$$C\frac{du_{dc}}{dt} = s_a i_r a + s_b r i_b + s_c r i_c - i_o \tag{2.6}$$

Based on discussion in [3] active and reactive power in three-phase system are expressed by equations 2.7 and 2.8. From equations for active and reactive power can be seen that the system in abc reference frame is non-linear and independent control of active and reactive power cannot be achieved.

$$P = e_a i_{ra} + e_b i_{rb} + e_c i_{rc} \tag{2.7}$$

$$Q = \frac{1}{\sqrt{3}}[e_a(i_{rb} - i_{rc}) + e_b(i_{ra} - i_{rc}) + e_c(i_{rb} - i_{ra}) \tag{2.8}$$

### 2.1.2 Dynamic model of two-level three-phase active rectifier in rotating dq0 reference frame

On the other hand, another approach to analysis is considering space vector of instantaneous power. Defining voltage fixed to x-axis and current shifted for angle $\varphi$, Equations 2.9 and 2.10 for expressing active and reactive power will be obtained. For constant amplitude of voltage active and reactive power will be linear function of current components with respect to the system fixed to the voltage space vector. The voltage space vector is rotating with the frequency of grid. This conclusion will be used for implementing transformations of system, from abc stationary reference frame to rotating dq0 reference frame.

$$P = \frac{3}{2}E_m I_{rm} \cos\varphi = \frac{3}{2}E_m i_{rd} \tag{2.9}$$

$$Q = \frac{3}{2}E_m I_{rm} \sin\varphi = \frac{3}{2}E_m i_{rq} \tag{2.10}$$

System obtained by applying transformation from Appendix A to set of equations 2.5 will be described with Equations 2.11, 2.12 and 2.13.

$$e_d = Ri_{rd} + L\frac{di_{rd}}{dt} - \omega L i_{rq} + u_{rd} \tag{2.11}$$

$$e_q = Ri_{rq} + L\frac{di_{rq}}{dt} + \omega L i_{rd} + u_{rq} \tag{2.12}$$

$$C\frac{du_{dc}}{dt} = \frac{3}{2}(s_d i_{rd} + s_q i_{rq}) - i_o \tag{2.13}$$

## 2.2 Permanent magnet machine-analysis and modeling

Even though usage of permanent magnet machines in various applications is under development and attention since recently, first permanent magnet machine occurred much earlier, in nineteenth-century [13]. But, it didn't reach its full potential at the time as very poor quality hard magnetic materials were used. Later on, the development of brushless permanent magnet machines using rare earth magnetic materials was showing as a promising technology for the future of permanent magnet machines. With the development of semiconductor-based control for the permanent magnet machine, PM machine drives could compete with dominate induction machine drives in various applications.

Benefits of using permanent magnet-based machine over motors with electromagnetic excitation are also summarized by Gieras in [13] as following:

- There are no power losses associated with excitation of the machine, which improves the efficiency of the machine significantly.
- Higher power density and torque density reduces the volume of the permanent magnet machine which is substantial for many applications.
- Dynamic response of the permanent magnet machine is improved due to higher magnetic flux density in the air gap.
- Simplified construction and maintenance.

Focusing on brushless PM machines, we can differentiate two types:

1. DC brushless permanent magnet machine
2. AC brushless permanent magnet machine

For purpose of this application, following discussion and features are directly applied on AC synchronous permanent magnet machines supplied with three-phase sinusoidal voltage.

Ongoing research is considering many aspects of permanent magnet machine applications which will influence future trends in drives. More information about permanent magnet materials, their magnetic features and mechanical construction of machines can be found in [13]. Following sections will focus on features of permanent magnet machine which are the basis for developing the general principal of modeling of the PM machine dynamics.

### 2.2.1 Magnetic flux distribution of PM machine

Unlike the induction machine, excitation flux generated from the rotor is coming solely from a permanent magnet, as there are no currents generated in the rotor. Thus, the vector of flux generated by the permanent magnet is fixed to the rotor, rotating with synchronous speed. The convention is defined such that the d-axis is aligned with magnet flux and q - axis leading 90 degrees, assigned as torque axis, shown on Figure 2-4. For the first, simplified approach, influence on stator d and q currents on flux vector are neglected and assumed equal magnetic permeability along d and q axis. Under these assumptions, excitation flux is originated solely from the permanent magnet and thus torque directly proportional to the $i_q$. These assumptions can be directly applied on the surface-mounted PM machine.

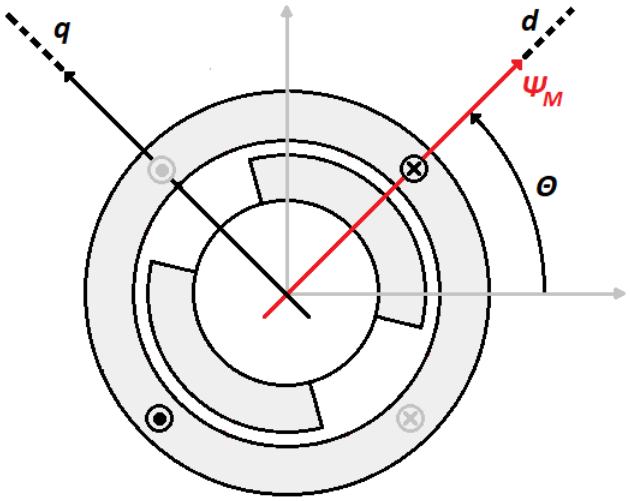


Figure 2-4: Model of permanent magnet machine

Still, for real machine coupling won't be eliminated and armature reaction due to stator currents will affect flux distribution and shift flux vector.

### 2.2.2 Saliency of PM machine

Important feature that should be introduced to describe different construction solutions of rotor of permanent magnet machine is saliency. The concept of saliency applied to different rotor structures is explained by the author in [2]. He compared two typical and most common used rotor types, surface-mounted PM machine and interior PM machine shown on Figure 2-5. Taking into account that the magnetic permeability of magnets used in PM machines is close to air ($\mu_r = 1$), the effective air gap in the magnetic flux path of d ad q axis is practically the same, as well as inductances ($L_d = L_q$). There is no inductance saliency for SPM machine. On the other hand, the interior PM machine with permanent magnets inserted in iron will clearly have lower permeability and inductance along q axis then along d-axis ($L_q > L_d$). Thus, saliency refers to variation of inductance seen on stator terminals for different rotor positions. Parameter for evaluating this feature is a salient ratio defined as the ratio between $L_q$ and $L_d$ inductance.

This concept is important for modeling and control of PM machine and the following derivation of the model will be performed for the salient PM machine. Model can be simply adjusted for non-salient machine applying condition $L_d = L_q$.

### 2.2.3 Dynamic model of PM machine in stationary three-phase abc reference frame

The behavior of the PM machine, as of any other dynamic system, can be defined with the set of equations. The model described with the following equations in abc reference frame is derived referring to [14] and [9]. Equations 2.14 are expressing stator phase voltages depending on voltage drop on stator resistance and rate of change of flux.

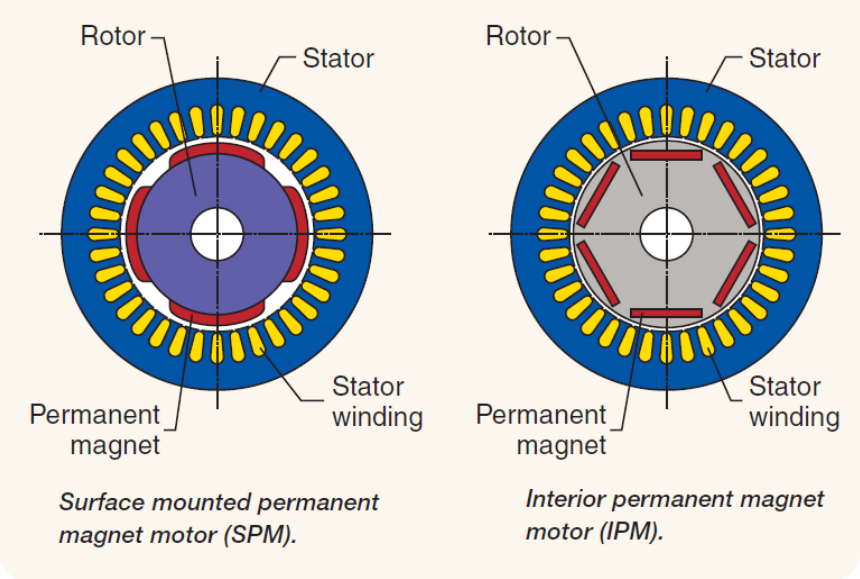


Figure 2-5: Saliency of PM machines with different rotor construction [2]

$$\begin{vmatrix} v_{sa} \\ v_{sb} \\ v_{sc} \end{vmatrix} = R_s \begin{vmatrix} i_{ma} \\ i_{mb} \\ i_{mc} \end{vmatrix} + \frac{d}{dt} \begin{vmatrix} \Psi_{ma} \\ \Psi_{mb} \\ \Psi_{mc} \end{vmatrix} \tag{2.14}$$

Flux linkage in each phase (2.15) consists of flux component of permanent magnet and linkage flux due to stator currents. Model assumes symmetry of machine ($L_{ij} = L_{ji}$).

$$\begin{vmatrix} \Psi_{ma} \\ \Psi_{mb} \\ \Psi_{mc} \end{vmatrix} = \begin{vmatrix} L_{aa}(\theta_e) & L_{ab}(\theta_e) & L_{ac}(\theta_e) \\ L_{ba}(\theta_e) & L_{bb}(\theta_e) & L_{bc}(\theta_e) \\ L_{ca}(\theta_e) & L_{cb}(\theta_e) & L_{cc}(\theta_e) \end{vmatrix} \begin{vmatrix} i_{ma} \\ i_{mb} \\ i_{mc} \end{vmatrix} + \begin{vmatrix} \Psi_{PMa} \\ \Psi_{PMb} \\ \Psi_{PMc} \end{vmatrix} \tag{2.15}$$

The general power equation for the three-phase system is given by equation 2.16. Expression for electromagnetic torque can be obtained by substituting voltage equations 2.14 in Equation 2.16 and dividing by rotor speed $\omega_r$, as derived in [14]. For the non-salient rotor type of machine, mutual and self inductances are also functions of rotor position.

$$P = v_{sa} i_{ma} + v_{sb} i_{mb} + v_{sc} i_{mc} \tag{2.16}$$

As the main purpose of electrical machines is the conversion from electrical to mechanical energy and vice versa, the missing equation for defining model is the one relating electrical an mechanical variables given by relation 2.17.

$$J\frac{d\omega}{dt} + B\omega = T_e - T_m \tag{2.17}$$

Observing equations can be seen that system is highly non-linear and would require complex control.

### 2.2.4 Dynamic model of the PM machine in synchronous dq0 reference frame

As concluded from Section 2.2.1, under certain conditions, the reference system locked to rotor can provide a decoupled linear system in which linkage flux ad torque can be controlled independently. The transformations are given in Appendix A are applied on the equations defining the model in abc reference frame, which are transformed to dq0 reference frame. As the balanced three-phase system is assumed, "zero" component equals 0. Equations defining the model in dq0 reference frame are explained in [9, 10, 14].

$$v_{sd} = R_s i_{md} - \omega_e \Psi_{sq} + \frac{d\Psi_d}{dt} \tag{2.18}$$

$$v_{sq} = R_s i_{mq} + \omega_e \Psi_{sd} + \frac{d\Psi_q}{dt} \tag{2.19}$$

$$\Psi_{sd} = L_d i_{md} + \Psi_{PM} \tag{2.20}$$

$$\Psi_{sq} = L_q i_{mq} \tag{2.21}$$

Flux in the air-gap has fixed permanent magnet flux component acting along d-axis 2.20, but also the component depending on armature current components (2.20, 2.21).

This principle is used for implementing flux weakening, applying a demagnetizing armature current component along the d-axis. It is used to extend the range of speed on the rotor shaft. Paper [15] discuss more in detail implementation of the flux weakening for different types of PM machine.

Substituting Equations 2.20 and 2.21 for d and q components of flux in Equations 2.18 and 2.19, Equation 2.22 and Equation 2.23 are obtained. From these equations of stator voltage components can be seen that there is still coupling present between d and q components of voltage.

$$v_{sd} = R_s i_{md} + L_d \frac{di_{md}}{dt} - \omega_e L_q i_{mq} \tag{2.22}$$

$$v_{sq} = R_s i_{mq} + L_q \frac{di_{mq}}{dt} + \omega_e L_d i_{md} + \omega_e \Psi_{PM} \tag{2.23}$$

Observing Equation 2.24 can be seen that the electromagnetic torque on the machine consists of two components, the permanent magnet torque and the reluctance torque. The permanent magnet torque is produced due to magnet flux and the reluctance torque due to anisotropy of rotor structure. [10, 14, 16, 17] For more demanding applications in terms of the power density and speed range, such as electric vehicles, salient rotor PM machines are favorable solutions due to their capability to produce the reluctance torque. [16–18]. As for this application operation in extended speed range and higher torque are not required this feature won't be further discussed.

$$T = \frac{3}{2} p \Psi_{PM} i_{mq} + \frac{3}{2} p (L_d - L_q) i_{md} i_{mq} \tag{2.24}$$

# Chapter 3

# Analysis and design of system control

## 3.1 Vector control systems for a machine drives

Development of the semiconductor-based converters led to the development of AC drives for industrial implementation, substituting DC drives, as AC machines proved to be more robust, reliable and efficient. However, that brought new challenges for the control system design and implementation. The DC drives have been a dominant solution for industrial drives for the long period since they enable relatively simple control implementation. Their advantages include DC control system variables that are easier to control, as well as decoupled control of machine excitation and mechanical output (torque or speed). On the other hand, AC machines use the multiply-phase system, implying AC control variables which introduces more control and stability issues, as well as non-linearity of the control system. These drawbacks of the AC drives are overcome by introducing the vector control. This strategy is using another mathematical tool for representing AC variables, a space vector. The space vector defines AC variables by its amplitude and position in time in the fixed coordinate system. The common conclusion from the analysis in Sections 2.1.2 and 2.2.1 is that space vector will become DC value with respect to the reference system rotating the same speed as space vector. With the development of novel control strategies,

including transformations of reference systems (Appendix A), compensation of values and precise encoders and observers, AC machine drives became more progressive and dominant solutions for industrial use.

Focusing on the application which is subject of this thesis, this chapter will discuss the design and implementation of the control system divided into two main parts:

1. Control of the active rectifier (grid side converter)

2. Control of the permanent magnet machine

The last sections will explain common parts related to controller implementation for both control strategies such as the discretization method used for further implementation in DSP and the Anti-Windup solution.

## 3.2 Control of the three-phase active rectifier

Development of the control of three-phase IGBT converters drew the attention of many researchers due to the aforementioned advantages, such as the ability of bidirectional power flow and power factor correction. There are different control strategies proposed by authors in [3, 12, 19, 20] depending on the performance and complexity of strategy used. The author in [3] gives a comparison between the Direct torque control and Voltage oriented control strategies, employing hysteresis switching or PWM modulation based on voltage reference. Among them, the one implemented in this application is VOC using PWM modulation, shown on Figure 3-1. Outer loop of cascade control implementation controls DC link voltage and provides the reference of d-component of line current $i_{rd}$, which will be discussed in detail in Section 3.2.3 about voltage control design. Inner current control loops also perform the power factor regulation. Taking conclusion based on Equation 2.9 and Equation 2.10 from previous chapter, decoupled control of active and reactive power can be achieved with control of $i_{rd}$ and $i_{rq}$. Thus, the unity power factor would be achieved by providing zero reference of $i_{rq}$. The position angle of the grid voltage for coordinate transformation is provided by the Phase Locked Loop (PLL).

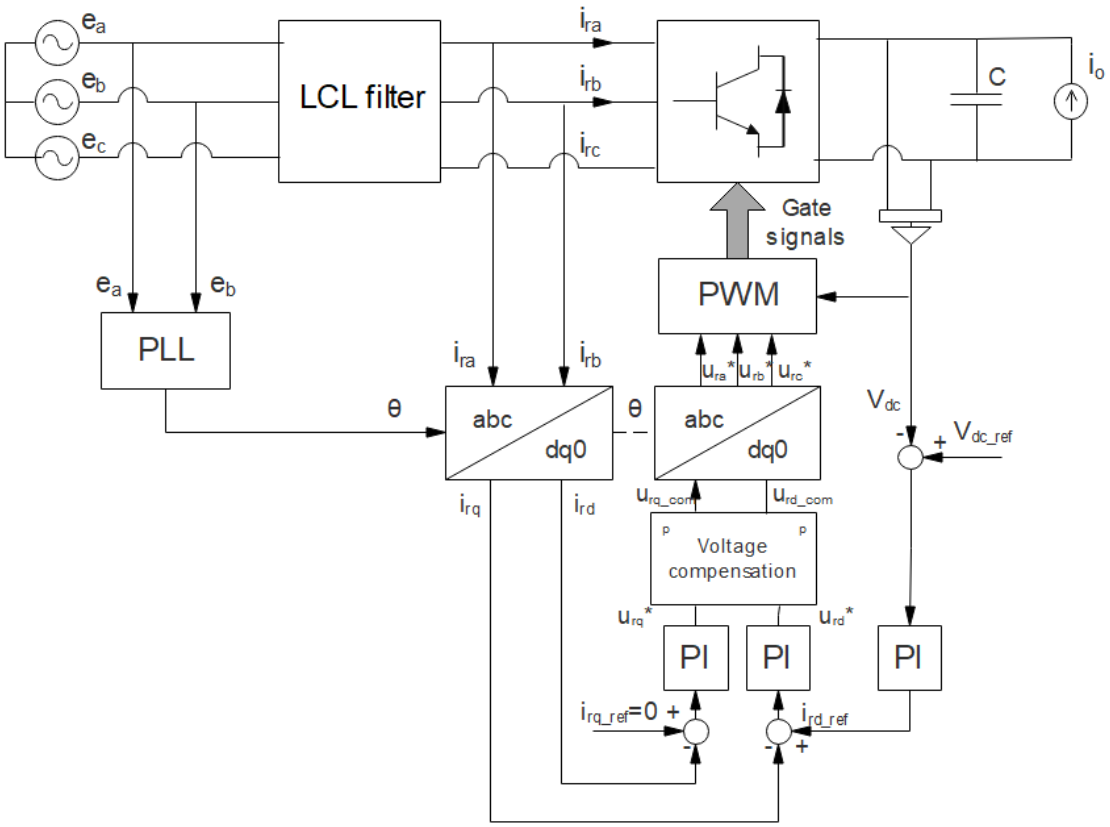


Figure 3-1: VOC of three-phase active rectifier

This strategy provides fast transient response and ensures better static performance with the inner current control loop. Still, the good performance of this control strategy comes with the cost of complexity. As can be seen from the schematic, it requires more computational effort for the coordinate transformations, voltage compensation, PWM, as well as additional hardware for providing measurements for feedback signal. Giving the advantage to performance of control over cost and complexity this control strategy is implemented and a step-by-step approach to design discussed in the following sections.

### 3.2.1 Implementation of pulse width modulation

Pulse width modulation based on reference voltage from control generates the gate signal pulses triggering IGBT switches. The modulation scheme used for this

application is natural sinusoidal PWM with constant switching frequency. The working principle of implementing this scheme is demonstrated on Figure 3-2. Sinusoidal reference voltage (red on the figure) is compared with the triangular carrier waveform following condition case given by Equation 3.1. The period of carrier waveform (one triangle) corresponds to the switching period. Maximum amplitude possible of the modulation signal is $\frac{V_{dc}}{2}$.

$$G = \begin{cases} 1, & V_{ref} \geq V_{carrier} \\ 0, & V_{ref} < V_{carrier} \end{cases} \tag{3.1}$$

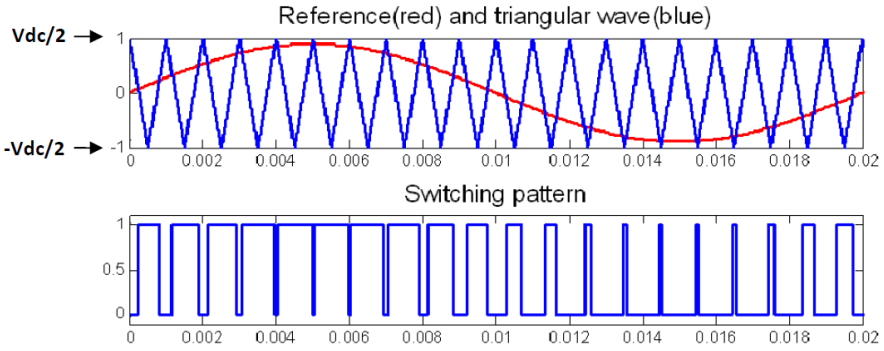


Figure 3-2: Natural sinusoidal PWM [3]

Yet, this technique implies ideal switches, which would switch on and off instantaneously, at the same moment switching command is applied to the gate. But in the real case, the semiconductor switches have some finite turn-on and turn-off times. As shown on Figure 6-8, in the ideal case of signals in black color, when one switch in leg turns on the complementary switch turns off and vice versa. As in a real case, there is some time needed for the switch to change state, there is a possibility that both switches in leg conduct in the same time around switching instant, causing short-circuit of the input power supply. For this reason, additional switching delay called dead-time is included to ensure some time for the switch to turn off before complementary one turns on (red signal on the figure). On the other hand, researchers are pointing out on the undesirable effect of dead-time on increasing high-frequency harmonics [21]. Taking into account that switching frequency of application is not

that high (4 KHz) this aspect won't be considered for application.

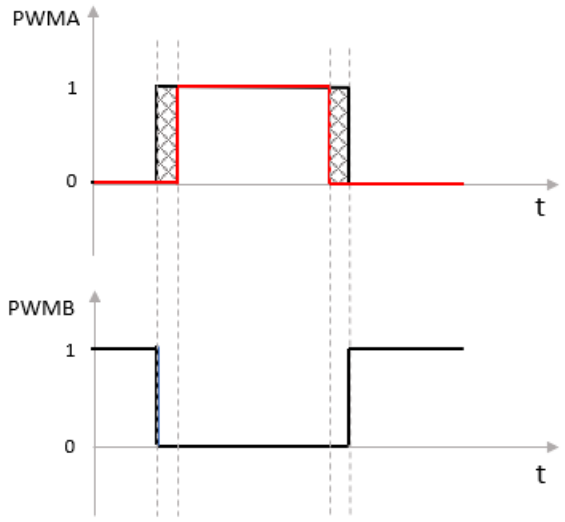


Figure 3-3: Dead-time applied on the complementary switches

### 3.2.2 Design of the current control loop

As mentioned while introducing concept of VOC control strategy, current control is inner control loop which is fastest loop in implemented control. Structure of loop is shown on Figure 3-4. The approach to the design of each part in the continuous domain will be explained separately in the following sections, based on the model derived in Chapter 2.

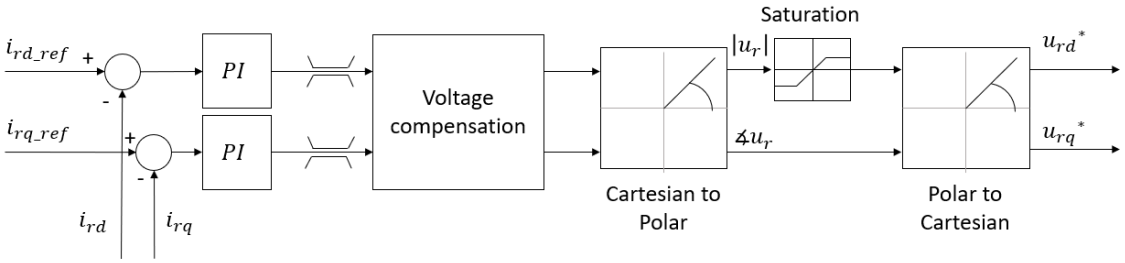


Figure 3-4: Current control loop of active rectifier

#### 3.2.2.1 Design of the current controllers

Aim of the control of the power factor of the converter, as explained in Section 2.1.2, is to enable independent control of $i_{rd}$ and $i_{rq}$ components of line current. However, there are still voltage coupling terms present in voltage equations 2.11 and 2.12. The coupling terms will be neglected in the first approximation for the design of the current controller and will be taken into account in the further development of current control. Thus, the current controller will control the corresponding component of the voltage drop on the AC filter. The preferred solution for AC filter used in this application, over L and LC filter, is LCL filter. More details on the design of this filter will be given in the following chapter, considering the hardware design and implementation. Simplified closed-loop control for calculating controller parameters is shown on figure 3-5. Plant of the loop of LCL filter is third-order transfer function that is complex to control. The approach used for control in this thesis is simplifying the third-order transfer function of the LCL plant to first-order transfer function, which showed satisfying performance and is relatively simple to implement. [22]The LCL circuit is replaced with serious connection of two inductors, grid side inductor and converter side inductor (neglecting parallel capacitor) proposed in [22]. Transfer function of modified plant is expressed by Equation 3.3.

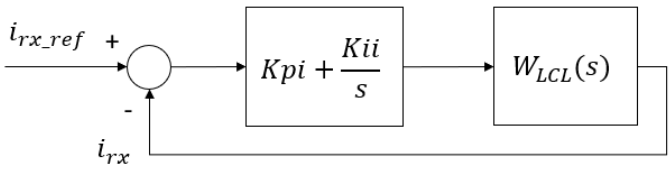


Figure 3-5: Simplified current closed loop control

$$W_{LCL}(s) = \frac{C_f R_f s + 1}{(L_g + L_c)s + (R_g + R_c)} = \frac{1}{L_e + sR_e} \tag{3.2}$$

$$W(s) = \frac{1}{(L_g + L_c)s + (R_g + R_c)} = \frac{1}{L_e + sR_e} \tag{3.3}$$

Considering the modified first-order system, a conventional zero-pole cancellation method is applied for the design of a PI controller. Proportional $K_{pi}$ and integral $K_{ii}$ components are defined by Equation 3.4 and Equation 3.5. For keeping consistent dynamics of all system bandwidth of the fastest control loop, which is current loop, is designed such that is 10 times slower than switching.

$$K_{pi} = 2\pi BW_i L_e \tag{3.4}$$

$$K_{ii} = 2\pi BW_i R_e \tag{3.5}$$

Yet, the transfer function of real LCL filter plant will introduce complex conjugate pole pair with low damping, which will produce oscillations of the response. The root locus of the open-loop system of the controller and LCL plant on Figure 3-6 shows that the system is sensitive and can have oscillations or even go to instability if forced. The step response of the closed-loop represented by Figure 3-5 for LCL filter is shown on Figure 3-7.

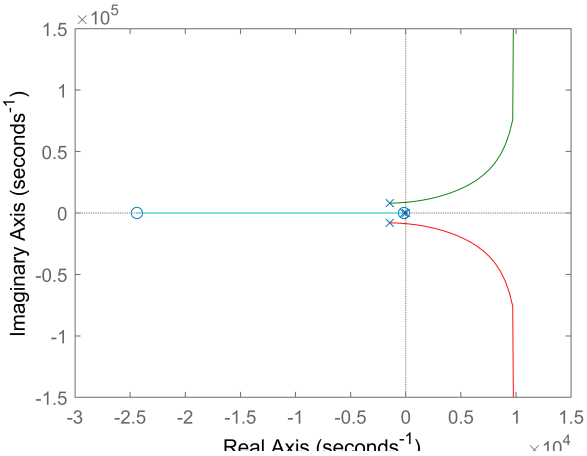


Figure 3-6: Root locus of open loop controller-LCL plant system

#### 3.2.2.2 Voltage compensation

However, for obtaining reference voltages on the input of the converter to be achieved by control, the coupling terms of d and q voltage components have to be

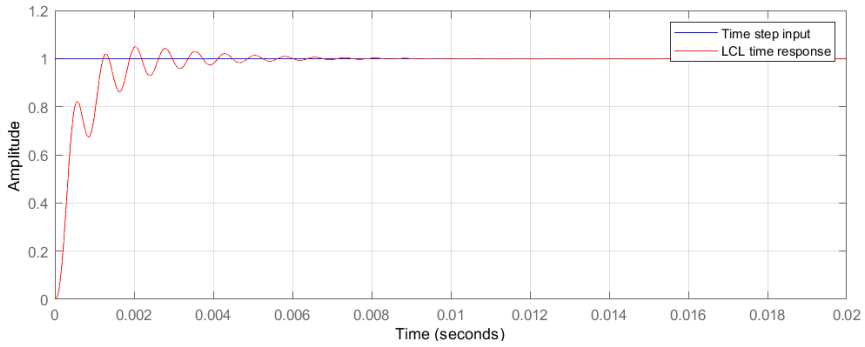


Figure 3-7: Step response of closed loop design for LCL filter

taken into account. That is accomplished by incorporating voltage compensation. Substituting LCL filter with the same equivalent circuit introduced in the previous section, voltage references of the active rectifier will be expressed by Equation 3.6 and Equation 3.7. Other components apart from voltage drop on the filter should be included in the voltage compensation.

$$u_{rd} = -[Ri_{rd} + L\frac{di_{rd}}{dt}] + \omega L i_{rq} + e_d \tag{3.6}$$

$$u_{rq} = -[Ri_{rq} + L\frac{di_{rq}}{dt}] - \omega L i_{rd} + e_q \tag{3.7}$$

#### 3.2.2.3 Limit of voltage command

For the design of control loop physical constraints of the system weren't taken into account. Output control voltage that could be applied for step change of reference current is limited by supply and maximum allowed ratings of components (IGBTs, DC link capacitor...). The maximum amplitude of reference voltage on the AC side of the active rectifier is $\frac{V_{dc}}{2}$. As shown on the model on figure 3-4 amplitude of the space vector defined by d and q voltage components are limited by performing Cartesian to Polar and then back transformation.

Still, this doesn't prevent the windup effect of integration caused by unlimited control effort which will build up integrator and cause high overshoots. Thus, various anti-windup techniques to limit control output are developed. The one implemented

for all controllers in the application will be explained in separate Section 3.5. This section will keep the focus on the determination of output reference voltage limit. The limit controller output applied is in range of $[-\frac{V_{dc}}{2}, \frac{V_{dc}}{2}]$, imposed by DC link voltage. However, this is not completely accurate since the output of the controller is the voltage drop on the AC line filter and not the one on converter.

One solution would be to further decrease the voltage range to minimize the windup effect on integration. But, there is the trade-off between minimizing the windup effect and performance of the controller. Reducing maximum voltage control effort that could be applied can significantly slow down controller response. That is an especially critical issue in cascade control as it can come close to the speed of the outer loop or be even slower. That can lead to instability, as a cascade control relies on the assumption that the inner loop is considered instantaneous with respect to the dynamic response of the outer loop.

### 3.2.3 DC voltage control

The design of control of DC link voltage will consider power balance in DC link circuit. Power flow through the capacitor will be expressed as the sum of power injected from the grid and power coming from the load (power from permanent magnet machine) by Equation 3.8.

$$\frac{1}{2}C\frac{dv_{dc}^2}{dt} = P - P_o \tag{3.8}$$

Substituting Equation 2.9 for active power previously derived in Equation 3.8, Equation 3.9 is obtained.

$$\frac{1}{2}C\frac{dv_{dc}^2}{dt} = \frac{3}{2}E_m i_{rd} - P_o \tag{3.9}$$

#### 3.2.3.1 Design of voltage controller

Relation derived in the previous section 3.9 is expressing DC voltage as a function of $i_{rd}$ current component. Square value of the DC link voltage will be replaced with new variable $W$, which will transform the problem to control of the linear system.

Power coming from the load will be considered as disturbance of the system. After applying Laplace transform on equation 3.9 transfer function of the plant obtained is used for the design of the controller. Closed-loop of the control variable $W$ ($W = v_{dc}^2$) is shown on figure 3-8. The inner current loop is considered instantaneous with respect to the voltage loop.

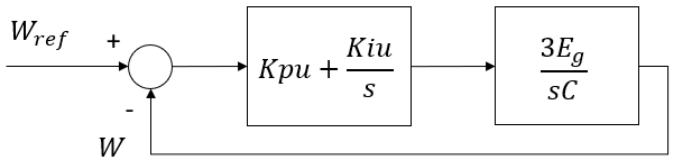


Figure 3-8: Closed loop of squared voltage (W)

The plant of the system contains just integrator. Thus, a proportional component will provide zero steady state error tracking of step reference, but an integral component is introduced to enable disturbance rejection imposed by load [23]. Proportional component of DC voltage controller is calculated using equation 3.10.

$$K_p = 2\pi BW_u \frac{C}{3E_m} \tag{3.10}$$

#### 3.2.3.2 Saturation limit of $i_{rd}$ current reference

The $i_{rd}$ current component is directly controlling active power flow. Thus, reference of d current component $i_{rd\_ref}$, which is output of voltage controller, is limited by power rating of the whole system. Power elements of whole system are sized to rated power of PM machine. Consequently, maximum reference current available can be expressed from Equation 2.9 by Equation 3.11.

$$i_{rdMAX} = \frac{2}{3}\frac{P_n}{E_m} \tag{3.11}$$

### 3.2.4 Design of the Phase Locked Loop

This section explains the implementation of the Phase Locked Loop for providing information on the grid voltage angle required for coordinate transformations. Principal used is one of conventional PLL solutions for three-phase systems described in [24] called **dqPLL**. The block diagram of the implementation of dqPLL is shown on Figure 3-9. It is based on abc stationary to dq0 synchronous reference frame coordinate transformation, explained in Appendix A. The graphical representation of transformation is shown on Figure 3-10, based on which d and q components of the grid are expressed with Equation 3.12 linearized around the operating point.

Closed-loop of q-component of the grid voltage $e_q$ tracks a zero reference. For imposing zero reference of $e_q$ voltage the component error $e$ will be expressed with Equation 3.28. For no steady state error tracking the output angle will match the grid angle ($\theta_x = \theta$) and voltage space vector will align with d-axis. This method assumes a balanced grid supply. [24]

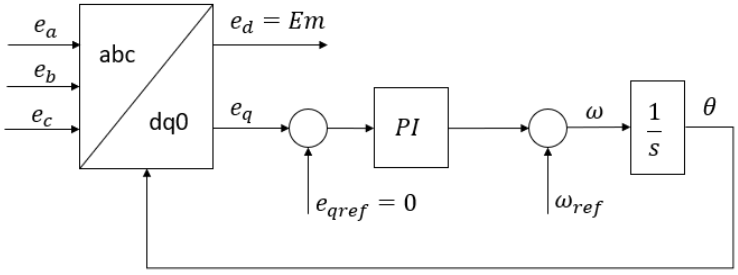


Figure 3-9: The dq Phase Locked Loop

$$\begin{aligned} e_d &= E_m \cos(\theta - \theta_x) = E_m \\ e_d &= E_m \sin(\theta - \theta_x) = E_m(\theta - \theta_x) \end{aligned} \tag{3.12}$$

$$e = E_m(\theta_x - \theta) \tag{3.13}$$

The linearized closed-loop control of the grid angle based on which PI controller

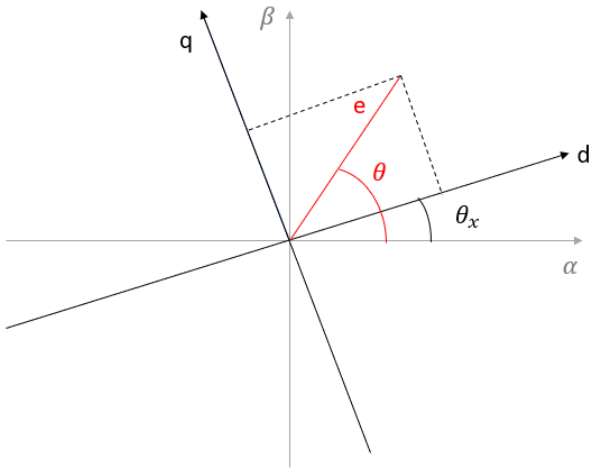


Figure 3-10: dq0 transformation of grid voltage

components are derived is shown on Figure 3-11. From the second-order transfer function of closed loop system, the proportional and integral components will be calculated using Equation 3.14 and Equation 3.15.

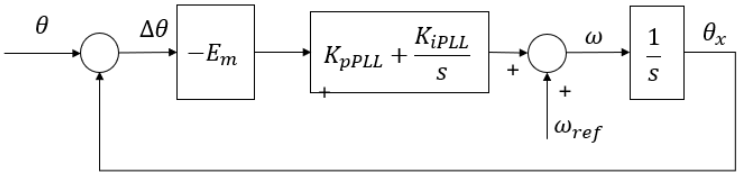


Figure 3-11: Linearized closed loop of grid angle

$$K_{pPLL} = \frac{4\pi BW_{PLL}}{E_g v} \tag{3.14}$$

$$K_{iPLL} = \frac{(2\pi BW_{PLL})^2}{E_g v} \tag{3.15}$$

## 3.3 Control of the permanent magnet machine

Mature control strategy that is one of the standards for control of AC machines is Field Oriented Control. FOC control is the vector control strategy that enables

separate control of the excitation flux and mechanical variable (torque and/or speed) using coordinate transformations. This effect is achieved by performing control of transformed variables in the rotating dq0 reference frame which is aligned with teh rotor flux vector. As explained more detailed in Section 2.2.1, comparing all AC machines, the position of flux vector is the easiest to determine for PM machine as it is rotating with rotor speed. Block diagram of control structure is given by Figure 3-12. This part will focus on control of the permanent magnet machine and thus DC link will be replaced with ideal voltage supply. For this application, the outer loop controls rotor speed, and the controller provides the reference of $i_{mq}$ component of stator current. That will be further explained in Section 3.3.2 about the design of the speed control loop. Control of the current d and q component loops is a direct consequence of the chosen strategy for regulating excitation flux and torque respectively. This application doesn't require operation above rated speed and thus neither implementation of flux weakening control. For sake of robustness of application only excitation torque is used and reference of d component of stator current $imd$ set to zero (equation 2.24) It follow that adapted torque equation 3.16 is obtained. Information about the position required for coordinate transformation is obtained from an encoder. Gain $K_n$ on the figure is constant multiplication to obtained electrical speed in $rad/s$ from mechanical speed in $rpm$ which is a function of the number of pole pairs.

$$T = \frac{3}{2} p \Psi_{PM} i_{mq} = K_t i_{mq} \tag{3.16}$$

Looking at the structure of FOC given by Figure 3-12 doesn't surprise that many authors refer to earlier discussed VOC for control of active rectifier as Virtual Flux Control. This analogy will be used in further discussion on the FOC strategy for the PM machine.

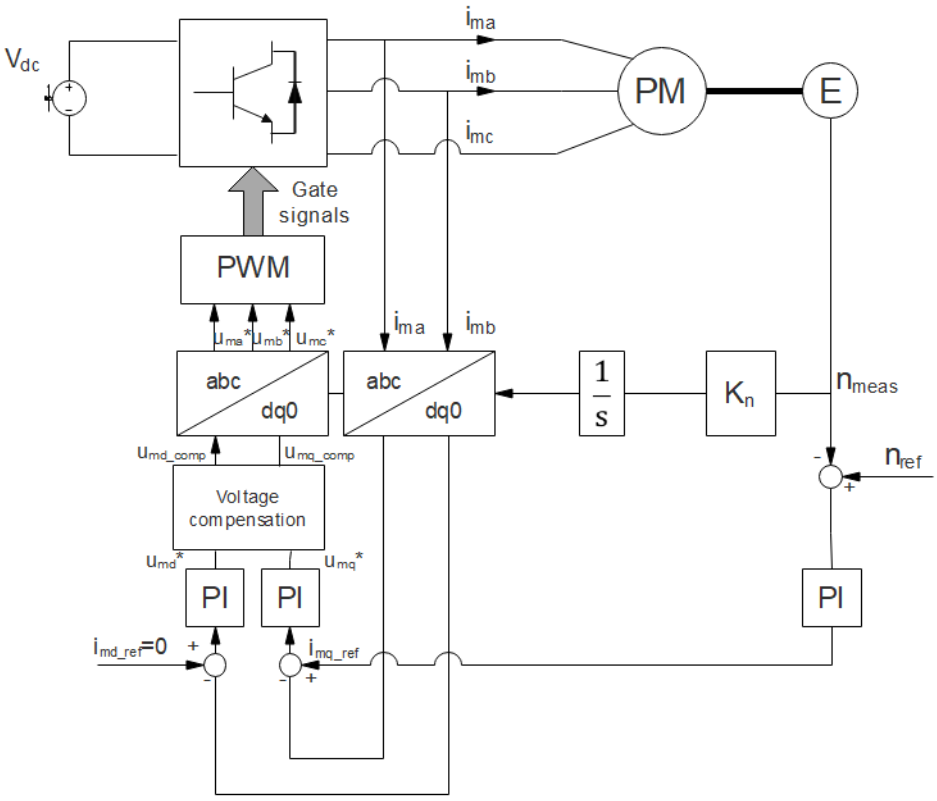


Figure 3-12: FOC of permanent magnet machine

### 3.3.1 Current control loop of the permanent magnet machine

Similar to the control of active rectifier, the goal of the current control of the permanent magnet machine is to control current components independently. Still, as can be observed from equations 2.22 and 2.23 for stator voltage components, the d and q axis are not completely independent of each other as coupling terms between them are still present. Thus, the approach to the design of current control will develop in the same manner as for active rectifier. The analogy refers to the structure of the control loop as well, which will have the same structure as one on Figure 3-4.

#### 3.3.1.1 Design of the current controller

The role of the current controllers is to perform independent control of stator current components and based on error between reference and measurement generate

voltage command. So, the coupling terms will be neglected for the controller design. Taking it into account, closed loop system with plant obtained is shown on Figure 3-13, where x is replaced with the corresponding axis (d and q). Since the model is assuming salient machine, d and q axis inductance values will differ.

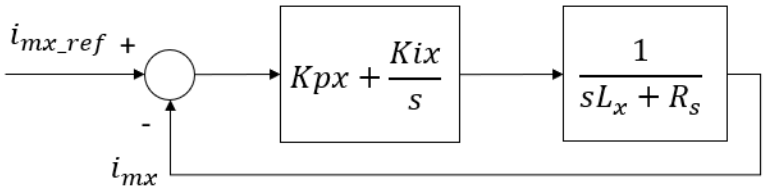


Figure 3-13: Simplified current closed loop of PM machine

By closing the loop, second order transfer function is obtained. Based on bandwidth and overshoot requirements for second order closed loop system performance, Equation 3.17 and Equation 3.18 for calculating proportional and integral parameters of the controller are derived. Parameter $\zeta$ is damping factor and directly related to overshoot as expressed by Equation 3.19. As the fastest control loop in FOC implementation is a current loop, the chosen bandwidth is 5 times slower from switching and desired overshoot 10%.

$$K_{px} = 4\pi BW_c \zeta L_x - R_s \tag{3.17}$$

$$K_{ix} = (2\pi BW_c)^2 L_x \tag{3.18}$$

$$\zeta = \arctan(-\frac{M_p}{\pi}) \tag{3.19}$$

#### 3.3.1.2 Voltage compensation

According to the design of controllers, the output voltage of the controller in the ideal case will be voltage drop on stator resistance $R_s$ and self inductance $L_d$ or $L_q$

for corresponding axis controller. To have stator voltage as output control command coupling terms also have to be included on the output of controllers according to voltage equations, Equation 2.22 and Equation 2.23.

#### 3.3.1.3 Output voltage saturation

For the big step changes of the reference value control may require high control effort to achieve it, which cannot be provided by power system. As the consequence of that will occur windup effect of integration in which integrator will build-up trying to compensate for the error, and cause overshoot and slow down the system. To prevent this voltage command has to be saturated and controller " notified" of it, so that windup effect doesn't occur. That is achieved using anti-windup control methods. The one implemented for controllers in theb whole system will be explained in Section 3.5. Imposed by limitation of PWM, stator voltage command has to be in range of $[-\frac{V_{dc}}{2}, \frac{V_{dc}}{2}]$. For limiting the output of controller same allowable range of output voltage is used which didn't account on the influence of coupling terms.

### 3.3.2 Speed control

The main goal of this control strategy regarding the application is to control the speed of the rotor shaft. It is logical to start from the dynamic equation of model describing the mechanical system (Equation 2.17), where it can be seen that rotor speed is a function of parameters of the system and electromagnetic torque. Substituting torque with Equation 3.16, Equation 3.20 which provides relation between rotor speed and $i_{mq}$ stator component is derived. The conclusion is that speed of rotor can be regulated by acting on $i_{mq}$ current component in outer loop.

$$J\frac{d\omega}{dt} + B\omega = K_t i_{mq} - T_m \tag{3.20}$$

#### 3.3.2.1 Design of speed controller

Speed controller is acting in outer loop and for speed error input generates reference of $i_{mq}$. Approach to the design of cascade control used is that inner loop has much faster response, and thus can be considered instantaneous with respect to the outer control loop. Assuming unity closed loop transfer function of inner loop, closed loop of outer, speed loop will be graphically represented by block diagram on Figure 3-14. By its definition rotor speed in Equation 3.20 is in $rad/s$. For imposing control action of speed in $rpm$ coefficient K is adapted ($K = K_t\frac{30}{\pi}$). Furthermore, load torque $T_m$ represents disturbance for the system. Based on obtained second order closed loop transfer function and performance requirements (bandwidth and overshoot) Equations 3.21 and 3.22 for calculating proportional $K_{ps}$ and integral component $K_{is}$ are derived. For the design of the system coupled to the induction machine should be considered an equivalent moment of inertia of both PM machine and induction machine.

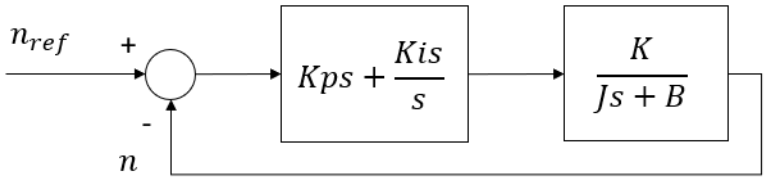


Figure 3-14: Speed closed loop of PM machine

$$K_{ps} = (4\pi BW_s\zeta J - B)\frac{1}{K} \tag{3.21}$$

$$K_{is} = (2\pi BW_s)^2 J\frac{1}{K} \tag{3.22}$$

#### 3.3.2.2 Output $i_{mq}$ current saturation

Limits of the operation of PM machine are determinate by rated values assigned by manufacturer. Providing that reference of $i_{md}$ component is zero, maximum allowable

value of $i_{mq}$ will be maximum value of rated current ($\sqrt{2}I_{rat}$), or given by Equation 3.23 if expressed as function of rated power.

$$i_{mq\_max} = \frac{P_{rat}}{K_t \omega_{rat}} \tag{3.23}$$

## 3.4 Controller discretization

For moving the system designed in continuous domain to discrete, method for approximation of definite integration called "Tustin" or trapezoidal is used. This method approximates real area under function with area of trapezoid under straight line connecting two successive samples. Written in z-domain integration will be defined by relation 3.24. Transformation from continuous to discrete PI controller is performed by substituting definition of integrator in s-domain for one in z-domain. Relation obtained is given by Equation 3.25 where $K_p$ and $K_i$ are generic values of proportional and integral component of PI controller in s-domain (continuous time).

$$Z\left\{\frac{1}{s}\right\} = \frac{T}{2}\frac{z+1}{z-1} \tag{3.24}$$

$$Z\{PI(s)\} = K_p + K_i\frac{T}{2}\frac{z+1}{z-1} \tag{3.25}$$

The same expression can be transformed in generic form given by Equation 3.26 with coefficients expressed as functions of $K_p$ and $K_i$ in the continuous time domain.

$$PI(z) = \frac{U(z)}{E(z)} = \frac{b_0 + b_1 z^{-1}}{a_0 + a_1 z^{-1}} \tag{3.26}$$

Rewriting equation in terms of samples, the output control command can be expressed as function of previous outputs, and current and previous errors [1] as expressed by equation 3.27.

[1]Notation used is referring to U(z) or u[0] as current sample value and $z^{-1}U(z)$ or u[1] as the previous sample

$$u[0] = \frac{1}{a_0}(b_0 e[0] + b_1 e[1] - a_1 u[1]) \tag{3.27}$$

This expression gives a tool to implement PI control action in DSP and generate new voltage command based on previously stored samples of voltage command and input error. Multiplication coefficients can be calculated as functions of controller components obtained by design in the continuous domain.

## 3.5 Anti-Windup implementation

Anti-windup is any control method used to prevent or reduce the effect of integration of error when the output command exceeds the saturation limit. The most convenient way to explain the applied method on a discrete controller is given by the algorithm on Figure 3-15. After the new controller output command is calculated, the execution of the anti-windup algorithm takes place. As explained on the figure, in case the output command exceeds the saturation limit, the output command is saturated. Moreover, the error will be updated for saturated control action as given by Equation 3.28, and prevent a windup of integrator.

$$e[0] = \frac{1}{b_0}(a_0 u[0] - b_1 e[1] + a_1 u[1]) \tag{3.28}$$

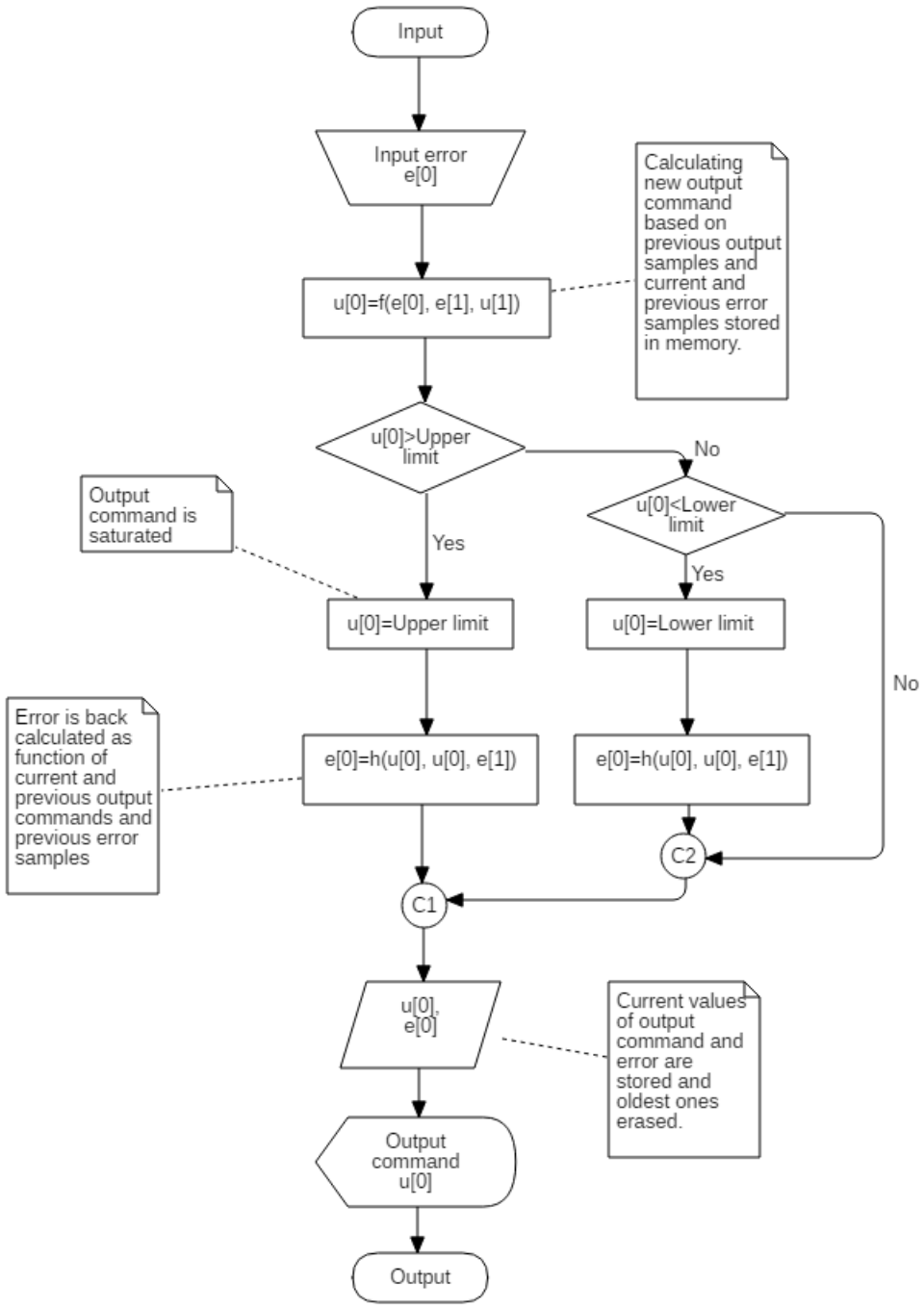


Figure 3-15: Algorithm of the implementation of Anti-Windup on the discrete controller

# Chapter 4

# Design of application setup

This chapter will cover all aspects of the design of the application setup to be implemented. The general idea of the complexity of the system is given by a schematic of its main elements of and their interaction. Approach to the design will be discussed through the three main parts:

1. Design of power setup

2. Design of PCB interface

3. Software implementation

The first part will consider the design of the elements required to provide power flow and interface application to the grid, taking into account constraints of the application. The design of the interface of the application to the control is including measurements obtained from transducers and PCB interface between the power stage and DSP providing a bidirectional flow of signals, discussed in second and third section. The final part is a software implementation of the control strategy that will provide control action to the power conversion stages, based on input references and feedback signals from the system.

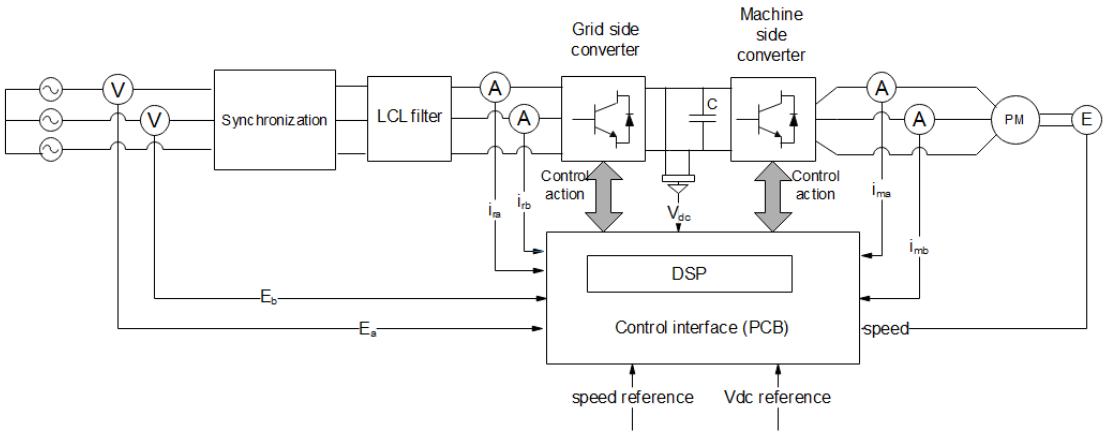


Figure 4-1: Setup of application system

## 4.1 Design of the power stage

Design of the power stage includes all the elements that participate in transfer of power through system, converting mechanical energy to electrical. It will include two categories, active and passive elements of power stage.

### 4.1.1 Active elements of power stage

Active elements of the power stage are defined as the elements which contain switching devices and can change state depending on applied command. These elements have an " active role " in performing control action.

#### 4.1.1.1 IGBT module and drive circuit

For the implementation of the back-to-back converter are used two ABB three-phase IGBT switching modules and drive circuit packages *FS450R17KE3/AGDR-72C S*. This section will point out on characteristic of converter important for switching operation and design of other elements in the setup. All rated values and safe operating limits of the IGBT module are defined in datasheet [25]. The IGBT module has as well included NTC thermistor, providing information about the working temperature of the module. That enables an additional state variable for observation and control

of the operation of IGBT modules.

Documentation with the description of the ABB drive circuit was provided by the company. Opto-isolation between I/O signals and power circuit driving IGBTs is predicted by design. The PCB drive requires an external voltage supply (5V and 24V). Gate switching circuit requires both " switch ON " and " switch OFF " command signals, which will convert to a positive voltage gate signal for switching ON and negative voltage signal for switching OFF the IGBT. Moreover, drive provides *Status* signal from IGBT indicating if IGBT switched. *Status* signal is " LOW " for switch turned on (no voltage drop on the IGBT) and " HIGH " for switch turned off. All I/O signals of the IGBT module drive circuit are available on pins of connector, including connection for external voltage supply.

#### 4.1.1.2 Synchronization to the grid

The control must ensure synchronization to the grid to be able to regenerate power back to the grid, which is achieved with PLL implementation explained earlier. The PLL control implemented has to be resistant to variations of the grid such as harmonics, voltage sags, and commutation notches. [26]. Furthermore, synchronization must as well handle any kind of measurement noise. For additional safety, required by project description, industrial synchronizer *Synchromax* is used. [27] It will disconnect application from the grid if amplitude, phase, and frequency between measured voltages are in disbalance, out of allowable tolerance set.

### 4.1.2 Passive elements of power stage

Design of all the elements in the power stage that have " passive role " and on which cannot be applied direct control command will be explained in this section.

#### 4.1.2.1 Permanent magnet machine

The central element of the power stage is a permanent magnet machine that will convert mechanical energy to electrical, acting as a generator. Rated characteristics

of the permanent magnet machine are defined according to requirements for testing a commercial inverter and rated power of induction machine mechanically coupled to PM machine. The PM machine that shall be used in the project is custom made machine to comply with characteristics listed in Table 4.1.

Table 4.1: PM machine parameters

| | | |
|---|---|---|
| **Rated power** | kW | 40 |
| **Rated speed** | rpm | 1500 |
| **Rated voltage** | V | 400 |

#### 4.1.2.2 Design of DC link capacitor

The DC link capacitor is one of crucial elements in AC-DC-AC conversion of energy, which should provide stable DC voltage. Key parameters that are defining operation of capacitor and should comply with requirements of application and provide satisfying performance are:

- Capacitance
- Rated voltage
- Current ripple
- Voltage ripple
- Hot spot temperature or power dissipation

**Capacitance** is the ability of a capacitor to store energy in the form of an electric charge. DC link capacitor is a high capacity capacitor intended to store a big amount of energy. Bulky capacitors commonly used for this kind of application are electrolytic capacitors due to high rated capacitance values available. Still, the limiting feature of this type of capacitor is relatively low current ripple that can be sustained, which will further prove to be substantial for this application design. Thus, the use of film capacitor solution with design adapted to DC link will be considered instead, with a high range of capacitance and allowable current ripple.

**Rated voltage** is the maximum allowable peak voltage value on capacitor in normal operating conditions. Thus, the capacitor has to be designed such that it can supply the required voltage to the permanent magnet machine and provide proper operation of the active rectifier. As stated in [3], it is required that the voltage of DC link is higher than peak voltage that could be generated solely by diode (passive) rectifier to ensure full controllability of active rectifier. The modulation technique used in this application is synchronous switching, as explained in Section 3.2.1. The relation between the average value of AC input voltage of converter and DC link voltage is expressed by Equation 4.1. [28] In case of overmodulation, with chosen M of $\sqrt{3}$, rounded value of reference voltage of DC link calculated from Equation 4.2 will be $V_{dc\_ref} = 1200V$. To ensure safe operation rated voltage of the capacitor should be higher than the reference voltage.

$$M\frac{V_{dc}}{2} = E_m \tag{4.1}$$

$$V_{dc} = \frac{2}{\sqrt{3}}E_m \tag{4.2}$$

**Current ripple** is another critical parameter for choosing the DC link capacitor. Switching applications introduce a high-frequency harmonics, and thus capacitor should be able to sustain ripple current imposed. The analytical equation used to calculate the maximum RMS value of the current ripple on the DC link capacitor is given by Equation 4.3, from [29].

$$I_{ripple} = 2I_r\sqrt{M(\frac{\sqrt{3}}{4\pi} + \cos\phi(\frac{\sqrt{3}}{\pi} - \frac{9}{16}M))} \tag{4.3}$$

For back calculated M using Equation 4.1 and chosen reference voltage, the value of current ripple calculated from Equation 4.3 is $I_{ripple} = 50,85A$. Also, it is closely matching to the one obtained by simulation on Figure 4-2 (red-obtained by simulation, blue-analytically calculated).

Based on the previously obtained values is chosen polypropylene-based film ca-

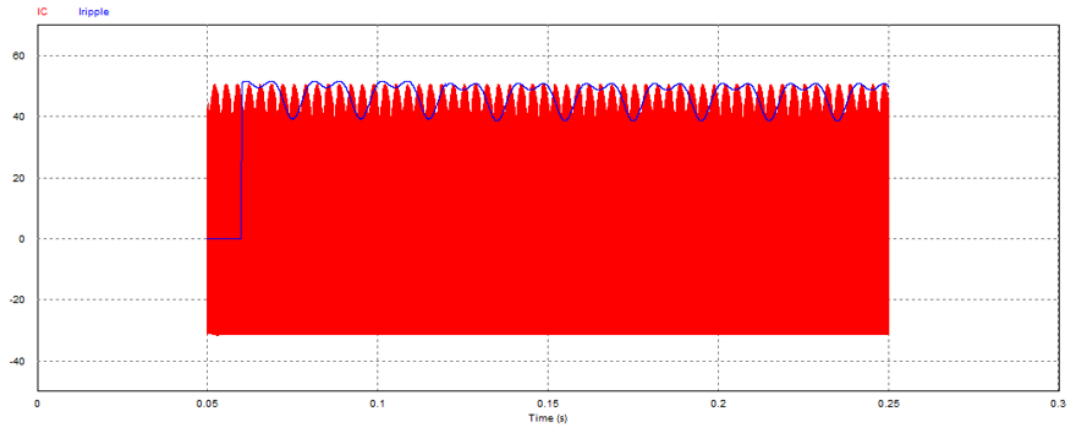


Figure 4-2: Current ripple through DC link capacitor

pacitor, fully described in [30]. The main parameters of interest for design are shown in Table 4.2. The rest of the main features listed have to be calculated according to parameters of the specific capacitor provided by the manufacturer.

**Voltage ripple** on the capacitor in steady state is calculated based on the capacitor equivalent circuit, which includes a series connection of capacitance, equivalent resistance and equivalent inductance of the capacitor. Substituting their values and ripple current value previously obtained in Equation **??** voltage ripple obtained is $V_{ripple} = 3,37V$. This is as low as $(0,3\%)$ of reference voltage and acceptable value for the design.

$$V_{ripple} = I_{ripple}\sqrt{(2\pi f ESL - \frac{1}{2\pi f C})^2 + ESR^2} \tag{4.4}$$

**Hot spot temperature** is calculated based on the mathematical model provided by the manufacturer, depending on losses in machine and ambient temperature. [30] Obtained hot spot temperature is $46°C$

#### 4.1.2.3 Design of LCL filter

Because of the switching of converters high order harmonics are generated and injected to the grid. To keep it inside allowed limits they should be attenuated implementing filter. The filter topology used for this application is the LCL filter.

Table 4.2: DC link capacitor parameters provided by manufacturer

| | | |
|---|---|---|
| **Capacitance** | $\mu F$ | 600 |
| **Rated voltage** | V | 1400 |
| **Rated current ripple** | A | 66 |
| **ESR** | $m\Omega$ | 3 |
| **ESL** | nH | 100 |
| **Maximum hotspot temperature** | $^{\circ}C$ | 95 |

According to researchers, the LCL filter is a preferable solution comparing to a line L filter. the LCL filter shows better attenuation capability on high order frequencies. [31,32] Also, it provides cost-effective solutions due to smaller inductance, which implies a smaller size of inductors, for achieving the same performance. [33,34] However, due to the resonance of the circuit, the filter will even amplify harmonics at the resonant frequency and contaminate the grid, or even cause instability. [31]. The solution implemented to prevent the damping on resonant frequency for this application is passive damping, with serious resistance connected as shown on Figure 4-3.

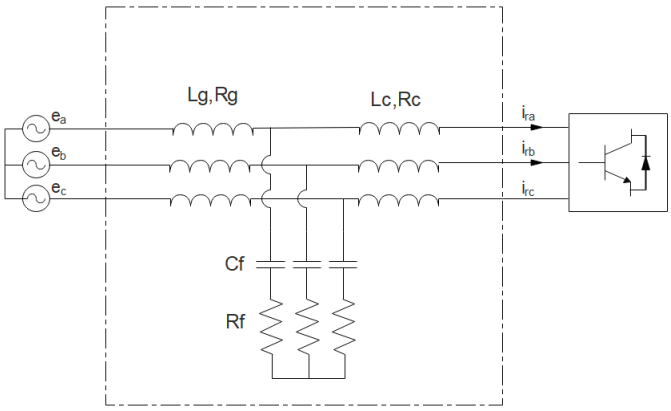


Figure 4-3: LCL topology implementation

Step by step procedure of the design of LCL filter performed is explained in [34]. With the given approach some base values used for simplifying calculation are defined. Equation 4.5, Equation 4.6 and Equation 4.7 are defining base, per phase, values of power, speed pulsation and input voltage respectively.

$$P_b = \frac{P_r at}{3} \tag{4.5}$$

$$\omega_b = \omega_r at \tag{4.6}$$

$$E_b = \frac{U_l}{\sqrt{3}} \tag{4.7}$$

The design of the filter capacitance $C_f$ is considering the limitation of reactive power injected to the grid by introducing filter capacitance. This constraint is expressed by Equation 4.8. The chosen value is the first lower commercial value of capacitance.

$$C_{fmax} = x_c \frac{P_b}{\omega_b E_b^2} \tag{4.8}$$

Converter side inductance $L_c$ value will be determinate based on limit of maximum current ripple that can occur on the AC/DC converter input. Equation 4.9 is expressing the maximum current ripple that occurs for M=0,5. [34]. Chosen maximum acceptable current ripple is 20% of maximum current value calculated by Equation 4.10. Combining both conditions, $L_c$ is calculated using Equation 4.11.

$$\delta i_{max} = \frac{V_{dc}}{6 f_{sw} L_c} \tag{4.9}$$

$$I_{max} = \sqrt{2} \frac{P_b}{E_b} \tag{4.10}$$

$$L_c = \frac{V_{dc}}{6 f_{sw} 0,2 I_{max}} \tag{4.11}$$

Furthermore, grid side inductance $L_g$ will be calculated in order to limit current harmonics injected to the grid, expressed by Equation 4.12. The equation is taking into account the relation between harmonics injected to the grid and harmonics generated by inverter itself ($k_a = \frac{i_g}{i_i}$). The parameter $r$ is the relation between the

converter and the grid side inductance.

$$L_g = \frac{\sqrt{\frac{1}{k_a^2}} + 1}{C_f(2\pi f_{sw})^2} \tag{4.12}$$

The LCL filter topology will introduce resonance in the circuit, which will cause an effect of amplifying high-frequency harmonics. Therefore, design predicts passive damping, introducing series resistance which will attenuate harmonics close to the resonant frequency. Equation 4.13 is expression for resonant frequency derived for the LCL equivalent circuit at high frequencies, shown on Figure 4-4. The resonant frequency calculated has to be inside limits of the ten times of grid frequency and Nyquist frequency ($10f_{grid} < f_{res} < \frac{f_{sw}}{2}$).

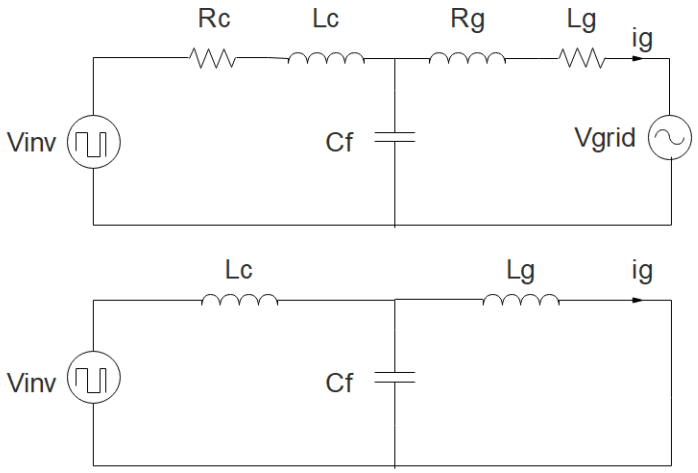


Figure 4-4: Equivalent circuit of LCL at fundamental frequency (upper) and at high frequencies (lower)

$$\omega_{res} = \sqrt{\frac{L_c + L_g}{L_c L_g C_f}} \tag{4.13}$$

For sufficient phase margin and high attenuation at the resonant frequency, the value of damping resistance will be calculated according to Equation 4.14. Damping is introducing zero which will attenuate resonance as it is shown on Bode plots on Figure 4-5, where the blue plot is the frequency response of the filter with passive damping.

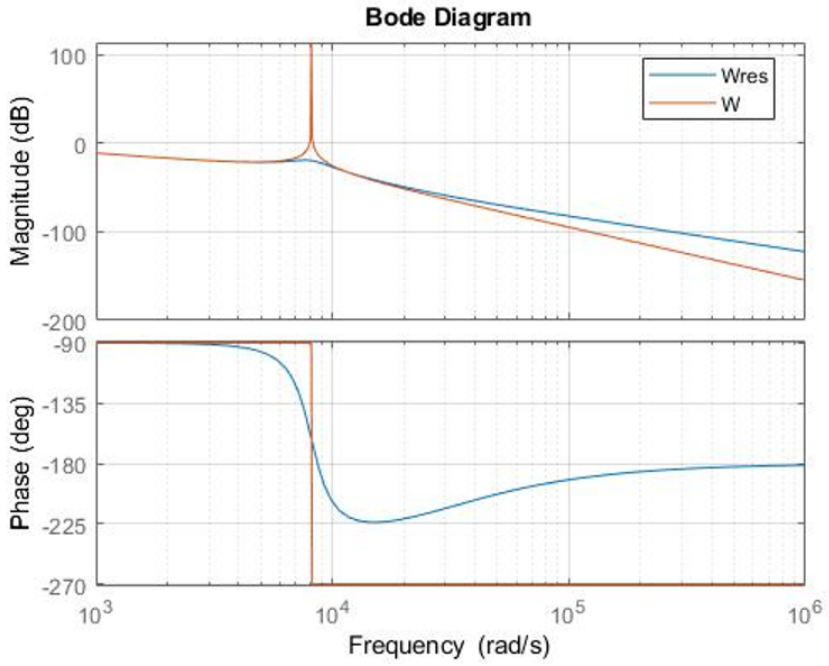


Figure 4-5: Bode diagram of undamped LCL filter (red) and of LCL filter with series damping resistor (blue)

$$R_f = \frac{1}{3\omega_{res}C_f} \tag{4.14}$$

Parameters obtained following previous discussion are listed in Table 4.3.

Table 4.3: PM machine parameters

| | | |
|---|---|---|
| **Filter capacitance** $C_f$ | $\mu F$ | 35 |
| **Damping resistance** $R_f$ | $\Omega$ | 1,17 |
| **Converter side inductance** $L_c$ | mH | 3,2 |
| **Grid side inductance** $L_g$ | $\mu H$ | 500 |

## 4.2 The selection of transducers

The closed loop design described in previous chapter requires feedback signals, obtained by measurements from power stage being controlled. Conditions to be considered for the choice of transducers are following:

- Required measurement range of variable,
- Isolation of measurement signal from the power circuit,
- External power supply.

As not predicted by requirements of the project, special requirements on mechanical, mounting or environmental conditions. Feedback variables needed to be provided by measurements are:

- Phase current of active rectifier of phase A and phase B,
- Phase stator current of phase A and phase B,
- Phase grid voltage of phase A and phase B,
- DC link voltage,
- Speed measurement.

### 4.2.1 The electrical transducers

For the measurement of electric variables (currents and voltages) Hall effect based transducers are chosen. This is a robust solution which provides electrical isolation of signaling circuit from the power circuit. *LEM* transducer from *DVL* series is chosen for voltage measurement and *LA 205-S* for current measurement. The specific transducer is chosen based on the primary measurement range. The output signal on the secondary side is the voltage drop on resistor connected in series with the secondary circuit, as depicted on Figure 4-6. Thus, " gain ", or measurement range on the output of transducer depends on chosen output resistance. Table 4.4 is giving information on the input measurement range and output measurement signal obtained from design, which will be input to the signal processing circuit of the PCB interface. The supply for each transducer is external of $+/-15V$ voltage level.

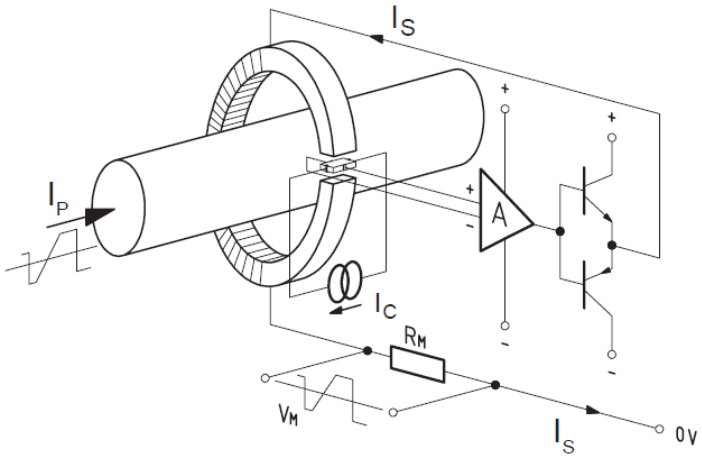


Figure 4-6: Hall effect based measurement of *LEM* current transducer [4]

Table 4.4: Measurements ranges of transducers

| **Variable** | **Primary measurement range** | **Secondary signal range** |
|---|---|---|
| Phase current | $[-200, 200]A$ | $[-6, 6]V$ |
| Phase grid voltage | $[-1500, 1500]A$ | $[-7,5; 7,5]V$ |
| DC link voltage | $[-2250, 2250]A$ | $[-7,5; 7,5]V$ |

### 4.2.2 Speed measurement

Speed measurement is obtained from incremental encoder by *Kübler* with parameters of interest for design given by Table 4.5. For quadrature encoder, which is counting both rising and falling edges of A and B signal, resolution will be four times bigger (4*1024 pulses per rotation).

Table 4.5: PM machine parameters

| | | |
|---|---|---|
| **Maximum speed** | rpm | 6000 |
| **Number of pulses per revolution** | | 1024 |
| **Voltage supply** | V | 5 |

## 4.3 Design of the PCB interface

The control implemented in this PM machine drive application requires a bidirectional flow of information and signals, as is conceptually shown on Figure 4-1. Thus, the application requires an interface between the power stage and DSP control. For that purpose is designed the PCB interface, which performs different functions that will be discussed in detail in the following sections.

### 4.3.1 The digital signal processor

The central element on the PCB interface is a digital signal processor, which processes all the information obtained from the system and perform control action executing imported code. The digital signal controller used for this project is *Texas Instruments TMS320F28335*. This series is recommended for a motor drives application by the manufacturer due to its high-performance processing, sensing, and actuation for closed-loop real-time applications. The features of DSP that are of interest for implementing application are [35]:

- High performance, defined with up to 150MHz system clock speed.
- Enabled interrupts with fast response and processing time.
- Control card available on-chip flash memory.
- programmable PWM output control peripherals.
- Analog-to-digital conversion with two sample-and-hold switches, switching simultaneously on up to 12 signals.
- eQEP feature for processing signals from the encoder.
- Supported numerous standards, particularly of interest JTAG industry standard.

The control card is placed in the connector on the PCB and there is direct access to all pins of the control card. Thus, the standard external supply of 5V should be provided from the PCB. All standard electrical characteristics for safe operation are given in [35]. The standard " high " voltage level of all General purpose I/O signals of a microprocessor is 3,3V. Range of analog-to-digital conversion input signal is 0 to 3V. [36]

### 4.3.2 Input signals interface

This section relates to the processing of PCB applied on input signals to DSP from any external source (power stage, PC). They will require a different approach to design depending on the input port type mentioned in Section 4.3.1 and signal interpretation and logic. Further clarification will come with the following sections.

#### 4.3.2.1 The measurement signals processing

**Analog measurement signals** of electrical variables required for control action need to be imported in microcontroller, using its analog-to-digital conversion feature. To do so, design for processing this signal will comprise three stages as shown on Figure 4-7.

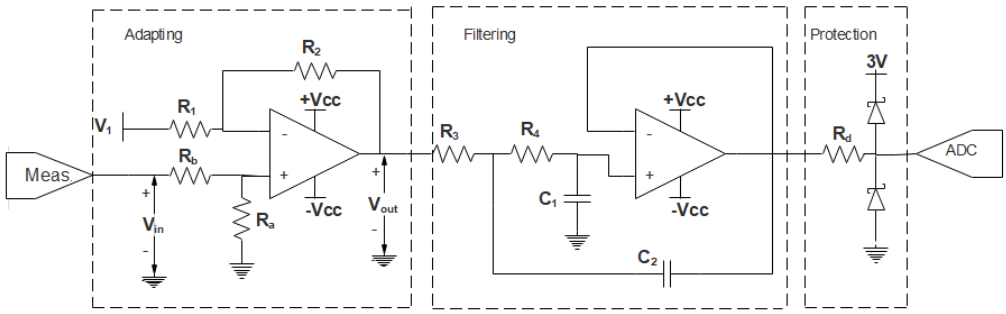


Figure 4-7: Design of the measurement signal processing

The function of the adapting stage is to adapt the input voltage level coming from the measurement of transducer (Section 4.2) to the voltage level allowed on the ADC

input of a microcontroller. The design implemented is using an operational amplifier with negative feedback. Assuming the conditions of ideal operational amplifier, the function relating the input and output voltage of this stage will be expressed by Equation 4.15.

$$V_{out} = \frac{R_a(R_1 + R_2)}{R_1(R_a + R_b)} V_{in} - \frac{R_2}{R_1} V_1 \tag{4.15}$$

With chosen reference voltage $V_1 = -5V$ Equation 4.15 will have the same structure as mathematical rule of transformation depicted on Figure 4-8. The minimum and maximum value of input voltage on the figure are the minimum and maximum value of the measurement signal coming from the transducer. Solving system of equations for defined mathematical rule of transformation, resistors can be chosen such that circuit performs required transformation of voltage level.

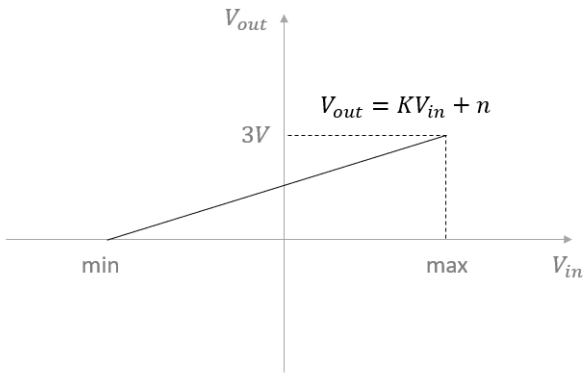


Figure 4-8: Mathematical transformation rule of adapting stage

Verification of the design for voltage measurement performed in *TINA-TI* simulation tool is shown on Figure 4-9. The adapting stage is adapting sinusoidal wave varying from -7,5V to 7,5V (minimum and maximum value of voltage measurement signal) to 0 to 3V.

The filtering stage is implemented with second order *Sallen-Key* low-pass filter. Cut-off frequency must be in the range between 10 times bigger than fundamental and half of a switching frequency. Chosen cut-off frequency for the design is 1kHz and design is obtained using *Texas Instruments* software tool *FilterPro*.

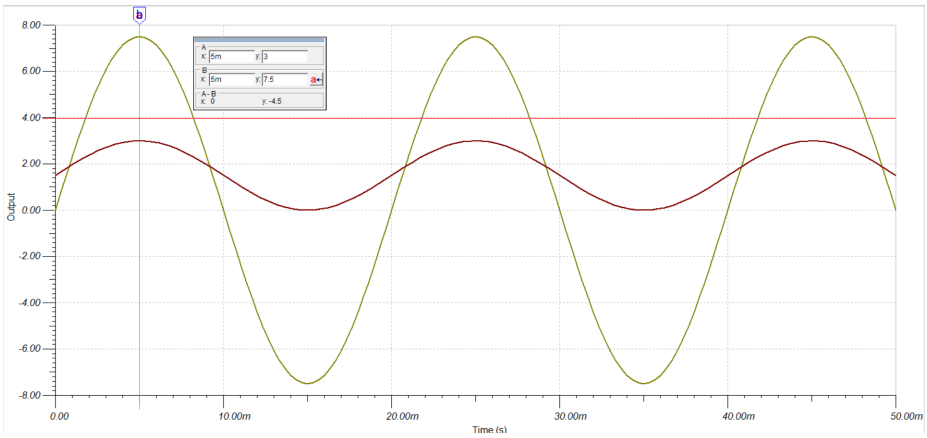


Figure 4-9: Simulation of adapting stage

The final stage before the microcontroller input is the protection stage. As the name is suggesting, it is intended to provide protection of ADC if the input voltage exceeds 3V. In the worst case, the operational amplifier can be saturated and 15V comes to the ADC input. To prevent this, a pair of series connected Schottky diodes act as a clamping circuit, which will clamp voltage to 3V if it exceeds it. This condition is also simulated and a result which is matching the expected behavior is shown on Figure 4-10. The red curve is the output of the filtering stage and the green curve is input to microcontroller clamped to 3V.

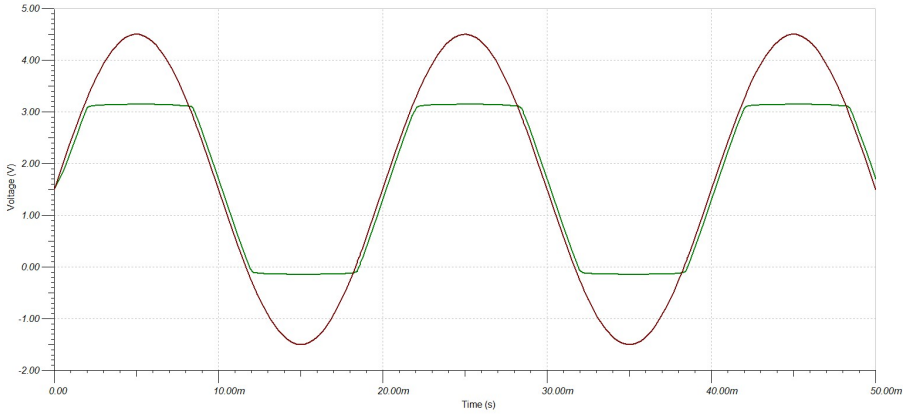


Figure 4-10: Simulation of adapting stage

Regarding **speed measurement**, the encoder used requires 5V supply provided from the PCB. Measurement is obtained by providing three pulse signals (A,B and I),a line pulse A, B line pulse shifted from A in order to determine the direction of

rotation and provide better resolution and I index signal which provides one pulse per revolution for verification. These signals will be connected to GPIO inputs with the programmed Enhanced Quadrature Encoder feature. Thus, 5V pulse signal obtained from the encoder will be adapted to 3,3V to connect to DSP.

Measurement of the temperature utilizes simple voltage divider on NTC Thermistor and additional resistor. The additional resistor is calculated such that voltage on NTC Thermistor varies from 0 to 3V, which is brought to ADC microcontroller input as shown on Figure 4-11. According to datasheet [25], minimum resistance measured (corresponding to maximum temperature) is 150Ω. Thus, calculated $R_1$ for obtaining 3V voltage drop on NTC is $R_1 = 100\Omega$.

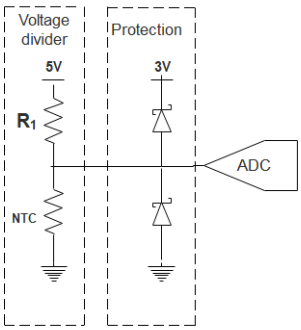


Figure 4-11: Temperature measurement

#### 4.3.2.2 " Status " input adaptation

Signal " Status " is a feedback signal provided by the IGBT module drive which will indicate if each IGBT switched from connecting to drain-source circuit. As already mentioned, the " Status " signal will be 0V when IGBT is on and 5V when IGBT is off. The idea was to eventually use this signal to provide additional redundancy to the system, comparing PWM output command from DSP with the " Status " signal which gives information about switching of IGBT. Still, the " Status " signal has opposite logic to the PWM. Solution implemented uses a single logic inverter supplied with 3,3V which will both invert signal and adapt it to 3,3V for connecting to GPIO. So, a signal on the top graph of Figure 4-12 obtained from the drive will covert to signal on the bottom graph, for input to DSP.

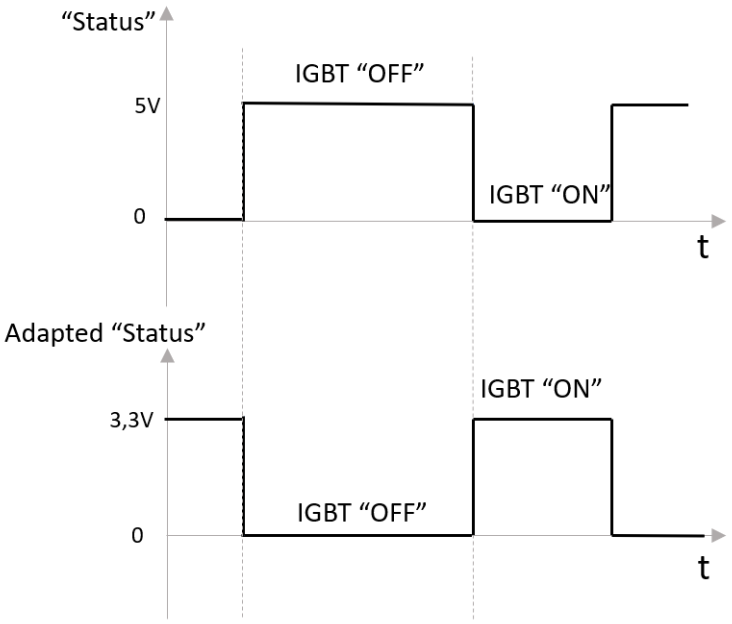


Figure 4-12: Processing of " Status " signal

#### 4.3.2.3 Analog control inputs

Implemented solution for setting **speed reference input** to control is employing potentiometer, which will vary the voltage on pin connected to ADC input from 0 to 3V. The potentiometer is connected to 3V reference supply from the PCB. This input on ADC will be later scaled in the execution of the program such that it sees it as real value in rpm.

Another function to be implemented is **Reset** button, to provide additional safety measure command for the microcontroller. " Reset " is a push-button connected to general purpose I/O pin of the microcontroller. As standard for GPIO signal of DSP is 3,3V, push-button will e connected such that when pressed will short GPIO input to 3,3V supply and send " Reset " signal.

#### 4.3.2.4 Communication interface for importing and executing code

The design will also have to provide a solution for importing code to the DSP, which will execute control action. The DSP has embedded Flash memory on chip, providing great benefit for users to store code internal to the chip. *Texas Instruments*

proposes few solutions for Flash programming interface. [37]. *The Code Composer Studio On-Chip Flash Programmer* is a plugin for *Code Composer Studio* that enables Flash programming using any emulator that supports C2000 and interfaces directly with Code Composer Studio. More about Flash programming will be explained in the Software implementation section. The chosen solution utilizes the JTAG standard. The JTAG emulator used to connect to a portable PC through USB connection is *XDS100v2*. For providing communication with emulator a PCB must have a 14-pin header, connected as shown on Figure 4-13. Description of the pin header signals, also connected to corresponding DSP pins, is given in [38]. Emulation enables execution of code directly from RAM, or from Flash memory.

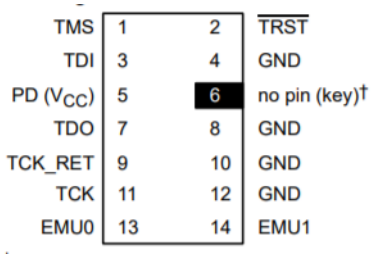


Figure 4-13: JTAG emulator-header pin connection

### 4.3.3 The gate output command signal interface

The PWM signals, generated by control implemented in DSP, will have to be adapted such that IGBT module drive " understands " it and generate appropriate gate voltage command. As mentioned in Section 4.1.1.1 talking about IGBT module and drive, gate drive circuit requires both gate " turn ON " and " turn OFF " signal for each IGBT. For " turn OFF " of IGBT, drive will generate negative voltage pulse on IGBT gate (lower graph). Figure 4-14 depicts how from " turn OFF " input command signal (upper graph) is generated gate signal on IGBT. Thus, " turn OFF " input command signal of the switch will be equivalent to " turn ON " command signal of the complementary switch of the leg and the same signal will be used for this two type of commands. It is required for the PCB to provide command signals for both the grid side and machine side inverter. To do so, six PWM signals will be

utilized in a manner shown in Table 4.6. The position of each IGBT in the converter is marked as shown on Figure 4-15.

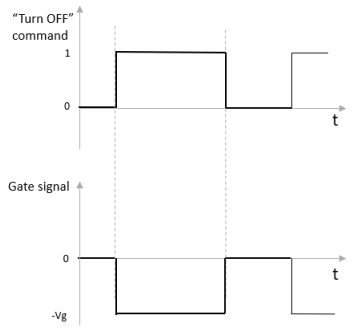


Figure 4-14: " turn OFF " gate voltage command generation

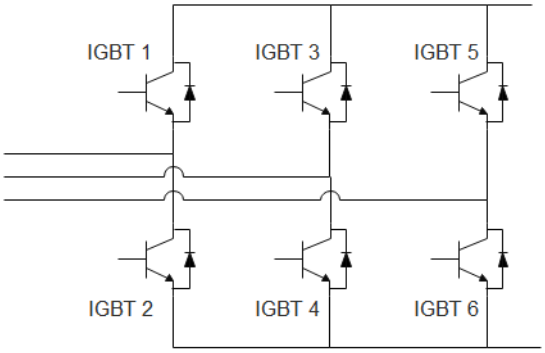


Figure 4-15: Notation of IGBTs placement in converter

These signals are not passed directly to the header connection to the IGBT module drive. Instead, the signals are first brought to buffer (one for grid side converter and one for machine side converter) which amplifies and pass through signals if enable signal is provided. This feature is used for having additional control on the system in case a fault occurs.

#### 4.3.3.1 Fault signals

*Enable* signal of the buffer will be used such to let command signals to get to output header pins, or to interrupt them in case that fault occurs. Function table

Table 4.6: Gate signals generation

| **Gate command signals** | **PWM output signals from DSP** |
|---|---|
| Machine side converter | |
| IGBT 1 ON | PWM1A |
| IGBT 1 OFF | PWM1B |
| IGBT 2 ON | PWM1B |
| IGBT 2 OFF | PWM1A |
| IGBT 3 ON | PWM2A |
| IGBT 3 OFF | PWM2B |
| IGBT 4 ON | PWM2B |
| IGBT 4 OFF | PWM2A |
| IGBT 5 ON | PWM3A |
| IGBT 5 OFF | PWM3B |
| IGBT 6 ON | PWM3B |
| IGBT 6 OFF | PWM3A |
| Grid side converter | |
| IGBT 1 ON | PWM4A |
| IGBT 1 OFF | PWM4B |
| IGBT 2 ON | PWM4B |
| IGBT 2 OFF | PWM4A |
| IGBT 3 ON | PWM5A |
| IGBT 3 OFF | PWM5B |
| IGBT 4 ON | PWM5B |
| IGBT 4 OFF | PWM5A |
| IGBT 5 ON | PWM6A |
| IGBT 5 OFF | PWM6B |
| IGBT 6 ON | PWM6B |
| IGBT 6 OFF | PWM6A |

of the buffer is given on Figure 4-16, where input A is PWM command signal from microcontroller and output Y command signal passed to the IGBT drive.

| INPUTS | | OUTPUT |
|---|---|---|
| $\overline{OE}$ | A | Y |
| H | X | Z |
| L | H | H |
| L | L | L |

Figure 4-16: Function table of buffer [5]

The logic scheme is implemented with the analog logic circuit, using available information provided by input signals, as shown on Figure 4-17. In the first level,

logic is making sure that none of the two switches in the same leg are switching at the same time, which would cause a short circuit on the capacitor. Output of that stage goes directly to the Trip zone which will trigger the error in the microcontroller. Output from the first stage, Undervoltage and overvoltage on DC link capacitor signal are brought to the " OR " gate. When any of those faults occur it will trigger enable on the buffer and bring all the commands to high impedance state, connected to pull-down resistors. This is the case of machine side converter fault signals. The only difference for the grid side converter is that Undervoltage condition is not included, and the third pin is connected to the ground.

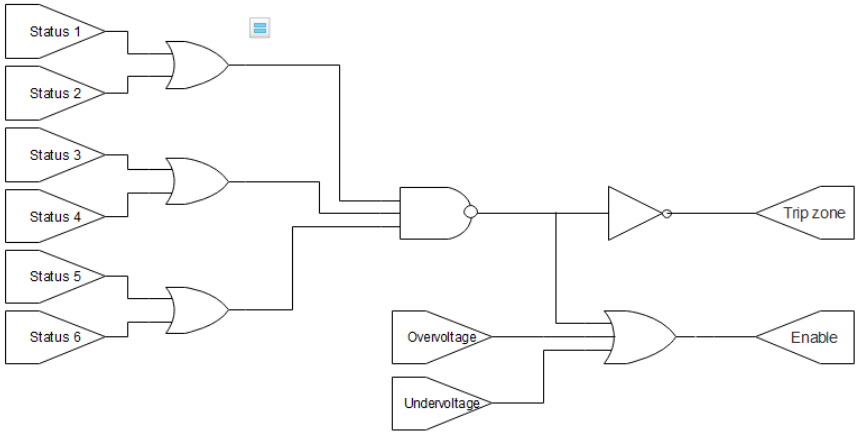


Figure 4-17: Faults logic implementation

The Undervoltage and overvoltage inputs are implemented as shown on Figure 4-18. Comparators are checking if adapted DC link voltage value (0 to 3V) is higher than allowed overvoltage limit, or lower than allowed Undervoltage limit and give 5V output in case of exceeding limits. Limits are imposed by choosing resistors of the voltage divider that have to correspond to value in 0 to 3V range. Referring to real measurement value, the low limit is as low as 600V to ensure that fault does not trigger in case of voltage dips imposed by load disturbance, but not to allow control action of the machine side converter for low DC link voltage. The high limit is 1415V which allows voltage peaks, but ensures that voltage doesn't exceed the maximum

allowable voltage of the DC link capacitor.

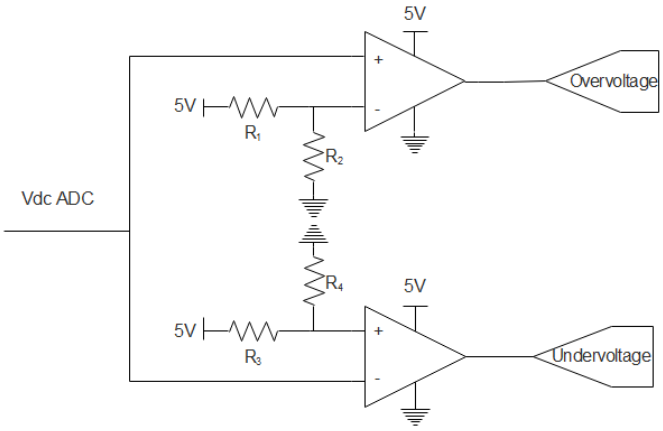


Figure 4-18: Undervoltage and overvoltage of DC link

### 4.3.4 Power supply and indications

All integrated circuits used in previously explained designs for signal processing are expected to have ideal behavior. To do so they will require stable **power supply** with suitable voltage level and sufficient current available from the power supply for normal operation. The PCB is utilizing a few different voltage levels. Voltage levels provided from the external power supply are 24V, 15V, -15V, 5V and ground. Additional voltage levels required for design 3,3V, 3V and -5V are provided from voltage reference IC's, powered by external 5V voltage level. The 3V supply of protection stages of the measurement processing part is using Zener for being able to sink current through Schottky in case the output of the filtering stage exceeds 3V (Figure 4-7).

**Indications** for user implemented by this design are LEDs, which will signalize presence of all voltage levels supply (24V, 15V, -15V, 5V, 3,3V, 3V, -5V) and will have red warning light if any of enable signals or under/overvoltage detects fault.

## 4.4 Software implementation

An integrated development environment that supports TI microcontrollers, which is a programmed control strategy, is *Code Composer Studio*. Its design includes various tools to develop and debug embedded applications. It utilizes C/C++ compiler. In addition, *controlSUITE*$^{TM}$ provides a specific set of software tools and documentation for the development of projects for C2000$^{\text{TM}}$ microcontrollers. It contains all required routine files as compiler, command files, libraries, as well as example programs. User is able to easily import files in the project and modify them. The development of a program for C2000$^{\text{TM}}$ microcontrollers is following the same general structure depicted with the algorithm on Figure 4-19. Depending on requirements of the project, the program will utilize different peripherals with specific configuration and define code branches executed inside interrupt routines called from the main program loop. The following section will comment on their configuration required to implement designed control of this application. B.

### 4.4.1 Configuration of peripherals

This section will discuss the configuration of available peripherals [39] of the DSP used to implement control strategy. Access to features from *Code composer* environment is done by programming assigned bit fields to each functionality within the register, allowing configuration of specific peripheral, which is the most intuitive approach for programming peripherals. The description of all bit fields within registers to access features of each type of peripherals, with included examples, is given by manuals [6, 7, 40, 41] and won't be further discussed in this section. Instead, the focus will be on the description and logic of functionalities that will be implemented by configuring peripherals.

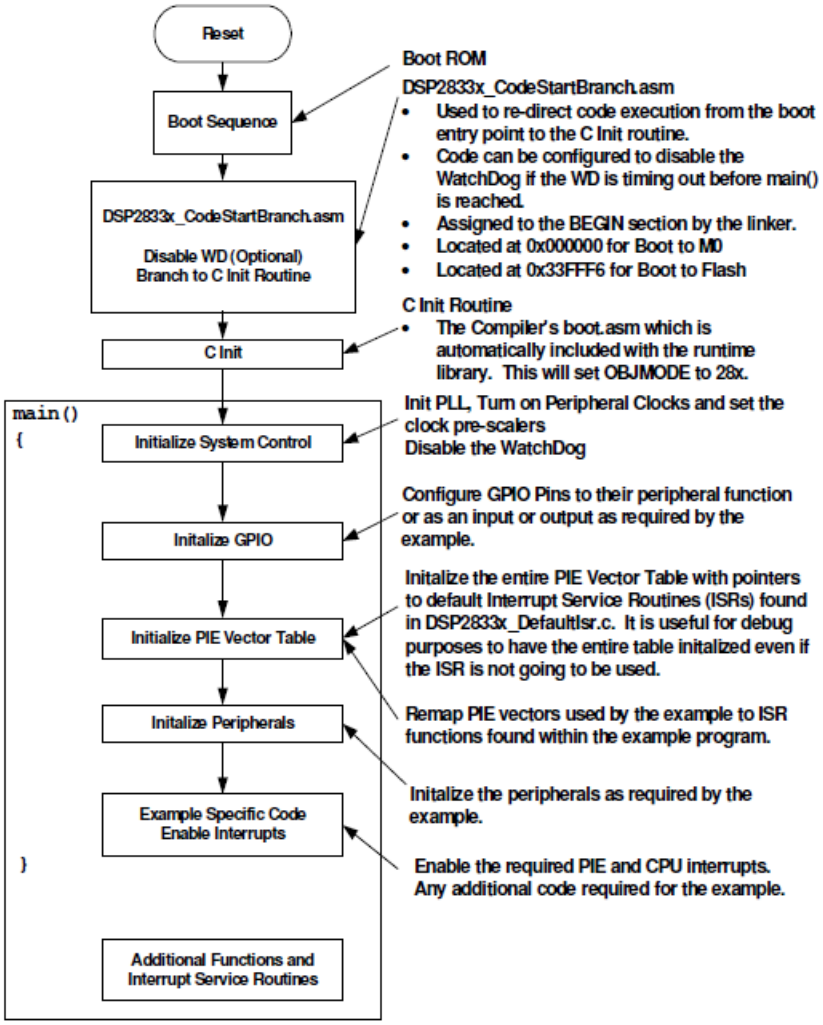


Figure 4-19: General program flow algorithm

#### 4.4.1.1 PWM configuration

Prior to the configuration of any type of peripherals, it is needed for specific GPIO to be initialized as I/O peripheral. The *PWM* control of both converters, based on conclusion derived in Section 4.3.3 about hardware design, will be achieved using six *PWMs*. For implementing synchronous switching method, the time-base counter of PWM module is set to synchronous up-down count, which will count from 0 to defined counter period (*TBPRD*) and back to 0. For synchronous switching one triangular cycle (up and down count) will correspond to the switching period. Thus,

the counter period will be a number of counts of *PWM* counter[1] up to the half of a switching period (pick of the triangle on Figure 4-20. For the DSP system clock configuration of 150MHz and switching frequency of the module of 4KHz, the counter period calculated will be 12750.

Changing switching states of PWM is performed by setting actions based on counter compare register (*CMPA*). The *CMPA* is counter compare register which value will be compared to PWM counter value and when they are matching PWM will change state based on configuration. As shown on Figure 3-2, the *EPWM1* is configured such that *EPWM1A* will be set (*EPWM1A*=1) when PWM counter matches compare register on up count, and cleared when it matches on down count (*EPWM1A*=0). State of *EPWM1B* control signal can be configured the same way as *EPWM1A* using second counter compare, or can be synchronized with *EPWMA1* as it is case in this configuration. Setting polarity control to active high complementary, *EPWM1B* will be signal complementary to *EPWM1A*, as shown on Figure 4-20. When the polarity synchronization feature is enabled, there is additional possibility of configuring **dead-time**. This is configured by setting falling-edge delay (*FED*) and rising-edge delay (*RED*) that are depicted on Figure 4-20.

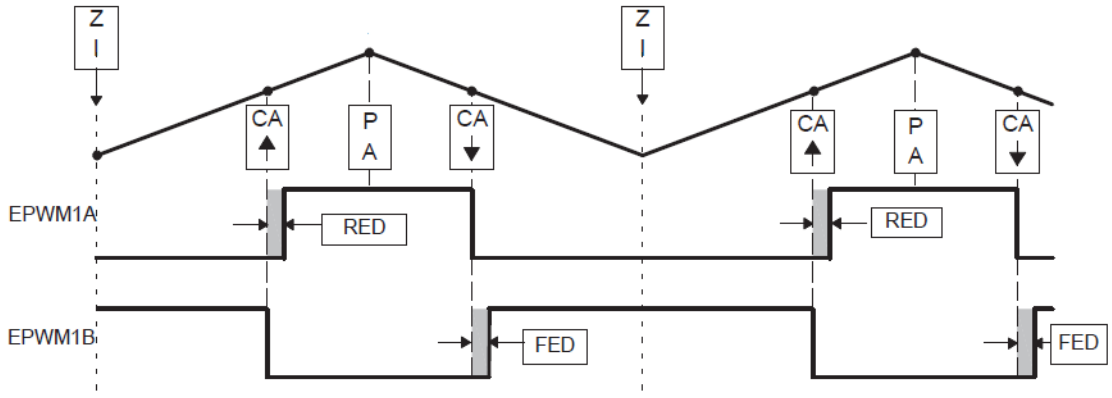


Figure 4-20: Generation of PWM signal [6]

Synchronization between PWM commands, to ensure proper operation of converters, is implemented using " Master/Slave " mode for which, for each converter, one *EPWM* is set as " Master" and the rest of two as " Slave " synchronized to " Master

[1]Frequency of *PWM* counter is the same as of a system clock, set to 150MHz

". For machine side converter *EPWM1* is " Master ", and *EPWM2* and *EPWM3* are " Slaves ", while for grid side converter *EPW4* is " Master " and *EPWM5* and *EPWM6* " Slaves ".

The sub-module that provides additional safety feature to the control is programmable **Trip zone**, triggered from combination of six trip zone peripheral signals. It has possibility of both cycle-by-cycle trip and one-shot trip on fault conditions. For sake of this application, two trip zone signals are used (*TZ1* and *TZ2*) as one-shot trip. The first one *TZ1* will act on machine side converter (*EPWM1*, *EPWM2*, *EPWM3*) and the second one *TZ2* will act on grid side converter (*EPWM4*, *EPWM5*, *EPWM6*) in a way that all upper switches are switched on, and lower ones switched off.

The important function of the PWM module for the application design is that any event which occurs on PWM can trigger CPU interrupts and ADC start of conversion (SOC), used for synchronization of calculation of control action and switching.

#### 4.4.1.2 ADC configuration

The analog-to-digital conversion module has an essential role in importing information on feedback measurement in DSP. It comprises of 12-bit ADC converter with dual sample-and-hold, able to sample two ADC signals simultaneously. It has a capacity of 16 channels that can perform in simultaneous or sequential sampling mode. Simultaneous sampling is performed in two sequences of 8 channels, which is a default setting. [7] Block schematic of the ADC conversion is shown on Figure 4-21. The *ADC* input signals *ADCINA0* and *ADCINB0* are sampled in the same instant, converted and placed in *ADCRESULTS* register, which are following *ADCAIN1* and *ADCINB1* until the last. Information of which system variable is connected to which specific ADC input for conversion and where is stored in *ADCRESULT* register is provided in Table 4.7. Selection of the inputs is done in the way that phase A and phase B variable of same three-phase system, line motor current of phase A and B for example, are converted in the same instant (*ADCINA0* and *ADCINB0*). That is done to eliminate error due to phase shift from sampling in different time instant. B.

It can be seen that only first sequence is used for all required conversion signals.

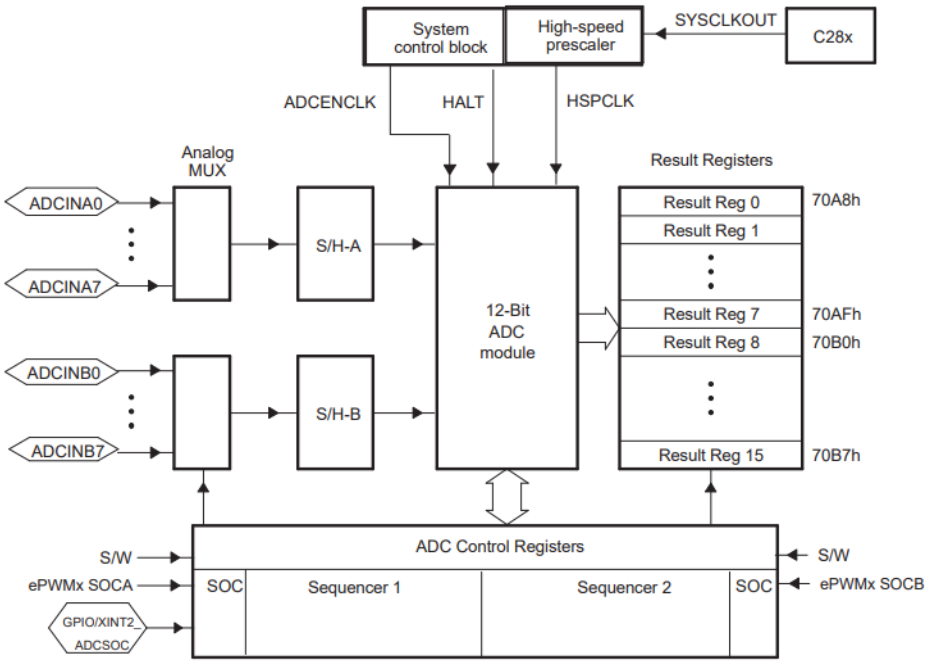


Figure 4-21: Block schematic of ADC conversion in simultaneous sequencer mode [7]

Table 4.7: ADC conversion of system variables

| **System variable** | **ADC input** | **Position in results register** |
|---|---|---|
| Line motor current-phase A | ADCINA0 | ADCRESULT0 |
| Line motor current-phase B | ADCINB0 | ADCRESULT1 |
| Line grid current-phase A | ADCINB1 | ADCRESULT3 |
| Line grid current-phase B | ADCINA1 | ADCRESULT2 |
| Phase grid voltage-phase A | ADCINB2 | ADCRESULT5 |
| Phase grid voltage-phase B | ADCINA2 | ADCRESULT4 |
| Temperature of machine side converter | ADCINA3 | ADCRESULT6 |
| DC link voltage | ADCINB3 | ADCRESULT7 |
| Reference speed | ADCINA4 | ADCRESULT8 |
| Temperature of grid side converter | ADCINB4 | ADCRESULT9 |

Start of conversion event on ADC of first sequence is set by *SOCA* interrupt generated by /textitEPWM1A. Start of the ADC conversion will take place each time *PWM* counter is equal to counter period (pick of the triangle on Figure 4-20).

#### 4.4.1.3 Flash programming

In case that user doesn't prefer to execute program from RAM, or doesn't have sufficient space available for code inside RAM, the code can be stored inside internal Flash memory of the DSP. For storing the application code, Flash memory must go through an erase, program, and verify procedure without interrupting. That implies stable supply of the DSP. In case of interrupting this procedure there is possibility that Flash memory would be permanently locked. For the programming in Flash, the application project will need a corresponding linker file which performs memory mapping. The time-sensitive parts of code that perform control action, such as interrupts, are copied in RAM during run time and executed. This is performed by creating a separate linkable section from code objects. Furthermore, functions defined in linker command file employed in *memcpy* function for coping number of characters, with load specific part of code from flash to RAM. This function has to be executed prior to the initialization of the flash. Procedure is used for executing interrupt routines inside RAM memory.

### 4.4.2 The user-specific program

The complete control action calculation is executed inside interrupt routines called from main flow of the program, while the main loop is running in infinite time loop. The idea of implementation is that control action is calculated inside ADC interrupt at half of current switching period, and based on it the calculated $EPWM$ command applied in succeeding switching period ($PWM$ counter equals 0). Global variables are initialized prior to entering main loop. That includes initialization of duty cycles and ADC interrupt counter to zero, and variable that delay is active ($Delay$=1). The code written for ADC interrupts routine is the following logic algorithm shown on Figure 4-22. The ADC interrupt won't enter control loops until PLL control reaches steady state. According to simulation, that time is less than 5ms (around 20 interrupt counts).

The **Bits to Units** function performs transformation from digital value, obtained

fr om 12-bits conversion, to the real measurement units based on formula given by Equation 4.16. The variables $V_{max}$ and $V_{min}$ correspond to maximum and minimum value of measurement range on primary side of transducer.

$$Units = \frac{V_{max} - V_{min}}{4095} Bits + V_{min} \tag{4.16}$$

The **Control of active rectifier** includes functions of a voltage and current controllers, voltage compensation, saturation of voltage reference and coordinate transformations. The **Machine control** includes functions of the speed controller and current controllers, as well as voltage compensation, saturation of voltage saturation and coordinate transformation. All controllers are implemented on the same principle as explained in Section 3.5 for corresponding controller parameters obtained from control design.

**Units to PWM** is the function that will calculate required " duty cycles " needed to be applied to counter compare register *CMPA* of corresponding *EPWM* to obtain voltages imposed by reference from control action, implemented according to Equation 4.17. In equation $V_{max}$ is DC link voltage measurement in Volts and $PRD$ is period of PWM calculated in Section 4.4.1.1.

$$duty = (\frac{V_{ref}}{V_{max}} + 0,5)PRD \tag{4.17}$$

Moreover, in the middle stage of project development, the **TestPCB code** is designed to provide PWM reference based on three-phase sinusoidal voltage command, for testing PCB and peripheral initialization. Comparing to the closed-loop control code explained previously, the test code will not have any control of calculation and sinusoidal voltage references will be generated inside *TIMER0* interrupt instead. The *TIMER0* interrupt will be executed every $100\mu s$.

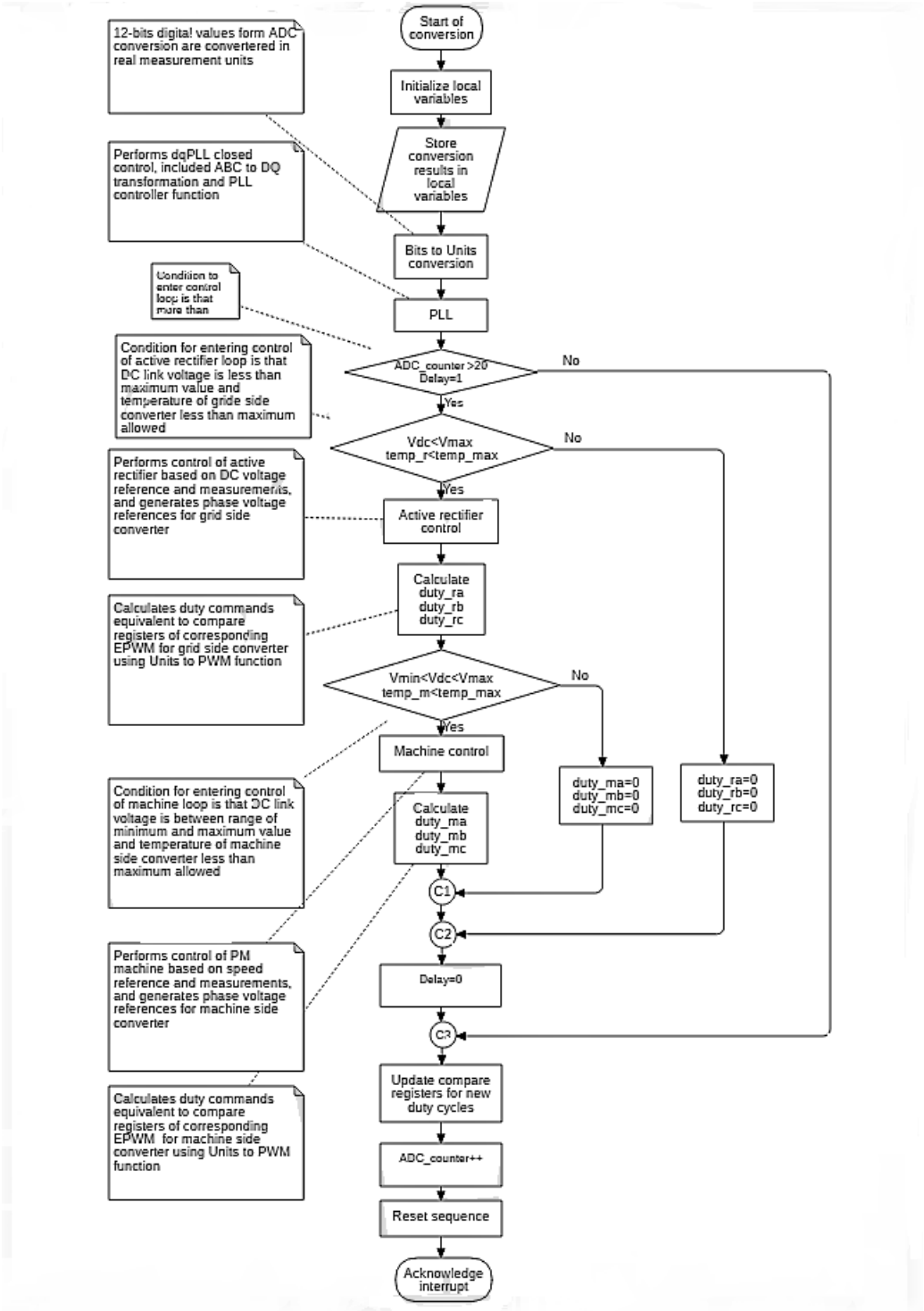


Figure 4-22: Flow algorithm of ADC interrupt routine

# Chapter 5

# Simulations of the control system

This chapter comprises of two parts. The first part summarizes the results of simulations obtained for the control design of active rectifier, intended to be implemented in operating conditions of system application. On the other hand, due to lack of data for PM machine to be used in the application, the control of the PM machine connected to the system could be neither designed, or simulated for the implementation of the system. Still, for the verification of the methodology used for the control design of PM machine, the second part of the chapter will discuss the simulation of the control strategy developed for PM machine model from *Matlab* library. The parameters of the rest of the system are redesigned and adapted to the rated conditions of the PM machine model used. Both are following the same approach, which is the development of the control in continuous time and then adapting it for discrete implementation in DSP. For the verification of the discrete control functions in simulations *Embedded Coder Support Package for Texas Instruments C2000 Processors* is used. Parameters used in continuous time simulations, calculated based on developed control strategy discussed in Chapter 3, are provided i Appendix B.

## 5.1 Simulation of the control of active rectifier

***The implementation of PLL***

The core of the vector control design is an accurate estimation of the position of

vector defining coordinate transformation. The control of active rectifier is developed with respect to the position of the grid voltage, and thus control strategy relies on accurate position estimation of the PLL. Figure 5-1 shows simulation results of the PLL control response for the three-phase balanced system. Graph b on the figure shows that the response of grid voltage $E_{gd}$ and $E_{gq}$ are according to the design of the PLL in Section **??**. The PI controller of PLL is imposing zero $E_{gq}$ component, while $E_{gd}$ is aligned with voltage space vector and equals to the amplitude of grid phase voltage ($E_{gd}$=326,6V). Angular velocity on Graph c of the grid is reaching $2\pi 50 rad/s$ speed. On Figure 5-2 there is a disbalance in the grid simulated by voltage dip of 20% in phase C, applied at 0,1s of simulation time. From Graph d ca e see that the estimation of the grid position is still stable.

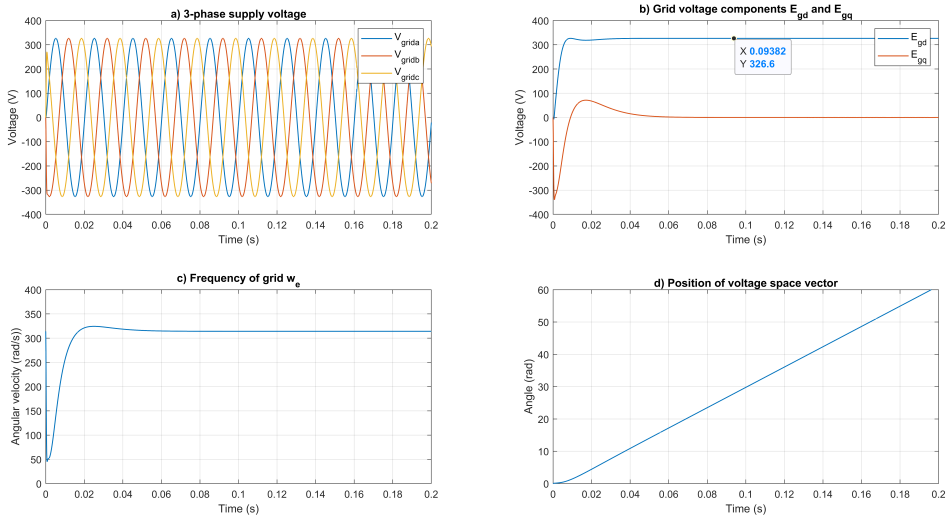


Figure 5-1: Response of PLL control for three-phase balanced system

### 5.1.1 Control performance in the continuous time

To qualify the response of the control of active rectifier, Figure **??** is showing the transient response of the control for achieving DC link voltage reference. The control action on switches is applied at 0,005s of simulation time, when PLL control reaches steady state, until when converter behaves as a diode rectifier. Thus, it requires less

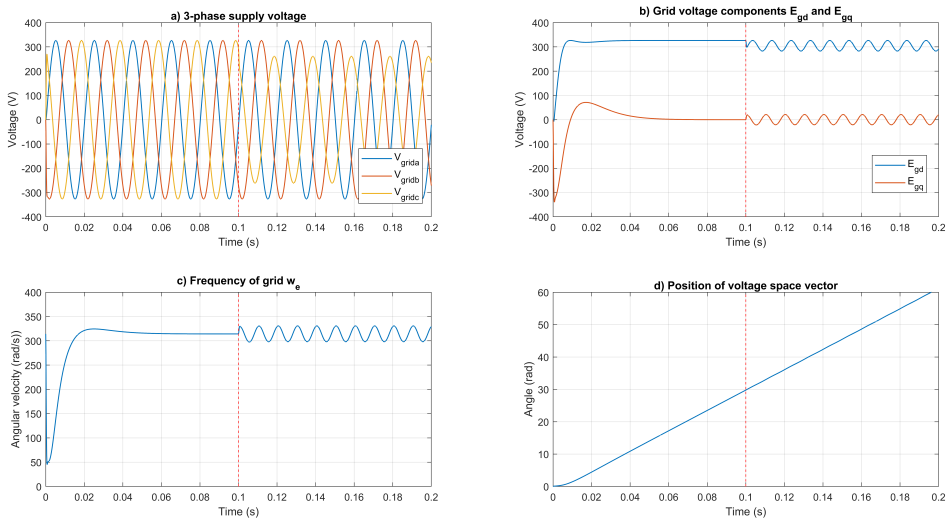


Figure 5-2: Response of PLL control for three-phase unbalanced system

control action to achieve reference voltage, with an overshoot of about 2,17%. Voltage is safe bellow the limit of the capacitor ($V_{dcrat} = 1400V$).

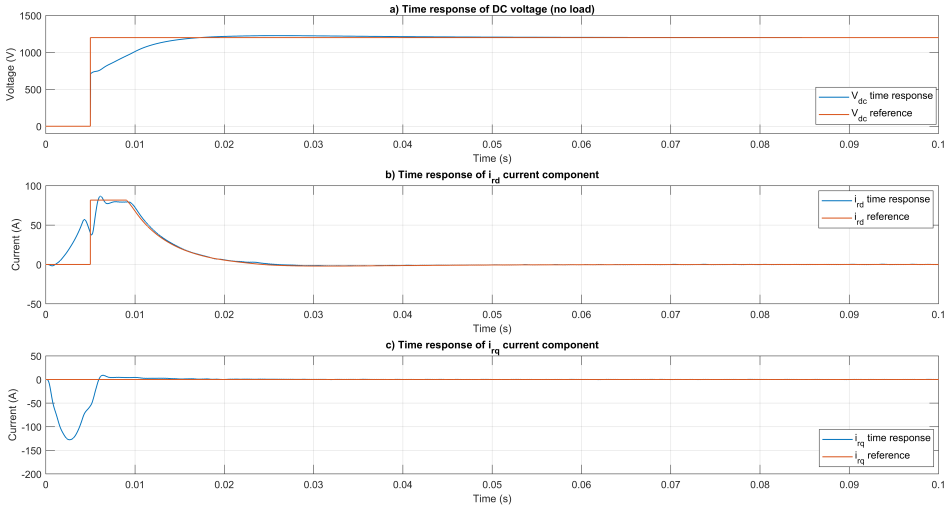


Figure 5-3: Control of active rectifier in continuous time

The information of the parasitic resistances of LCL filter inductors designed wasn't provided, and thus low values on resistance were assumed. The higher values of resistances system is more damped and provides a slower response to given reference, but better disturbance rejection.

***Current ripple on the DC link capacitor***

Another indicator for the validation of DC link capacitor design is that it has to be able to withstand maximum current ripple passing through. Thus, lifespan given by the manufacturer due to the influence of temperature on the capacitor is guaranteed. The RMS value of the current ripple obtained by the simulation of control in the continuous domain is given by Figure 5-4, for the maximum load, applied at 0,15s of simulation time. The RMS value of ripple obtained for maximum load is less than the maximum RMS of ripple given by the manufacturer in [30], which is 66A. Thus, the capacitor will withstand the current ripple for normal operating conditions.

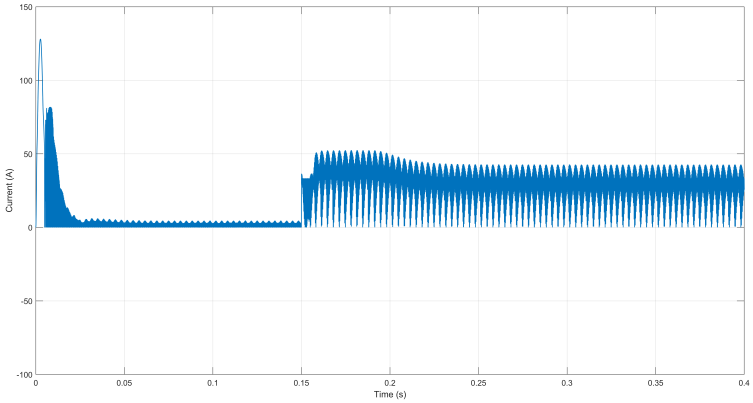


Figure 5-4: The RMS value of current ripple through DC link capacitor

***The effect of the LCL filter***

All the applications using switching converters connected to the grid will generate high-frequency current, which will pollute the grid, and is not acceptable by regulations. Thus, the effect of the LCL filter on reducing harmonic distortion should be verified. Figure 5-5 shows the reduction of the distortion from current measurements on the converter input side, on Graph a, to the measurements of the grid side, Graph b. Graph b clearly contains waveforms closer to the pure fundamental frequency. Better validation of effect is obtained by the *Fast Fourie Transform* analysis of the grid side phase current measurement, shown on Figure 5-6. The transform window considered is during no-load conditions, giving the highest THD of 7%.

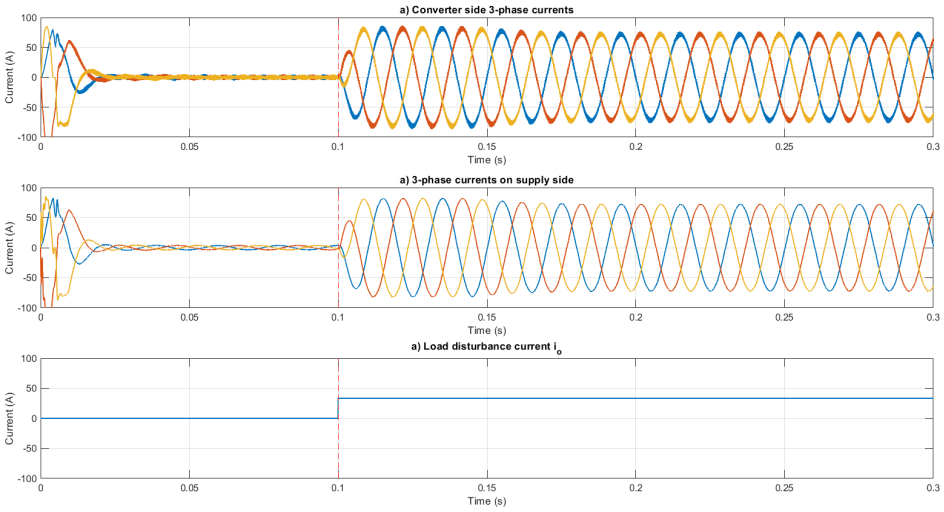


Figure 5-5: The effect of LCL filter on three-phase currents

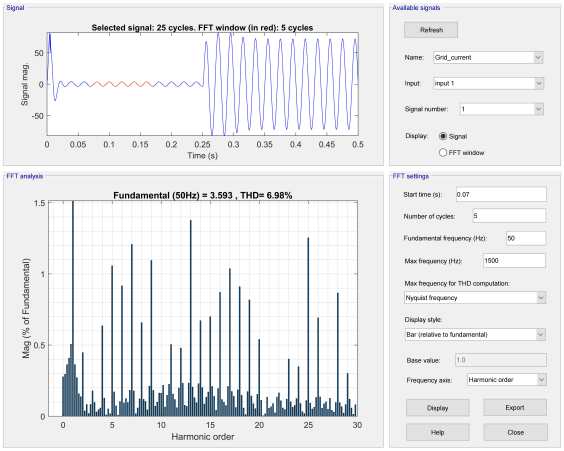


Figure 5-6: THD of phase current injected to the grid

### 5.1.2 The discrete time implementation

After adapting simulation with functions implemented in C code, the discrete time control is compared with the continuous time one, to verify if it achieves close enough performance. Comparison is done for time response of the DC link voltage, shown on Figure 5-11. It shows good performance with slightly higher overshoot and longer settling time, as it looses on bandwidth due to the discretization.

***Anti-Windup of current controller***

To point on the efficiency of the Anti-Windup strategy implemented for the current

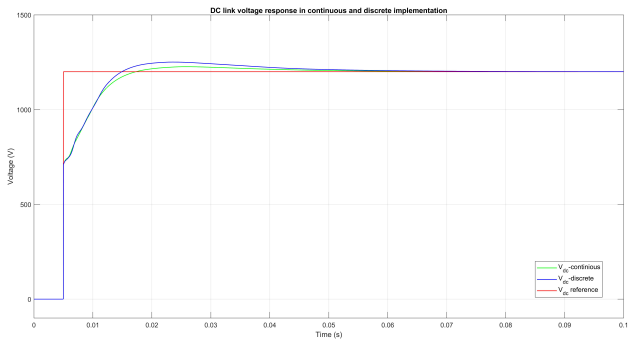


Figure 5-7: DC link voltage response-continuous and discrete implementation

controller, the simulations for a high value of $i_{rd}$ current reference ($i_{rd}$=400A) with and without Anti-Windup are performed. The results are given by Figure 5-8. Imposing high step reference without Anti-Windup results in a controller requesting for the high voltage command (Graph b), which is saturated due to constraints on the power stage. That causes a windup effect on the current controller (Graph a) resulting in huge overshoot and undershoot until it gets to steady state. On the other hand, implementation with Anti-Wind up saturates output command of controller and back calculates error. Thus. voltage command is almost equal to saturation voltage (Graph d) and consequently, the response is faster and there is no windup effect on integrator (Graph c).

***Response of the discrete control implementation with maximum load***

Final simulation was the test of the system performance with applied maximum load step, from zero up to the maximum current load (corresponding to the maximum power of application), at the 0,2s of simulation time, shown on Figure 5-9 (Graph b). System is using the highest allowable $i_{rd}$ current (from 0,2s to 0,4s) to reject load disturbance (Graph a) until it reaches steady state.

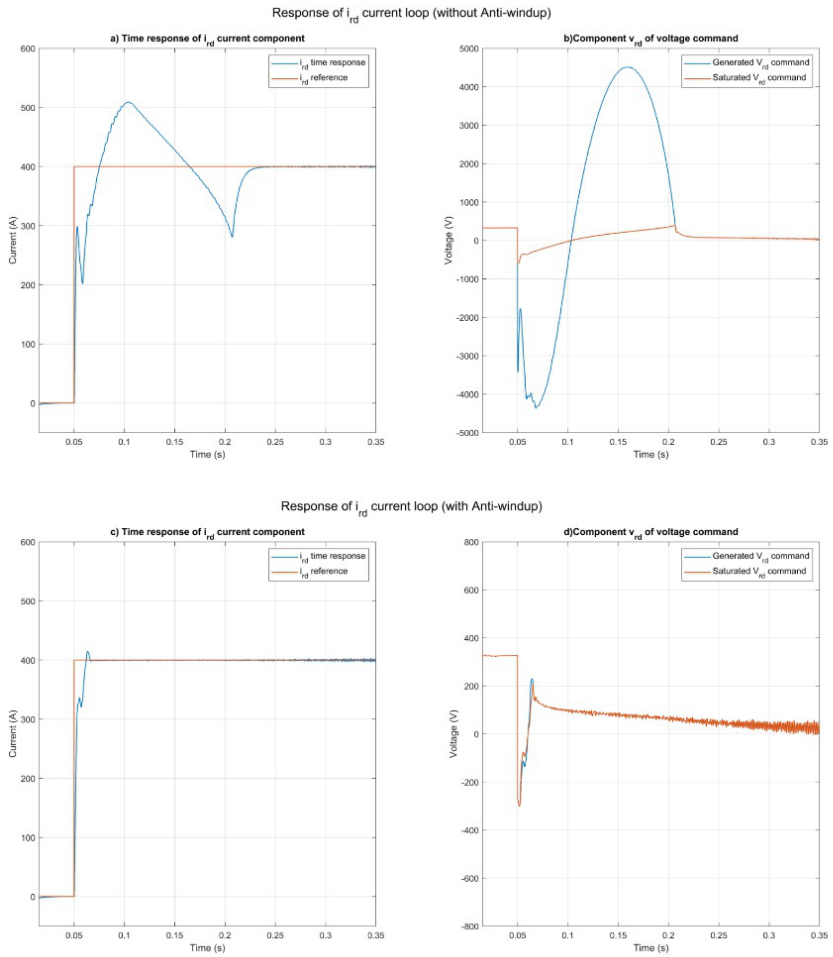


Figure 5-8: Performance of the Anti-Windup for $i_{rd}$ current controller

## 5.2 Simulation of the control of PM machine

### 5.2.1 Control of the PM machine in continuous time domain

For the development of the control of the PM machine prior to connecting the whole system, control was developed and verified assuming ideal voltage source instead of the capacitor, supplying machine side converter. The control response achieved for the continuous domain design is shown on Figure 5-10. Rated speed reference is applied to the control at 0,2s of simulation time speeding up with maximum torque available proportional to the stator current $i_{sq}$ (Graph d) while $i_{sd}$ follows zero reference. With the applied maximum step of load torque from zero to rated at

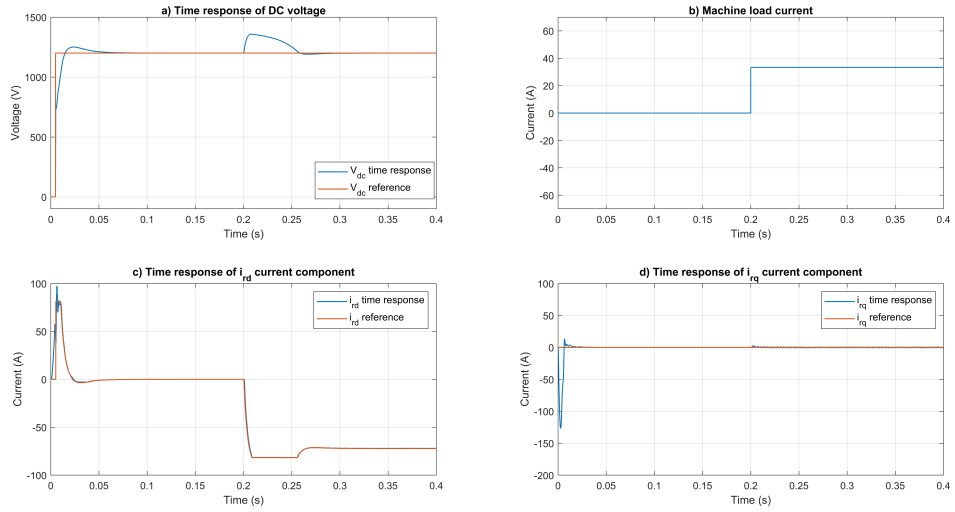


Figure 5-9: Discrete implementation of the control of active rectifier

0,4s (Graph b) speed controller is able to reject disturbance.

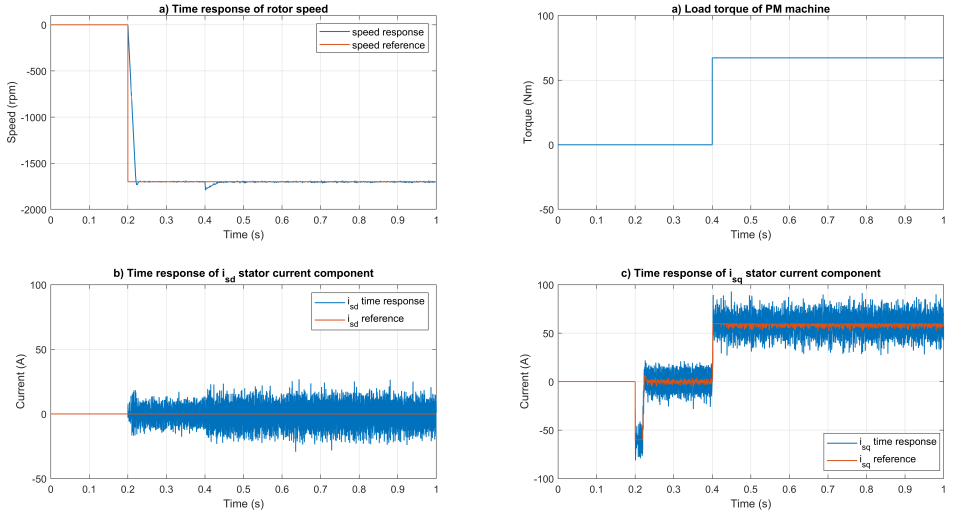


Figure 5-10: Control of PM machine in continuous domain

### 5.2.2 Control of the PM machine in discrete time domain

After substituting the continuous time control functions with ones in discrete time written in C code, comparison of their speed response obtained from simulations is given on Figure 5-11. Comparing to continuous time response discrete time one will

have higher overshoot during rise time and for disturbance rejection as well. Finally,

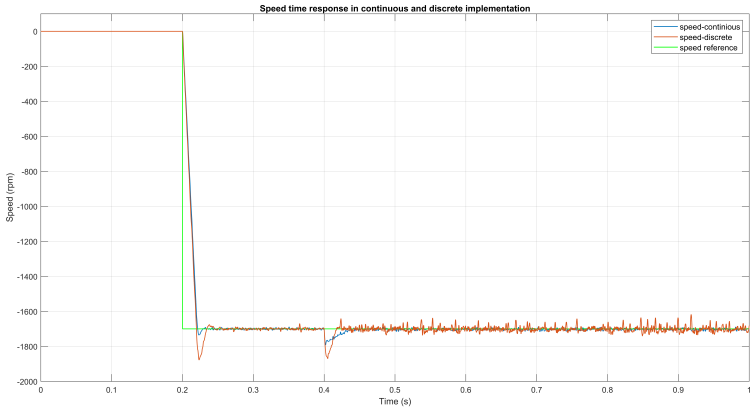


Figure 5-11: Time response of rotor speed-continuous and discrete implementation

the machine side converter supplied from ideal DC voltage source is substituted with a back-to-back converter supplied from the balanced three-phase grid voltage supply, which joins both control of DC link voltage and control of speed of PM machine. The results of the response obtained are shown on Figure 5-12. Graph a is showing speed response for the given rated speed reference applied at 0,2s of simulation time and further transient occurred due to disturbance rejection at 0,4s. Control of the grid side converter maintains stable DC link voltage (Graph b) with transients at 0,2s and 0,4s as a result of applied reference of speed, or withdrawn current required to speed up, and of applied load torque, due to increase of the current required to sustain the load.

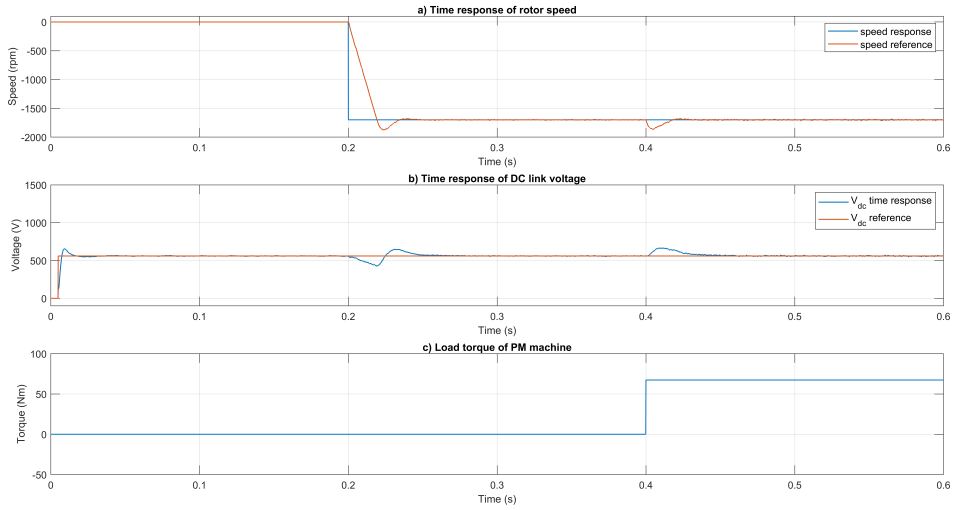


Figure 5-12: Control of the system in discrete implementation

# Chapter 6

# Experimental validation

This chapter will cover all stages through experimental testing of the design of PCB interface and the DSP configuration to achieve control of the output of IGBT module.

## 6.1 Testing of the PCB interface

This section will discuss on verification of the PCB design prior connecting to the rest of the setup. For the verification of the PCB design three parts are to be tested:

- Voltage supply
- Measurement processing stages
- Fault states

**First version of PCB design** (Figure 6-1) had problems with the footprints of the components to be mounted. The holes for headers of the external inputs from measurements and voltage supply were smaller than recommended, but still could be mounted for the purpose of testing.

During testing the voltage supply to the complete circuit, both external and provided from local voltage references, the voltage drop occurred on -5V supply from the voltage converter. This voltage was used for reference voltage to the operational amplifier of the adapting stages of measurement processing circuits. As voltage reference

was stable prior to empowering operational amplifiers, the conclusion was that the voltage converter is not capable to supply enough current to the operational amplifiers, as it is limited to 50mA. Bypassing this voltage converter with external voltage supply that was confirmed, as required current withdrawn by operational amplifier was about 120mA.

Furthermore, 3V voltage reference connected to the clamp Schottky diodes was not able to sink current and thus is replaced with 3V Zener for the second design of PCB.

Testing fault circuit, "OR" circuit of final circuit happens to be replaced with "AND" due to mistake with ordering components. Also, resistors had to be added to limit the current through LED diodes, as some of them got burned.

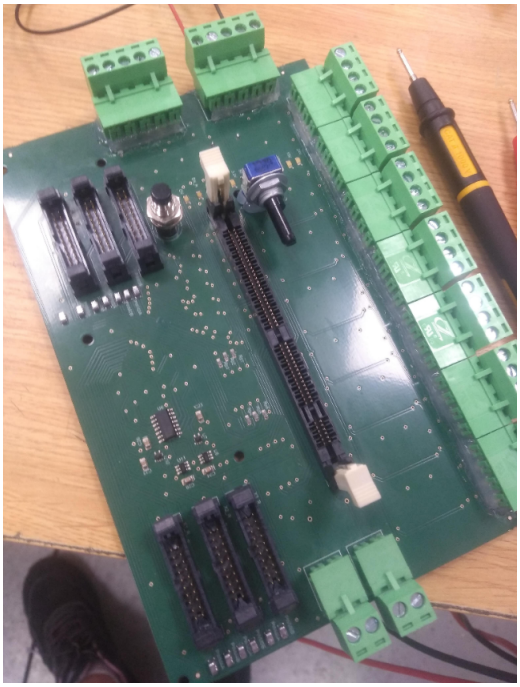

Figure 6-1: First version of the PCB design

**Second design of the PCB** to be tested is shown on Figure 6-2. Green LED lights are signalizing that all voltage supply levels are present in the circuit. Red LED lights are signalizing enable warning signals, which doesn't allow PWM signals to pass through a buffer. Since terminals of the PCB are not connected to the IGBT module, the absence of voltage from " Status " signals is equivalent to the signal

of closed switch. As fault circuit " understands " it as fault state (short circuit on DC link) it will signalize error and block signal through buffer. This shows proper operation of fault circuit.

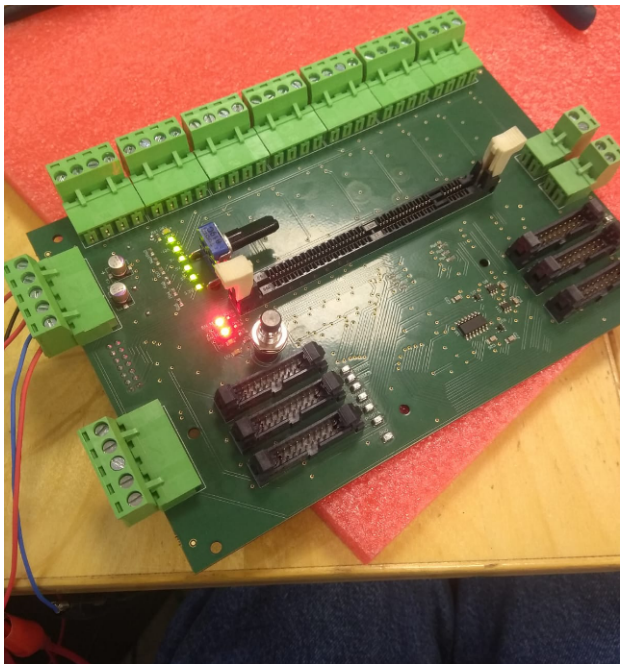

Figure 6-2: Second version of PCB design

The Zener diode used for 3V reference for the protection circuit already mentioned did not supply required voltage level because the series resistor limiting current from supply was too high and current wasn't sufficient to reach 3V on characteristic. This solution is replaced on spot with programmable voltage reference according to the feedback connection design circuit on Figure 6-3. Implementation done on the PCB is shown on Figure 6-4.

Due to the missing connection between negative reference and output of operational amplifier in filtering stage (Figure 4-7), coming from missing connection point in the PCB design file done in *Altium*, amplifier was getting saturated. By shorting those two connections with solder problem was solved.

The measurement processing stage was tested by imposing the sinusoidal input from signal generator, modeling measurement signal from the transducer. The signal is applied to AC voltage measurement input with maximum input voltage range

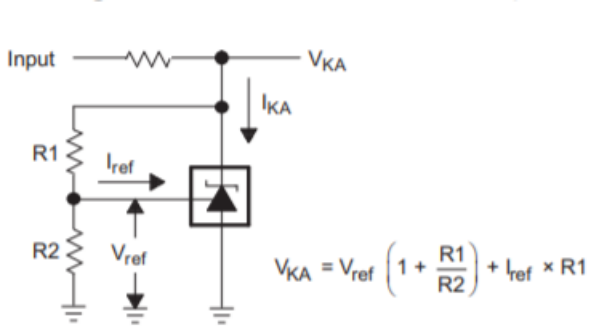


Figure 6-3: Schematic of programmable voltage reference [8]

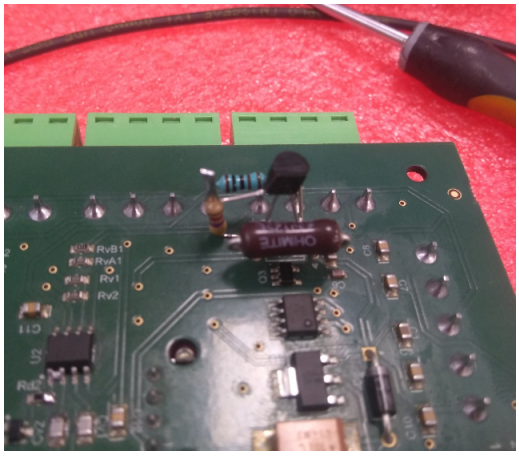

Figure 6-4: Implementation of programmable voltage reference on PCB

$[-7,5V \div 7,5]$. Two tests were performed, the one with sinusoidal input varying in given maximum measurement range (7,5V amplitude) and the second one sinusoidal input varying in the higher range for the testing protection stage (15V amplitude). Results obtained from the first case are shown on Figure 6-5. While the second case, for the higher input, is shown on Figure 6-6. Voltage on the peaks of the measurement is converting to below 0V and above 3V. This could occur due to the forward voltage drop on Schottky diode while conducting. Series resistor, that limits the current through Schottky diodes, should be resized for taking into account the highest possible forward current which will take place when the amplifier is saturated. The resistor used would limit forward current to 80mA, which would give a forward voltage of around 500mV according to the datasheet of diodes in [42]. This should be proved by repeating the test of the circuit without the protecting stage and/or trying with another series resistance.

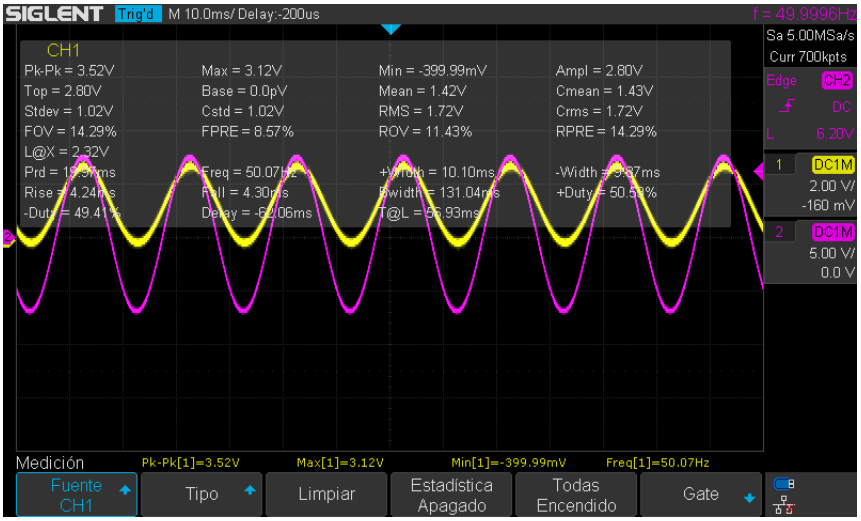


Figure 6-5: Performance of the measurement processing design for maximum measuring range


Figure 6-6: Performance of the measurement processing design for exceeding maximum measuring range

## 6.2 Testing configuration of DSP

In this stage of testing, the aim is to verify if the PWM command generated by running the imported program has expected features defined by configuration. Prior to it, the connection between portable PC, with installed *Code Composer Studio* software environment and developed C code project of the application, and DSP board in slot of PCB interface was tested. The emulator was detected and the debugging

code in RAM was successful. Also, an adapted version of the program was imported into flash memory, passing through all required procedures (erase, program, verify). Then, results obtained shown on Figure 6-7 are *EPWM1A* and *EPWM1B* complementary outputs. Given the closer look on Figure **??** showed the dead-time between them imposed by DSP.

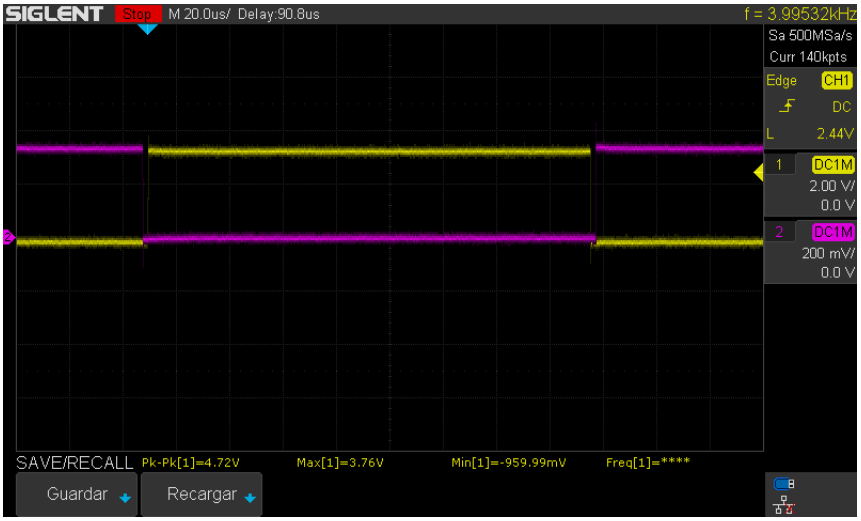


Figure 6-7: *EPWM1A* and *EPWM1B* complementary outputs from DSP

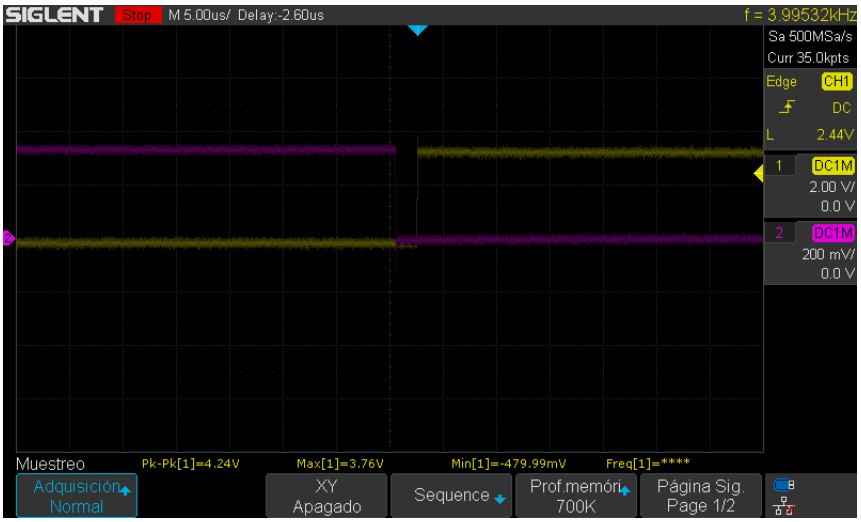


Figure 6-8: Dead-time generated between *EPWM1A* and *EPWM1B* complementary outputs from DSP

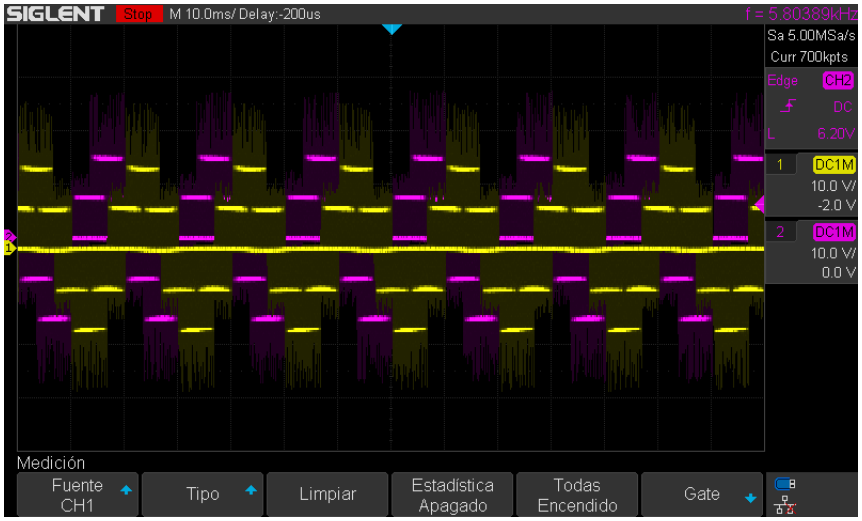


Figure 6-9: Output voltage waveforms on output of IGBT module generated by DSP command

## 6.3 Control of IGBT module

The final stage of the testing was to connect the PCB interface with the IGBT module and verify if the output of the converter could be controlled as expected. The IGBT module was supplied from the DC voltage source with 20V. The output voltages on two phases on passive balanced L load were measured. The waveforms obtained for imposed three-phase voltage command from DSP is shown on Figure 6-9. This shows that the synchronization of *EPWM* outputs is well configured and the desired output can be obtained based on set voltage reference.

# Chapter 7

# Conclusions and future work

## 7.1 Conclusions

The subject of the thesis is the implementation of speed control of a permanent magnet machine fed up from back-to-back IGBT converter connected to the grid. Moreover, the system provides bidirectional power flow and will regenerate power back to the grid. Thesis aims to provide a systematical approach to the problem of the design from the idea up to the realization and practical implementation of the system. This is brought to the realization by following defined project objectives.

At first, the thesis addresses the problem of the design of power elements that provide bidirectional power flow through the application itself. Thus, it covers the sizing of the PM machine for providing the required power and speed range for testing, the DC link capacitor to sustain the DC link voltage reference and the LCL line filter for filtering high-frequency harmonics injected to the grid.

The theoretical basis required for the modeling of system dynamics is covered in the thesis. The problem of the application system control is decomposed into two parts, control of the three-phase active rectifier and control of a permanent magnet machine. The derivation of the control strategy is accounting for physical constraints of the system imposed by design and power system requirements. In particular, it gives a detailed explanation of the calculation of controller parameters and the Anti-Windup method used for improving controller performance.

The design of the closed loop control is verified through simulations in the *Simulink* simulation environment from software package *Matlab*. The control of the active rectifier is simulated for the parameters of the power system design obtained with the realization of the first objective. Moreover, the verification of the whole system control through simulations is completed for the resized system. Examination of the control performance is done by a comparative simulation of both continuous and discrete time implementation.

Besides, the thesis covered the complete process to the design of the interface elements defined with the objective of the thesis. That includes the design of the measurement transducers, the PCB interface between DSP and power stage, and configuration and control implementation in the DSP program.

Following the objectives, the developed design of the PCB interface is implemented and experimentally tested. The further adaptation to the design is proposed and validate. The experimental validation is concluded with the successful testing of the synchronization between the DSP and the IGBT module.

The final assembling of the setup could not be completed as some components required by design were not available for implementation before the project deadline. Consequently, experimental validation of the whole system could not be achieved.

## 7.2 Future work

The scope of the thesis in a way implies extensive tests and experiments and on-spot adaptations to optimize system and connect in a single functional unit. Assembling of the power stage and tests required for verification of the designed system are left for future work of the project due to the lack of time for completing the project. The initial idea was to do experimental validation of the setup through three stages. The first stage was verification of the control of the IGBT module in an open loop, providing voltage references, that are already verified. The second stage would test the closed loop control of active rectifier with connecting passive load instead of the PM machine. Thus, the grid side converter control would work in closed loop,

and the machine side converter controlled in the open loop. Finally, the proposed test on the third stage would be the closed loop control of both active rectifier and PM machine, connecting complete setup.

On the other hand, the future work to be proposed in this chapter will also go beyond the defined scope of the project to extend the range of possibilities of implemented application. The proposals of the future work that might be an enhancement to the application are:

- A more efficient PWM method as a space vector could be considered.
- Passive damping resistor used for attenuating resonance frequency of the LCL filter could be replaced with active damping control strategy, which could attenuate just resonance frequency comparing to passive one that also affects high frequencies.
- The switching behavior of the converter could be simulated and analyzed on a model with real IGBTs parameters. Specifically, it could be studied on optimal dead-time implementation for providing safe operation and minimum harmonic distortions (especially on higher frequencies).
- Even though not required by the project task, the range of the application could be extended for higher speeds by implementing flux weakening and MTPA control strategy.
- The monitoring of the application could be improved y replacing analog inputs to the DSP ad control ad measurements itself with interactive display or application using some of the available communication protocols of DSP (SCI, I2C, CAN), providing more accurate ad user-friendly configuration of setup.

# Appendix A

# dq0 Transformations

In general, many control strategies relay on transformation of stationary abc reference system to rotating dq0 reference frame. Form can slightly vary depending on convention used such as amplitude invariant, power invariant, 3/2 convention or similar. Just amplitude invariant convention will be discussed and used in thesis. Transformation is performed in two steps, Clarke and Park transformation. The Clarke transform converts the time domain components in abc reference frame to the orthogonal $\alpha\beta 0$ stationary frame. The Park transform converts the components in the $\alpha\beta 0$ frame to the rotating dq0 reference frame.

The Clarke transformation applied is called cosine-based transformation for which in t=0 a-axis of three phase abc reference system is aligned with $\alpha$-axis of the two-axis $\alpha\beta 0$ stationary frame. Mathematical law relating two transformations is given by equation A.1. Relation between components of stationary $\alpha\beta 0$ and rotating dq0 reference frame obtained by the Parke transformation is given by equation A.2. In order to simplify computation these two transformations are connected into one direct abc-to-dq0 transformation given by set of equations A.3. Inverse transform, derived by inversion of matrix is in form of matrix A.4.

$$\frac{2}{3}(f_a + f_b e^{-j\frac{2\pi}{3}} + + f_c e^{j\frac{2\pi}{3}}) = f_\alpha + j f_\beta \tag{A.1}$$

$$f_s = f_d + f_q = (f_\alpha + j f_\beta) e^{-j\omega t} \tag{A.2}$$

$$\begin{vmatrix} f_d \\ f_q \\ f_0 \end{vmatrix} = \frac{2}{3} \begin{vmatrix} \cos\omega t & \cos(\omega t - \frac{2\pi}{3}) & \cos(\omega t + \frac{2\pi}{3}) \\ -\sin\omega t & -\sin(\omega t - \frac{2\pi}{3}) & -\sin(\omega t + \frac{2\pi}{3}) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{vmatrix} \begin{vmatrix} f_a \\ f_b \\ f_c \end{vmatrix} \tag{A.3}$$

$$\begin{vmatrix} f_a \\ f_b \\ f_c \end{vmatrix} = \begin{vmatrix} \cos\omega t & -\sin\omega t & 1 \\ \cos(\omega t - \frac{2\pi}{3}) & -\sin(\omega t - \frac{2\pi}{3}) & 1 \\ \cos(\omega t + \frac{2\pi}{3}) & -\sin(\omega t + \frac{2\pi}{3}) & 1 \end{vmatrix} \begin{vmatrix} f_d \\ f_q \\ f_0 \end{vmatrix} \tag{A.4}$$

However, this transformation is conservative to amplitude, but not to the power. For system to be consistent and value of power equal in both system ($P_{abc} = P_{dq0}$) power in dq0 reference frame should be calculated using equation A.5.

$$P_{=} v_a i_a + v_b i_b + v_c i_c = \frac{3}{2}(v_d i_d + v_q i_q) \tag{A.5}$$

# Appendix B

# The Parameters of the control simulation

## B.1 Simulation of the control of active rectifier

Table B.1: The parameters of the control of active rectifier

| | | |
|---|---|---|
| Phase lock loop | | |
| **Bandwidth** | $BW_{PLL}$ | 20 Hz |
| **Proportional gain** | $K_{pPLL}$ | 0,7695 |
| **Integral gain** | $K_{iPLL}$ | 48,35 |
| $i_d$ current controller | | |
| **Bandwidth** | $BW_i$ | 400 Hz |
| **Proportional gain** | $K_{pi}$ | 9,3 |
| **Integral gain** | $K_{ii}$ | 1508 |
| **Limit of voltage amplitude** | $AW\_i$ | 600V |
| DC link voltage cotroller | | |
| **Bandwidth** | $BW_u$ | 40 Hz |
| **Proportional gain** | $K_{pu}$ | 0,000154 |
| **Integral gain** | $K_{iu}$ | 0,0077 |
| **Upper limit of output current** | $AW\_v_d\_up$ | 81,65A |
| **Lower limit of output current** | $AW\_v_d\_down$ | $-81,65A$ |

## B.2 Simulation of the control of complete system

Table B.2: The parameters of the control of permanent magnet machine

| $i_{sd}$ current controller | | |
|---|---|---|
| **Bandwidth** | $BW_c$ | 400 Hz |
| **Overshot** | $M_o$ | 10% |
| **Proportional gain** | $K_{pd}$ | 2,57 |
| **Integral gain** | $K_{id}$ | 5700,7 |
| **Limit of voltage amplitude** | $AW\_i_s$ | 280V |
| $i_{sq}$ current controller | | |
| **Bandwidth** | $BW_c$ | 400 Hz |
| **Overshot** | $M_o$ | 10% |
| **Proportional gain** | $K_{pq}$ | 2,88 |
| **Integral gain** | $K_{iq}$ | 6300,8 |
| **Limit of voltage amplitude** | $AW\_i_s$ | 280V |
| Speed controller | | |
| **Bandwidth** | $BW_s$ | 80 Hz |
| **Overshot** | $M_o$ | 10% |
| **Proportional gain** | $K_{ps}$ | 0.432 |
| **Integral gain** | $K_{is}$ | 183,74 |
| **Upper limit of output current** | $AW\_speed\_up$ | 58,35A |
| **Lower limit of output current** | $AW\_speed\_down$ | $58,35A$ |

Table B.3: The parameters of the control of active rectifier

| | | |
|---|---|---|
| Phase lock loop | | |
| **Bandwidth** | $BW_{PLL}$ | 20 Hz |
| **Proportional gain** | $K_{pPLL}$ | 1,54 |
| **Integral gain** | $K_{iPLL}$ | 96,7 |
| Current controller | | |
| **Bandwidth** | $BW_i$ | 400 Hz |
| **Proportional gain** | $K_{pi}$ | 6,26 |
| **Integral gain** | $K_{ii}$ | 1005,3 |
| **Limit of voltage amplitude** | $AW\_i$ | 280V |
| DC link voltage cotroller | | |
| **Bandwidth** | $BW_u$ | 40 Hz |
| **Proportional gain** | $K_{pu}$ | 0,000308 |
| **Integral gain** | $K_{iu}$ | 0,00314 |
| **Upper limit of output current** | $AW\_v_d\_up$ | 48.99A |
| **Lower limit of output current** | $AW\_v_d\_down$ | $-48,99A$ |

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