Switching Frequency Optimization for a Solid State Transformer with Energy Storage Capabilities

Pablo García, Sarah Saeed,
Ángel Navarro-Rodríguez, Jorge Garcia
Dept.of Elec., Computer & System Engineering
University of Oviedo. Gijón, 33204, Spain
Email: garciafpablo@uniovi.es, sarasaeedhazkial@gmail.com, navarroangel@uniovi.es, garciajorge@uniovi.es
Hannes Schneider
University of Stuttgart
Keplerstrasse 7, 70174 Stuttgart. Germany
Email: hannesschneider1988@googlemail.com

***Abstract*—This paper is focused on determining the efficiency dependency on the switching frequency for a solid state transformer (SST) with one of the ports connected to an energy storage device (Lithium-Ion battery). Some contributions for measuring the efficiency/losses for different power converter structures for energy storage applications can be found in the literature. However, there are few references which consider the impact of the high frequency behavior of the battery in the complete system performance. Moreover, to the best of the authors' knowledge, there is no study considering these effects when the energy storage system is directly coupled to an SST port. This research will firstly obtain parametric high frequency models of the battery cells and modules, the SST, and the power converter based on a vector fitting method in frequency domain. The models will be used to evaluate the system losses depending on the converter switching frequency and the dc-link capacitance. Experimental results confirm the accuracy of the proposed model as well as the battery losses dependency on the switching frequency, the dc-link capacitance and the State of Charge (SoC).**

I. Introduction

In the last years, there is an increased interest in the use of isolated multiport converters for interfacing multiple energy sources, loads and/or Energy Storage Systems (ESS) [1]. One solution for this interface is based on the so-called Solid-State Transformer (SST), which allows for removing the low frequency transformer usually employed for achieving the required galvanic isolation. There are several key aspects to be improved in the SST design, efficiency being one of the most important. For the efficiency estimation, there are some contributions in the literature reporting values ranging from 88% to 97% [2]–[5] .

When an ESS is integrated in one of the converter ports, it is critical to consider its contribution to the overall efficiency and, moreover, to determine the safe operation conditions for the ESS itself. The impact of the converter switching harmonics on Lithium-Ion batteries has been already discussed [5]. For the integration of the ESS there are two main options: 1) to use a dedicated DC/DC converter for the interface or 2) to directly connect the battery to the DC side of one of the ports. When possible, the second option is preferred due to both cost reduction and increased reliability on the power electronics interface. However, the interface without any active element will impose on the battery higher stress due to the current harmonics. In order to mitigate the current ripple effects, a film capacitor for the dc-link can be put in parallel with the battery and, if required, a series inductance on the converter DC terminals. Still, adding passive elements decreases the overall reliability of the system and thus their use should be optimized.

Considering the switching harmonics effects, it is clear that the switching frequency value will affect different system elements in opposite ways. For the case of the power converter, increasing the switching frequency will mainly increase the switching losses. However, considering the impact on the battery, higher switching frequency values will reduce the current ripple and the losses due to the dominant inductive behavior at high frequencies [5], [6]. For these reasons, the losses at the different elements in the system must be considered. In this paper, the following losses are included: 1) losses at the SST input and output bridges, including voltage drop in the semiconductors and dead-time effects; 2) overall losses at the high-frequency transformer; 3) conduction losses at the series filter; 4) high-frequency losses at the dc-link and 5) high-frequency losses at the battery pack.

The discussion is organized as follows. Section II includes a description of the system where the ESS is used. Section III shows the proposed high frequency analytical model as well as the experimental characterization of the battery cells and the parameter estimation. Section IV considers the high frequency model for the converter passive elements, i.e. transformer, series inductances and dc-link capacitor. Section V develops the simulation results as well as the experimental validation for the calculation of the power converter efficiency under different operating conditions.

The present work has been partially supported by the predoctoral grants program Severo Ochoa for the formation in research and university teaching of Principado de Asturias PCTI-FICYT under grants ID BP14-135 and BP16-133. This work also was supported in part by the Research, Technological Development and Innovation Program Oriented to the Society Challenges of the Spanish Ministry of Economy and Competitiveness under grants ENE2013-44245-R and ENE2016-77919-R and by the European Union through ERFD Structural Funds (FEDER)

II. System description

Integration of an ESS in a multiport power converter can be achieved by different options. Fig. 1 shows three alternative muliport DC-DC power converter topologies. If galvanic isolation is required for the ESS or in the case there is a high mismatch among the three dc-link voltage levels, option 1a) is a viable choice. For option 1a), an additional power conversion state between the ESS and the power converter port can also be used (with the same topologies proposed in 1b) or 1c)).

In this paper, option 1a) is analyzed for the interface of the ESS. Even if the real setup consists on a Tripple-Active-Bridge (TAB) converter, only two of the ports are considered during the analysis. This simplification will allow to focus the study on the energy storage losses, removing the additional control complexity in the TAB converter. It is also worth noting that, even if some previous research has been conducted for the efficiency calculation in power converters with energy storage capabilities, [5], [7], there are not investigations considering active bridge converter based configurations without resonant network topologies. On these kind of converters, it is expected that the pulsating nature of the DC currents (often filtered with a parallel connected dc-link capacitor) potentially affects the battery-aging. An initial study considering this power topology was published by the same authors in [8]. However, on that publication, the losses at the energy storage were evaluated just considering the high-frequency model for the cells at a constant SoC value. This paper experimentally validates the proposed model for different SoC values, includes the high-frequency model of the battery module and analyzes the effect of the dc-link capacitance.

The TAB with the ESS is used as the interface of a low-voltage distribution microgrid, as shown in Fig. 2. The TAB internal structure and the laboratory setup are shown in Fig. 3 and 4 respectively. The high-side DC link for the first port is connected to the AC main grid three-phase active rectifier, the second port is connected to the ESS and the third one to the low-side DC link. At the low-side DC link there are two independent 4-wire inverters, namely head nanogrid converters (HNGC), providing the AC distribution downstream to the so called nanogrid (nG). For the control of the TAB, the power-flow at the high-side (i_{hs}) and ESS (i_{ess}) ports are controlled by means of the corresponding currents at each port, whereas the dc-link voltage at the low side (v_{ls}) is controlled by the low-side port. A more detailed explanation can be found in [9].

For this paper, a simplified power and control structures are selected in order to keep the focus on the losses impact due to the ESS. The high-side port is disconnected, and the analysis is restricted to the ess and ls ports. The v_{ls} voltage is controlled by one of the HNGC and the SST operates in power control mode, thus enabling the evaluation of the bidirectional power flow between the battery and the low-side port. This allows for investigating the effects on the losses due to the charge/discharge of the battery operated at different power levels. Under that considerations, the analyzed system is reduced to a dual-active-bridge (DAB), as shown in Fig. 5.

III. Battery cells high frequency model

In order to derive the model for the ESS, the battery has to be modeled at cell level. For that purpose, firstly the cells' high frequency impedance has been recorded in the laboratory. Secondly, the parameters of the battery model have been estimated by a vector fitting method. The investigated cell is a 18650-sized high-energy round cell with a nominal capacity $C_{Nominal,Cell}$ of 3.2 Ah and a nominal cell voltage $U_{Nominal,Cell}$ of 3.3V. On obtaining the proposed high frequency model, it has to be mentioned that the impedance spectrum of a battery is dependent on the actual SoC, the temperature and cycling [10]–[12]. The SoC effect will be later shown during the presentation of the experimental results.

For the impedance spectrum recording, an Agilent 4294A Precision Impedance Analyzer has been used. The device is capable of taking measurements in the impedance range of 1mΩ to 1MΩ with an accuracy of 0.08% and operates in the frequency range of 40Hz $-$ 110MHz. For a good accuracy the cell was connected via high frequency coaxial cables to the terminal connection, applying the four-point probes method [13]. The scheme of the setup, as well as the considered high frequency model, is shown in Fig. 6. The high frequency model topology has been already proposed in previous literature references [6].

All measurements have been recorded in the range of $40Hz$ $-$ 200kHz in potentiostatic mode (constant voltage amplitude for the excitation signal) with a 100mV amplitude and an averaging factor of 16. Moreover, a DC-Bias voltage has been applied in order not to charge or discharge the battery. The ambient and the cell's temperature were kept constantly at 27 degrees during the measurement. The temperature was observed with an HIBOK75 infrared thermometer.

As presented in [6], the impedance based high frequency model shown in Fig. 6, consists of two resistors and two inductors. The parameters of this model were derived by approximating the frequency response of the cells for different SoC with the expression shown in (1), where s is the Laplace variable [14]–[16].

$$f(s) \approx \sum_{m=1}^{N} \frac{c}{s-a} + d + s \cdot e \tag{1}$$

The relationship between the coefficients shown on (1) and the high-frequency model parameters have been done as follows. Using the equivalent high-frequency model shown in Fig. 6, the cell high frequency impedance can be approximated by a $m = 1$ order system given by (2)

$$Z_{cell}(s) = R_1 + sL_1 + \frac{L_2 s R_2}{L_2 s + R_2} \tag{2}$$

By comparing the polynomial coefficients of (1) and (2), the equivalences in (3) can be obtained.

$$R_1 = \frac{d \cdot a - c}{a}; \quad R_2 = \frac{c}{a}; \quad L_1 = e; \quad L_2 = -\frac{c}{a^2} \tag{3}$$

The estimated parameters for the two different SoCs of 50% and 100% are presented in Table I.

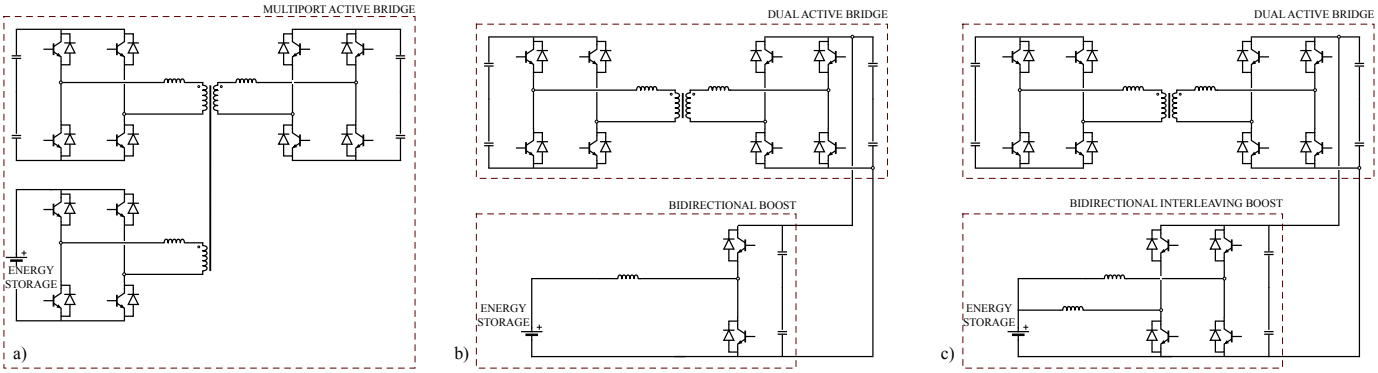

Fig. 1. Considered bidirectional multiport DC-DC converters with galvanic isolation. a) Triple-Active-Bridge with ESS integrated in one of the ports, b) Dual-Active-Bridge with ESS integrated by using a bidirectional boost converter, c) Dual-Active-Bridge with ESS integrated by using a bidirectional interleaving boost converter.

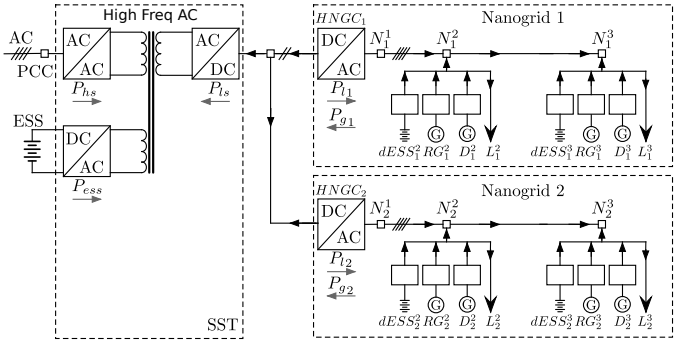

Fig. 2. Proposed MG structure. The 3P-SST allows for the exchange of power among the different grid points (AC mains, centralized ESS and AC nG). Each of the nG is powered by a 4-wire HNGC. The internal nodes (N_x^y) of the two nG represent buildings to which the different loads (L_x^y), DG (both renewable, RG_x^y, and dispatchable, D_x^y) and dESS are connected.

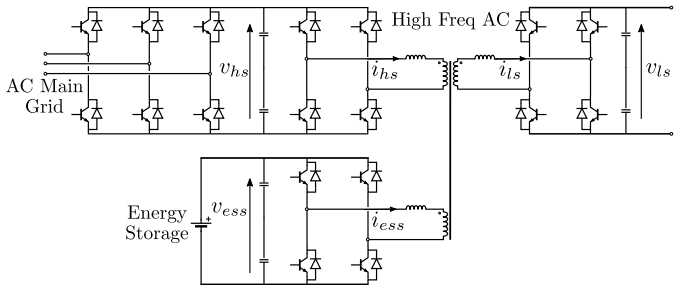

Fig. 3. TAB internal structure and variables used for the control implementation.

Fig. 4. Experimental setup. The figure shows the TAB and low-side converter as well as the ESS.

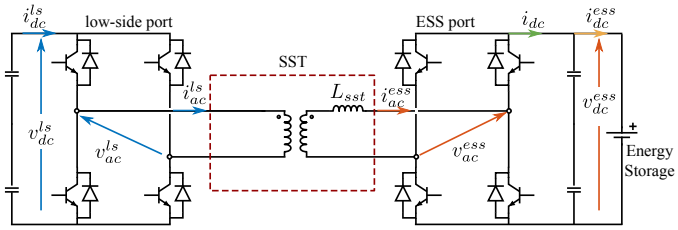

Fig. 5. Dual-Active-Bridge topology used for the paper analysis.

A comparison between the measured and the modeled impedance (magnitude and phase) is presented in Fig. 7 and Fig. 8 for 50% and 100% SoC respectively. In order to find an equivalent model, several measurements have been taken and the resulting average value has been estimated by the fitting method explained previously. As it is clearly shown, there is a good matching between the real data and the approximation. Regarding the data dispersion, both cells have a similar behavior, even if the phase for the 50% of the SoC shows a difference of around 10 deg. From the obtained data, an initial high-frequency model of the complete energy storage system will be built by the needed parallel/series connections. This assumption is also consistent with the low dispersion found in the parameters of the Lithium-Ion cells when dealing with the traditionally used low-frequency models [17], [18]. Also, it is easy to perceive the expected inductive behavior of the cells on the high frequency region. As it can be also seen, there is a noticeable difference in the impedance values, depending on the SoC which could potentially affect the overall performance of the power converter, as later discussed in Section V.

The complete ESS is built by 8 modules connected in series. Each of the modules has an arrangement of 15 parallel strings, being each string made by 15 cells connected in series. This leads to the final electrical model for the overall impedance: 120 series cells (N_s) and 15 parallel strings (N_p). The complete system transfer function is then given by the

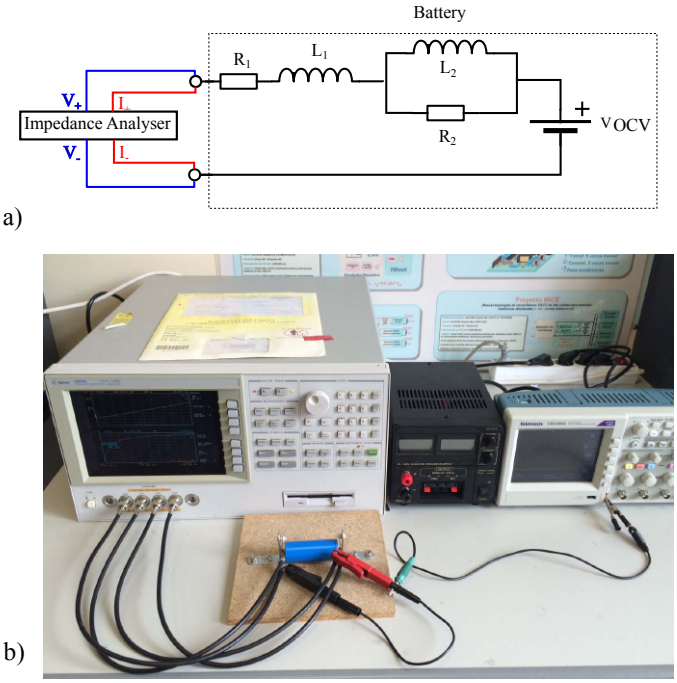

Fig. 6. Impedance measurement setup. a) Connection scheme and used high-frequency model. b) Measurement setup using the impedance analyzer.

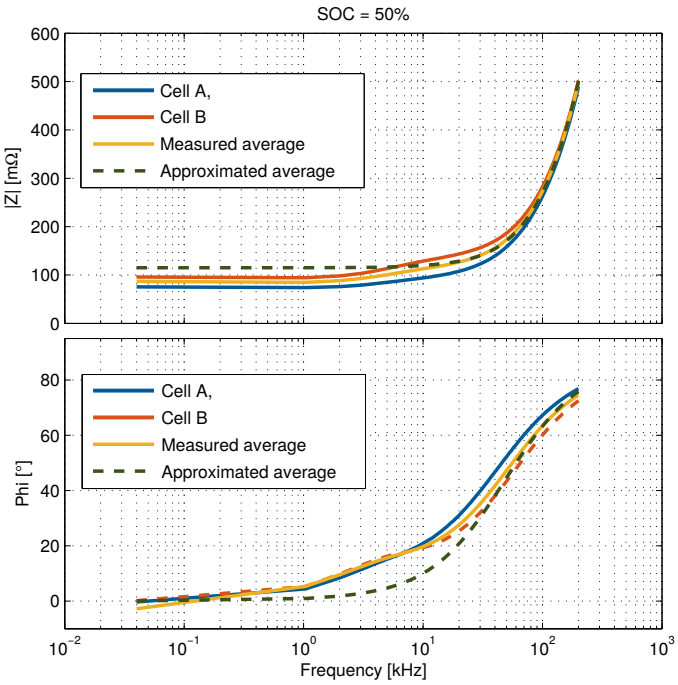

Fig. 7. Measured and approximated impedance for SoC = 50%

TABLE I
ESTIMATED BATTERY PARAMETERS

Parameter	100% SoC	50% SoC
R_1	50.66 $m\Omega$	115.0 $m\Omega$
R_2	28.4 $m\Omega$	6.9 $m\Omega$
L_1	2.6847 μH	2.4307 μH
L_2	0.13364 μH	0.61274 μH

equivalent impedance (4).

$$Z_{batt}(s) = \frac{N_s}{N_p} = \frac{120}{15} = 8 \cdot Z_{cell}(s) \tag{4}$$

IV. Power Converter High Frequency Model

For the power converter characterization, different elements have been measured in the high frequency region by first using the same impedance analyzer than for the battery cells. The SST, series inductances and power stack have been considered. This will allow to build a precise high frequency model of the complete system.

The transformer impedance, series inductances and power stack impedances are shown in Fig. 9, 10 and 11. It is worth noting that for the case of the power stack measurements, the impedance between the positive and negative terminals of the stack has been recorded. That impedance accounts for the dc link, the snubbers and the discharge resistance. This overall impedance is connected in parallel with the ESS and thus affects the share of the high frequency components.

From the data depicted at Fig. 9, the parameters for the transformer high frequency model have been obtained. The equivalent circuit as well as the corresponding values are shown in Fig. 12. It is recalled here that even if the transformer

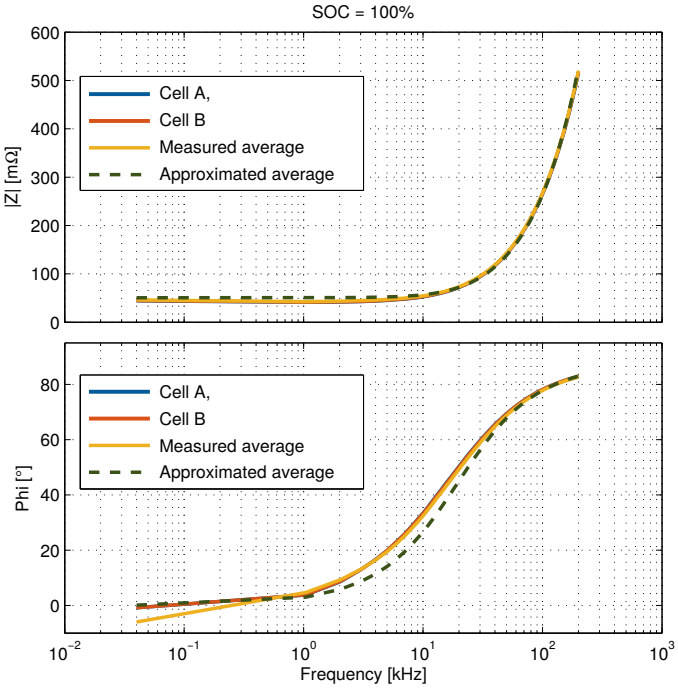

Fig. 8. Measured and approximated impedance for SoC = 100%

is a three port, just the two ports interfacing the ESS and the low-side dc link are represented. Still, for setting the values, the standard procedure for three-winding transformers has been used [19].

V. Power Converter Operation and Efficiency Measurement

Measurement of the system efficiency has been done in frequency domain, considering the contribution of the different

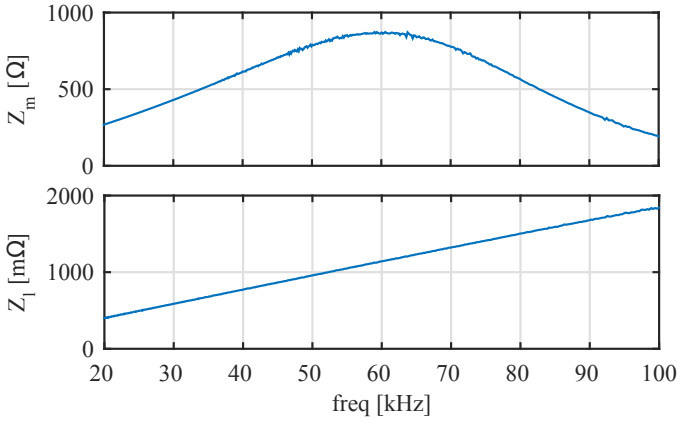

Fig. 9. Transformer high frequency impedance module. Top, magnetizing impedance. Bottom, leakage impedance $20-100$kHz.

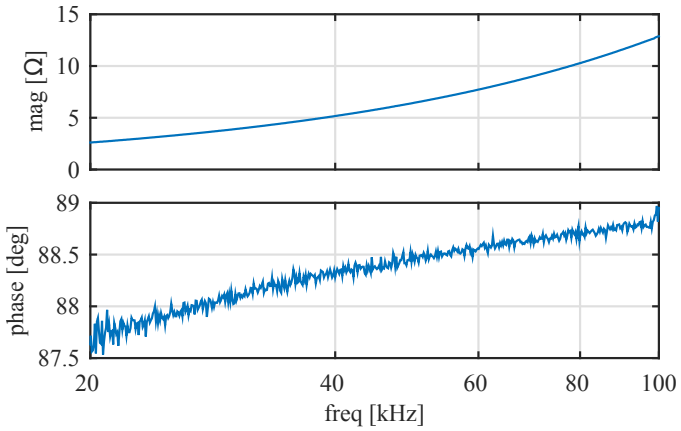

Fig. 10. Series inductance high frequency impedance in the range $20-100$kHz.

harmonics. For that, the power converter was tested at different operating points in steady state condition. A sample time of 0.5μs was used for recording the data and 2M samples were used for the analysis, thus leading to a 1Hz resolution in frequency domain. Input/Output voltages and currents have been measured at the different elements and the ratio between the input and the output power was used for determining the efficiency. Active power definition in frequency domain is given by (5)

$$P = \sum_{f_i=f_1}^{f_i=f_2} P_{fi} = \frac{1}{2} \cdot \sum_{f_i=f_1}^{f_i=f_2} |V_{fi}| \cdot |I_{fi}| \cos\left(\angle V_{fi} - \angle I_{fi}\right) = \frac{1}{2} \cdot \sum_{f_i=f_1}^{f_i=f_2} Re(Z_{fi}) \cdot |I_{fi}|^2 \quad (5)$$

, where $|V_{fi}|$, $|I_{fi}|$ are the modulus of the harmonic complex values for the voltage and the current repectively and $Re(Z_{fi})$ is the real part of the impedance at f_i frequency.

For determining the system efficiency and the losses, different frequency bands in (5) have to be considered. For that, it is necessary to know both the mathematical expression for the power transmission in a DAB converter and the relationship between the ac-side and the dc-side currents. Considering the

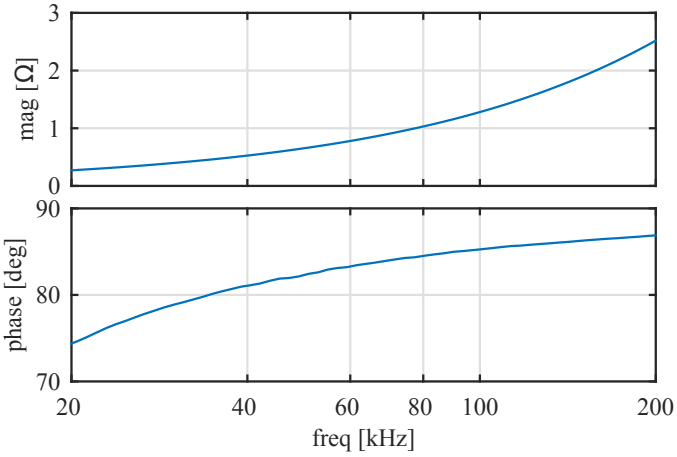

Fig. 11. Stack high frequency impedance in the range $20-200$kHz.

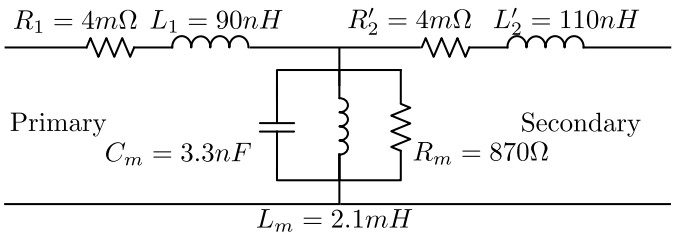

Fig. 12. SST model and experimentally measured parameters including parasitic elements.

DAB operation principle using single-phase shift method [20], the power transfer between the two ports depends on the switching frequency, and is given by (6)

$$P_{DAB} = \frac{V_{ac}^{ls} \cdot V_{ac}^{ess}}{(2\pi f_{sw}) L_{sst} \pi} \phi(\pi - \phi) \quad (6)$$

, where the variables are defined according to the schematic shown in Fig. 5, f_{sw} is the switching frequency and ϕ is the phase between the voltages at the two ports.

For analyzing the losses' contribution of the different parts connected to the dc-side of the power converter (dc-link, snubber, battery), it is necessary to determine the expression of the overall dc-side current as a function of the ac-side voltage and current. A good approximation, neglecting the diode recovering time is given by (7).

$$i_{dc} = i_{ac}\left(S_1 - S_2\right) \quad (7)$$

, where S_1 and S_2 are the states ($[0,1]$) of the full-bridge complementary switches that can be obtained from the ac-side voltage as $S_1 = (v_{ac} > 0)$ and $S_2 = (v_{ac} <= 0)$.

In Fig. 13, the key waveforms needed for the efficiency calculation are shown. As it can be seen, the fundamental frequency at the ac-side is equal to f_{sw}. The fundamental frequency of the ripple at the dc-side is a second harmonic, $2f_{sw}$. According to that, losses are calculated in bands centered at f_{sw}, $2f_{sw}$ and $4f_{sw}$, considering each band with a bandwidth of 4kHz. The measurement of the efficiency at each element is described as follows:

- **Power converters**. Considering the power transfer from the sending port (s) to the receiving port (r), the effi-

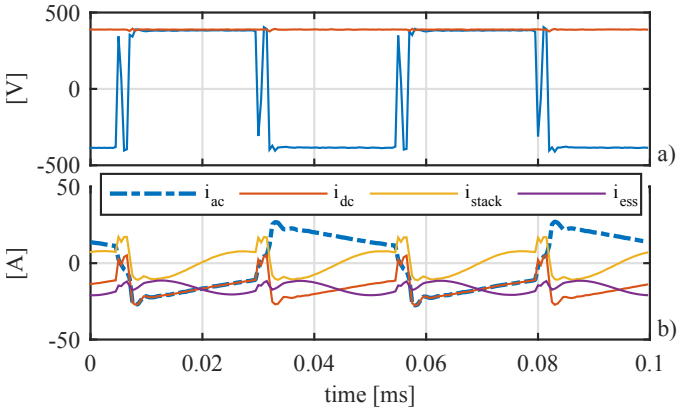

Fig. 13. Fundamental waveforms for the efficiency calculation. a) voltages v_{ac} (blue) and v_{dc} (red), b) currents. $f_{sw} = 20$kHz.

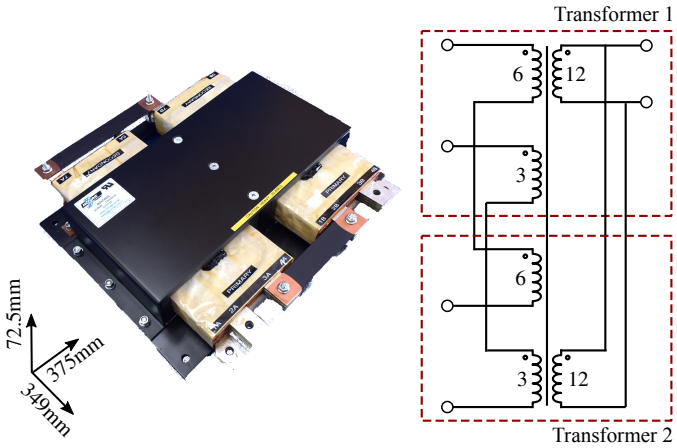

Fig. 14. SST design. On the left, a picture of the final design. On the right, the winding arrangement for the three ports.

ciency at the sending power converter is calculated as $\eta_s = \frac{v^s_{ac} i^s_{ac}}{v^s_{dc} i^s_{dc}}$ and at the receiving as $\eta_r = \frac{v^r_{dc} i^r_{dc}}{v^r_{ac} i^r_{ac}}$.

- **High frequency transformer and series inductor**. The efficiency of both elements is measured as a single element, using the ratio of the AC power at the receiving port (output) to the power of the sending port (input). $\eta_{sst} = \frac{v^r_{ac} i^r_{ac}}{v^s_{ac} i^s_{ac}}$. The used transformer is a planar transformer with the parameters shown in Fig. 12. A detailed figure about the final design is shown in Fig. 14. In order to accommodate for the power requirements, two transformers are coupled together according to the winding arrangement shown in the figure. The proposed efficiency measurement does not allow for the separation of the different transformer losses, but only their aggregated contribution.
- **Stack losses**. Those losses account for the dc-link and the snubbers. Stack losses are calculated using the expression (8) considering the stack high-frequency model obtained by frequency fitting and the estimated stack current.

$$loss_{stack} = \frac{1}{2} \sum_{f_i=2f_{sw}}^{f_i=4f_{sw}} Re\left(Z^{stack}_{fi}\right) \left| i^{stack}_{dc\ |f_i} \right|^2 \quad (8)$$

- **Battery losses**. Similar to the stack losses, the battery losses are calculated using the proposed high frequency model and the battery current by using (9).

$$loss_{ess} = \frac{1}{2} \sum_{f_i=2f_{sw}}^{f_i=4f_{sw}} Re\left(Z^{ess}_{fi}\right) \left| i^{ess}_{dc\ |f_i} \right|^2 \quad (9)$$

- **Battery port efficiency**. Considering the proposed losses calculation in (8) and (9), the overall battery port efficiency at the dc-side is calculated as (10).

$$\eta_{ess} = \frac{v^{ess}_{dc} i^{ess}_{dc\ |f_i=0}}{v^{ess}_{dc} i^{ess}_{dc\ |f_i=0} + loss_{stack} + loss_{ess}} \quad (10)$$

For obtaining the frequency-domain-based efficiency, the DAB has been operated in open-loop power transfer mode by adjusting the phase shift between the ess and the ls ports. At the low-side port, a bidirectional DC/AC converter is used for controlling the dc-link voltage. The battery was operated at three different SoC: 90%, 75% and 50% and all the experiments have been carried out with the power going from the ess port to the ls port.

A. Simulation results

With the developed high-frequency model of the cell, several simulations have been carried out. The operation has been tested by integrating the ESS into a DAB power converter, as shown in Fig. 5. The power converter has been initially designed for a nominal switching frequency of 20kHz. Different switching frequencies below and above the nominal one (range of 16kHz to 40kHz) have been used.

For the following measurements the phase shift angle, ϕ, has been set to 90 degrees in order to achieve the maximum power transfer capability. The resulting efficiency measurements are depicted in Fig. 15. Important conclusions can be obtained from the results analysis. First of all, there is a reduction in the efficiency due to the battery high frequency losses. Also, there is a dependency on the SoC. Since the efficiency is increased with increased frequencies (inductive behavior of battery high frequency model), it is expected that this changes the optimal switching frequency. It is also worth noting the reduction in the losses by adding a parallel capacitor to the battery ($C = 3.28\mu$F). This behavior is due to the low ESR of the parallel capacitance in comparison with the one provided by the battery. This two aspects will be experimentally analized during the experimental results.

B. Experimental results

Considering the results given by the simulation results, the experimental results are intended to test both the influence of the switching frequency and the stack paralell capacitance over the overall efficiency. For the experimental results validation, a relaxing time of 15 minutes was kept between each experiment to ensure the battery is at rest conditions. Losses calculation due to the switching harmonics has been carried out in frequency domain following the procedure explained before. The setup previously shown in Fig. 4 has been used for

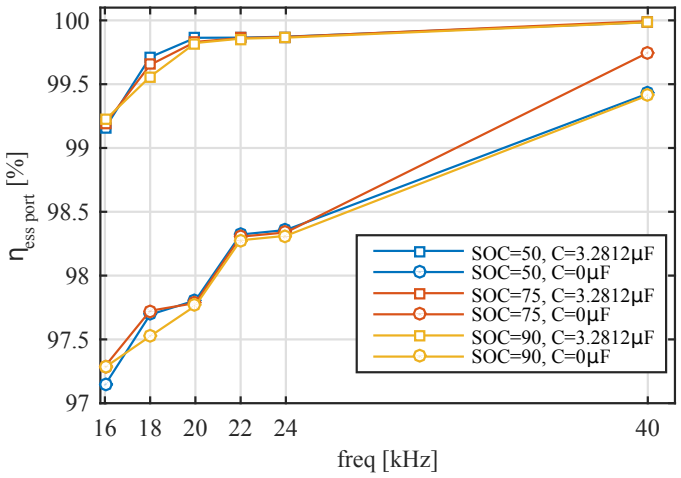

Fig. 15. Estimated efficiency calculations for the energy storage system according to expression (10). Three different SoCs and two different values for the stack capacitance are represented.

TABLE II
PARAMETERS FOR THE EXPERIMENTAL SETUP

Parameter	Value
Power Converter	
Power	150kVA
Switching freq.	20kHz
Port 1	Header Converter 750Vdc
Port 2	ESS 400Vdc
Port 3	Inner Microgrid. Low DC link 750Vdc
DC-link capacity (each port)	420μF
Series inductors (Port 2 and 3)	38μH
Li-Ion Battery	
Rated voltage	384V
Max. voltage	438V
Max. discharge current (2C)	96A
Max. charge current (3C)	144A
Nom. capacity	18.4kWh

the experiments. The most important parameters both for the converter and the ESS are shown in Table II.

Several experiments were conducted in order to evaluate the impact of the switching frequency over the efficiency. The different signals involved in the efficiency calculation (v_{dc}^{ls}, i_{dc}^{ls}, v_{ac}^{ls}, i_{ac}^{ls}, v_{dc}^{ess}, i_{dc}^{ess}, v_{ac}^{ess}, i_{ac}^{ess}), were captured with a scope with a sample time of 0.5μs. Isolated voltage probes (Yokogawa 700924 100MHz bandwidth, 100 : 1, 2% gain accuracy) were used for the voltage measurements and current probes (Yokogawa 701930 DC-10MHz, 300A-Peak, 1% accuracy) for the currents. The DAB was operated in open loop under different switching frequencies, $[16-40]$kHz. The power was kept nearly constant at the different frequencies by adjusting the phase shift between the two ports. The data was stored and processed offline for getting the efficiency values. The resulting waveforms are shown in Fig. 16. Corresponding frequency domain signals used for the efficiency calculation at the ess port are shown in Fig. 17.

Using the proposed cell's high frequency model shown in (2) for the estimation of the losses allows to evaluate the effect of different capacitance values in the battery efficiency. However, this requires to evaluate if the measured high frequency response at cell level can be extended to the module

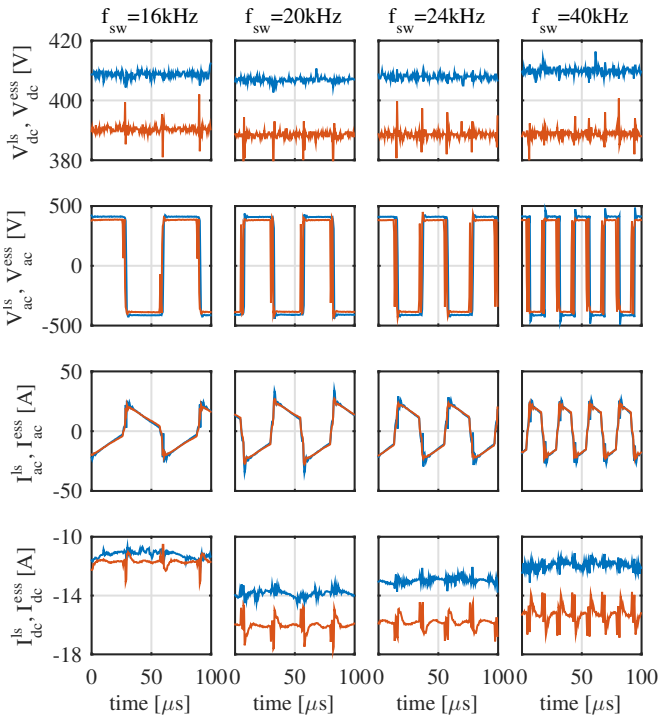

Fig. 16. Experimental results. Recorded waveforms for the dc voltages, ac voltages, ac currents and battery dc current for four different switching frequencies. Blue color is used for the ls port and red for the ess port.

level (15 series cells per string and 15 strings). For that, the module response in the high frequency region has been measured using a bidirectional boost converter. A periodic square-wave voltage disturbance has been commanded to the power converter, and the voltage and current at the module terminals have been measured using the same equipment described before. The frequency response for the impedance has been calculated as $\frac{fft(V_{dc}^{ess})}{fft(I_{dc}^{ess})}$. The recorded signals and the corresponding frequency response are shown in Fig. 18. The resulting estimated impedance has been compared to the one given by the cell's model and the results are shown in Fig. 19. The obtained impedance is shown scaled to battery level by considering the eight modules connected in series. Clearly the proposed model is a good approximation at the studied switching frequency region (20-40kHz), even if the impedance is higher than predicted and the phase below 20kHz shows a significant deviation. The higher impedance values at module level could be related with the additional impedance because of the connections between the individual cells. Considering those differences between the individual cells high-frequency response and the module response, the final efficiencies will be calculated using the module measured impedance (Z_{mod}). Considering the battery system is built by the series connection of 8 modules, the overall battery impedance can be calculated as $Z_{ess} = 8Z_{mod}$. The obtained equivalent circuit parameters depending on the SoC, according to the described polynomial fitting procedure, are shown in Fig. 20.

By repeating the described experiment for different SoCs=$[40, 55, 70, 85, 100]$% and pulse frequencies, f_{sw} =

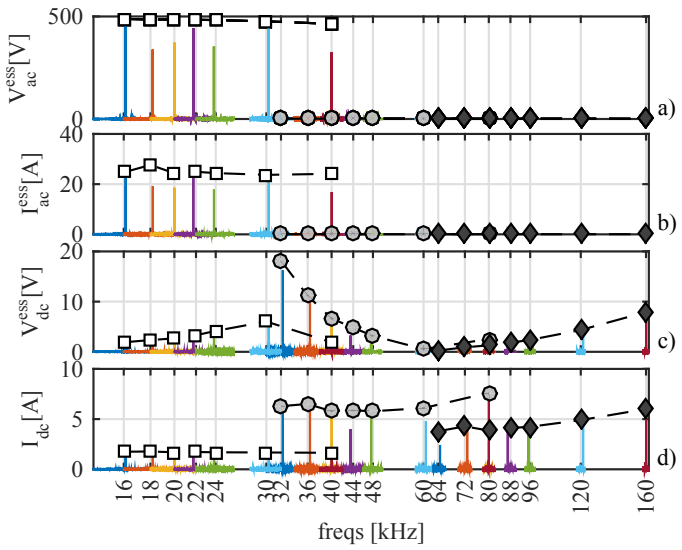

Fig. 17. Experimental results. Spectrum of the a) v_{ac}^{ess}, b) i_{ac}^{ess}, c) v_{dc}^{ess} and d) i_{dc}^{out} signals for all the tested switching frequencies. Battery SoC is 90%. Dashed line shows the equivalent energy signal at each of the switching frequencies, calculated as $\sqrt{\sum_{i=f_c-2kHz}^{f_c+2kHz}|s_i|^2}$, where s_i is the analyzed signal. White squares are for the $f_c = f_{sw}$ band, grey circles for the $f_c = 2f_{sw}$ and black diamonds for $f_c = 4f_{sw}$.

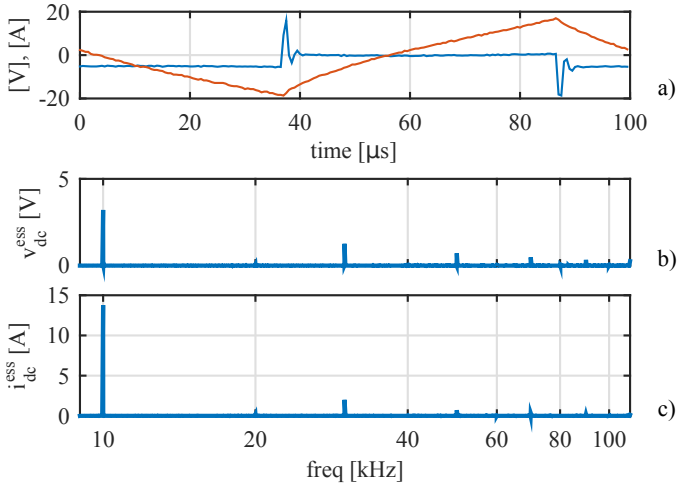

Fig. 18. Experimental results. Pulse injection for the identification of the module impedance. Different frequencies for the square-wave pulses (5, 6, 7, 8, 9, 10, 20kHz) were used for getting the module frequency response. Figure shows the 10kHz experiment. a) v_{dc}^{ess} (blue) and i_{dc}^{ess} (red), b) and c) frequency response of the voltage pulse and the current response respectively.

$[5, 6, 7, 8, 9, 10, 11, 12, 20]$ kHz, the change of the battery impedance with respect to the operating conditions can be obtained. The resulting values are shown in Fig. 21. As it can be seen, both the module and the phase impedance increase with the frequency, according to an inductive behavior. It is also clearly visible the variation with respect to the SoC, particularly for the module.

The effect of the dc-link capacitor and snubber values has been also evaluated using the following procedure. The measured stack high-frequency impedance model in frequency domain has been approximated by a series connected resistance, inductance and capacitance, i.e: $z_{stack} = R_s + L_s \cdot s + 1/(C \cdot s)$.

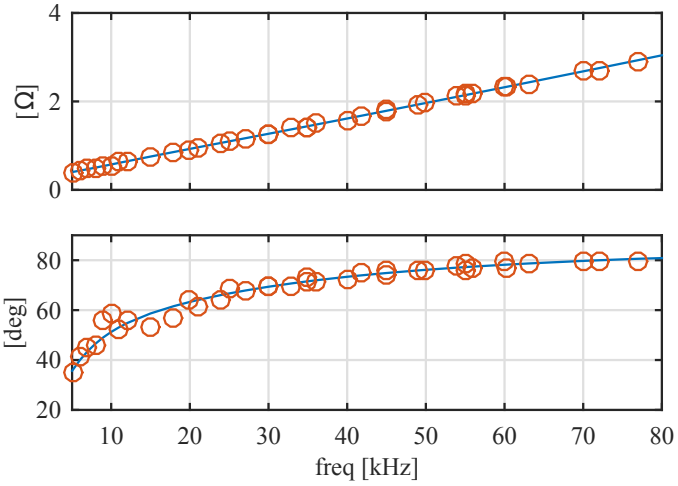

Fig. 19. Experimental results. Battery impedance. Comparison between the cell high frequency model using (2) (blue) and the measured module response (red). Results are scaled, both from the cell-level and the module-levels measurements by multiplying the impedance by the number of series modules used in the battery, $N_s = 8$. Results are shown for a $SoC = 70\%$.

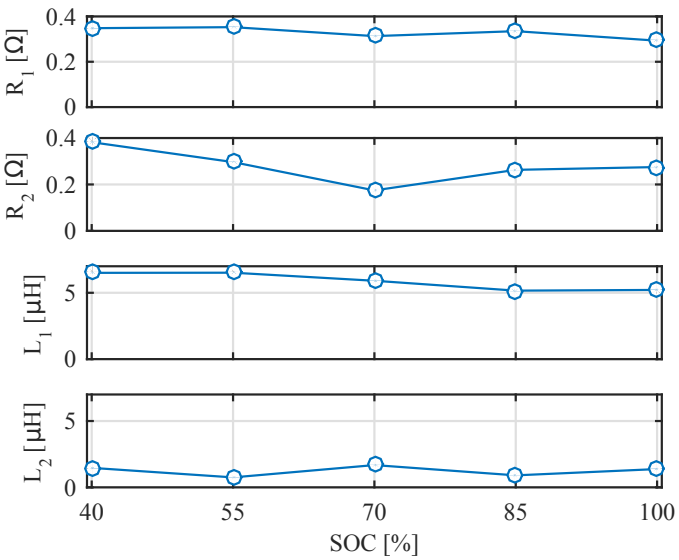

Fig. 20. Experimental resuluts. Evolution of battery equivalent parameters in function of the SoC.

The frequency response and the estimated parameter values are shown in Fig. 22.

After that, the obtained capacitance value has been varied by simulation, while keeping the series resistance and inductance constant. The resulting stack impedance plotted together with the battery one is shown in Fig. 23. As clearly seen, the stack impedance module is larger than the battery one in the lower frequencies region and smaller in the high frequency. Decreasing the capacitance value shifts the crossing point to higher frequencies. Considering the analyzed switching-frequency region ($16-40$kHz), the stack impedance is smaller even for capacitance value around 13μF. The main conclusion that can be obtained from this study is that it is feasible to reduce by a significant fraction the dc-link capacitor in the battery side barely affecting the harmonic current going to the battery, and thus the losses.

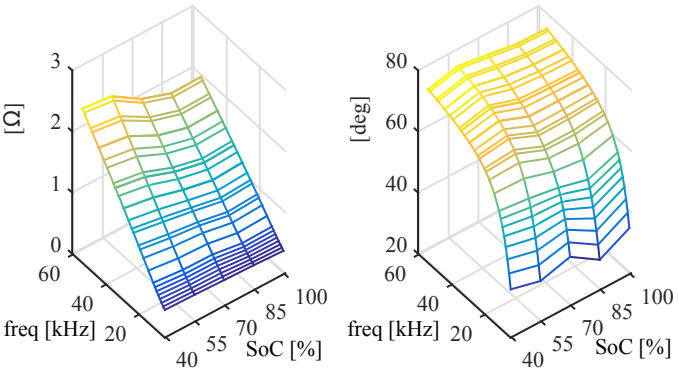

Fig. 21. Experimental results. Evolution of the battery impedance module (left) and phase (right) with respect to different SoC and switching frequency values.

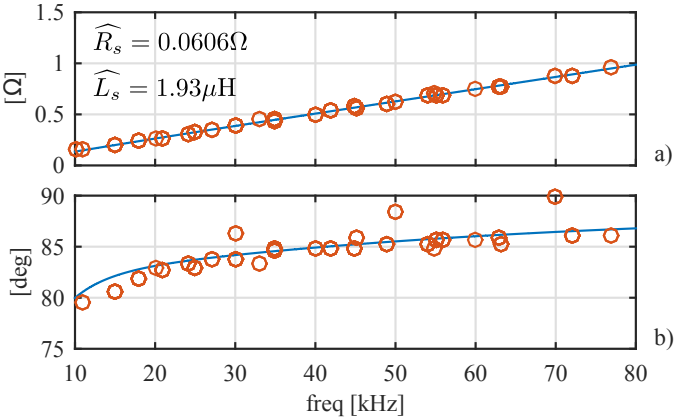

Fig. 22. Experimental results. Measured stack high-frequency impedance. a) module, b) phase.

In Fig. 24, the different powers measured at the two involved transformer ports are shown for the three different SoCs. As it can be seen, the power transferred for the different experiments is kept nearly constant for all the switching frequencies except for the 18kHz value. This is due to the phase-shift control being implemented in open-loop. Taking into account that the efficiency values will be normalized with respect to the transmitted power, the importance of this variations are considered to be not significant.

In Fig. 25, the efficiencies for the individual elements of the power converter are shown. For calculating the battery efficiency, the proposed stack high-frequency model has been used, considering a parallel capacitance of 3.2μF. As it can be readily seen, the efficiency of the battery and the efficiency of the two power converters and the transformer follow opposite trends. As already explained, this is due to the inductive behavior of the battery and the switching losses at the switches and at the transformer. Because of that opposite trend, an optimal point for the switching frequency is expected.

This is confirmed with the results depicted in Figs. 26 and 27, where the converter efficiency with and without the battery is represented for two different capacitance values. Obviously, taking into consideration the battery efficiency will result in a lower overall efficiency. However, it is more important the fact that the overall efficiency curves for the different SoCs have

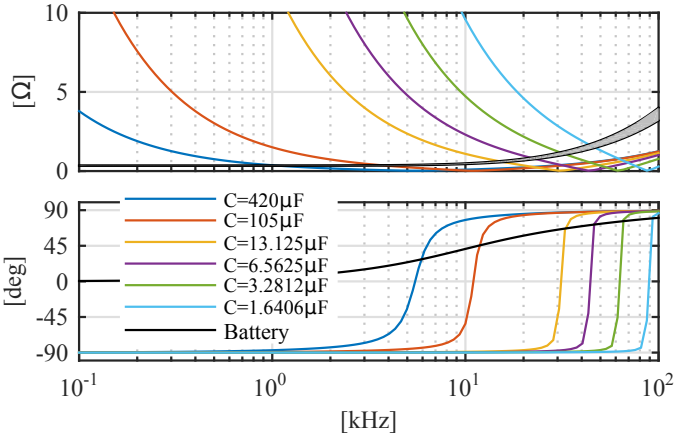

Fig. 23. Experimental results. Influence of dc-link capacitance over the stack impedance. The battery impedance region for all the considered SoC is also plotted in light grey for the comparison.

maximums at different frequencies, 18 to 20kHz, which moves apart from the converter nominal frequency by a 10%. The boost in the efficiency with respect to the nominal frequency is, depending on the SoC, slightly higher than 1%, which is an important contribution to the complete system efficiency.

In Fig. 28, a similar analysis is carried out but this time with a varying stack parallel capacitor. The parallel capacitor has been added considering the remaining parameters of the stack high frequency model (Fig. 28) to be the same. As it can be seen, values above 13μF do not improve the system efficiency. This allows to reduce the value of the dc-link capacitor, thus reducing the system costs. Even more, considering that the improvement in the efficiency is barely increased above 3.3μF, even removing the dc-link capacitor while keeping the snubber could be valid for some applications.

VI. Conclusion

This paper has developed an analysis on the selection of the switching frequency effects and the stack capacitance for an isolated power converter with integrated ESS. As remarkable conclusions, the presented research enables system designers to reduce the value of the dc-link capacitance. It also allows existing designs to be operated with improved efficiency by adaptively varying the switching frequency in function of the SoC value. As shown in the results, the battery losses are dependent on the switching frequency. Moreover, the contribution of the battery losses to the overall efficiency can have a noticeable effect. This makes the selection of the optimal switching frequency a non-trivial task. For determining the switching frequency effects on the complete system, the high frequency model of the solid state transformer, the power stack and the battery cells at different SoCs have been experimentally obtained. The efficiency of the power converter has been calculated using a full scale laboratory setup. By operating the converter at different switching frequencies, $[16-40]$kHz, the losses at the real battery, for three different SoCs of $[90, 75, 50]$%, have been experimentally calculated and their impact has been extensively discussed. A boost of 1% in the overall system efficiency can be achieved by proper

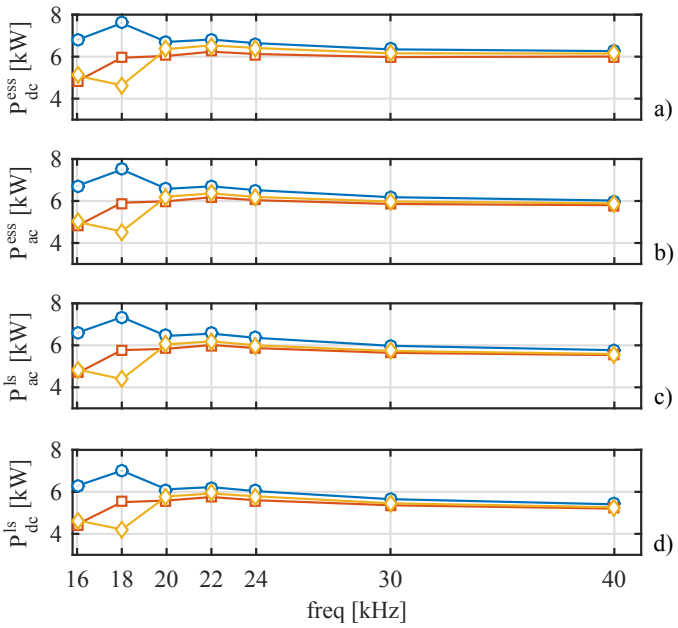

Fig. 24. Experimental results. Power distribution in function of the switching frequency for the three different SoCS (blue-50%, red-75%, yellow-90%). From top to bottom: a) power at the dc side of the ess port, b) power at the ac side of the ess port, c) power at the ac side of the ls port, d) power at the dc side of the ls port.

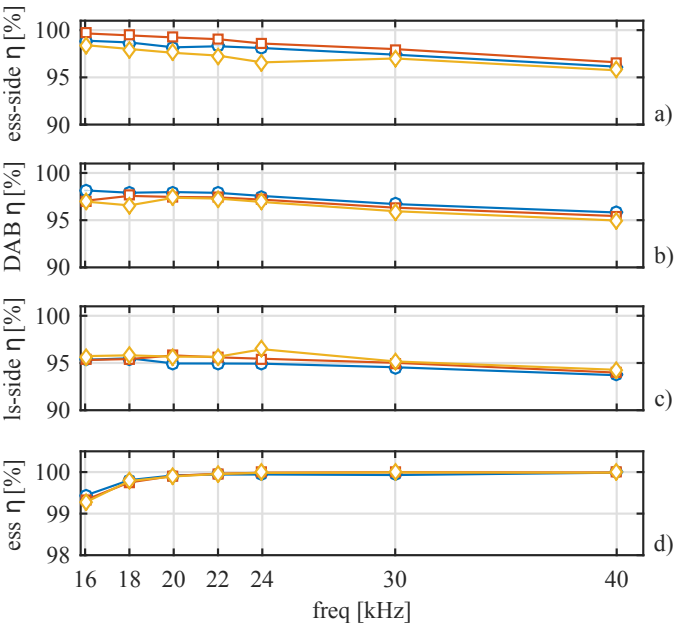

Fig. 25. Experimental results. Power converter efficiency in function of the switching frequency for the three different SoCS (blue-50%, red-75%, yellow-90%). From top to bottom efficiencies for the: a) ess-side power converter, b) DAB, c) ls-side power converter, d) battery.

selection of the switching frequency. It is worth remarking the contribution regarding the reduction of the dc-link capacitance at the battery port, even allowing the operation with only the capacitance imposed by the snubber. This reduced capacitance barely affects the overall system efficiency.

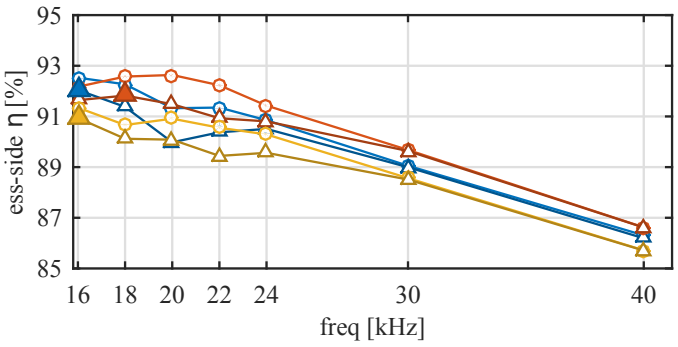

Fig. 26. Experimental results. Compared overall system efficiency for the $\frac{P^{ls}_{dc}}{P^{ess}_{dc}}$ without (○) and with (△) the battery for the three different SoCS (blue-50%, red-75%, yellow-90%) in function of switching frequency. Maximum efficiency marks are colored in the same color than the respective SoC. As it can be seen the maximum efficiency depends on the battery SoC. Parallel capacitance $C = 1.6\mu$F.

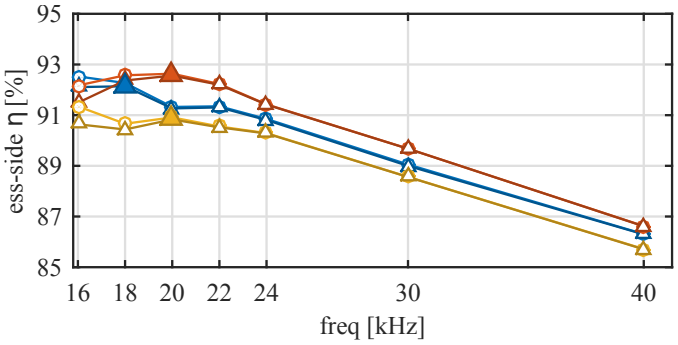

Fig. 27. Experimental results. Compared overall system efficiency for the $\frac{P^{ls}_{dc}}{P^{ess}_{dc}}$ without (○) and with (△) the battery for the three different SoCS (blue-50%, red-75%, yellow-90%) in function of switching frequency. Maximum efficiency marks are colored in the same color than the respective SoC. As it can be seen the maximum efficiency depends on the battery SoC. Parallel capacitance $C = 3.2\mu$F.

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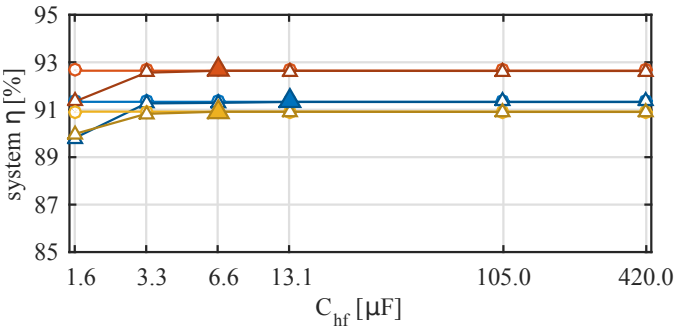

Fig. 28. Experimental results. Compared overall system efficiency for the $\frac{P_{dc}^{ls}}{P_{dc}^{ess}}$ without (○) and with (△) the battery for the three different SoCS (blue-50%, red-75%, yellow-90%) in function of stack parallel capacitance. Maximum efficiency marks are colored in the same color than the respective SoC. As it can be seen the maximum efficiency depends on the battery SoC.

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