Series-Connected GaN Transistors for Ultra-Fast High-Voltage Switch (>1kV)

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***Abstract*— The feasibility of a 1.2kV GaN switch based on two series-connected 650V GaN transistors is demonstrated in this paper. Aside to achieve ultra-fast transitions and reduced switching energy loss, stacking GaN transistors enables compatibility with high-voltage GaN-on-Silicon technologies. A proof-of-concept is provided by electrical characterization and hard-switching operation of a GaN Super-Cascode built with discrete components. Further investigations to enhance stability with auxiliary components are carried out by simulations and co-integrated prototypes are proven at wafer level.**

I. INTRODUCTION

Among the different voltage domains of the power electronics market, the one covering 1.2 to 1.7 kV is expected to grow the fastest until year 2020 [1]. In this segment, currently dominated by Silicon IGBTs, SiC emerges as a performant replacement in several applications. In the meanwhile, GaN has been mainly relegated to the 600V range, thus being expected to compete in a near future with Silicon power MOSFETs. In part, the better thermal performance of SiC makes it more suitable at higher voltage, which normally implies higher power. However, the lack of investigation on GaN-on-Silicon substrates with high-voltage capability is also influencing. GaN substrates based on bulk GaN [2] and GaN-on-Sapphire [3] are capable of reaching very high voltages but do not project competitive wafer price with respect to Silicon; only GaN-on-Silicon does it. On the other hand, GaN-on-Silicon with high-voltage capability requires dedicated substrates with an epitaxial layer stack thicker than 5µm on top of the Si substrate [4]–[6] (see Fig. 1). Increasing the thickness of GaN and buffer layers (t_{GaN} and t_{buffer}) is not straightforward in production. Besides the elevated wafer cost, it could induce numerous issues related to bow control and wafer breakage. Moreover, the device thermal resistance is also increased, thus complicating the device survival under short-circuit test [7]. This work proposes a new solution to extend GaN-on-Silicon technologies beyond 1 kV by connecting in series several depletion-mode GaN transistors (DHEMTs). More concretely, an experimental proof-of-concept and simulation analysis is presented by means of a

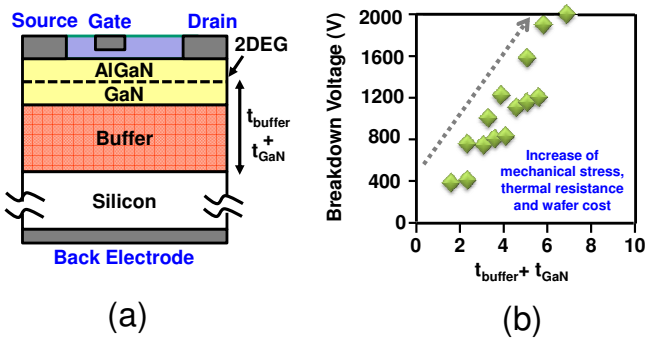

Fig. 1. (a) Schematic cross section of a generic DHEMT in GaN-on-Silicon substrates. (b) Breakdown voltage vs. t_{buffer}+t_{GaN} based on [4]–[6].

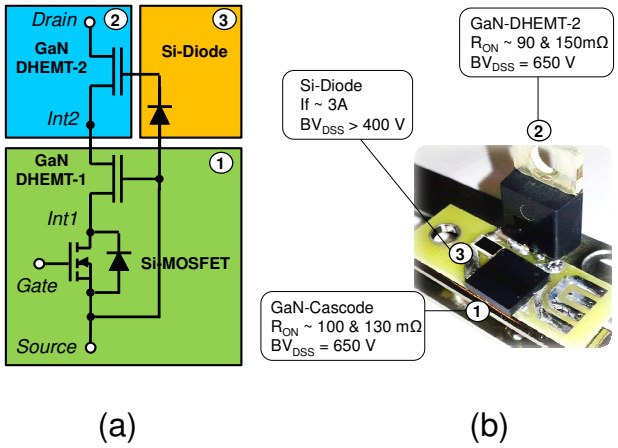

Fig. 2. (a) Schematic description of a 1.2kV GaN-SC. (b) 1.2kV GaN-SC built with 3 packaged parts mounted on a PCB board (Si-Diode in the backside) and corresponding electrical characteristics.

GaN Super-Cascode (GaN-SC in Fig. 2a). Differently from previous works addressing SC with SiC-JFETs [8]–[10], designing a GaN-SC presents new challenges and opportunities that can be summarized in three points:

- new leakage current paths should be considered to achieve a stable voltage distribution in steady-state.
- low GaN capacitances result in critical selection of auxiliary components (Si-Diode, capacitances, etc.).
- novel co-packaged and co-integrated designs are enabled by GaN-DHEMT lateral architecture.

Although reliability aspects are out of the scope of this work, current-collapse-free GaN-DHEMTs are expected to constitute an equally reliable GaN-SC.

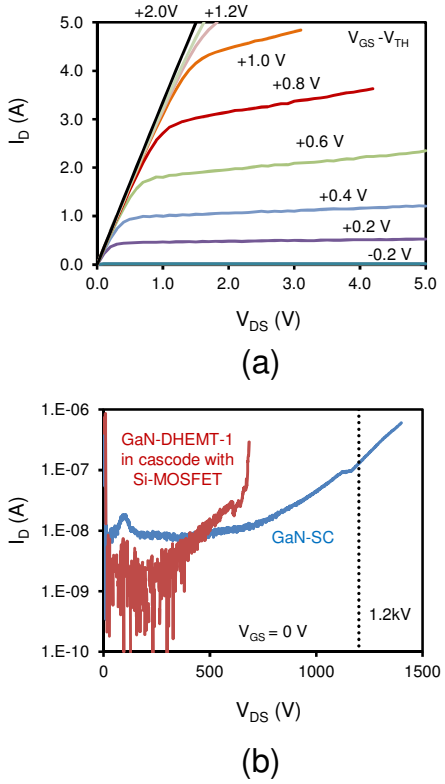

Fig. 3. Measured (a) I_D vs. V_{DS} and (b) reverse blocking curves for a GaN-SC (R_{DSON} = 280 mΩ). Leakage currents below 1 µA are obtained for reverse blocking voltage exceeding 1.2 kV.

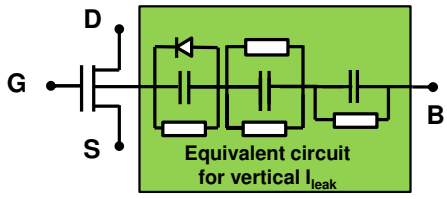

Fig. 4. Equivalent circuit proposed for GaN-DHEMTs in [14] to model vertical I_{leak} flowing from back electrode to 2DEG (2D-Electron-Gas).

II. Experimental Demonstration

Different GaN-SC prototypes are built with three discrete components mounted on a PCB board (see Fig. 1b). All the GaN-DHEMTs described in the following are proprietary components [11], [12] rated for 650 V with a non-avalanche failure at a V_{DS} ranging from 700 to 950 V. Component (1) is a GaN-DHEMT-1 in cascode with a low-voltage Si-MOSFET (30 V); both of them assembled together in an SMD 8x8 mm^2 package. This special assembly offers accessibility to the floating node between Si-MOSFET and GaN-DHEMT-1 (Int1). The on-state resistance (R_{DSON}) for GaN-DHEMT-1 ranges from 100 to 130 mΩ. Component (2) is a single GaN-DHEMT (i.e. GaN-DHEMT-2) connected in series to GaN-DHEMT-1 through another floating node (Int2). Two different GaN-DHEMT-2 were used along experimental tests: a 90 mΩ with TO-220 package or a 150 mΩ with SMD 8x8 mm2 package. Finally, component (3) is a balancing high-voltage Si-Diode connecting the gates of both GaN-DHEMTs. Similarly as in SC with SiC-JFETs [8]–[10], the role of this diode is to ensure that both GaN-DHEMTs withstand voltage during a stationary V_{DS} ramp. Although the PCB board is prepared to include other auxiliary passive components (resistors, capacitances), this option is not exercised in a first instance.

A. *Steady-State Analysis*

A B1505A analyzer has been used to perform steady-state electrical characterization in GaN-SC. As a matter of example, Fig. 3 shows experimental I_D vs. V_{DS} and reverse blocking curves for a specific built with an R_{DSON} = 280 mΩ. It is inferred from Fig. 3b that leakage current (I_{leak}) remains below 1 µA for reverse blocking voltages exceeding 1.2 kV. Oppositely, components (1) and (2) always show a fast I_{leak} increase for V_{DS} < 950 V when being measured individually. It is worth to remark that I_{leak} previously reported for 1.2kV GaN-on-Silicon transistors was 2 orders of magnitude larger than this work [13].

Interestingly, GaN-SC does not exhibit the stepped I_{leak} vs. V_{DS} observed in SiC-JFET stacks [8]. In fact, I_{leak} steps are due to the sequential withstand of the reverse blocking voltage in the stack of switches. The additional I_{leak} level in every single step is added by the gate inherent diode of the SiC-JFET that is turned-off. Instead, the gate of our GaN-DHEMTs is MIS-type and, as a result, gate leakage current is restricted to less than 10 nA. Nonetheless, a new I_{leak} path is introduced in GaN-DHEMTs by means of vertical conduction through GaN layer, buffer layer and Si substrate. This effect, predominant at high V_{DS}, has been largely studied and modeled with equivalent circuits like the one in Fig. 4 [14]. According to this model, I_{leak} rises with V_{DS} in a more gradual way than the avalanche mechanism. In component (2) of our GaN-SC, substrate electrode B is connected to S but, in general, it represents a new degree of freedom for a SC design. As it has been thoroughly described in [15], the relative I_{leak} level defines the steady-state voltage drop distribution in series-connected transistors (with I_{leak} exclusively flowing from drain to-source). In this sense, if I_{leak} is larger in GaN-DHEMT-2, then the GaN-Cascode will initially withstand the voltage. Unfortunately, our equipment is unable to sense V_{Int1} and V_{Int2} during the V_{DS} ramp. Another GaN-SC with an R_{DSON} = 190 mΩ has been measured and compared to electrical parameters of commercial 1.2kV SiC transistors in Table I. It is noticeable that, for a similar R_{DSON} range, all the electrical parameters related to gate charge (Q_{GD}, Q_{GS}, Q_G and R_G) are significantly lower in the GaN-SC.

TABLE I. COMPARISON OF ELECTRICAL PARAMETERS BETWEEN 1.2KV GAN SUPERCASCODE AND COMMERCIAL 1.2KV SIC TRANSISTORS

Device	R_{DSON} (mΩ)	Voltage Rating (V)	Q_{GD} (nC)	Q_{GS} (nC)	Q_G (nC)	R_G (mΩ)
GaN-SC	190	1200	3	4	18	1.0
SiC 1 [16]	160	1200	20	14	62	13.7
SiC 2 [17]	160	1200	14	7	34	6.5
SiC 3 [18]	169	1200	11.7	7	45	7.0

SiC data is extracted from product datasheets (V_{GS} range is normally higher for SiC transistors).

TABLE II. OPERATING CONDITIONS AND COMPONENTS OF THE BOOST CONVERTER TO TEST 1.2KV TRANSISTORS

Gate Driver	EL7104CSZ
Output Capacitor	B32774D1305K000
Freewheeling Diode	C4D02120A
Balancing Si-Diodes	BYV27-200 & 1N5625
Balancing Capacitor	C1808V683KDRACTU (68 pF)
Gate Resistance	7 Ω
Output Power	335 W
Output Voltage	800 V
Switching Frequency	100 kHz

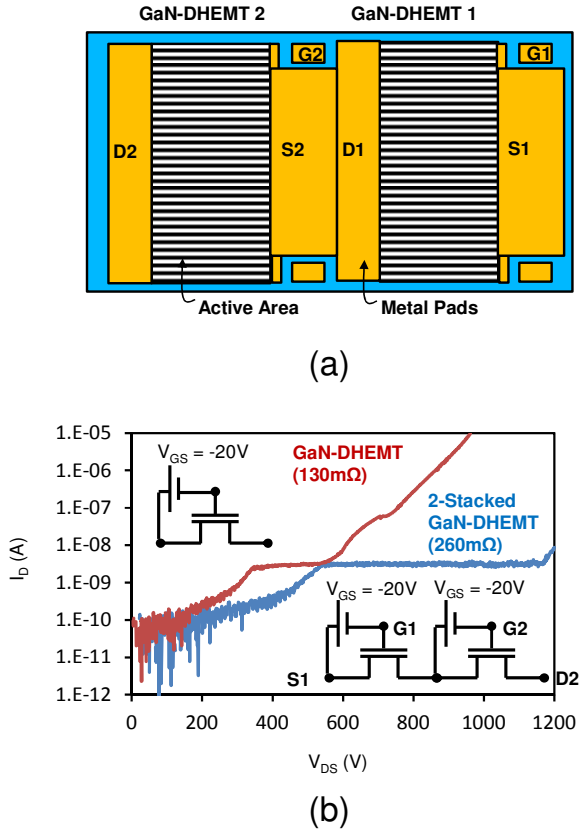

Fig. 5. (a) Layout scheme for 2 series-connected GaN-DHEMTs in the same die. (b) Measured I_D vs. V_{DS} in reverse blocking for single and co-integrated series-connected GaN-DHEMTs (at wafer level).

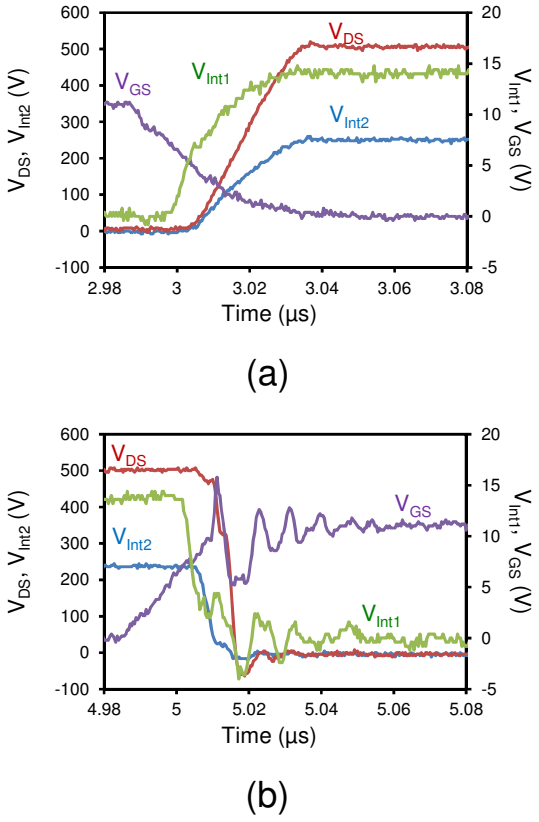

Fig. 6. Measured waveforms at (a) turn-off and (b) turn-on for GaN-SC incorporating a Si-Diode with optimum C_{AK}. V_{DS} = 500 V, I_D = 1.5 A.

Thanks to their lateral architecture, two GaN-DHEMTs can be monolithically stacked in the same die by connecting the back electrode to their common floating node. The layout design depicted in Fig. 5a has been implemented and tested at wafer level by using the same B1505A analyzer. In this specific design, the backend metal provides series-connection between GaN-DHEMT-1 and 2. Reverse blocking curves in Fig. 5b prove that voltage capability is twice compared to a single GaN-DHEMT (I_{leak} < 10nA). For this experiment, G1 is biased to -20V from the analyzer whereas an external voltage source applies -20V between Int2 and G2. Although not addressed in this work, the co-packaging of GaN-SC components in SMD, IPMs and PIMs is very attractive and deserves consideration in forthcoming investigations.

B. Transient Analysis

GaN-SC prototypes built with discrete parts have been tested in a boost converter operating under continuous conduction mode. A dedicated evaluation board with a socket to insert adaptive boards has been used. This methodology was already proposed in [19] for testing and benchmarking of SMD-packaged power transistors. Test operating conditions and boost converter components are summarized in Table II. Initial tests were done at reduced output voltage (V_{OUT}) of 350 and 500 V for the sake of precaution. Turn-on and -off waveforms are plotted in Figs. 6 and 7 for two different balancing Si-Diodes; i.e., one with an optimum C_{AK} (1N5625) and another one with a too large C_{AK} (BYV27-200).

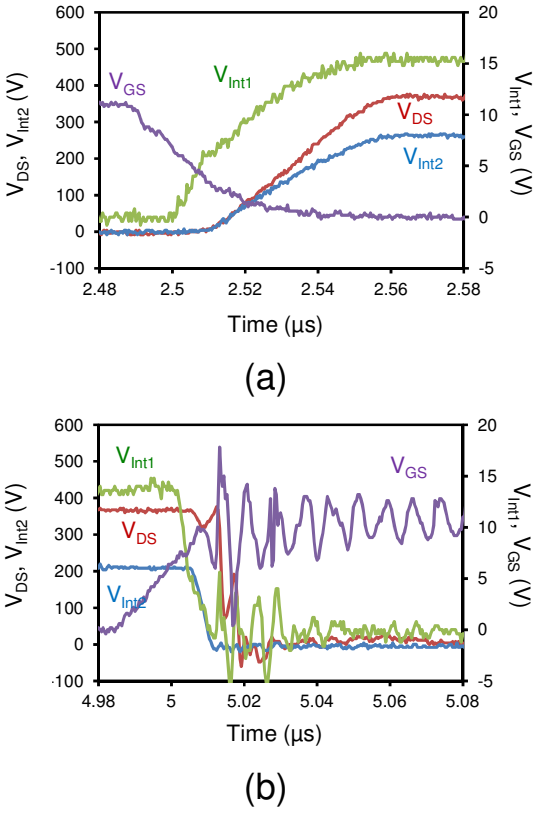

Fig. 7. Measured waveforms at (a) turn-off and (b) turn-on for GaN-SC incorporating a Si-Diode with large C_{AK}. V_{DS} = 350 V, I_D = 1.0 A.

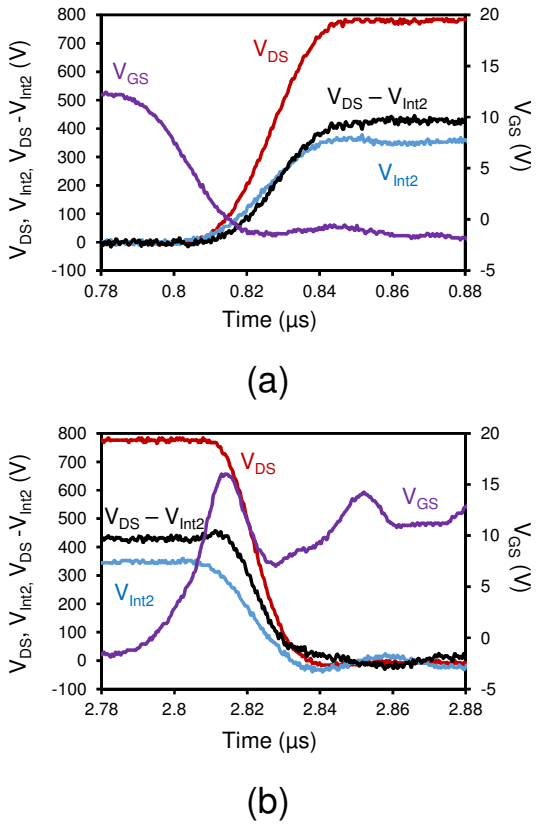

Fig. 8. Measured waveforms at (a) turn-off and (b) turn-on for GaN-SC incorporating a Si diode with optimum C_{AK} and GaN-DHEMTs with dissimilar size. V_{DS} = 800 V, I_D = 3.0 A.

In all prototypes and measured conditions V_{INT1} < 30V, thus meaning that the Si-MOSFET never enters into avalanche and remains in a safe operation regime. In contrast, V_{INT2} is strongly dependent on C_{AK} and needs careful GaN-SC design to ensure proper functionality. When C_{AK} is too large, a very prominent ringing is observed at turn-on and V_{DS} distribution is unequal across GaN-DHEMTs during the reverse blocking time (see Fig. 7). With an optimum C_{AK}, the ringing disappears and V_{DS} is fairly balanced as it can be observed from Fig. 6. However, a transitory V_{DS} imbalance is still present during a few ns of the turn-on. During this time, the voltage fall is not synchronized in the two GaN-DHEMTs and, consequently, GaN-DHEMT-2 withstands the totality of V_{DS} (V_{DS} - V_{INT2} peak). This effect is not critical when operating at low V_{OUT}, but it could originate issues when moving to V_{OUT} = 800 V. In order to overcome this problem, some GaN-SC prototypes were built combining GaN-DHEMT-1 and 2 with different sizes. After resizing of GaN-DHEMT and adding a balancing capacitor of 68 pF in parallel to Si-Diode an equilibrated distribution of voltages between GaN-DHEMTs is achieved. A good GaN-SC balance is exhibited in Fig. 8 where, for a V_{OUT} = 800 V, V_{DS} - V_{INT2} remains close to 430 V during the reverse blocking time and rises less than 20 V during the turn-on. Transients are smooth with V_{DS} falling and rising times of 20 ns and 30 ns, respectively, for 330 W output power. The optimization of C_{AK} and GaN-DHEMT sizes has been upfront supported by means of the simulation analysis in the following section.

III. Simulation Analysis

An extensive simulation analysis has been carried out to support the optimization of GaN-SC during ultra-fast switching. Mixed-mode simulations combining TCAD (Technology Computer-Aided Design) with SPICE are performed with commercial software [20]. In a preliminary stage each component of the tested GaN-SC follows a calibration that includes GaN physical models. These models are combined with package and test circuit parasitic elements to provide a holistic approach of our system.

Following the same procedure of our experimental tests, the initial simulations address low V_{OUT} to eventually attain high V_{OUT} with less risk of device failure. As shown in Fig. 9a and 9b, simulated waveforms match experimental results in Fig. 6a and 6b. The impact of C_{AK} on switching energy losses (E_{SW}) is elucidated by resizing the Si-Diode area. It is inferred from Fig. 10 that E_{SW} is practically independent of C_{AK}, however an optimum C_{AK} is needed for an even E_{SW} distribution. From a thermal perspective, the E_{SW} balance between GaN-DHEMTs is desirable to reduce conduction loss and improve ruggedness. An additional capacitance parallel to GaN-DHEMT-2 (C_{GaN2}) is also investigated with regard to its influence on transient overshoots. The benefits of C_{GaN2} in reducing the turn-on V_{DS}-V_{Int2} peak are displayed in Fig. 11. In our real prototypes the variation of C_{GaN1} and C_{GaN2} has

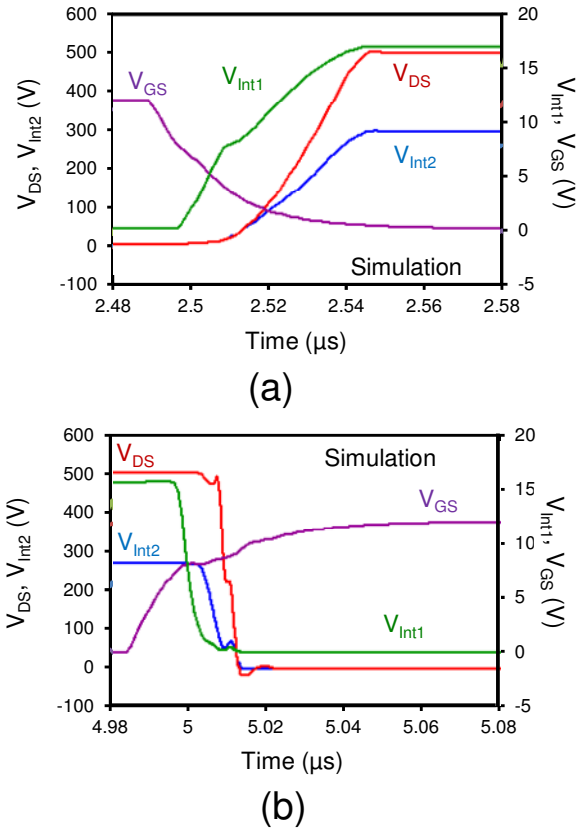

Fig. 9. (a)-(b) Simulated waveforms at turn-on and turn-off for GaN-SC with an optimum size Si-Diode. V_{DS} = 500 V, I_D = 1.5 A.

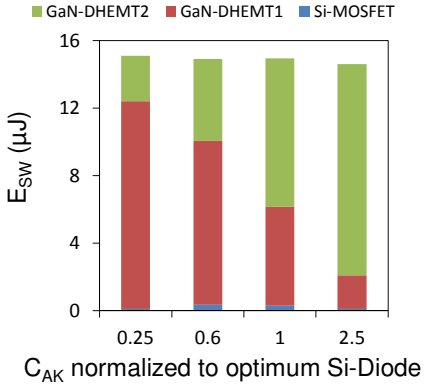

Fig. 10. E_{SW} vs. C_{AK} in GaN-SC. Contributions from GaN-DHEMT-1 (red), GaN-DHEMT-2 (green) and Si-MOSFET (blue) are indicated.

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been implemented by resizing GaN-DHEMTs. Finally, E_{SW} extracted from GaN-SC simulations is compared in Fig. 12 to measured data reported for 1.2kV GaN and SiC transistors [13]. After adapting our GaN-SC model and balance components to 100 mΩ, a projected improvement of 30% E_{SW} reduction is predicted for V_{DS} = 600 V and I_D = 5 A.

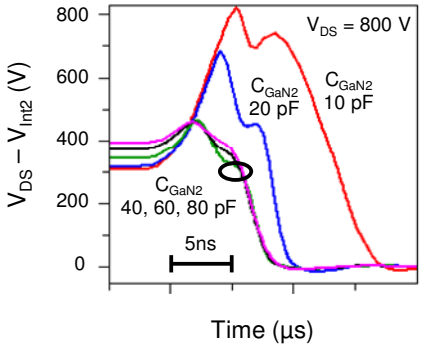

Fig. 11. Simulated V_{DS}-V_{Int2} during turn-on for different C_{GaN2} (10, 20, 40, 60, 80 pF). V_{DS} = 800 V, I_D = 1.5 A.

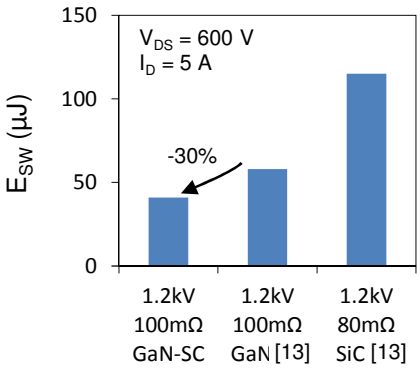

Fig. 12. E_{SW} comparison between simulated 1.2kV GaN-SC and measured 1.2kV GaN and SiC transistors in [13]. V_{DS} = 600 V, I_D = 5.0 A.

IV. Conclusions

The demonstration and optimization of a 1.2kV-rated GaN SuperCascode (GaN-SC) is reported for the first time in this work by means of electrical characterization and application test. After proper optimization, supported by numerical simulation tools, GaN-SC exhibits excellent switching speed and stability, thus being a promising switch to address high-voltage/high-frequency power converters. Despite GaN-SC is firstly demonstrated with discrete components, a co-integrated prototype is also proposed as a more compact solution.

Acknowledgment

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References

[1] P. Gueguen, "Data Center Market and Technology Trends in Power Electronics", keynote presentation at IEEE Applied Power Electronics Conference and Exposition (APEC), 2016.

[2] H. Nie, Q. Diduck, B. Alvarez, A. P. Edwards, B. M. Kayes, M. Zhang, G. Ye, T. Prunty, D. Bour, and I. C. Kizilyalli, "1.5-kV and 2.2-m-cm2 vertical GaN transistors on bulk-GaN substrates," IEEE Electron Device Letters, 35(9), pp. 939-941, 2014.

[3] N. Tipirneni, A. Koudymov, V. Adivarahan, J. Yang, G. Simin, and M. A. Khan, "The 1.6-kV AlGaN/GaN HFETs," IEEE Electron Device Letters, 27(9), pp. 716-718, 2006.

[4] N. Ikeda, S. Kaya, J.Li, Y. Sato, S. Kato, and S. Yoshida, "High power AlGaN/GaN HFET with a high breakdown voltage of over 1.8 kV on 4 inch Si substrates and the suppression of current collapse," in ISPSD, pp. 287-290, 2008.

[5] I. B. Rowena, S. L. Selvaraj, and T. Egawa, "Buffer thickness contribution to suppress vertical leakage current with high breakdown field (2.3 MV/cm) for GaN on Si," IEEE Electron Device Letters, 32(11), pp. 1534-1536, 2011.

[6] S. Iwakami, O. Machida, M. Yanagihara, T. Ehara, N. Kaneko, H. Goto, and A. Iwabuchi, "20 mΩ, 750 V high-power AlGaN/GaN heterostructure field-effect transistors on Si substrate," Japanese Journal of Applied Physics, 46(6L), pp. L587–L589, 2007.

[7] T. Nagahisa, H. Ichijoh, T. Suzuki, A. Yudin, A. O.Adan, and M. Kubo, "Robust 600 V GaN high electron mobility transistor technology on GaN-on-Si with 400 V, 5 µs load-short-circuit withstand capability," Japanese Journal of Applied Physics, 55(4S), 04EG01, 2016

[8] P. Friedrichs, H. Mitlehner, R. Schorner, K. O. Dohnke, R.Elpelt, and D. Stephani, "Stacked high voltage switch based on SiC VJFETs," in 2003 IEEE 15th International Symposium on Power Semiconductor Devices & IC's (ISPSD), pp. 139-142, 2003.

[9] J. Biela, D. Aggeler, D. Bortis, and J.W. Kolar, "5 kV/200 ns pulsed power switch based on SiC-JFET super cascode," in Proc. IEEE Int. Power Modulator Conf., pp. 358–361, 2008.

[10] J. Bendel and X. Li, "Using "Normally on" JFETs in Power Systems in Power Systems," Bodo's Power, pp. 40-43, March 2015

[11] P. Moens, C. Liu, A. Banerjee, P. Vanmeerbeek, P. Coppens, H. Ziad, A. Constant, Z. Li, H. De Vleeschouwer, J. Roig-Guitart, P. Gassot, F. Bauwens, E. De Backer, B. Padmanabhan, A. Salih, J. Parsey, and M. Tack, "An industrial process for 650V rated GaN-on-Si power devices using in-situ SiN as a gate dielectric," in 2014 IEEE 26th International Symposium on Power Semiconductor Devices & IC's (ISPSD), pp. 374–377, 2014.

[12] P. Moens, A. Banerjee, P.Coppens, F. Declercq, and M. Tack, "AlGaN/GaN power device technology for high current (100+ A) and high voltage (1.2 kV)," in 2016 IEEE 28th International Symposium on Power Semiconductor Devices and ICs (ISPSD), pp. 455-458), 2016.

[13] D. C. Sheridan, D. Y. Lee, A. Ritenour, V. Bondarenko, J. Yang, and C. Coleman, "Ultra-low loss 600V-1200V GaN power transistors for high efficiency applications," in International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management (PCIM Europe), pp. 1-7, 2014.

[14] M. J. Uren, M. Cäsar, M. A. Gajda, and M. Kuball, "Buffer transport mechanisms in intentionally carbon doped GaN heterojunction field effect transistors," Applied Physics Letters, 104(26), 263505, 2014.

[15] J. Roig, F. Bauwens, A. Banerjee, W. Jeon, A. Young, J. McDonald, B. B. Padmanabhan, and C. Liu, "Unified theory of reverse blocking dynamics in high-voltage cascode devices," in 2015 IEEE Applied Power Electronics Conference and Exposition (APEC), pp. 1256-1261, 2015.

[16] www.st.com; datasheet SCT20N120

[17] www.rohm.com; datasheet SCT21160KE

[18] www.cree.com/power; datasheet C2M0160120D

[19] J. Roig, M. Fernandez, G. Gomez, F. Declercq, D. G. Lamar, and F. Bauwens, "An Insightful Evaluation of a 650V High-Voltage GaN Technology in Cascode and Stand-Alone Transistors," in International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management (PCIM Europe), 2016.

[20] Sentaurus TCAD Tools Suite. Synopsys 2013.