

Improved Efficiency of Local EPS through Variable Switching Frequency Control of Distributed Resources

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Abstract—This contribution explores the possibility of improving the global efficiency of three-phase inverter-based distributed resources (DR) embedded in low-voltage (LV) distribution feeders, by the adaptation of their switching frequency (SF) to the operation point of both the converter and local loads. The core of this proposal lies on the fact that in a good number of applications, in both services and residential sectors, the owner of the DR is also in charge of the losses caused in the local electric power system (EPS). This fact leaves room for a global optimization of the power losses, i.e., converter losses will be considered together with those losses caused by the current harmonics injected into the local grid. A dynamic adaptive SF frame of the DR is considered in this proposal to allow its operation beyond its rated frequency at light loads, subjected to the thermal constraints of the device. Simulation results obtained using PLECS software as well as an experimental validation of the method are included.

I. INTRODUCTION

The soaring use of inverters in distributed generation and energy storage applications has increased the attention paid to the efficiency of these devices in recent years. The efficiency of power converters interconnected to the EPS is influenced by regulations such as [1], which states limits for the harmonic current injection of these devices at the PCC. In common applications, such as solar and wind, power converters operate rarely at rated values, being the efficiency at light loads a source of great concern [2]. According to [3], the tests to comply with [1] takes only into account the first 40 harmonics. This allows using relatively low switching frequencies (SF), typically higher than 3 kHz, as the high-frequency harmonics induced by PWM will be in this case over the stated limit.

The efficiency of the inverter as a separate unit is the only concern of the owner when he is not responsible for the losses upstream. In this case, once verified that the selected switching frequency complies with the harmonic emission limits, it can be maintained constant at any operating condition. In most cases, increasing the SF reduces the efficiency of the device due to the rise of the converter switching losses, while decreasing this parameter could make the device not conform with [3]. Notice that the tests must be conducted not just at 100% but also at 66% and 33% of the output rated current.

In a good number of common applications, e.g. PV and small wind turbines used in residential buildings and connected to the LV grid, the owners of the DR are also responsible for the local losses caused by the inverter current

harmonics both in the line and local loads, up to the metering location at the distribution transformer (either on the LV or MV side). In assessing the efficiency of the DR in this scenario, the inverter losses should be taken into account together with the distortion losses caused in the local grid. Furthermore, the high impedance of the transformer at high frequencies allow us to neglect those losses up from this point. Even if by design, a thermal constraint in the increment of the SF at rated power is likely to exist, the possibility of operating the device at higher frequencies when working at light loads is still there. Increasing the SF rises the converter switching losses but reduces the distortion losses in the local grid at the same time. This fact, together with the great advances carried out in recent years in the field of grid impedance estimation techniques [4]–[9], opens the door for a dynamic optimization of the SF capable of achieving an improved overall efficiency.

In Section II a study of the effect of the SF on the harmonic emission in three-phase VSCs is carried out. Three-phase two-level inverters with first-order inductive filters are considered, as one of the preferred technologies in LV applications. The evaluation of inverter losses, considering thermal constraints, is presented in Section III. Section IV deals with the estimation of the distortion losses caused by the inverter in the local grid. The proposed method for the on-line optimization of the SF is described in Section V. Section VI presents a case study to demonstrate the validity of the proposal and experimental results are given in Section VII. Finally, the conclusions of the study are drawn in Section VIII.

II. SWITCHING FREQUENCY AND CURRENT HARMONICS

As a general rule, a higher SF leads to a displacement of the harmonic spectrum of the voltage at the converter's terminals to a higher frequency range. Consequently, the inductive behavior of the filter and grid upstream yields to a reduction in the induced current harmonics due to the higher impedance of these inductances at the new frequencies. However, it is important to note that the IGBTs' dead-time limits the validity of the said statement, leading to the emergence of low-frequency harmonics (mainly 5th and 7th order) [10], [11] with a growing impact at higher SFs. Nevertheless, this effect can be mitigated by current regulators, whose bandwidth use to fall within these values. Fig. 1 shows the current distortion of an inverter given by the parameters shown in Table I as a

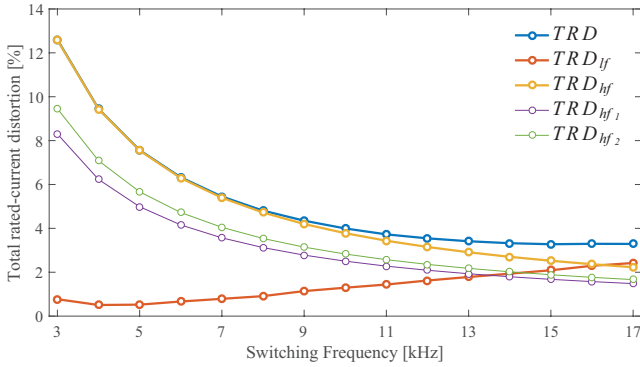


Fig. 1. Current TRD as a function of the SF for different frequency bands. Effect of the dead-time in low-frequency harmonics

function of the SF. This distortion has been reported as the total rated-current distortion (TRD) according to [1], which can be defined as the total root-sum-square of the current harmonics created by the DR unit divided by the rated current capacity of that unit, I_n . In Fig. 1, TRD has been split in two terms, TRD_{lf} and TRD_{hf} using the 40th harmonic included in [3] as a limit between low and high frequencies. Thus, those parameters can be related as

$$TRD = \sqrt{TRD_{lf}^2 + TRD_{hf}^2}, \quad (1)$$

which allows to show the different behavior of the theoretical PWM harmonics and the non-idealities induced by the dead-time. As it is shown in Fig. 1, the effect of the dead-time reaches such an importance in TRD that increasing the SF over a certain limit becomes counterproductive. The use of dead-time compensation techniques [12], [13] could potentially raise this limit. It is also interesting to point out that the results shown in Fig. 1 are independent of the load of the converter, as only the fundamental component varies on a significant scale with this parameter. On the contrary, the values shown in this graph can be affected to some extent by the system impedance at the converter terminals, especially in weak systems. This suggests that an online measurement of harmonic distortion will provide better results than a theoretical estimation. Nonetheless, the simplicity of this estimation can be valuable in most cases.

III. CONVERTER LOSSES AND THERMAL LIMITS

Converter losses, P_{VSC} , are mainly determined by switching losses, P_{sw} , and conduction losses, P_{cd} [14], [15]. Other issues should be considered when assessing the efficiency of these devices, such as cooling power; however, as they are not normally affected by the SF, they will not be considered in this work. Switching losses are strongly influenced by the SF, f_{sw} , as well as the load of the converter, c . Even if the power factor of the converter also affects this parameter due to variations in the commutation phenomenon, this effect is hardly noticeable and can be neglected with little error for the aim of this study. As increasing the SF results in a proportional rise of switching events, the relationship between SF and

TABLE I
CONVERTER PARAMETERS

Hardware	
Grid voltage	$V_{rms} = 400$ V, $f = 50$ Hz
Rated power/current	$S = 30$ kVA, $I_n = 43.3$ A
System impedance	Ideal grid
Coupling inductor	$L_{filter} = 1.0$ mH, $R_{filter} = 0.16$ m Ω
DC link	$v_{dc} = 800$ V, $C = 350$ μ F
IGBT modules	2MBI200HH-120-50
Dead-time	$t_d = 1$ μ s
Control	
PWM Type	Sym. regular sampled w/ 3 rd harm. injection
SF at rated power	$f_{sw} = 3$ kHz
PLL	Dual SOGI
Anti-aliasing filter	Butterworth 2 nd order, $f_c = f_{sw}/2$
Current reg. bandwidth	300 Hz
Power factor	1

switching losses is almost lineal. Conduction losses, for its part, are mainly affected by the load of the converter, and in a more subtle way, by the SF due to the increased current distortion that arises at lower frequencies. Taking these facts into consideration, an approach to the converter losses, taking c and f_{sw} as parameters, can be faced up by using

$$P_{VSC}(c, f_{sw}) = P_{sw}(c, f_{sw}) + P_{cd}(c, f_{sw}). \quad (2)$$

The assessment of the aforementioned power losses for the specific IGBT power modules mounted in the converter used for the experimental validation included in Section VII, is shown in Fig. 2. To obtain the said graph, a PLECS model of the converter was implemented. This model includes the thermal performance of the IGBT power modules, which allows to depict the operational constraints of the converter in terms of SF. Thus, the imperative derating of the device is shown in Fig. 3. This figure was calculated for each SF by assessing the load level of the converter at which the junction temperature of the solid state devices equals the temperature reached at rated values. The inclusion of these data in a two-dimensional look-up table together with the use of interpolation, is enough to obtain a good estimation of converter losses as a function of c and f_{sw} in the optimization scheme proposed in this work. The exploitation of this table for control purposes by operating the converter at variable SF is analyzed in Section V. In any case, it is clear from Fig. 3 that if the SF command f_{sw}^* lies on the forbidden area of the graph, it has to be reduced to the nearest feasible value, f_{sw}^{**} .

IV. DISTORTION LOSSES IN THE LOCAL GRID

Even if limited by regulations, the injection of current harmonics into the distribution grid can cause significant power losses that are classified in two categories: (1) copper losses in the distribution line and distribution transformer and, (2) power losses in local loads. Notice that additional losses could exist upstream from the distribution transformer which are not on the Local EPS owner's responsibility. However, this term can be neglected not only because of the low value of the resistive contribution from the MV level when compared with the LV side, but also because of the low capability of high-order

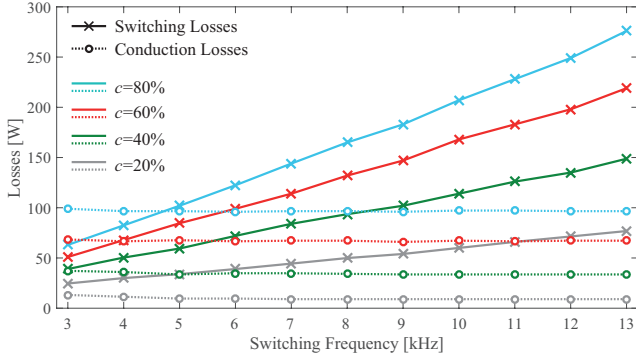


Fig. 2. Converter switching and conduction losses as a function of the SF

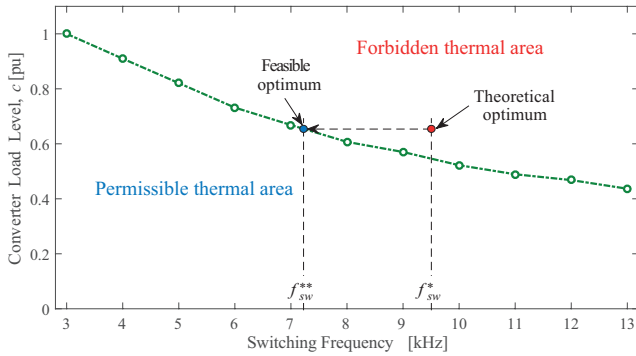


Fig. 3. Thermal constraints for variable SF operation

current harmonics to travel deep into the EPS. Fig. 4 shows a layout of the benchmark system considered in this paper. The Local EPS, with embedded DRs, is connected to the Area EPS through a distribution transformer, being the metering devices connected either in the MV or LV side according to the ownership of this piece of equipment. Both the DRs and the local loads are connected to the distribution line. Those local loads located close to the power converters are more prone to suffer from distortion losses. In Fig. 4, a local load is connected directly to DR point of coupling, PC, to highlight this phenomenon. The effect of the distortion power in local loads is different according to the type of device (motor, lighting, heating, etc.) and its nature (linear/non-linear). In any case, distortion power can be, as a general rule, considered undesirable [16]. Different types of penalization criteria could be considered in order to take into account the harmful effects of higher levels of injected current distortion in particular loads, e.g. cost associated to the loss of life. However, in this work only the cost associated with the power transmitted at non-fundamental frequency is taken into account. A pure resistive load is considered in this contribution as the easiest way to underline the benefits of the proposal.

A precise calculation of the power transmitted by the converter at harmonic frequencies can be done by assessing the expression

$$P_{losses} = Re\left\{\sum_{i=2}^N \mathbf{v}_{PCi} \cdot \mathbf{i}_{conv i}^*\right\}, \quad (3)$$

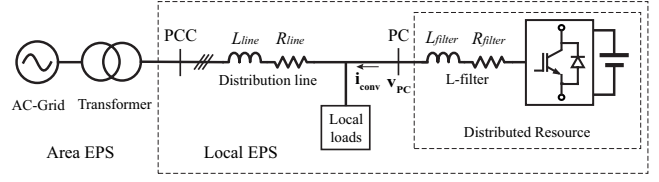


Fig. 4. Area EPS with embedded DRs

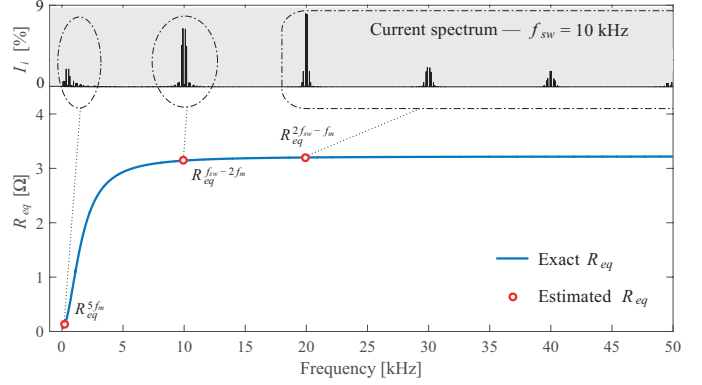


Fig. 5. Estimation of the resistive component of system impedance at the PC as a function of frequency

where $\mathbf{i}_{conv i}$ and $\mathbf{v}_{PC i}$ are the power invariant space vector harmonic components of the converter current and voltage at its point of coupling, obtained by applying the DFT algorithm. For the practical implementation of (3), natural sampling of voltages and currents at SF is not enough due to Nyquist limit, but oversampling can help in complying with these requirements. In any case, other simplified methods such as Goertzel algorithm [17] are better suited for on-line applications [18]. In this light method, just a selected number of harmonics are identified, which can be enough to calculate the resistive component of grid impedance, R_{eq} , at the most significant bands of the spectrum. This reduced set of values can be used together with the expected injection of current harmonics, as given in Fig. 1, to formulate a good estimation of the said power losses. Fig. 5 shows the value of R_{eq} for the installation depicted in Fig. 4, with the parameters shown in Table II. The identification of just 3 impedance values, one at the low-frequency band (5^{th} or 7^{th}) and two at the two lower PWM frequency bands (e.g. $f_{sw} - 2f_m$ and $2f_{sw} - f_m$, f_m being the modulation frequency), can be enough to estimate distortion losses by using

$$P_{losses} \approx 3I_n^2 \cdot (R_{eq}^{5f_m} \cdot TRD_{lf}^2 + R_{eq}^{f_{sw}-2f_m} \cdot TRD_{hf1}^2 + R_{eq}^{2f_{sw}-f_m} \cdot TRD_{hf2}^2). \quad (4)$$

Notice that with this aim, TRD_{hf} has been segregated in two components, TRD_{hf1} , for the harmonic band around the SF and TRD_{hf2} , for the rest of higher frequency values. The specific contribution of these components can be observed in Fig. 1.

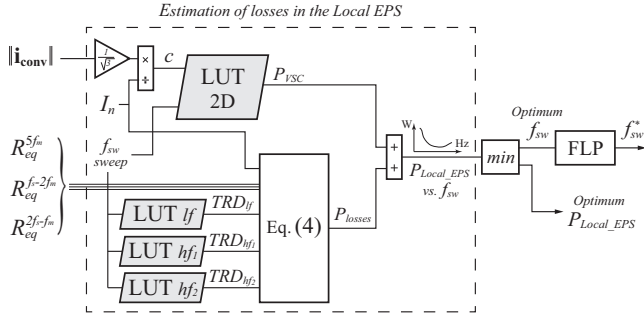


Fig. 6. On-line method for the optimization of the SF

V. ON-LINE OPTIMIZATION OF THE SWITCHING FREQUENCY

The fundamentals of the on-line optimization of the SF proposed in this work are schematically summarized in Fig. 6. The inputs for the algorithm are the space vector of the converter current, which is already available as calculated from current samples for the operation of its inner controller, and the resistive component of grid impedance for the different frequency bands considered in Section IV. The application of a look-up table system together with a SF sweep allows the on-line calculation of the P_{Local_EPS} vs. f_{sw} curve for the present operating point. With this aim, the converter losses, P_{VSC} , are obtained from a 2D-look-up table built by adding the conduction and switching losses of the specific converter according to (2). A set of three 1D-look-up tables, built from the distortion data depicted in Fig. 2, provides the TRD of the converter at the different frequency bands for each SF used in the sweep. From these results, the losses at the line and local loads, P_{losses} , are obtained by using (4). The addition of both converter and line and local loads losses at each SF leads to the desired curve. Then, the minimum of this curve is identified, which gives the optimum losses at the local EPS and, even more important, the optimum SF for the current operating point. Notice that the bandwidth of the SF command, f_{sw}^* , must be much lower than the inner controllers of the inverter not to interfere with its dynamic performance. As a consequence, a low update rate of this command is acceptable and the required computational burden can be assumed by the controller without a significant effort either in a synchronous or asynchronous scheme. In order to avoid the effect of noise in the sampled parameters, as well as steep frequency variations due to sudden changes in the inverter load level or in the grid impedance – due to the connection/disconnection of local loads, a first-order low-pass (FLP) filter is used to smooth the frequency command.

Although not depicted in Fig. 6 for the sake of clarity, the frequency command, f_{sw}^* , should pass a final limitation stage in order to make the control compatible with the thermal constraints shown in Fig. 3. As already stated in Section III, if the pair (f_{sw}^*, c) lies in the forbidden area of this graph, the SF command is reduced to the maximum SF compatible with the present converter load level, f_{sw}^{**} .

TABLE II
INSTALLATION PARAMETERS

Transformer	
Rated power	$S_n = 100$ kVA
Short-circuit impedance & resistance	$Z_{pu} = 0.06, R_{pu} = 0.01$
Distribution Line	
Length	$l = 200$ m
Resistance	$R_{line} = 0.2$ mΩ/m
X/R ratio	0.32
Local Loads	
Power factor	1
Active power	$P = 50$ kW

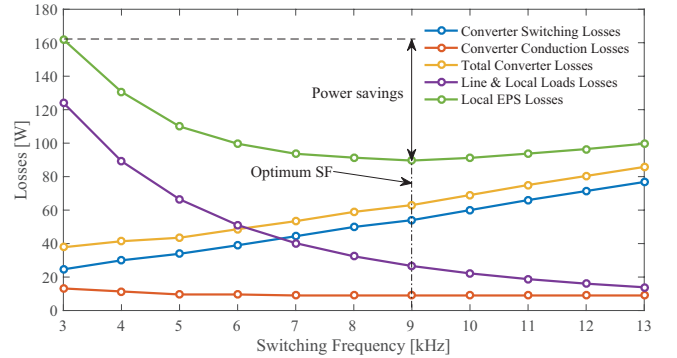


Fig. 7. Local EPS losses as a function of SF – $c = 20\%$

VI. CASE STUDY

In this section a case study is used to illustrate the advantages of using an overall efficiency optimization of the DR within its Local EPS. With this aim, the LV distribution feeder and the distributed generator (DG) depicted in Fig. 4 are considered. The parameters of the grid infrastructure are shown in Table II while those from the inverter-based DG are given in Table I (except for the system impedance, that for this case study is derived from Table II). Fig. 7 shows the total losses in the Local EPS, together with its different components, i.e. converter losses and grid & local loads losses for a DR working at 20% of its rated power with unity power factor. It is concluded from this drawing that increasing the SF from the design parameter, 3 kHz, to 9 kHz, reduces the Local EPS losses in a 44.6%, and improves the overall efficiency at this load level (i.e. the ratio between the Local EPS losses and the power delivered by the converter) in 1.20%.

Fig. 8 expands the analysis to different load levels of the DR. As it is depicted in this figure, connecting the values of the minimum Local EPS losses at each converter load level, c , leads to the optimum trajectory of the inverter SF. Furthermore, the thermal limit of the device is also given in Fig. 8. This limit is established by calculating the maximum acceptable SF at each load level, which is determined by the frequency that leads to the design temperature (i.e. the one obtained at 3 kHz and rated power). From the said graph it can be concluded that for the device under test, a variable SF mode with losses optimization is only feasible for loads lighter than 80% of rated power. Moreover, it is also observed that the

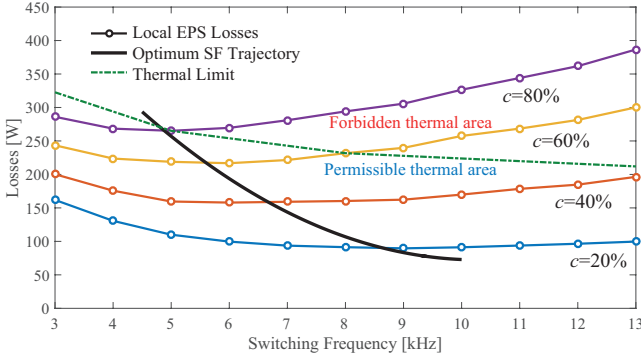


Fig. 8. Optimum trajectory of the SF as a function of converter load

benefit of the proposal is much more relevant at light loads: e.g. the saved power is higher at 20% than at 80% on both relative and absolute terms (72 W vs. 21 W and 1.20% vs. 0.09%).

Fig. 9 shows simulation results of the application of the on-line optimization method proposed in Section V to the present case study. An update rate of 10 ms was used for the SF command and a bandwidth of 0.6 Hz was selected for the FLP filter. The SF sweep included in the algorithm is conducted with a resolution of 100 Hz in order to limit the computational burden. As it is shown in Fig. 9 (a), the converter load level is started at $c = 20\%$ and increased to $c = 80\%$ after 2 s always with unity power factor. Moreover, the local loads stay at rated power according to Table II and are reduced to 50% of this value, i.e. 25 kW, at 4 s. Fig. 9 (b) shows the effect of the steep variation on the resistive component of grid impedance induced by the local load reduction, together with the slight changes caused by the modification of the SF along the process. The optimum SF value obtained by the algorithm along with the final SF command is depicted in Fig. 9 (c). The converter is started with a conservative SF value of 5 kHz and, from this instant, the algorithm competently tracks the optimum SF increasing the efficiency of the installation. In Fig. 9 (d) the optimum and real power savings, compared to a traditional operation of the DR at constant SF, are depicted. As expected, greater power savings are obtained with the converter working at light loads as well as with and increased value of the resistive component of grid impedance.

VII. EXPERIMENTAL RESULTS

Two sets of experimental tests were carried out in this work: the first one is aimed to prove the power saving potential of the stated proposal, and the second, to demonstrate the validity of the on-line SF optimization method described in Section V.

A. Test 1

The test setup used in this case is shown in Fig. 10. A 4-quadrant grid simulator, TC.ACS by Regatron, is used to emulate the electric system, 400 V – 50 Hz, and a 0.32 mH inductor, L_1 , is used to emulate the LV line and transformer according to Fig. 4. An almost purely resistive air-heating

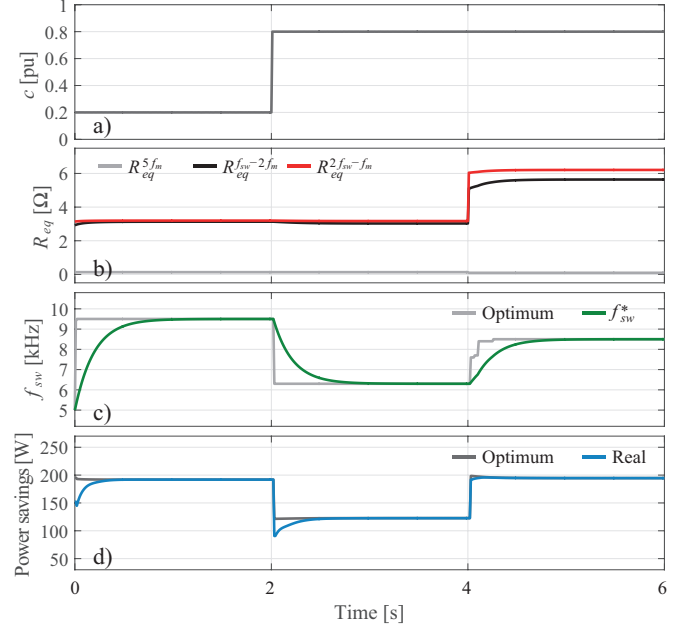


Fig. 9. Application of the optimization method to the proposed case study. (a) converter load profile, (b) grid impedance, (c) SF command, and (d) power savings

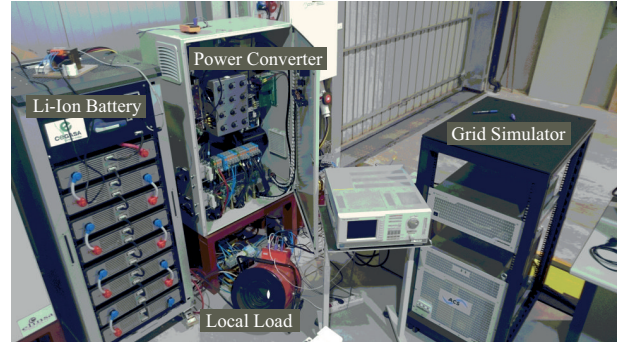


Fig. 10. Test setup.

system with a rated power of 9 kW is used to emulate the local loads according to the said figure. Finally, a custom-made three-phase two-level VSC, with a rated power of 30 kVA and a design SF of 6 kHz, is coupled to the grid through a 0.88 mH inductor, L_2 , to play the role of the DR.

During this test the converter is operated in STATCOM mode at a light load, 10 kVA (i.e. $c = 33\%$), delivering reactive power to the LV grid. Similar results are expected from other operation modes, due to the small influence of the power factor in converter losses, as it was stated in Section II. The three-phase voltages and currents at the coupling point of the DR (PC in Fig. 4) were registered in steady-state for different SFs within the range 6 kHz to 16 kHz. An off-line handling of these measurements were carried out to calculate their DFT, and subsequently, the losses at harmonic frequencies at the line and local loads (i.e. those caused by the air-heating system and stray resistance of L_1) were calculated by the application of

TABLE III
EXPERIMENTAL RESULTS – $c = 33\%$

SF	Losses			Pwr. savings
	Converter	Line&Loads	Local EPS	
6 kHz	781.2 W	253.8 W	1035.0 W	0.0 W
8 kHz	790.5 W	178.4 W	968.9 W	66.1 W
10 kHz	814.0 W	139.8 W	953.8 W	81.1 W
12 kHz	836.3 W	111.2 W	947.6 W	87.5 W
14 kHz	868.1 W	91.6 W	959.7 W	75.3 W
16 kHz	896.9 W	76.9 W	973.8 W	61.2 W

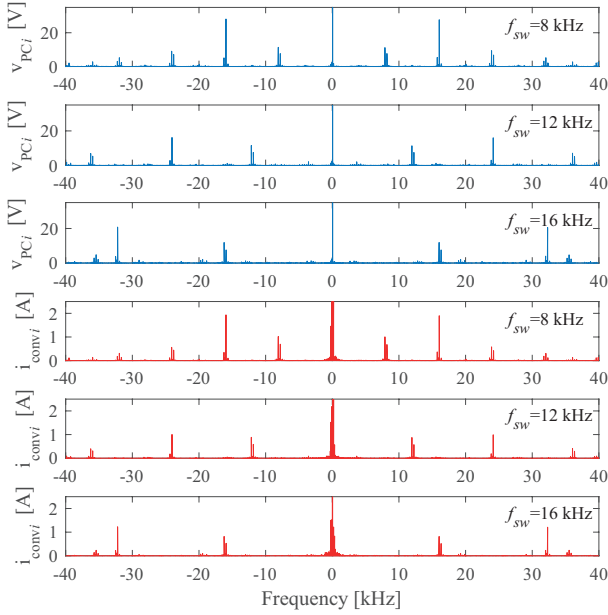


Fig. 11. Voltage and current spectra for different SFs during experimental tests

(3). For the particular case of the STATCOM operation mode, just adding the term at the fundamental frequency in (3) leads directly to the converter losses, so finally, the losses at the Local EPS can be computed in a simple way as

$$P_{Local_EPS} = Re\{\sum_{i=2}^N v_{PCi} \cdot i_{conv i}^*\} - Re\{\sum_{i=1}^N v_{PCi} \cdot i_{conv i}^*\} \\ = -Re\{v_{PC1} \cdot i_{conv 1}^*\}. \quad (5)$$

Notice that this is just a particular result, valid only for STATCOM operation mode. In a general scheme (inverter/rectifier mode), with the DR participating in the active power flow, a look-up table with an estimation of converter losses as a function of the SF and the load of the converter is to be used, as stated in Section III.

The test results are presented in Table III and Fig. 11. As expected, an optimum SF is obtained, capable of achieving the minimization of system losses. As it is highlighted in the said table, the operation at 12 kHz reduces system power losses in 87.5 W when compared with the operation at the design value. This means a reduction of around 8.4% of the losses at this operation point, and an improvement of the Local EPS efficiency of 0.87%.

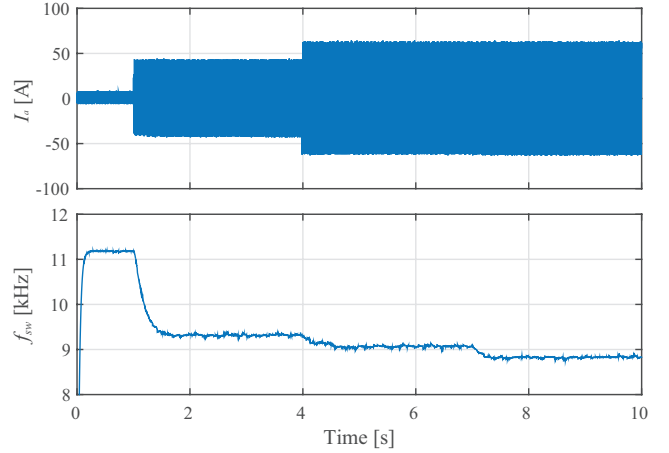


Fig. 12. On-line SF optimization test: (a) converter ac current - phase a , and (b) converter SF

B. Test 2

Slight changes are introduced in the test setup for this case. The 30 kVA converter is now operated in inverter mode to effectively replicate the performance of a DR. With this aim the DC-bus of the converter is fed from the Li-Ion battery shown in Fig. 10 through a DC-DC stage. Furthermore, the converter is now coupled to the utility grid, 400 V – 50 Hz, through a dedicated distribution line and transformer according to the values shown in Table II. Four separate air-heating systems, each with a rated power of 9 kW, are used to emulate the local loads. The connection/disconnection of these systems allows to test the effect of a sudden change in system impedance.

The custom-made converter is operated through a controller using a TI C2000 Delfino™ TMS320F28335 MCU. The algorithm described in Section V was included in the firmware with the LUT system embedded in non-volatile RAM memory. Moreover, a variable SF inner current controller for the converter was specifically designed for this test, including an adaptive tuning of the associated regulators.

During the test the converter is started at a light load, 2.8 kVA (i.e. $c = 9.3\%$), delivering active power to the grid with unity power factor. After 1 s the converter load level is increased to 17.1 kVA (i.e. $c = 57.1\%$) and then to 26.9 kVA (i.e. $c = 89.8\%$) at time 4 s. Fig. 12 shows the phase current of the converter during these variations together with the performance of the SF in reaction to those load step changes. Finally, at time 7 s one of the air-heating systems is added to the three devices already connected to the local grid, thus shifting the local demand from 27 kW to 36 kW. As predicted, the consequent change in system impedance at the converter point of coupling causes a variation of local losses moving the optimum value of the SF.

VIII. CONCLUSIONS

This work presents an operation strategy for DRs based on an adaptive SF framework with the aim of achieving an overall

improvement of the efficiency within the Local EPS. The proposal demonstrates the interest in considering the converter losses together with the induced harmonic losses in the local line and loads when the ownership/operation of both assets are held by the same entity. The thermal limits of the power modules used in the inverter have been taken as a constraint in order to assure a safe operation of the device beyond its design SF when working at light loads. A LUT-based system, valid for an on-line implementation, was designed to provide the DR with a smart regulation of its SF. The results demonstrate that an improvement of the overall efficiency of the system at light converter loads by about 1% is readily achieved with the proposed method.

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