SuperJunction Cascode, a Configuration to Break the Silicon Switching Frequency Limit

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***Abstract*— This paper evaluates the SuperJunction MOSFET in cascode configuration with a low-voltage silicon MOSFET. The structure combines the good switching performance provided by the cascode configuration with advantages of the silicon technology as the robustness, the maturity and the low-cost. The objective of this paper is to elucidate and to demonstrate the reduction of switching losses of SuperJunction MOSFETs in cascode configuration with respect to their standalone counterparts (directly driven). A detailed simulation analysis of power loss contributions is carried out under hard-switching operation. Eventually, experimental evidence is provided by using a boost converter (100 V-to-400 V) in continuous conduction mode for a wide range of switching frequency (100 kHz-to-400 kHz) and output power (180W-to-500W).**

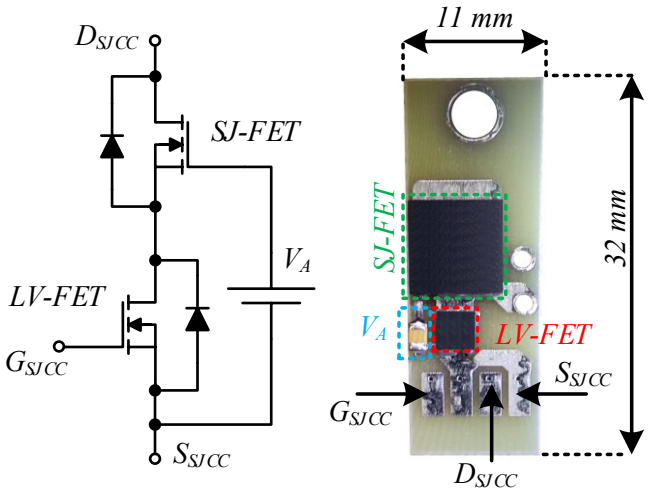
Keywords*— *High-frequency, high-efficiency, cascode configuration, SuperJunction MOSFET, silicon.

I. INTRODUCTION

A stagnation of the current density capability has been theoretically predicted in forthcoming generations of SuperJunction MOSFETs (SJ-FETs) [1]. In its turn, a limit on lowering SJ-FET parasitic capacitances will be encountered by restrictions in downsizing active area. As a result, a research for alternative silicon solutions, different to shrinking the device cell-pitch, is mandatory in future competition with Wide-Bandgap (WBG) materials.

During the last 5 years, the Cascode Configuration (CC) has become the preferred approach for some semiconductor companies to achieve normally-off GaN and SiC power switches [2]-[6]. In the range of 600V, GaN in CC (GaN-CC) has demonstrated superior switching performance than widely used SJ-FETs [7]-[9]. However, a recent work [10] states that most of the improvement achieved in GaN-CC is due to the low input capacitance provided by the Low-Voltage Silicon MOSFET (LV-FET) rather than the WBG material. Hence, the same work concludes that a SJ-FET used in CC (SJ-CC) would be equally valid for switching performance enhancement (Fig. 1(a)). However, there is an absence of insight and variety of operation conditions to proof the SJ-CC possible benefits [11]. In general terms, there is a lack of prior art about High-Voltage (HV) silicon devices in CC, with exception of some 30-year old literature about Bipolar Junction Transistors (BJT) [12], [13]. Although the efficiency improvement is not proven yet in a specific application, the authors of the present paper recently published a theoretical model of the switching mechanism of SJ-CCs with special focus on the critical parasitic elements [14].

The aim of this paper is to prove that the SJ-CC outperforms the SJ-FET in standalone configuration when is used in ultra-fast hard-switching operation conditions. For this purpose, a SJ-CC, arranged as shown in Fig. 1(b), has been built by means of discrete components. Moreover, the experimental demonstration and numerical simulations provide a quantitative definition of power losses. It will be demonstrated that the SJ-CC achieves substantial power savings with respect to the SJ-FET at high-switching frequency and/or at high load current. The paper is organized as follows. A brief description of the SJ-CC behaviour during the on-state, off-state, turn-on transition and turn-off transition is provided in section II. An exhaustive analysis of switching energy losses in the SJ-CC is given in III. This section (mainly based on numerical simulations) compares switching energy dissipated in the SJ-FET and in the SJ-CC for different operating conditions. In this sense, the most favourable operating conditions of the SJ-CC are identified. Finally, the experimental results are provided in section IV and the conclusions are gathered in section V.



(a) (b)

Fig. 1. SuperJunction Cascode Configuration (SJ-CC): (a) Ideal circuit schematic. (b) Plug-in board with SJ-CC prototype.

II. Behaviour of the SuperJunction MOSFET in Cascode Configuration (SJ-CC)

A. Operating Principle During On-State and Off-State

The SJ-CC is composed of a SJ-FET and a LV-FET as high-voltage and low-voltage silicon devices respectively (see Fig. 1(a)). A constant voltage source (V_A) connected between the gate of the SJ-FET and the source of the LV-FET is needed due to the positive threshold voltage of the HV device. From a general point of view, the SJ-CC operates as a single switch that has an equivalent gate (G_{SJCC}), drain (D_{SJCC}) and source (S_{SJCC}).

During the off-state, as can be seen in Fig. 2, the SJ-FET blocks most of the voltage while the LV-FET blocks a voltage that is equal or lower than the avalanche voltage of its parasitic diode (V_{AV}). In this paper it is assumed that this diode always achieves the avalanche state. During the off-state, the gate to source voltage of the LV-FET is equal to the output voltage of the driver in low-state, while the gate to source voltage of the SJ-FET corresponds to (V_A - V_{AV}), which must be lower or equal to 0 V to properly provide the off-state .

During the on-state, the gate to source voltage of the LV-FET is fixed by output voltage of the driver in high-state, while the gate to source voltage of the SJ-FET is the difference between the constant voltage source V_A and the voltage drop of the LV-FET channel during conduction which can be neglected. Hence, both MOSFETs are conducting with a different contribution to the whole on-resistance. In general, it is designed to be about 90% and 10% for the SJ-FET and LV-FET devices respectively.

B. Brief Description of Turn-On and Turn-Off Transitions

The schematic circuit proposed in [14] is shown in Fig. 3 to explain the behaviour of the SJ-CC during the turn-on and turn-off. This model includes both MOSFETs and their relevant parasitic elements: the antiparallel diode (D_{SJ}) and the drain to source (C_{DSHV}), gate to source (C_{GSHV}) and drain to gate (C_{DGHV}) capacitances of the SJ-FET; and the antiparallel diode (D_{LV}) and the drain to source (C_{DSLV}) gate to source (C_{GSLV}) and drain to gate (C_{DGLV}) capacitances of the LV-FET. In addition, it evaluates the parasitic inductance (L_{PAR}) that appears between the source of the SJ-FET and the drain of the LV-FET. This parasitic element causes a delay between the evolution of the gate to source voltage of the SJ-FET (v_{GSHV}) with respect to the evolution of the drain to source voltage of the LV-FET (v_{DSLV}). The schematic also shows the constant voltage source V_A, a current source (I_{LOAD}) that represents the current that flows through the inductive load, the freewheeling diode (D) with its parasitic capacitance (C_D) and the voltage (V_O) that the SJ-CC has to block during the off-state. The driver of the LV-FET is modelled as a Pulse Width Modulation (PWM) voltage source (v_{DRI}) in series with R_{GLV}. v_{DRI} provides V_{DRI} and 0 V during the high-state and low-state respectively. It is important to note that R_{GLV} models the output resistance of the driver plus the gate resistance of the LV-FET. Moreover, in the case of the SJ-FET there is a resistance (R_{GHV}) that represents the internal gate resistance of the device.

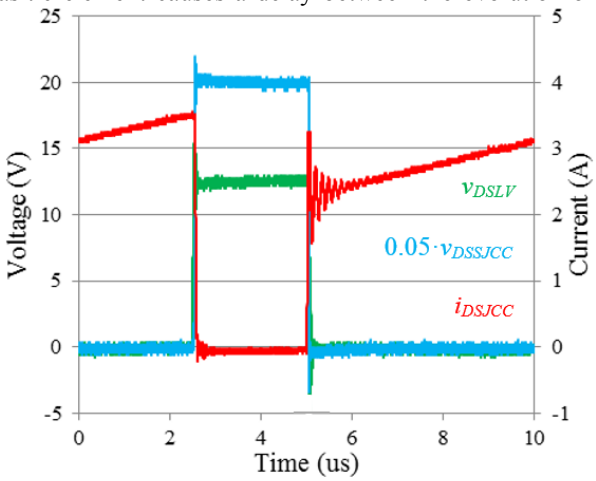


Fig. 2. Main waveforms of the boost converter at 100 kHz and 300W (100 V-to-400 V).

A qualitative description of both transitions based on this model is included below. It has been assumed that both transitions are sequential, which means that either the turn-on or turn-off of the SJ-FET never starts before the end of either the turn-on or turn-off of the LV-FET. [14] explains that this consideration is not completely true because the transition of the SJ-FET always starts before the end of the transition of the LV-FET. However, this assumption simplifies the explanation and does not invalidate the energetic analysis detailed in next sections, which is the main contribution of this work.

Turn-On

Before the turn-on transition starts, both MOSFETs behave as open circuits and the current of the inductive load (I_{LOAD}) flows through the freewheeling diode D. The transition starts when the output voltage of the driver changes from low-state (0 V) to high-state (V_{DRI}).

1) Turn-On of the LV-FET: The driver charges C_{GSLV} and discharges C_{DGLV}. Hence, the gate to source voltage of this device rises until the threshold voltage. After that, the LV-FET channel starts to behave as a current source that depends on v_{GSLV} and which discharges C_{DSLV} and charges C_{GSHV} with a certain delay between them due to the action of L_{PAR}. The explanation is simplified by considering that C_{DSLV} is fully discharge before

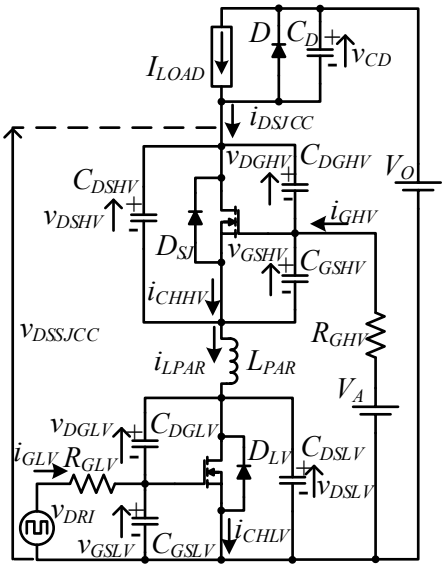


Fig. 3. Schematic circuit used to study the switching behaviour of the SJ-CC, which includes the most important parasitic elements.

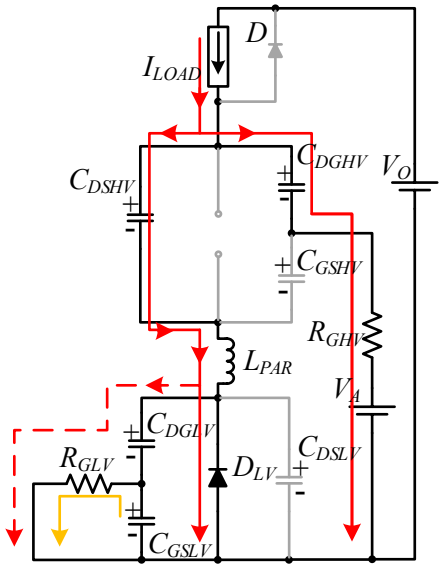


Fig. 4. Equivalent circuit of the model shown in Fig. 3 during the avalanche state of the LV-FET. The current paths provided by the inductive load (I_{LOAD}) are highlighted in red.

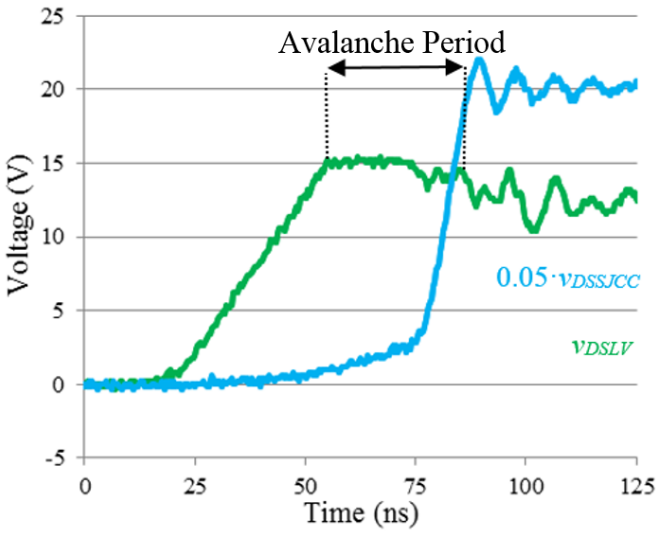


Fig. 5. Experimental waveforms of the drain to source voltage of the LV-FET and the total drain to source voltage of the SJ-CC (scaled) during the avalanche state of the LV-FET.

any appreciable change of the state at the SJ-FET occurs. However, this simplification can be assumed with slight loose of accuracy.

2) Turn-On of the SJ-FET: Once the turn-on of the LV-FET has finished, the constant voltage source V_A starts to charge C_{GSHV}. After v_{GSHV} achieves the threshold voltage, the SJ-FET channel starts to behave as a current source that depends on this voltage. It is important to note that C_{DGHV} remains clamped to (V_O - V_A) while the freewheeling diode continues forward biased. This assumption is only true if R_{GHV} is equal to 0 Ω. This implies that all the gate current provided by V_A is fully used to charge C_{GSHV}, which implies a faster rise of the current through the SJ-FET channel. In practice, this advantage could be considered true only for certain SJ-FETs where R_{GHV} is negligible. It is important to note that this resistance ranges between 0.2 Ω and 6 Ω depending on the SJ-FET technology [15]. The existence of this small resistance implies a limitation of the current that V_A provides (i.e. the higher R_{GHV}, the lower the current) and that C_{DGHV} is not fully clamped. As v_{GSHV} rises, the channel is able to conduct a higher level of current which comes from a part of the current of the inductive load. The rest of I_{LOAD} continues flowing through the diode D. There is an instant in which this diode does not conduct any current. After that, the channel of the SJ-FET conducts all the current of the inductive load, plus currents that discharge C_{DSHV} and C_{DGHV}, plus a current that charges the parasitic capacitance of D. During this period of time, most of gate current flows through C_{DGHV}. In other words, the Miller effect occurs at the SJ-FET. The turn-on transition ends when C_{DSHV} and C_{DGHV} are fully discharged and C_D is fully charged. It has been considered that the diode D is a SiC Schottky diode.

Turn-off

Before the turn-off transition starts, the SJ-CC drives all the current of the inductive load through the channel of both MOSFETs, while the diode D blocks V_O. The transition starts when the output voltage of the driver changes from high-state (V_{DRI}) to low-state (0 V).

1) *Turn-Off of the LV-FET*: The driver discharges C_{GSLV} and charges C_{DGLV}. Due to the fall of v_{GSLV}, the LV-FET channel starts to behave as a current source that depends on this voltage, to finally become an open circuit.

2) *Turn-Off of the SJ-FET*: The part of current of the inductive load that does not flow through the LV-FET channel charges C_{DSLV} and discharges C_{GSHV}. When v_{GSHV} falls to a certain value, the channel of the SJ-FET starts to behave as a current source that depends on the value of this voltage. The lower the voltage, the lower the level of the current through the channel. The part of the current of the inductive load that does not flow through the channel charges C_{DSHV} and C_{DGHV}. The current that flows through C_{DSHV} and the current which continues flowing through the channel also charges C_{DSLV} and discharges C_{GSHV}. There is an instant in which v_{GSHV} falls to the threshold voltage of the SJ-FET, and therefore, the channel becomes an open circuit. Again, the charge of C_{DSLV} and the discharge of C_{GSHV} is done by the action of the current through C_{DSHV}. At a certain instant v_{DSLV} achieves a value that causes the avalanche state of the parasitic diode of the LV-FET. Due to this, v_{GSHV} remains constant (i.e. V_A - V_{AV}). After that, the current of the inductive load continues charging C_{DSHV} and C_{DGHV}, but now the part of I_{LOAD} that flows through the first capacitor, also flows through the LV-FET, remaining in avalanche state. This phenomenon is a source of losses that does not appear in the standalone configuration. Fig. 4 shows the equivalent circuit of the schematic shown in Fig. 3 during this stage. Fig. 5 shows experimental voltage waveforms, where the avalanche state of the LV-FET is highlighted. The turn-off transition and the avalanche state ends when the drain to source voltage of the SJ-FET (v_{DSHV}) achieves its final value (i.e. V_O - V_{AV}). After that, the diode D is forward biased and drives I_{LOAD}.

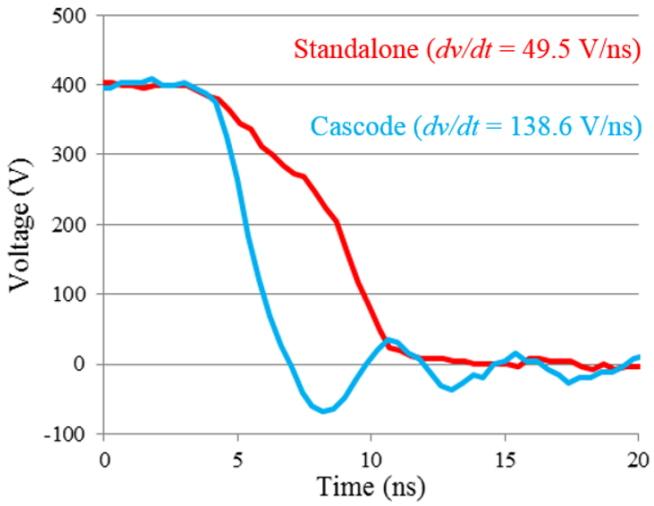


Fig. 6. Comparison between the experimental waveforms of the drain to source voltage during the turn-on of the same SJ-FET in CC and in standalone configuration.

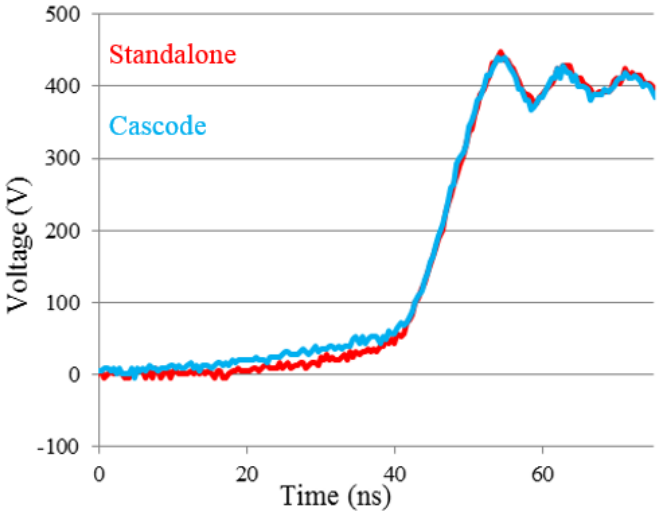


Fig. 7. Comparison between the experimental waveforms of the drain to source voltage during the turn-off of the same SJ-FET in CC and in standalone configuration.

III. Energy Analysis

A. Source of Losses in a SJ-FET in Standalone Configuration and in CC

(1) defines the switching energy dissipated by a SJ-FET in standalone configuration (E_{SSW}) as the sum of the energy dissipated by the coexistence of voltage and current in the SJ-FET channel during both transitions (E_{SON} y E_{SOFF}) and the energy dissipated in the gate resistance (E_{SRg}) when the input capacitance (C_{iss}) is charged and discharged. The switching energy dissipated by the SJ-CC (E_{CCSW}) is expressed in (2). E_{CCSW} is equal to the sum of the energy dissipated in the SJ-FET and the LV-FET channels during both transitions (E_{CCHVON}, $E_{CCHVOFF}$, E_{CCLVON} and $E_{CCLVOFF}$), the energy dissipated in the gate resistance of the LV-FET (E_{CCLVRg}) and of the SJ-FET (E_{CCHVRg}) during the charge and discharge of their input capacitances, and the energy dissipated during the avalanche state of the LV-FET (E_{CCAval}).

$$E_{SSW}[J] = E_{SON}[J] + E_{SOFF}[J] + E_{SRg}[J], \quad (1)$$

$$E_{CCSW}[J] = E_{CCHVON}[J] + E_{CCHVOFF}[J] + E_{CCLVON}[J] + E_{CCLVOFF}[J] + E_{CCHVRg}[J] + E_{CCLVRg}[J] + E_{CCAval}[J]. \quad (2)$$

Commonly, most of the switching losses of a SJ-FET in standalone configuration are caused by the voltage and current coexistence at the device channel during both transitions. In the case of the SJ-CC, the switching losses of the LV-FET are negligible and the most relevant source of switching losses is the coexistence of voltage and current at the SJ-FET channel. Moreover, the switching losses at the input of the switch (i.e. gate resistor during the charge and discharge of the input capacitance) are negligible in both configurations in comparison to previous ones. Taking into account these considerations, the expressions (1) and (2) can be rewritten as (3) and (4) respectively. (5) defines the switching energy saved (ES_{CCSW}) when the same SJ-FET is implemented in CC instead of standalone configuration. It is the difference between E_{SSW} and E_{CCSW}, and it is defined as the energy saved during both transitions (ES_{ON} and ES_{OFF}) minus the energy dissipated in the LV-FET during its avalanche state.

$$E_{SSW}[J] \cong E_{SON}[J] + E_{SOFF}[J], \quad (3)$$

$$E_{CCSW}[J] \cong E_{CCHVON}[J] + E_{CCHVOFF}[J] + E_{CCAval}[J], \quad (4)$$

$$ES_{CCSW}[J] \cong ES_{ON}[J] + ES_{OFF}[J] - E_{CCAval}[J]. \quad (5)$$

As it will be demonstrated in section III.C, the SJ-CC reduces the coexistence time of voltage and current at the channel during both transitions, mainly in the turn-on (i.e. $ES_{ON} \gg ES_{OFF}$). This fact makes attractive the use of the SJ-CC in comparison to the SJ-FET in standalone configuration, and it is the main result which must be highlighted in this paper. Fig. 6 and Fig. 7 show a comparison of the drain to source voltage experimental waveforms for the same SJ-FET in CC and in standalone configuration during the turn-on and turn-off respectively, corroborating previous conclusion.

It is important to note that in the case of the SJ-CC, the avalanche of the LV-FET adds an additional source of losses which can not be neglected in some configurations. In fact, if the selection of the LV-FET is unsuitable, the penalization of these losses are more important than the improvement achieved during the turn-on. Due to this, non-adequate combinations of SJ-FET and LV-FET in SJ-CC could provide worse efficiency than the standalone configuration under certain operation conditions.

The conduction losses of the SJ-CC are higher than standalone configuration due to the addition of the LV-FET on-resistance. However, the extra conduction losses of the SJ-CC is negligible because the LV-FET on-resistance is several times lower than the SJ-FET on-resistance. In addition, it is important to note that the increase of the SJ-FET on-resistance by self-

heating is lower in the case of the SJ-CC. This is because the SJ-FET of the CC dissipates less switching power and the same conduction power.

B. Reasons of the Superior Switching Behaviour of the SJ-CC

The theoretical reduction of the current and voltage coexistence time achieved at the output of the SJ-CC during the turn-on is due to the faster charge of the input capacitance of the SJ-FET (charge of C_{GSHV} and discharge of C_{DGHV}). In the case of the SJ-CC, the resistance that appears in the charging path of this capacitance includes the LV-FET on-resistance (negligible) and the internal gate resistance of the SJ-FET. For the standalone configuration, the resistance that appears in this path is higher because it includes the internal gate resistance, the output resistance of the driver and the external gate resistance needed to mitigate the oscillations of the gate to source voltage due to the parasitic inductance.

In both cases, the total resistance is an element that generates switching losses and that limits the total gate current provided (by V_A for the SJ-CC and by the driver for the standalone configuration). The higher the resistance, the lower the gate current and the greater the amount of time spent in the charge of the input capacitance. It is important to note that in the case of the SJ-CC, it is not needed an external resistance connected to the gate of the SJ-FET in order to prevent v_{GSHV} from overshooting. This is because L_{PAR} can be reduced to values below 5 nH even if discrete devices are used for the implementation. Moreover, the overshooting that could appear due to the parasitic inductance between the voltage source V_A and the gate of the SJ-FET can be reduced by the addition of an external capacitance connected in parallel and close to the high-voltage device.

In the case of the SJ-CC, the faster charge of the SJ-FET input capacitance implies a reduction of the time spent in two stages of the turn-on in which there is a coexistence of voltage and current at the channel of the SJ-FET:

1) The stage when the channel blocks a constant voltage $V_O - V_{AV}$ (C_{DSHV} remains charged) and the current through the channel rises from 0 to I_{LOAD}. During this stage, the SJ-FET channel can be modelled as a current source that depends on v_{GSHV}. The faster rise of this voltage implies that the current through the channel achieves the final value in a shorter time (less coexistence of current and voltage at the channel of the SJ-FET). As in the standalone configuration, most of the SJ-FET total gate current in CC flows through the gate to source capacitance during this stage. The total gate current is higher in the case of the SJ-CC due to the less resistive charging path, which implies a faster rise of the SJ-FET gate to source voltage, and therefore, less coexistence time.

2) The stage when the channel conducts all the current of the inductive load, plus currents that discharge C_{DSHV} and C_{DGHV} and plus a current that charges the parasitic capacitor of the freewheeling diode. During this stage, as in the standalone configuration, the Miller effect occurs at the SJ-FET and most of the total gate current flows through the SJ-FET drain to gate capacitance. As in the previous stage, the total gate current is higher in the case of the SJ-CC, which implies a faster discharge of C_{DSHV} and C_{DGHV}, and a faster charge of C_{GSHV} with respect

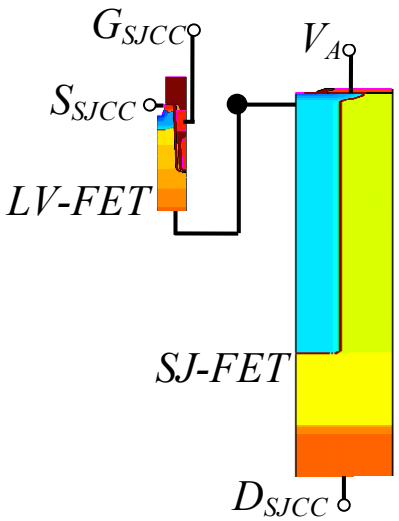


Fig. 8. SJ-CC model used in mixed-mode simulation.

to the standalone configuration. In other words, the Miller effect also occurs at the SJ-FET of the SJ-CC but it takes a shorter time than in the standalone configuration (i.e. shorter coexistence time).

C. Suitable Operation Conditions for the Use of the SJ-CC

The operation conditions in which the use of the SJ-CC achieves a higher improvement compared to the standalone configuration are studied in this section. The exercise is based on the mixed-mode simulation of a boost converter with a 100 V input voltage and 400 V output voltage. Mixed-mode simulation combines the SPICE circuit shown in Fig. 3 with the TCAD structures in Fig. 8. Hence, the physical effects in the SJ-FET and in the LV-FET are captured with more accuracy than using SPICE-based models. The boost converter is composed of ideal elements with exception of the main switch. The simulation comparison is developed for a 100 mΩ SJ-FET

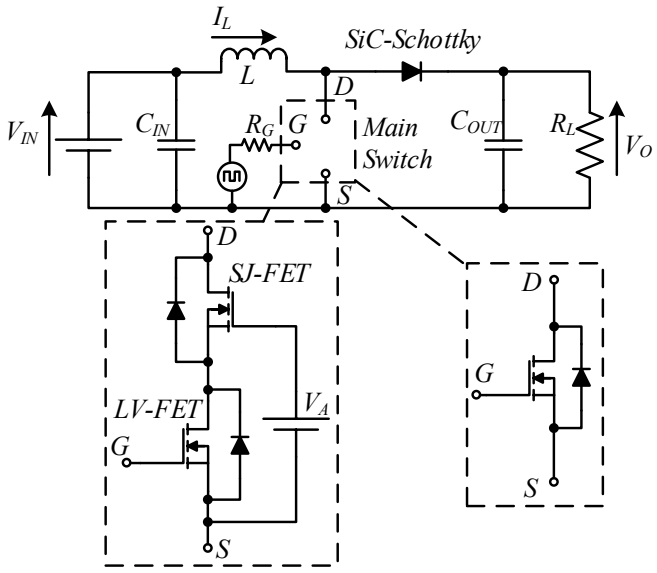


Fig. 9. Schematic circuit of the boost converter utilized in simulation and for the experimental results.

TABLE I. Characteristics of the SJ-FET used in the mixed-mode simulations.

Q_g (nC)*[1]	Q_{gd} (nC)*[1]	Q_{gs} (nC) *[1]	C_{oss} (pF) *[2]	C_{oss} (pF) *[3]
146	77	22	1450	130

*[1] at V_{GS} = 12 V, I_D = 12 A
*[2] at V_{GS} = 0 V, V_{DS} = 25 V
*[3] at V_{GS} = 0 V, V_{DS} = 400 V

in standalone configuration and in CC with a 10 mΩ LV-FET (see Fig. 9). Other characteristics of the SJ-FET used in the mixed-mode simulation are shown in TABLE I. The external gate resistance (R_G) is 6.8 Ω in both cases. Fig. 10 shows the energies dissipated exclusively in the SJ-FET during both transitions for these two configurations versus the current of the inductive load. These energies include the energy dissipated by the coexistence of voltage and current in the SJ-FET channel, the energy dissipated in the gate resistance (internal in the case of the SJ-CC because R_G is connected to the LV-FET and internal plus external for the standalone configuration) due to the charge and discharge of the input capacitance of the HV MOSFET. As it can be seen, as the current is increased, the energy dissipated rises, especially in the case of the SJ-FET in standalone configuration. Moreover, the SJ-CC shows lower power dissipation due to the shorter coexistence time of voltage and current at the channel of the SJ-FET. As was indicated in section III.A, most of the improvement appears during the turn-on while the improvement achieved in the turn-off is only appreciable at higher currents. It is important to note the low increase of the energy dissipated in the case of the SJ-CC as the current rises: when the current is 1.8 A, the energies dissipated during the turn-off and during the turn-on are 21.5 uJ and 16.5 uJ respectively, while when the current is 12 A, they are 28.8 uJ and 25.3 uJ.

At this point, this comparison is unfair because in the case of the SJ-CC, the extra energy dissipated by the LV-FET during both transitions must be taken into account. This energy includes the energy dissipated by the coexistence of voltage and current in the channel of the LV-FET, the energy dissipated in gate resistance (internal plus external) due to the charge and discharge of its input capacitance and the energy dissipated during the avalanche state. As Fig. 11 shows, these energies are 1 or 2 order of magnitudes below the energies dissipated by the SJ-FET of the SJ-CC (Fig. 10). Also, Fig. 11 shows that the

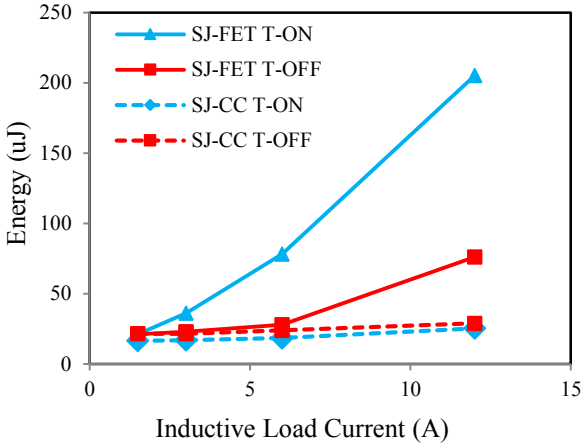


Fig. 10. Comparison of the energy dissipated by the same SJ-FET during both transitions when it is used in CC and in standalone configuration.

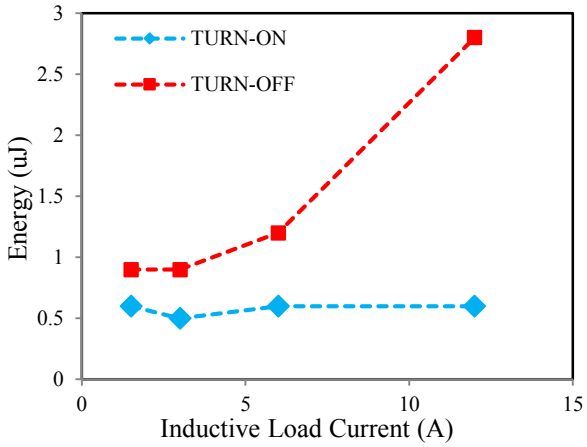


Fig. 11. Comparison of the energy dissipated by the LV-FET during both transitions.

energy dissipated during the turn-off is higher due to the avalanche.

Finally, Fig. 12 shows the total power saved when the same SJ-FET is used in CC instead of standalone configuration for different switching frequencies versus current. As current rises, switching and conduction losses rise. The reason that explains the increase of the power saved by the SJ-CC when the current rises is the fact that the improvement achieved in the turn-on has more impact than the impact of the increase of conduction losses introduced by the LV-FET. Moreover, as switching frequency rises for a fixed value of current, only switching losses rise. Due to this, the SJ-CC dissipates less power thanks to its superior switching behaviour.

IV. Experimental Results

A. Converter Specifications

A boost converter in which the device under test (DUT) was a SJ-FET in standalone configuration or the same SJ-FET in CC was implemented to verify the previous analysis. The input and output voltages are 100 V and 400 V respectively. To test their behaviour versus current, different operation points had been compared (180 W, 300 W, 400 W and 500 W). To make this,

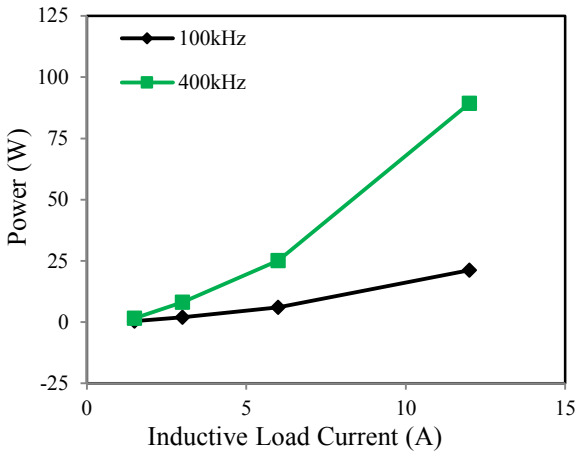


Fig. 12. Power saved when the same SJ-FET is used in CC instead of standalone configuration for different switching frequencies versus current.

TABLE II. Main characteristics of the SJ-FET and of the LV-FET used in the experimental tests.

	R_{on} (mΩ)	V_{DSmax} (V)	R_g (Ω)	Q_g (nC)	Q_{gd} (nC)	V_{th} (V)	I_{Dmax} (A)
SJ-FET	170	600	1	57	21	3	20.2
LV-FET	7.5	12	0.7	5.1	0.8	0.8	22

the load was modified, which implies different values for the average current through the inductive load (1.8 A, 3 A, 4 A and 5 A). The inductance was designed to operate in Continuous Conduction Mode (CCM) at all tested switching frequencies (from 100 kHz to 400 kHz). In addition, the inductance was designed also to provide low high-frequency ripple in order to make both switching transitions with a similar current.

The SJ-CC was implemented in an independent PCB using Surface Mounted Devices (SMD). As Fig. 1(b) shows, a SMD capacitor has been placed in parallel with the voltage V_A in order to stabilize this voltage. The main characteristics of the SJ-FET and the LV-FET used to implement the SJ-CC are shown in TABLE II.

The rest of the components of the converter are the same in all the comparative tests. The freewheeling diode is a 600 V SiC-Schottky in order to reduce the reverse recovery effect. The driver selected is the EL7104, which is connected to the SJ-FET in the standalone configuration and to the LV-FET for the SJ-CC with a 6.8 Ω gate resistor. The PWM signal applied between gate and source has a high value of 11 V for the SJ-FET standalone configuration and 7 V for the SJ-CC. The value of V_A is 11 V.

B. *Efficiency Measurements*

The efficiency of the converter has been obtained by measuring the input and output voltages and currents. This kind of measurement allows us to know the total power losses of the converter. However, the power dissipated by the DUT can not be known. It is important to note that only the DUT is changed from one test to another. Hence, the differences that appear in the total power losses can be assumed that comes from the change of the main switch. From the point of view of power losses of the DUT, conduction losses and most of the switching losses are considered. In other words, losses that appears during the conduction state, losses caused by the coexistence of voltage and current at the channel of the SJ-FET and of the LV-FET during the transitions and losses caused by the avalanche state of the LV-FET during the turn-off are considered. Losses that appear in the gate resistances when the current flows through them in order to charge and discharge the input capacitances were not measured because, as was indicated in section III.C, they are negligible.

At this point, it is important to define the power saved as the power dissipated by the converter when a SJ-FET in standalone configuration is used as the main switch minus the power dissipated by converter when the same SJ-FET is used in CC. As was indicated before, this difference can only be attributed to the DUT. Fig. 13 shows the power saved when the switching frequency and the current through the inductive load are modified. These experimental results verify that when the current through the inductive load and the switching frequency are increased, the SJ-CC provides a higher improvement from an energetic point of view. It is important to note that the comparison could not be made under certain operation conditions, like 300 kHz and 5A, because the SJ-FET in standalone configuration was not able to dissipate all the power that was needed.

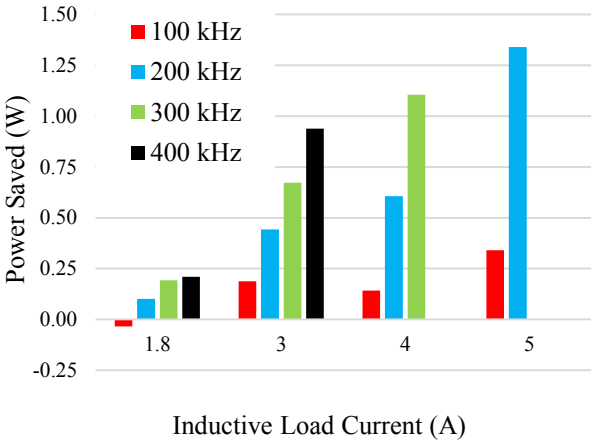


Fig. 13. Power saved when the same SJ-FET is used in CC instead of standalone configuration when the switching frequency and the current through the inductive load are modified.

V. CONCLUSIONS

The SJ-CC opens a new paradigm to extend HV silicon technologies to high-frequency domains (>100 kHz) and, subsequently, enabling the adoption of SJ-FETs in applications that where exclusively conceived for WBG devices. Aside to drastically reduce switching times and energies, the SJ-CC benefits from ruggedness, maturity and cost of silicon.

Despite of the widely use of the cascode configuration in the radiofrequency scope, it has only been explored in the power electronics applications for WBG high-voltage transistors or BJTs. This paper explains and demonstrates that the use of the SJ-FET also takes advantages of the good switching behaviour by using the CC in order to save more power than the standalone configuration.

It has been concluded that the improvement achieved by the SJ-CC is due to the fast charge of the equivalent gate capacitance of the SJ-FET. This fact reduces the time in which there is coexistence of voltage and current in the channel of the SJ-FET. This implies that if the switching frequency is increased, the SJ-CC saves more power than the standalone configuration. In addition, the SJ-CC is more efficient than standalone configuration as the current through the switch rises. This is because the penalization in the conduction losses due to the extra on-resistance of the LV-FET has a lower impact than the improvement achieved during the turn-on. In the case of the SJ-CC, the avalanche state of the LV-FET is an additional source of losses that does not appear in the standalone configuration. Besides reducing the SJ-CC efficiency, this kind of losses could degrade the LV-FET.

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