

# Switching performance comparison of a power switch in a Cascode Configuration using a SuperJunction MOSFET

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**Abstract-** This paper is focused on the analysis of the cascode connection of Superjunction MOSFETs (SJ-FET) working as a high voltage normally-off power switch, based on Silicon technologies. In order to carry out this analysis, it will compare the cascode structure with the standalone connection, in which only one SJ-FET is used. The comparison is carried out in terms of switching behaviour, in order to verify if the cascode has a faster switching than a directly controlled SJ-FET. Experimental measurements are presented for both topologies working on a boost converter with an input voltage of 150 V, output voltage of 400 V, power range between 100 W and 400 W and a switching frequency range between 100 kHz and 400 kHz. Finally, an analysis of losses on the boost converter for both topologies is included.

**Keywords:** Cascode; SuperJunction FET; Power switch; Efficiency; Switching losses

## I. INTRODUCTION

High Electron Mobility Transistors (HEMT) of Gallium Nitride (GaN) in cascode configuration are today the preferred approach by many companies to achieve a normally-off power switch for high frequency applications with voltages are around 500 V [1] [2]. It is also possible to find commercial devices based on a Silicon low voltage MOSFET and a JFET of Silicon Carbide (SiC) in cascade configuration [3], mainly used for the switching of inductive loads and in order to increase the efficiency in applications like solar inverters and charging process on electric vehicles.

These GaN and SiC devices [4] show a better switching behaviour than the mainly used Silicon Superjunction MOSFETs (SJ-FETs) due to the excellent dynamic characteristics of the material [5]. However, recently works [6] suggest that parts of these advantages are mainly attributed to the cascode configuration. In spite of that, nowadays there are few references related with Silicon devices for high voltage applications in cascode configuration, with the exception of the topologies based on Bipolar Junction Transistors (BJT) [7].

The aim of this paper is focussed on the study of the cascode configuration as a high voltage, normally-off, power switch based on Silicon technologies. The cascode is a well-known topology in the case of using bipolar transistors, however, the cascode topology in this paper is formed by the union of a Superjunction Silicon MOSFET working as a high voltage MOSFET (HV-FET) and a low voltage Silicon MOSFET (LV-FET). In Fig. 1 the cascode configuration diagram is shown.

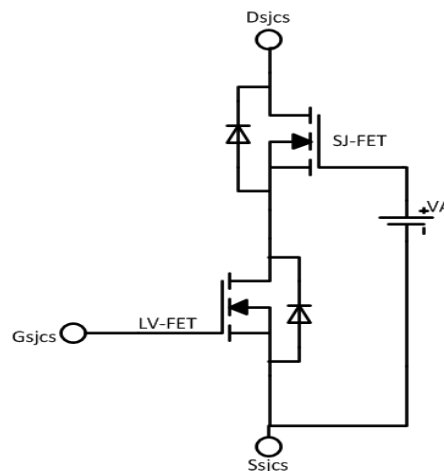


Fig. 1. Schematic of a Superjunction MOSFET in cascode configuration with a low voltage silicon MOSFET

Another important purpose of this paper is to analyse the switching behaviour of the cascode configuration in comparison with the standalone configuration, in which a SJ-FET is directly controlled. This analysis is carried out to verify if the cascode presents a faster switching behaviour than a standalone SJ-FET.

The paper is organized as follows. Section II describes the static behaviour of the cascode configuration under study in this paper, which is composed by a SJ-FET and LV-FET. Section III describes the switching operation of the cascode configuration, focusing on the main differences with a directly controlled SJ-FET. In section IV, the losses of both configurations are estimated. Section V presents the experimental results that verify the previously presented analysis and the good performance of the cascode configuration. Finally, conclusions are drawn in Section VI.

## II. SUPERJUNCTION CASCODE STRUCTURE

In the proposed analysis, a SJ-FET working as a high voltage device and a low voltage Silicon MOSFET compose the cascode topology. A constant voltage source ( $V_A$ ) in the gate of the SJ-FET is necessary to polarize the SJ-FET during the on-state and to achieve that this MOSFET works as a normally-on device. As can be seen in Fig. 1, the cascode configuration is composed by two transistors, but the complete topology works as a single switch with an equivalent gate ( $G_{SJCC}$ ), drain ( $D_{SJCC}$ ) and source ( $S_{SJCC}$ ).

The LV-FET is controlled by a pulse wide modulated (PWM) signal, so the gate-source voltage in the LV-FET will be determined by the voltage values of this PWM signal. During the off-state, the SJ-FET blocks most of the output voltage, while the LV-FET blocks a voltage which is less or equal to the avalanche voltage of its parasitic diode ( $V_{AV}$ ).

During the off-state, the lower value of the PWM signal (0 V), determines the gate-source voltage of the LV-FET, and the gate-source voltage of the SJ-FET is equal to the difference between the constant voltage  $V_A$  and the avalanche voltage of the parasitic diode of the LV-FET ( $V_A - V_{AV}$ ), being this difference less or equal to 0 V.

During the on-state, the higher value of the PWM signal (12V) determines the gate-source LV-FET, and the gate-source voltage of the SJ-FET will be equal to the difference between the constant voltage  $V_A$ , and the conduction voltage drop in the LV-FET (practically negligible, due to the small values of the  $R_{DSon}$  in the LV-FETs). It will be assumed that, during the on-state, the gate-source voltage on the SJ-FET will be  $V_A$ .

### III. SWITCHING BEHAVIOUR OF THE SUPERJUNCTION CASCODE STRUCTURE

To analyse the switching behaviour of the cascode topology, a more complex circuit than the presented in Fig. 1 is needed. The circuit used in this paper to study the switching process in a cascode configuration is shown in Fig. 2. In this circuit, there are two ideal MOSFETs with the most important parasitic elements, such as the parasitic diodes in both transistors, and the parasitic capacitances. It also includes a freewheeling diode (D), the constant voltage source ( $V_A$ ), and the output voltage ( $V_o$ ), which is the voltage that the cascode withstands during the off-state. The model is completed with a PWM source, which its lower value corresponds to 0 V and its higher value corresponds to the value of  $V_{Dri}$ . Finally, a resistor ( $R_{GLV}$ ) which includes the output resistor of the PWM source and the gate resistor of the LV-FET are also shown in this new model. Using the proposed circuit the turn-ON and the turn-OFF transitions of the cascode topology will be briefly explained. A more detailed analysis of this process can be found in [8].

#### 1. Turn-ON transition:

Before the turn-ON transition starts, both FETs are open circuits, so all of the current ( $I_L$ ) flows through the freewheeling diode (D).

First, the gate-source voltage of the LV-FET begins to rise, so the equivalent input capacity begins to charge until the gate-source voltage of the LV-FET reaches the threshold voltage. This rise in the gate-source voltage makes that the drain-source voltage of the LV-FET begins to fall, and  $C_{dSLV}$  begins to discharge. The LV-FET working on its current source state, discharges  $C_{dSLV}$  and charges  $C_{gSHV}$  making that the gate-source of the SJ-FET begins to rise with a certain delay. Once the LV-FET is on, the constant voltage source  $V_A$  charges  $C_{gSHV}$  (without Miller effect because all the current is still flowing through D). The rise in the gate-source voltage of

the SJ-FET produces an increase of the current through its channel. Finally, this transition is finished when the SJ-FET is completely on and  $C_{dSHV}$  are discharged.

When both MOSFETs are on, their channels behave as a resistor ( $R_{DSon}$ ). The value of the  $R_{DSon}$  of the LV-FET is approximately 10 % of the  $R_{DSon}$  of the SJ-FET. The total  $R_{DSon}$  value, due to the both MOSFETs, is an important element, which generates losses and draws out the charge and discharge process of  $C_{gSHV}$ .

#### 2. Turn-OFF transition:

Before the turn-OFF transition starts,  $I_L$  is flowing across the cascode topology and D is blocking  $V_o$ . The high to low step level on the PWM signal determines the beginning of the turn-OFF process.

First, the gate-source voltage of the LV-FET begins to decrease, so the equivalent input capacity of the LV-FET begins to fall until the channel of the MOSFET behaves as a current source. Then, the current through the channel of the LV-FET decreases and the current that is not going through its channel, discharges  $C_{gSHV}$  and charges  $C_{dSLV}$  till the LV-FET channel behaves as an open circuit. Now, the current through the SJ-FET channel drops as the drain-source voltage of the LV-FET continues rising and therefore, the gate-source voltage of the SJ-FET decreases. Because of that, the SJ-FET channel behaves as a current source depending on its gate-source voltage. As this voltage decreases, less current goes through the SJ-FET channel and a part of the current charges  $C_{dSHV}$  and  $C_{dghv}$ . Once the SJ-FET channel behaves as an open circuit, the gate-source voltage of the SJ-FET continues decreasing as the drain-source voltage of the LV-FET continues rising until reach a value in which the parasitic diode of the LV-FET enters in avalanche mode ( $V_A - V_{AV}$ ). Finally, all the inductive current charges  $C_{dSHV}$  and  $C_{dghv}$ , and also this current flows through the parasitic diode of the LV-FET in avalanche mode (which can produce important losses). The turn-OFF stage finishes when the drain-source voltage of the SJ-FET reaches its final value ( $V_o - V_{AV}$ ).

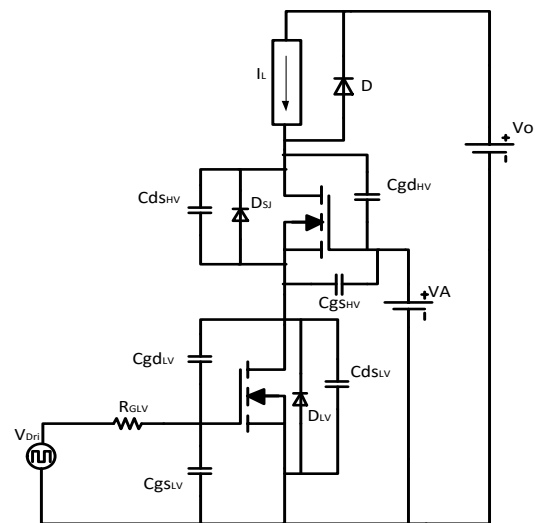


Fig. 2. Proposed schematic of the cascode configuration to analyse its switching behaviour including the MOSFETs and its most relevant parasitic elements

#### IV. ANALYTICAL ESTIMATION OF LOSSES

The main aim of this section is to present a brief analysis of the conduction and switching losses for both topologies. Other analysis based on Mixed-Mode simulations, among others, can be found in [9] and [10].

Conduction losses in the LV-FET must be added to the conduction losses in the SJ-FET. In general, conduction losses in the LV-FET are of a lower order and they are almost negligible on some operation points.

The switching losses in a MOSFET are basically generated due to the coexistence between voltage and current in the device channel during the transitions. In the case of the cascode, the main switching losses occur in the SJ-FET due to the coexistence of voltage and current in its channel, being the switching losses in the LV-FET practically negligible. However, the losses due to the avalanche of the parasitic diode of the LV-FET can have a strong effect in the total losses. In general, it is difficult to make an accurate analytical estimation of switching losses, due to the strong dependence of non-linear parasitic components (like the parasitic capacitances of the MOSFETs). Therefore, in order to compare the switching losses in both topologies, simulations using the double pulse circuit have been carried out, with the standalone configuration and the cascode topology. A switching frequency of 100 kHz, a power of 200 W, an input voltage of 150 V and an output voltage of 400 V were selected for these tests.

Table 1 shows the simulation results of the switching losses for both topologies during the turn-ON and turn-OFF stages. As Table 1 shows, the cascode configuration presents lower switching losses in turn-OFF and in turn-ON than the standalone configuration. As it is shown, in the cascode topology, the switching losses of the LV-FET are practically negligible, being the SJ-FET the device that generates more switching losses, due to the coexistence between voltage and current on the transitions, mostly on the turn-ON. These simulation results are a rough approximation to the switching losses, but a comparison of the results can explain the faster switching behaviour of the cascode topology.

However, during the turn-OFF the parasitic diode of the LV-FET enters in avalanche mode, and the current flowing through this diode can generate important losses that grow with the frequency. One possible way to improve the global behaviour in the cascode during the switching process is picking out a LV-FET in which the extra losses due to avalanche are not above the benefits that the cascode provides especially in the turn-ON.

Table 1. Simulation results of switching losses comparison between the standalone and the cascode configurations

Switching losses				
	Standalone	Cascode		
		SJ-FET	LV-FET	TOTAL
Turn-OFF	0.24317W	0.2294W	0.0085W	0.2379W
Turn-ON	0.40124W	0.3448W	0.01385W	0.3587W

Another possible way to compare the performance of the SJ-FET in standalone configuration with the cascode configuration is from the thermal point of view. A boost converter has been developed using the same specifications than in the previously detailed simulation. Some thermal images of the SJ-FET have been taken when a standalone configuration and a cascode topology is used (for both images the same power is processed during the same amount of time and the temperature is almost constant).

Fig. 3 shows how in the standalone configuration, the SJ-FET reaches a temperature of approximately 51.6 °C, while in the cascode topology the temperature reached by the SJ-FET is slightly lower, approximately 49.1°C. The reduction in temperature does not directly imply less losses of the cascode configuration because some losses can be in the LV-FET. However, on some applications a reduction of the temperature of the SJ-FET, even due to a distribution of the losses, can be important, mainly due to the increase of the  $R_{DSon}$  for high temperatures.

Fig. 4 shows a breakdown of the distribution of losses on the elements that composed the developed boost converter.

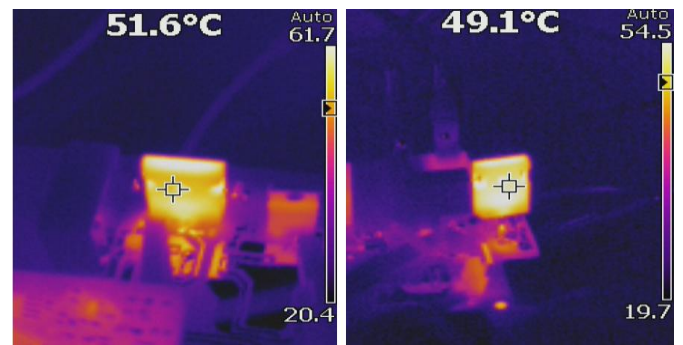


Fig. 3. Thermal images of the SJ-FET in the standalone configuration (Left) and in the cascode topology (Right)

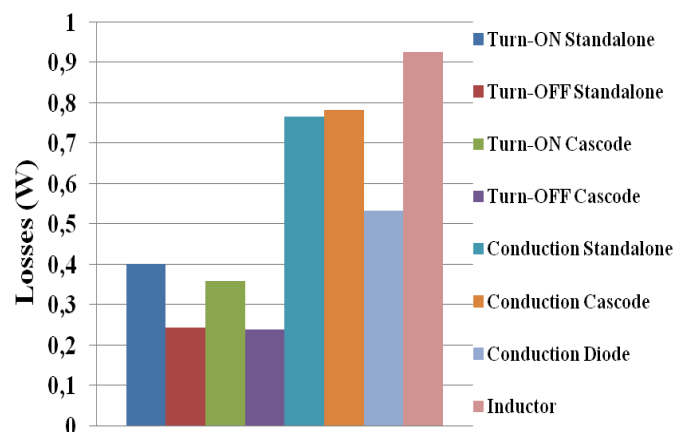


Fig. 4. Losses breakdown in the boost converter ( $F = 100$  kHz,  $P = 200$  W,  $V_{in} = 150$  V and  $V_{out} = 400$  V)

## V. EXPERIMENTAL RESULTS

All the results shown in this section were obtained using a boost converter in which the device under test (DUT) is the standalone topology or the cascode configuration. The converter operates in Continuous Conduction Mode (CCM) with low current ripple, in order to obtain information about both switching transients (turn-ON and turn-OFF). The input voltage ranges between 100 V and 150 V, the output voltage ranges between 266 V and 400 V, and the power ranges between 100 W and 400 W. The inductor is designed to have very low current ripple. The freewheeling diode is a 600 V SiC-Schottky, to minimize the reverse recovery effect. The driver that has been selected is the EL7104 and the resistor connected at the gate of the SJ-FET in the standalone configuration and at the gate of the LV-FET in the cascode topology is 5  $\Omega$ . Finally, the switching frequency range is between 100 kHz and 400 kHz. The confidentiality of the company that promotes this work, does not allow us to provide more information related with the SJ-FETs.

The experimental tests are based on the comparison of the efficiencies of both topologies. The efficiency is calculated measuring the input and output voltages and currents of the boost converter (driving losses are neglected). This way, power losses due to coexistence between voltage and current in the channel of SJ-FET and LV-FET, the avalanche losses in the LV-FET and the small differences in the conduction losses are taken into account.

For each different comparison test, only the DUT (standalone configuration or cascode) is changed in the boost converter. As the other components in the converter are the same for both configurations, the efficiency differences only can be due to the DUT.

As an example of the experimental waveforms of the cascode, Fig. 5 shows the turn-OFF transition in the cascode topology in which appears the avalanche effect of the parasitic diode in the LV-FET.

In the following sections, the experimental efficiency comparison is presented. Different operation points are shown to evaluate which is the best scenario to improve the performance of the cascode topology.

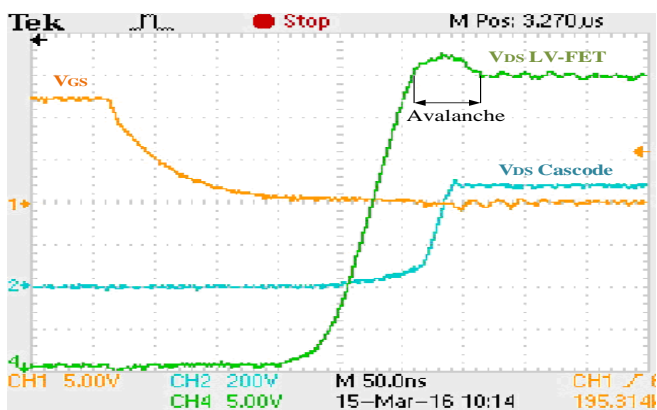


Fig. 5. Turn-OFF stage on the cascode topology  
F = 200 kHz, P = 200 W

### 1. IP135N03LG like LV-FET and a switching frequency of 200 kHz

The specifications for this test are based on an input voltage of 150 V, an output voltage of 400 V, the converter load ranges between 400  $\Omega$  and 1600  $\Omega$ , and the use of an IP135N03LG like the LV-FET.

In this operation point, the efficiency of the standalone configuration is above the cascode topology (Fig. 6). The main reason is that, at a switching frequency of 200 kHz, the conduction losses are predominant in comparison to the switching losses, so that the cascode achieves a lower efficiency due to the higher value of the equivalent on-resistor in the conduction state.

### 2. IP135N03LG like LV-FET and a switching frequency of 400 kHz

This is the highest switching frequency test performed. The main purpose of the increase of the switching frequency is to analyse how as the switching frequency increases and the switching losses becomes more relevant, facing the conduction losses, the cascode topology presents an improvement in its performance, facing the standalone configuration.

Fig. 7 shows that the efficiencies obtained by both topologies are closer than when the switching frequency was 200 kHz. In addition, at low powers (170 W – 250 W) the efficiency of the cascode topology is almost the same as the standalone configuration. This can validate that, when the switching frequency increases and the switching losses becomes more relevant in the total losses, the best switching behaviour of the cascode topology provides higher efficiency. In this operation points the improvement on the switching behaviour is enough to compensate the additional losses caused by the operation of the LV-FET parasitic diode in avalanche mode, during the turn-OFF.

### 3. Si9426DY like LV-FET and a switching frequency of 200 kHz

The LV-FET that has been used in the previous comparison tests has a maximum drain-source voltage of 30 V. The idea of this test is to use another LV-FET, in this case a Si9426DY, which has a maximum drain-source voltage of 20 V. The aim is to show how using a LV-FET with less drain-source voltage and therefore a less voltage value of avalanche in its parasitic diode, the switching losses can be reduced in the turn-OFF stage, improving the efficiency of the cascode topology.

Fig. 8 shows that the efficiencies achieved with the cascode topology are higher when the LV-FET of a maximum drain-source voltage of 20 V is used. For low powers (170 W – 250 W), Fig. 8 shows that the efficiency achieved by the cascode topology is slightly higher to the standalone efficiency, when only one SJ-FET directly controlled is used. At high power, while the cascode efficiency is below the standalone efficiency, the differences between efficiencies are

lower than the measurement on Fig. 6, when a LV-FET of a higher maximum drain-source voltage (30 V) was used.

#### 4. Study of the reduction of the avalanche time in the parasitic diode on the LV-FET Si9426DY for a switching frequency of 200 kHz and for a power of 200 W

One of the possible options in order to minimize the avalanche losses in the parasitic diode of the LV-FET is to achieve that the charge of the parasitic capacity between drain and source in the LV-FET becomes slower. In order to do that, an external capacitor ( $C_{EXT}$ ) has been connected between drain and source in the LV-FET. Different values for this capacitor has been selected in order to analyse their effect in the boost converter efficiency ( $\eta$ ), the LV-FET switching transition and the avalanche time ( $T_{aval}$ ), for a specific power. The selected values for this external capacitor are 1 nF, 3 nF, 5 nF, 8 nF and 10 nF. According to the results presented in Table 2, when the value of this external capacitor increases, the avalanche time of the parasitic diode in the LV-FET decreases and therefore, the avalanche losses become smaller, slightly increasing the efficiency in the cascode topology. However, if the value of the external capacitor is very high (10 nF), as the avalanche time decreases, the switching time in the LV-FET ( $T_{sw}$  LV-FET) increases, even affecting the switching of the SJ-FET, causing a worse switching behaviour and therefore, reducing the efficiency in the cascode topology (Table 2).

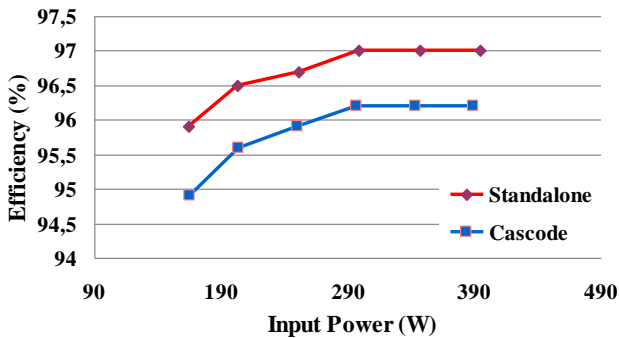


Fig. 6. Efficiency comparison between the standalone and the cascode configuration for a switching frequency of 200 kHz

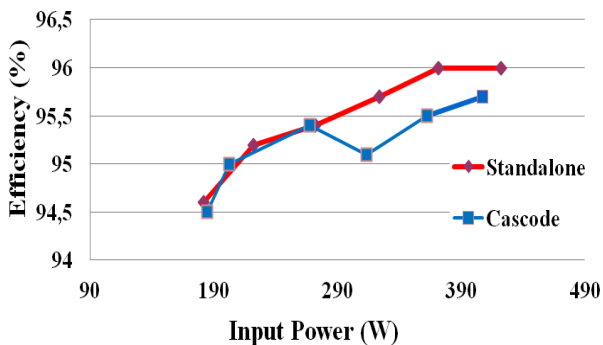


Fig. 7. Efficiency comparison between the standalone and the cascode configuration for a switching frequency of 400 kHz

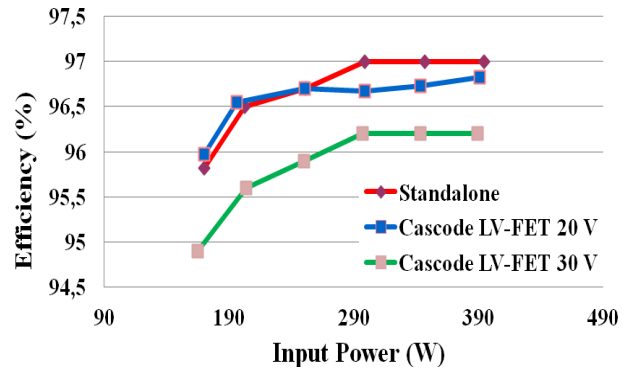


Fig. 8. Efficiency comparison between the standalone and the cascode configuration for a switching frequency of 200 kHz. LV-FETs  $V_{DS}$ : 30 V and 20 V

Table 2. Experimental measurements for the reduction of the avalanche time in the LV-FET Si9426DY for different values of the external capacitor  $C_{EXT}$

$C_{EXT}$ (nF)	$\eta$ (%)	$T_{aval}$ (ns)	$T_{sw}$ LV-FET (ns)
No Cap	96.55	70	90
1	96.56	70	100
3	96.62	65	110
5	96.81	60	140
8	96.61	40	150
10	96.52	30	180

## VI. CONCLUSIONS

In this paper, a high voltage switch in a cascode configuration based on Silicon technologies with a SJ-FET has been presented, including a brief analytical study of its switching process behaviour. This model has been compared with the standalone configuration in which a SJ-FET is directly controlled. The comparison has been carried out from the point of view of the efficiencies achieved for both topologies, as well as the generated losses. The model and the proposed explanation of the operation of the cascode have been validated by simulation and experimental results.

The experimental results have shown how when the switching losses become predominant (mainly due to an increase of the switching frequency), the cascode topology presents a slight improvement on its performance due to its faster switching transients. Due to this improvement in the switching behaviour, the cascode topology can be used to increase the switching frequency on a switching-mode power supply, keeping the same SJ-FET as high voltage device.

It has also been tested the significance of the selection of the LV-FET in a cascode topology. The experimental tests show that when a LV-FET with less drain-source voltage is used, the efficiency on the cascode improves due to the less value of the avalanche, reached by its parasitic diode. Therefore, the switching losses on the LV-FET are reduced and the efficiency on the cascode is higher than when LV-FETs with high drain-source voltages are used.

Finally, a mechanism to minimize the avalanche time in the LV-FET has been analysed. It has been tested that when the value of the capacity between drain and source of the LV-FET is higher, the avalanche time decreases, improving the efficiency of the cascode. However, when this charging process is too slow, the SJ-FET switching is affected, causing in general a worse switching behaviour in the cascode topology, and consequently a lower efficiency in the switch.

#### ACKNOWLEDGMENT

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