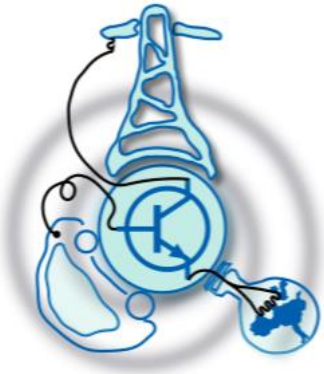
Design and Construction of an Isolated DC to DC Switching Converter for Integration of Energy Storage Systems in Power Electronic Applications

By

Sarah Saeed Hazkial Gerges



Submitted to the Department of Electrical Engineering, Electronics, Computers and Systems
In partial fulfillment of the requirements for the degree of
Master in Electrical Energy Conversion and Power Systems
at the
UNIVERSIDAD DE OVIEDO
July 2015

Author……...

Certified by……..…….

Jorge García García
Associate Professor
Thesis Supervisor

Design and Construction of an Isolated DC to DC Switching Converter for Integration of Energy Storage Systems in Power Electronic Applications

By

Sarah Saeed Hazkial Gerges

Submitted to the Department of Electrical Engineering, Electronics, Computers and Systems
On July 23, 2015, in partial fulfillment of the requirements for the degree of
Master of Science in Electrical Energy Conversion and Power Systems

Abstract

With the current trend towards greener energy sources, the integration of Energy Storage Systems (ESS) is the key to sustain the grid against fluctuations of energy generation. This raises a major concern for the inclusion of an efficient, fully controllable power conversion stage to allow an intermediate processing of energy flow.

The Dual-Active-Bridge (DAB) converter provides full controllability as well as galvanic isolation. DC-DC Isolated conversion is a critical process in some applications such as Electric (EV) and Hybrid Electric Vehicles (HEV). Also linking ports up in a Multi-port DAB converter via multiport transformer allows for the integration of additional energy sources to the system. This converter can thus be employed in applications ranging from a front-end converter in points of common coupling at facilities, to a high power modular structure used on distribution system levels.

The motivation behind the thesis is to study the Dual-Active-Bridge bidirectional dc-dc converter topology, and validate its operation for a 2kW rated power setup. A starting approach for the design procedure, covered in this work, is to employ the converter as a unidirectional power flow converter, supplying a load that resembles the behavior of a typical micro-grid, such as a resistance in parallel with a DC link. Thus, the operation of the converter at rated power can be analyzed, studied and optimized. Towards this, hereafter are the milestone objectives that have defined the work.

First step is to analytically characterize the converter topology, by defining key equations that explains its operation, and checking the validity of the equations against simulations.

Second step covers the development of a control structure for the converter that fits the addressed application. The process targets zero steady state error, as well as fast stable ride-through during transient events, such as variation of voltage reference or load condition.

Next step, the third one, is the design and construction of an experimental platform to practically test the Dual-Active-Bridge converter for operation at rated power (2kW). The design process thus targets the major hardware and software elements allowing for a proper converter implementation.

Finally, the fourth and last step consists of testing the built converter for operation. This is done under a variety of power levels to define the converter behavior under wide operating conditions. Therefore, the procedure will test initially lower safe power levels, gradually increasing up to targeted nominal level. The steady state operation waveforms as well as the dynamic converter behaviors have been captured and analyzed against theoretical and simulated results in order to assess a performance validation. Some side analysis for dead time effect have also been practically experimented and introduced.

Thesis Supervisor: Jorge García García
Title: Associate Professor

Acknowledgements

I'm greatly thankful to my beloved mother and father, for being the reason and the motivation for my sought of success. Let my work be always for the honor of their names, as a little repay for their suffering and love in building me up.

For his dedication, and his precious gift of time and knowledge, I am forever thankful to my teacher and supervisor Prof. Jorge García. His recognition of my effort, and his faith in my learning capabilities have paved my way through the course of work. For the possibility he gave and the possibilities he yet opens in front of me, I dedicate this Master thesis to him.

For my twin sister Mariam, my colleague and my friend, for her presence, I express my gratitude. For showing me new aspects of myself, and believing in the good I can be, I'm thankful.

For the Master Degree coordinators, Prof. Pablo Arboleya, Prof. Jorge García, and Prof. Pablo García, for creating the Master idea, designing it with excellence as the main objective, and supporting it with collective expertise in each scientific aspect. For their constant struggle to make it all possible, I'm forever in debt to them. They inspire me with their unique fusion of scientific success and life enjoyment.

For being around through the work, and always creating motivation for an advanced work, I'm grateful to Prof. Pablo García. His valuable advice saved me much effort.

I'm deeply grateful to all my professors throughout the master course, they pulled us up with their experiences and speared no effort to pass us their knowledge. Each has put a brick under my feet that I couldn't have reached that high without.

I also thank my lab colleagues, Angel and Ramy for being there when I needed them, making the first days in the laboratory easier by passing their experiences.

Table of Contents

List of Figures

List of Tables

Chapter One

1. Introduction

1.1 Background

The modernization of electricity grid into the Smart Grid [1] [2] [3] concept, and its decentralization into many Micro-grids catering to clusters of loads, have increased reliability of electric energy supplies, as well as allowing for integration of greener electricity sources, such as wind, and photovoltaics. And wherever there exist renewable energy sources, Energy Storage Systems (ESS) are a need, basically to sustain the grid against fluctuations in energy generation from those non-scheduled sources, i.e. sun, wind, etc. The means to tie those ESS to the grid is thus challenging.

The inclusion of Power Electronic Converters (PEC) into the system is the first step, thus an intermediate processing of energy flow is allowed. Being a part of the smart grid, those PEC circuits are expected to provide functionalities such as: *low-voltage DC link*, *power-quality* related features; mainly power factor correction and reactive power compensation, and *smart protection* isolating load and grid side transients.

These demanded features cannot be fully fulfilled by a standard Low-Frequency Transformer (LFT), 50/60 Hz. The consequent development of the Solid-State-Transformer (SST) concept, being a High-Frequency (HF) transformer -tens of kHz and beyond-, as the core of an AC/AC PEC system, provides simultaneously galvanic isolation along with full power flow control.

This thesis addresses the design and construction of an isolated bi-directional SST structure for a Micro-grid application, where a voltage level of 500V, and a power level of 2kW are sought.

The undertaken topology is a Dual-Active-Bridge (DAB) converter. It is in principle, the basic definition for an SST system, consisting of two H-bridge inverters connected across an intermediate HF transformer.

1.2 Objectives

The central theme of the thesis is to characterize the DAB converter and validate its practical operation for the specified application. This study is expected to bring an optimization of the design, to solve any implementation issue that arises. The fundamental objectives guiding the work process can thus be listed to:

- Analysis of the DAB converter topology. The analysis should result in the basic expressions that characterize the converter operation, and allow for further implementation of the control structure.
- Develop a Closed Loop Control structure. The controller design is intended to allow for proper converter operation under the specific studied application.
- Simulations of the DAB converter operation within the studied application. This involves exploration of the studied concepts and control structure as a prior step to practical realization.
- Design of an experimental setup for assessing the studied converter design. The design comprises the construction of the power stage, the implementation in a digital controller of the control system developed, as well as the interface between the control and the power stage.
- Verification of the built prototype DAB converter performance. This includes the validation of the expected converter open-loop and closed-loop behaviors through matching with practical obtained results.

1.3 Thesis Structure

Towards the previously mentioned objectives, the thesis work was developed, and the structure is organized as follows:

Chapter1: Introduction

This present chapter introduces the motivation for the work carried out in this thesis. It points out the application targeted and the converter topology selected for this specific application. On this basis, the main objectives of the work were listed, followed by a summarized overview of the structure of the thesis in terms of chapters.

Chapter 2: Literature Review

This chapter reviews the research literature that is an allowing entrance for the work carried out in this thesis. Initially, the chapter provides the development history of the isolated bidirectional DC-DC converter specifically with a HF-Link. Secondly, a review of the modulation schemes is presented, pointing out advantages and drawbacks of each. And lastly, closed loop control system is explored, studying different targeted control parameters proposed through literature, the control loop structures, and the basic tuning of regulators.

Chapter 3: DAB Converter Modelling

This chapter presents a thorough analytical characterization of the DAB converter topology, depicting the figure expressions that explains the operation and allows for the

control of the converter. The chapter is thus finalized by an average model for the DAB converter.

Chapter 4: Closed Loop Control

This chapter designs the converter control loop, following three main steps; choice of target controlled parameter, choice of loop structure, and tuning of selected regulator. According to the application, the controller design is a compromise between reference tracking and disturbance rejection performances.

Chapter 5: Description of Simulation and System Design

This chapter is the allowing study for a practical construction of the DAB converter. It is consequently divided into two main topics; the conducted simulations of the converter, and the design of the system to attain a feasible implementation.

Chapter 6: Simulation and Experimental System Results

This chapter covers the practical implementation of the DAB converter. Therefore, it presents the results obtained from putting the converter into operation within the specified application. Interestingly, this chapter provides matching of simulated converter characteristic behavior with the analogous practical one.

Chapter 7: Conclusions and Outlook

This chapter indicates the conclusions reached out of the thesis work, and outlooks a future path for research in this field.

Chapter Two

2. Literature Review

To put the light on the Dual-Active-Bridge (DAB) converter situation within the research literature, a review is carried out in the present chapter. This review targets the Power Electronic Conversion systems specifically employing a High-Frequency (HF) Link.

The chapter is structured as follows.

First, the development history of the DAB converter is reviewed, focusing on the major system components. Under this aspect, the major candidate converters are pushed forward and compared, the Solid-State-Transformer (SST) concept is brought about, discussing its unprecedented functionalities and previously proposed structures. The development history is concluded by the application prospects of the SST system in general, and the DAB converter specifically.

Secondly, the modulation strategies proposed in literature are recalled, and their principles of operation are summarized contrasting their major advantages and drawbacks.

Thirdly, the research literature in closed loop control is consulted for previously proposed control structures for linear controllers, the previously targeted controlled parameters for an isolated bidirectional DC/DC converter, and the tuning of the typical PI regulators.

The review is then assessed in answer to the requirements of the application under study, and the insight gained is then applied to select the converter topology, the appropriate modulation scheme, and the target controlled parameter.

2.1 Topology Development History

The core circuit for the High-Frequency-Link (HFL) Power-Conversion-Systems (PCS) is the Isolated Bidirectional DC-DC Converter (IBDC). In principle, IBDC follows the generic structure depicted in Figure 1.

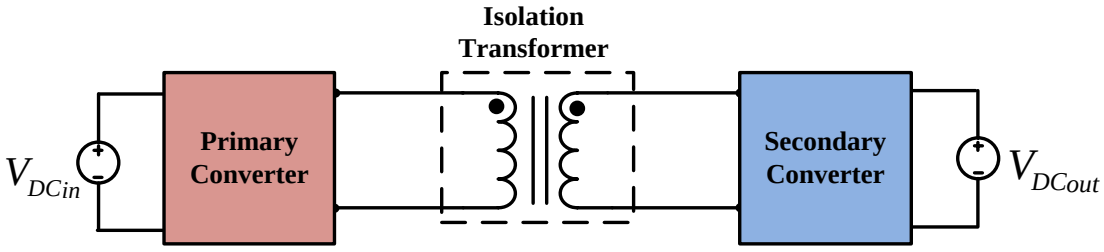


Figure 1: General Bi-directional DC-DC Converter Topology.

Bidirectional DC–DC converter topologies with a system configuration according to Figure 1 are called *Single-Stage Topologies* [4] [5].

This class of conversion system is essentially made up of:

a) ***Two switching converters***, the primary side converter which is a DC/AC converter that converts the incoming DC voltage to an AC one, which is applied to the intermediate transformer, and the secondary converter which is an AC/DC converter then rectifies the AC voltage providing DC power to the receiving port [6]. The symmetry of this structure allows the primary and secondary converters to swap roles without issue, allowing bi-directional power flow through the converter [7].

b) ***High frequency transformer***, which is an AC link that provides the necessary scaling, and further achieve electric isolation to enable high voltage and current transfer ratios. With high frequency, the magnetic components are allowed to be smaller, leading to reduction of converter size, which makes a high frequency transformer superior over low frequency one.

c) ***Reactive HF networks*** provide energy storage capability within the HF AC part and are used to modify the shapes of the switch current waveforms in order to achieve low switching losses [8] [9]. Even though, these parts are not necessarily required for a fully functional bidirectional DC–DC converter, they will always be present in practice due to the parasitic components of the HF transformer, i.e. stray and magnetizing inductances, parasitic capacitances.

2.1.1 Candidate Converters

The HFL two-port isolated topologies have been classified in many ways in literature, among these the classification of topologies by

- Number of switches [10], low switch count or higher switch count,

- Conversion stages [6], Single-Stage or Multi-Stage converters, or

- Converter-source type, voltage-source converters (VSC), current source converters (CSC), and Impedance source converters (ISC). Combining a CSC with a VSC might also be a solution as presented in [6].

Table 1 provides the major converters following the mentioned classifications.

Based on the summarized advantages and drawbacks of these classes of converters, this section discusses the candidate converter topologies which are seen to be the most convenient for the studied application.

	Single-Stage Topologies		
	Low-Switch Count	***Dual-Bridge Converters***	
		Two Voltage-Sourced Ports	***Voltage and Current-Sourced Port***
Examples	- Forward - Flyback - Forward-Flyback - Isolated Cuk	- Dual-Active half-Bridge (DAHB). - Dual Active Bridge (DAB), Single-Phase and Three-Phase. - Series Resonance Converters (SRC). - Series-Parallel Resonant Converter (SPRC), LLC configuration.	- Current-Sourced Push-Pull Converter - Full or half-bridge Voltage-Sourced + Full-bridge Current-Sourced - Parallel Resonant Converter (PRC). - Series-Parallel Resonant Converter (SPRC), LCC configuration.
Power Range	< 2 kW	>= 2kW	
Advantages	Simple circuit structures and low numbers of required switches.	- Achieve much more effective converter utilization. - Soft-switching Capabilities, thus low switching losses. - High Power Density Converter is Feasible.	- Ease of parallelization of converters since the converter represents a current source. - Lower current ripple at both converter ports.
Drawbacks	Ineffective transformer and switch utilizations.	- Problems of Saturation of HF transformer, and dead time effect in case of non-resonant converters. - Additional required power components in case of resonant converters.	- Limitations on switching states due to output inductor. - Higher converter complexity. - Additionally required power components, such as snubbers to avoid stresses in switches.

Table 1: Classification of Candidate Single-Stage Converter Topologies.

A) Dual-Active Bridge Converters

Bridge converters provide much flexibility in their applications. DAB converters are a powerful topology in isolated bidirectional DC-DC converters, known by many research studies as the core circuit for next generation of HFL PCS.

Dual-Active Half-Bridge (DAHB)

The DAHB converter consists of single-phase leg, i.e. half-bridge circuit, on each converter port, with a split capacitor as illustrated by Figure 2. The converter is advantageous in terms of reduced switch counts, however, their major disadvantage compared to the single and three-phase DAB converters is the size and cost of the input and output capacitors. Moreover, these capacitors sustain large ripple currents, as the full AC inductor current will flow through them during operation [11][12]. Therefore, as power and voltage levels rise, these capacitors become prohibitively bulky and expensive [11] [13].

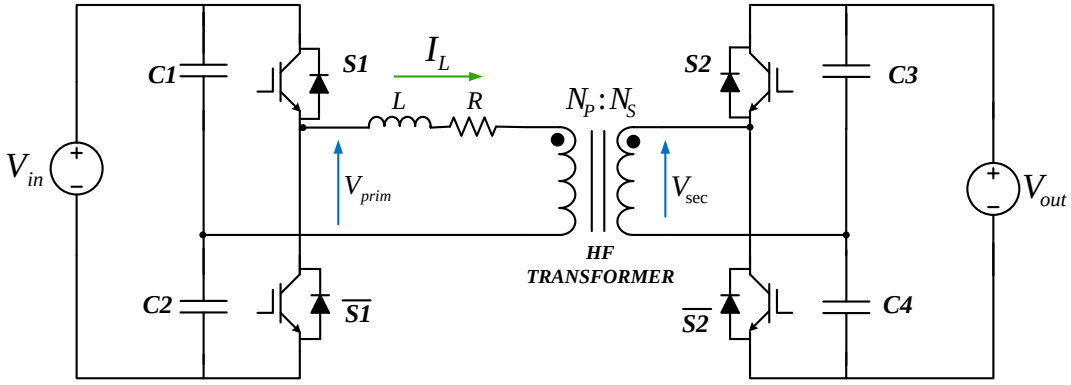


Figure 2: Dual-Half-Bridge Converter Topology with Split Capacitor.

Single-Phase and Three-Phase Dual-Active Full-Bridge (DAB)

The single-phase and three-phase structures consist of two or three single-phase legs, i.e. full-bridge circuit, respectively, on each converter port as illustrated by Figure 12 and Figure 3.

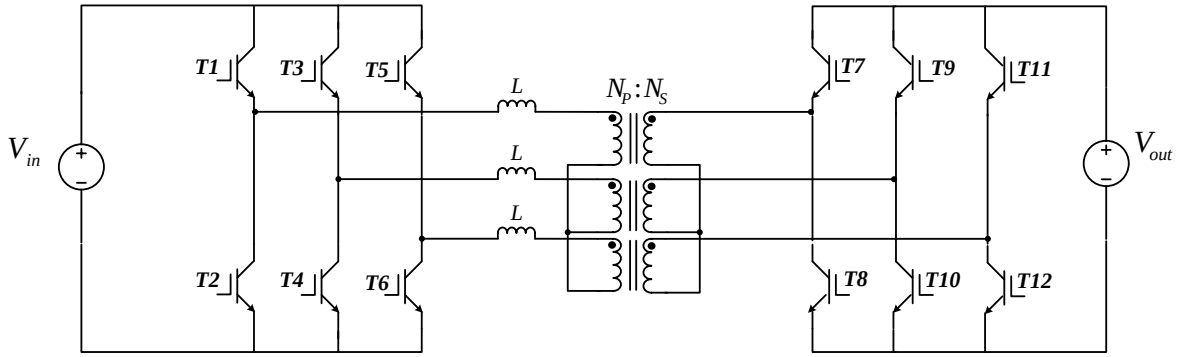


Figure 3: Three-Phase Dual-Active-Bridge.

In order to choose between these two alternative full-bridge structures, the benefits and drawbacks of each topology must be evaluated. [7] has used Fundamental AC circuit theory to compare the single-phase and the three-phase topology alternatives, and predicts significant advantages in favor of the three-phase bridge;

- AC total power flow in case of single-phase DAB requires large DC link capacitance to absorb oscillations in energy flow, which is not the case for three-phase DAB converter where the power flow is DC due to the 120 degrees phase-shift between phase legs [14] [15].

- In the case of three-phase DAB, the 120 degrees phase shift between phase legs also results in 120 degrees phase-shifted flux components that, for a balanced system, cancel each other allowing for a reduced transformer core material [15] [16].

- Reduced switch VA ratings for three-phase DAB, since the current is shared on more phase legs.

[6] also concluded that a very good overall performance can be achieved with the three-phase DAB. Moreover, publications such as [17] [19] have examined and evaluated these issues in detail. However, the conclusion is that the theoretical benefits of a three-phase structure presented above do not translate for practical converters;

- Firstly, the three-phase DAB requires high number of active components; 12 semiconductor switches and, accordingly, thus, while the lower peak current seen in three-phase converters reduces device current stress, any loss benefit is negated by the higher switch count [17] [19].

- Secondly, the practical realization of a three-phase symmetrical transformer with identical leakage inductances in each phase is a considerable difficulty.

- Thirdly, high conduction and switching losses result for certain operating points if the converter is operated within wide voltage and power ranges, due to the restrictions regarding the employed modulation scheme, thus, any potential size reduction benefits for the three-phase transformer are almost completely negated for thermal reasons, since the smaller core does not provide enough surface area to dissipate the heat generated by the magnetic/ohmic losses [20] [19].

B) Resonant DC-DC Converters

The most popular resonant converter topologies are the unidirectional series, parallel, and series-parallel resonant converters, a comparative study is presented in Table 2.

However, with a circuit modification, bidirectional power flow can be achieved [8] [9] [21] [22].

With these converters, nearly sinusoidal waveforms of the transformer currents result. Thus, low switching losses are feasible, which facilitates the use of a high switching frequency to obtain a high power density of the converter [9].

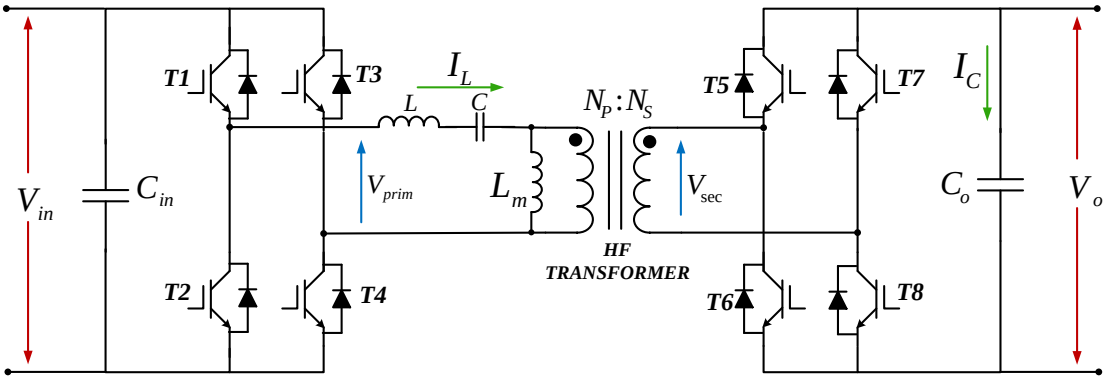


Figure 4: Bidirectional, series-parallel resonant *LLC* converter with two voltage sourced ports.

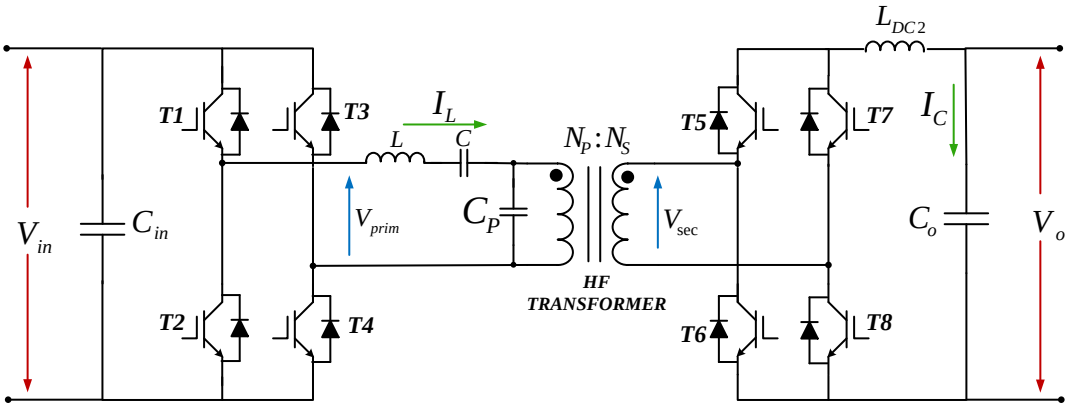


Figure 5: Bidirectional, series-parallel resonant *LCC* converter.

	Series Resonant (SRC)	*Parallel Resonant (PRC)*	*Series-Parallel Resonant (LCC and LLC)*
Advantages	The series resonant converter contains a capacitor in series with the transformer, thus blocking any DC voltage component, avoiding saturation of the transformer. The RMS currents in the switches and the resonance network are lower as load decreases. No restrictions for control can take place in case of bidirectional power flow as a result of the two voltage-sourced ports.	The output voltage can be controlled at no load. With the employed output DC inductor, the PRC is better suited for applications with low output voltages and high output currents than the SRC is.	The output voltage can be controlled at no load and the range of the required switching frequency is smaller than for the SRC. Compared to the PRC, considerably lower switch and transformer RMS currents can be achieved at low load conditions. For bidirectional LLC, no restrictions for control can take place as a result of the two voltage-sourced ports.
Disadvantages	Not convenient for wide operation voltage and power ranges, since the operation switching frequency strongly varies with depending on input voltage and load condition. In case of no load, the current tends to infinity. No galvanic Isolation can be added. High RMS Output currents in case of low output voltage applications, along with the voltage sourced output, render this converter unsuitable for this applications.	The currents through the switches and through the resonant network do not decrease with decreasing load. , which makes the converter less suitable for applications with wide voltage and power operation ranges.	For the LCC converter, there are limited allowable switching states on LV full-bridge, due to the output inductor, and the magnetizing capacitor, which can be overcome by using the quadrant switch arrangement mentioned in [krismer], however it brings about additional hardware effort.

Table 2: Series, Parallel, and Series-Parallel Resonant Converters in terms of Advantages and Disadvantages.

2.1.2. Solid State Transformer (SST)

Reference [23] first introduced the concept of a high-frequency AC/AC link, termed as electronic transformer. Since then, the concept has been developed significantly [24] [25] [26]. The recent paper [27] reviewed the applications of the SST, and presented the state-of-the-art. The generic SST structure is illustrated in Figure 6.

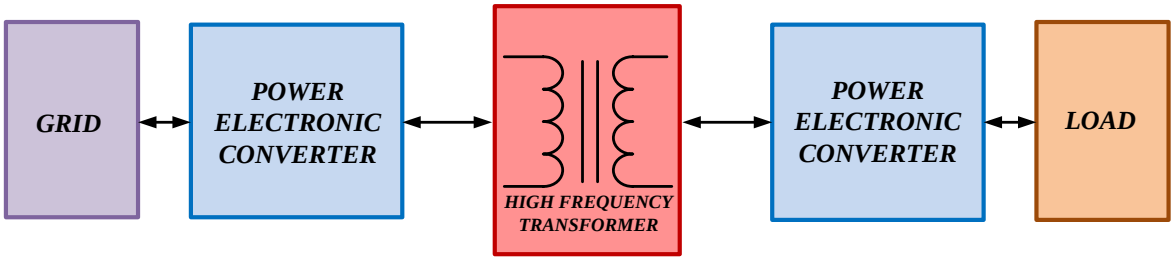


Figure 6: Generic SST Structure.

This section thus presents some of the functionalities of SST structure that motivates for its use, along with a discussion of the arrangement of power electronics conversion stages in an SST structure which allows for selecting the topology of convenience for SST implementation within the specific studied application.

A) SST Functionalities

Some of the features of SST are summarized below;

- Size and weight reduction due to high frequency transformer.
- Galvanic isolation
- Enables the direct connection of power electronic converters to MV networks while realizing the task of isolation and voltage adaptation, e.g. within an isolated DC/DC converter.
- The availability of power electronic circuits on the front and load end of the system allows a complete control of the power flow, enabling a transfer of energy with high power-quality level.
- Provides the links for the integration of distributed energy resources, distributed energy storage, and intelligent loads [25].
- On-demand support to the grid, such as reactive power support, power quality, current limiting, storage management and a DC bus.
- Availability of a LV-DC port, adding numerous features, as including connection to an energy storage system, thus enabling operation as a Uninterrupted-Power-Supply (UPS), direct connection of Photo-Voltaic (PV) arrays [28] or implementation of future local DC-grids [29], among others.

Such features cannot be covered using a passive low frequency transformer (LFT). A comparative study performed by [27] concluded that a straightforward solution represented by a LFT coupled to a rectifier-inverter stage, the SST offers a significant

improvement in power density and efficiency with a comparable cost level, rendering this solution very attractive for Smart-Grid applications.

B) SST Structures

Approaches introduced in [30] [1] [25] have distinguished SST structures using stage-based classification according to specific needs. Authors in [27] have also described previously reported SST concepts and their respective classification concerning different modularization criteria.

The topology comparison performed in [25] undertook some of the potential topologies that provide the bidirectional power flow requirement, and compared for the most appropriate topology to implement SST in an energy storage application for grid support to provide functionalities such as on-demand reactive power support, voltage regulation, and current limiting. The application typically represents a 100-150kW power level. The concluded topology is the three-stage SST, which is the final step in modularization of the SST in the power flow direction, where independent rectification, DC-DC conversion and inversion stages are utilized.

The selected three-stage approach is based on a DC-DC DAB, as shown in Figure 7, which in that case provides all the desired SST functionalities while simplifying the control design.

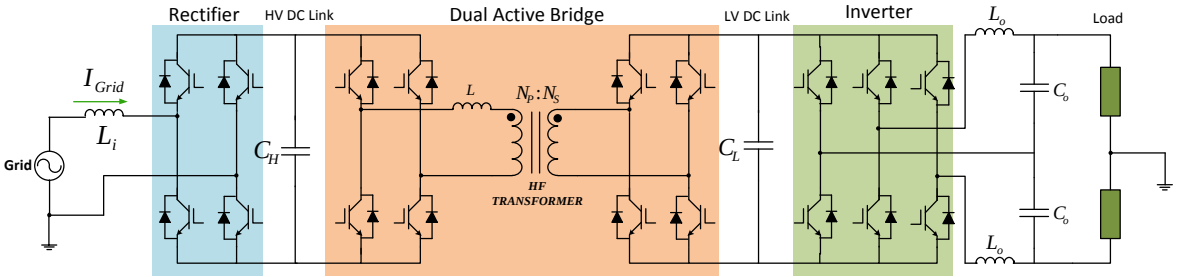


Figure 7: Three-stage SST Structure.

For higher power levels, multilevel converters are deployed, also modular structures have been proposed by Marquadt et al. in [31], and are typically used for High-voltage DC link.

However, this increase in functionality must be weighed against the increased losses due to the introduction of new conversion stages into the supply chain.

In case of space constrained applications, where a high power-density level is mandatory, the reduction in losses achieved by the operation of the transformer with MF results in an overall system loss reduction. In Smart-Grid applications, where the space limitation is not as critical as in e.g. traction applications, the introduction of additional conversion stages of the SST results in an increase in overall losses with respect to the state-of-the-art LFT transformer-based system [27].

For the application studied in this context, the SST topology is deployed for feeding a Smart Grid load, such as a resistive load or an inverter, a power level of 3kW is sought. As an initial approach system characterization should be carried out at low power level, which is most convenient using a single-stage direct AC-AC conversion SST structure. However, in a later stage an auto-transformer will allow an increased input supply voltage, which implies a rectifier stage at the input to provide the DC voltage required by the primary converter port.

2.1.3. DAB Converter and Applications

From the review, a single-phase single-stage DAB converter is the topology of most convenience for the studied application. The topology was first introduced in the early 1990's by *Rik W. A. A. De Doncker et al.* in a paper [18], a few months before which a patent was released [32]. The early publications [33] [4] [34] [35] [36] characterized the topology and tried to develop it. However, the performance limitations of power switches at that time rendered the topology out of attention. With the advances in new power devices and magnetic materials, the DAB has been recalled again as a feasible topology to replace LFT [37] [38].

The converter has thus been proposed and studied for different applications, below is a summary of some.

2.1.3.1. Automotive Applications

The most promising vehicle technologies with respect to an effective reduction in fuel consumption are hybrid electric vehicles, electric vehicles, and fuel cell vehicles [39]. DAB application for automobiles has been discussed in [40] [41].

2.1.3.2. Renewable Power Systems

DAB converters represent an SST structure, which, among other features, provide access to a LV DC link, thus can be considered as the core circuit interfacing an ac power system with a renewable power source [42] - [46].

2.1.3.3. Uninterruptable power Supply

The DAB dc-dc converter has been used in battery-application systems, such as uninterruptible power supplies (UPS), battery energy storage systems (BESS) [47] [48], and auxiliary power supplies for electric vehicles or hybrid electrical vehicles. For instance, an off- line UPS design based on the DAB topology is investigated in [49].

2.1.3.4. Multi-port Systems

Linking ports up in a multiple port DAB converter via multiport transformer allows for the integration of additional energy sources. The concept of the three-port DAB converter is discussed in [50] - [56]. The energy is exchanged from and to all ports, with the transformer providing isolation among all ports.

2.1.3.5. Traction and Smart-Grid System

Traction and subsea systems are applications where space is critical; any reduction in weight and volume of the system directly boosts its performance [27].

For Smart Grid Concept, an efficient, flexible flow of electric power is required, effectively integrating renewable energy sources and powering loads of DC and AC nature. On this basis, power quality issues, such as reactive power compensation, active filtering and grid-side/load-side protections are necessary. For a standard LFT based system, an independent power electronic system is implemented for each of the integrated source or load, thus the previously mentioned tasks are distributed among several power electronic converter systems, which requires precise coordination. However, an SST incorporating a central rectification stage and a DC-DC converter represents an attractive solution [27].

2.2.Modulation

Basically, all modulation schemes aim at creating a train of switched pulses. Two key modulation schemes have been applied in literature to isolated bidirectional DC/DC converters, Pulse Width Modulation (PWM), and Block Modulation [11] [12] [18]. This section presents a basic overview of the strategies, their advantages and drawbacks, from the point of view of an H-bridge converter.

2.2.1. PWM Modulation

The technique provides high frequency switching pulse train whose widths vary more slowly to give a Low Frequency average (fundamental) output AC waveform. The PWM schemes range from Naturally Sampled and Regular Sampled PWM through to Discontinuous Modulation schemes, to Space Vector modulation strategies [12]. Figure 8 illustrates the operation of a Naturally Sampled sine-triangle PWM modulator.

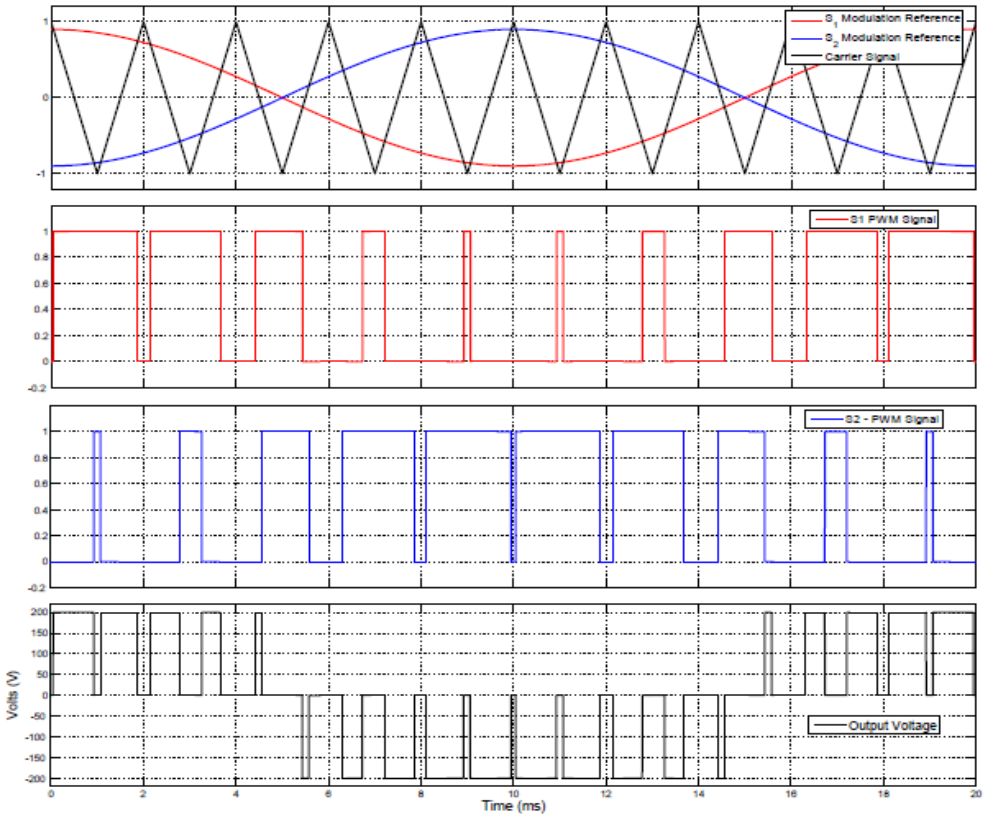


Figure 8: PWM Modulation [7].

- *Advantages*

This strategy is popular in power electronics because the output AC waveform has very low levels of distortion. This is because PWM ensures that the bulk of the waveform energy is transferred at the frequency of the fundamental harmonic.

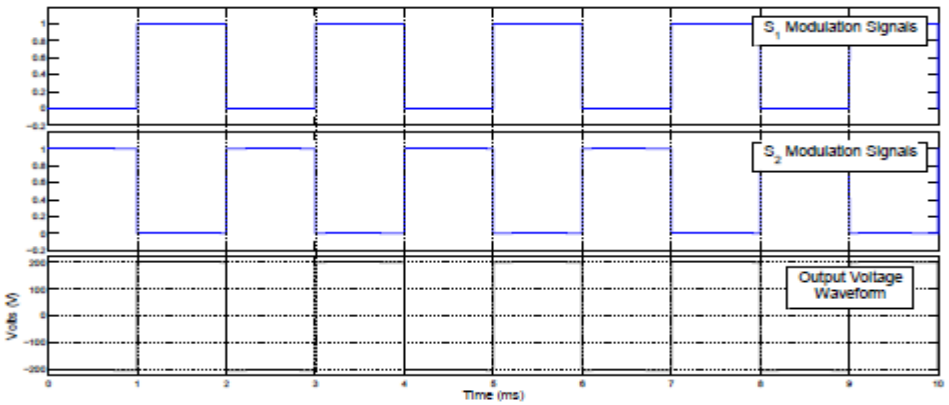
- *Drawbacks*

The relatively low frequency of energy transfer leads to bulky magnetic components [11] [16].

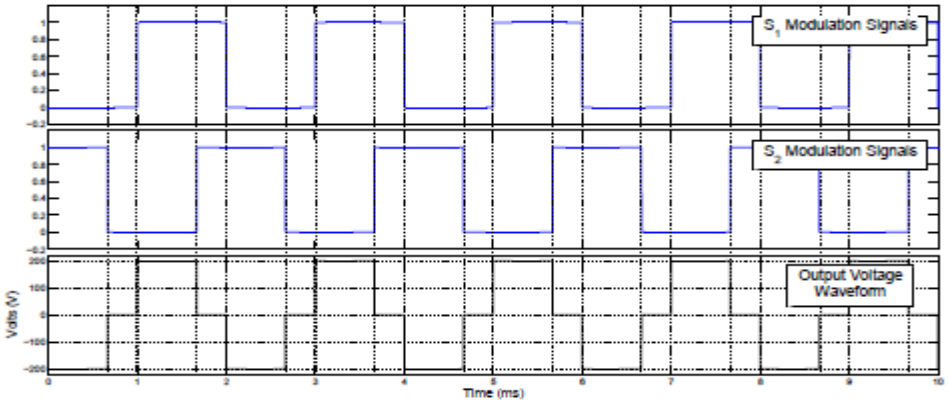
2.2.2. Block Modulation

The technique provides high frequency switching pulse train whose widths are constant. The technique is based on modulating each bridge leg with square waves, thus a resulting AC voltage waveform at the bridge terminals.

Fixing the duty ratio to 50% while phase shifting both legs by 180 degrees, a two-level modulation scheme is generated, however, phase shifting one leg from the other, a three-level modulation scheme results. Figure 9 illustrates these two cases.



(a) Two-level Modulation



(b) Three-level Modulation

Figure 9: Block Modulation – Two-Level and Three-Level Strategies [7].

- *Advantages*

Instead of the low frequency average output as it is the case of PWM schemes, in block modulation, the waveform energy is transferred at higher frequencies, defined as the switching frequency and its higher order harmonics [12]. This allows for reduction of size and weight of magnetic components, i.e. inductors and transformers, as identified in [57] - [62], [19] [33].

Moreover, the block modulation can also give a faster dynamic response, as suggested by [12] [63] [20] [64], because the flow of energy can be changed and varied more quickly.

- *Drawbacks*

When this modulation is applied as the only control strategy for a DAB converter, known also as "Single Phase Shift" or SPS Control, it imposes limitations in converter operation; when the magnitudes of voltages across the high frequency transformer are not matched, this leads to high circulating currents. Also in this situation, the converter cannot be operated in a soft switching manner over the whole operation range.

2.2.3. Soft Switching

One of the major loss mechanisms in a power electronic converter is the switching losses, which scales up with the increase of switching frequency. With the modern semiconductor materials, such as Silicon carbide, capable of providing higher switching frequencies, thus possibility of dramatic reduction of converter size, it is a necessity then to allow for the use of these ranges of frequencies by deploying soft switching techniques. This research subject, specifically for a DAB converter, has been increasingly attracting attention recently. One of the earliest views of this idea was proposed by Divan et al. in [65] to minimize the switching losses. Two main soft switching modes were introduced by this study; Zero Voltage Switching (ZVS), and Zero Current Switching (ZCS). The concept of ZVS is discussed in [66].

- *Advantages*

As higher switching frequencies is the key to the reduction of transformer and magnetic components size, to allow for realization of extremely high power-density converter, a form of zero-switching loss converter must be reached [18]. As the difference between the voltage magnitudes at the transformer sides increases, transformer RMS currents, the inductor and transformer copper losses, and the semiconductor conduction losses increase considerably, dropping the efficiency of the converter [67].

- *Drawbacks*

Converters suffer a limited soft-switching range depending on load conditions, which in turn leads to narrowing the converter operation range making it less flexible in applications [7]. Although many attempts to extend this range have been proposed [18] [68], the feasibility of solutions is reduced at higher levels of power [18].

2.2.4. Conclusion of Modulation

For a higher power converter, the phase shift square wave block modulation is more attractive in terms of reduced size and weight of magnetic components. Also its fast dynamic response makes it appealing for these kinds of applications. From the schemes of the square-modulation presented, the two-level modulation scheme is more convenient for Smart Grid applications more than its counter schemes, since, for a known point of operation, it is capable of achieving the maximum power transfer [18].

Hard-switching is also favored than soft-switching, recognizing that the switching frequency of operation targeted in this context is medium frequency of 20kHz, thus a comparable converter performance can be achieved, thus sparing the resources in terms of cheap implementation and less complexity of system design.

2.3. Closed Loop Control

Closed loop controller follows the principle of feedback, illustrated in Figure 10.

This feedback controller structure is made up of a plant, G, that needs to be controlled, and a controller, C. The plant output, y, is compared to its target reference value, r, and the difference between them, ε, is fed into the controller. The controller then adjusts the control signal u, such that the plant output achieves its target value [69].

For this literature review, only the linear controllers will be considered. The design of a linear controller follows the next procedure:

1. Choice of Target Controlled Parameter.
2. Control Loop Structure.
3. Controller Design.

2.3.1. Target Controlled Parameter

The literature proposed some typical controlled parameters for control of Isolated Bidirectional DC/DC Converters, summarized as follows [7].

2.3.1.1 Input Power (Pin)

Tao et al. [70] [71] proposes a Triple Active Bridge converter powered by a Fuel Cell. Input power regulation is then used to minimize the dynamic stress on the Fuel Cell, as these devices are unable to change their power output quickly.

2.3.1.2 Input Current (Iin)

Haihua et al. [72] presented the use of several parallel connected DAB converters sourced from the same ultra-capacitor. Input current control is used to ensure sharing between the converters.

2.3.1.3 Output Current (Iout)

Output current control is proposed in Kunrong et al. [73] to allow a DAB converter to safely and effectively charge a battery load.

2.3.1.4 AC Inductor Current (IL)

Demetriades et al. [70] and Lei et al. [119] propose controlling the intermediate AC inductor current in a DAB converter to provide inherent current limiting as part of a dual loop controller.

2.3.1.5 Output Voltage (Vout)

Output voltage control is very effective in managing the most popular load scenarios for isolated bi-directional DC-DC converters, which are resistive loads and AC inverter

loads [62] [74] [75] [76]. It is therefore the most popular control variable used in the literature.

It is noteworthy to mention here that the converter might be exposed to saturation of HF transformer, unless the controlled parameter is the AC inductor current, thus assuring a certain fixed current flow, avoiding any DC magnetic flux component that may appear, and builds up causing transformer saturation [77], as will be discussed later in detail the context of magnetic core saturation.

The choice of the controlled parameter is, therefore, basically dependent upon the application.

2.3.2. Control Loop Structure

Single-Loop

Figure 10 shows the single-loop controller structure. This is the simplest control loop. It comprises only one controller regulating the output of a single plant. Consequently, a single sensor is required for the feedback of the controlled quantity. Literatures [78] [79] [76] have adopted the single-loop structure for regulating the converter output voltage.

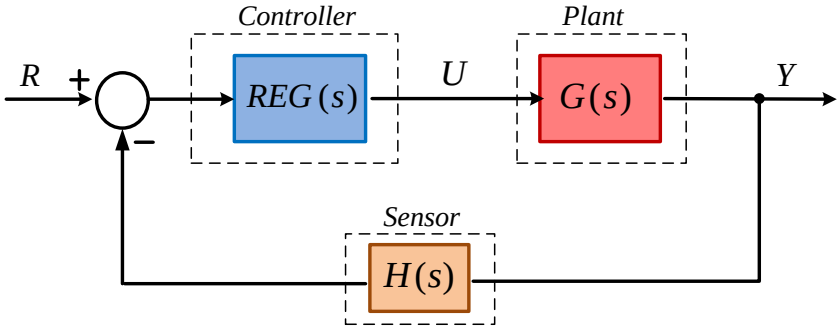


Figure 10: Single-Loop Controller Structure.

Cascaded-Loop

Figure 11 shows the cascaded-loop controller structure. The loop is made of an outer controller which provides the reference for an inner controller [7]. To minimize the interaction between the two loops, the outer controller band width is set to be a number of times less than that of the inner controller´s. This assures that the response of the inner controller is seen as nearly instantaneous from the point of view of the outer one, thus avoiding instability at the cost of a slower overall system response.

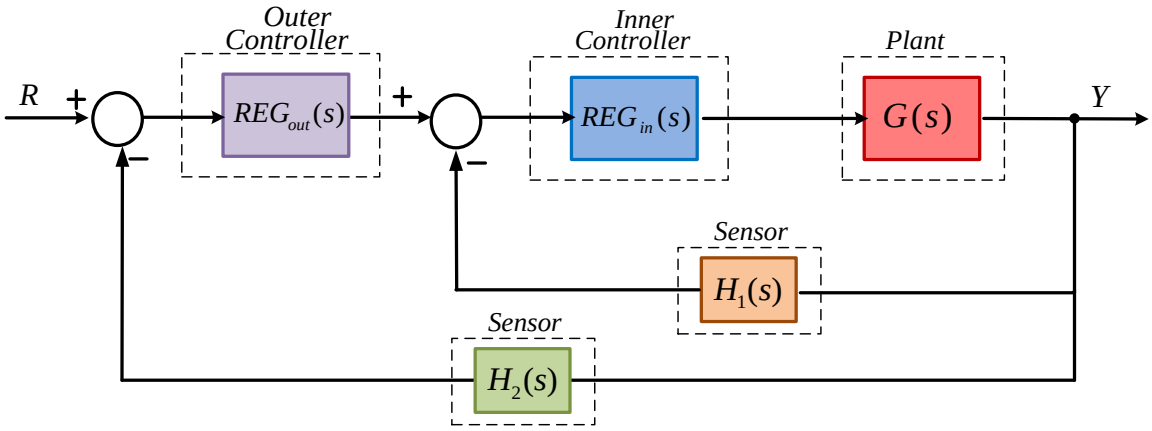


Figure 11 Cascaded-Loop Controller Structure.

2.3.3. Controller Design

The transfer function of a PI controller is given as [69]:

$$PI(s) = K_p.\left(1 + \frac{1}{T_i.s}\right) \tag{3}$$

where K_p is the proportional gain, and T_i is the integrator time constant.

K_p determines the controller speed, and is typically selected based on the desired bandwidth and the plant nature. While T_i is responsible for assuring the steady state error is zero, and is typically selected based on zero-pole cancelation technique. The technique aims at defining the system pole, and adjusting the zero offered by the integrator to cancel this pole.

This concept will be used for the design of the controller implemented for the study, thus transfer functions will be discussed in detail, Section 4.2, for the specific controlled plant.

2.4.Conclusions

This chapter has reviewed some of the candidate DC/DC Isolated bidirectional converter topologies used for bidirectional power flow, discussed their different modulation schemes, and the closed loop control structure and design.

Since the converter topology is sought for a Smart Grid application, where usually the typical voltage requirements is above 200V, and in the range of kilowatts, thus this review suggests a full-bridge converter for those applications.

A single-phase is also more appropriate in this case than a three-phase, since it offers reduced number of components; semiconductor switches, transformers, and inductors. Moreover, according to the study carried out in [6] the average expected efficiency of a three-phase DAB converter, in particular, is less than that of a single-phase DAB.

The Modulation Scheme suggested for such application is the hard-switching, two-level block modulation, since it transfers power at high frequency, thus allowing for reduction of magnetic components size. Thus at this stage of converter realization, a single phase shift, known as Phase-Shift Modulation, is employed for power transfer. A soft switching technique becomes more appealing as the difference between the voltage magnitudes at both transformer sides is larger.

Regarding the control strategy, the output voltage control is the most appropriate for tackling typical Smart Grid load scenarios such as resistive loads, or inverters. Moreover, at this stage of converter realization and basic characterization, a current control imposes an unjustified complexity on the control implementation, since it requires accurate measurement of the current, which is not a simple issue since the shape of the current waveform depends on the phase shift employed between bridges. Since the applications implies that the DAB converter has only one output, which is the voltage, and only one controllable input, which is the phase shift between bridges, thus a single-loop controller structure is the most appropriate for this case.

Chapter Three

3. DAB Converter Modeling

Through the literature review, presented in Chapter 2, it has been concluded that the most appropriate DC/DC converter topology for Smart Grid application is the single-phase DAB converter. A comprehensive study of the converter behavior is thus a first step to characterize its behavior and allows for its closed loop control.

This chapter thus provides the analytical study of the DAB converter, and is constructed as follows.

First, the principles of operation of the converter under two-level modulation is presented, in terms of characteristic converter waveforms and derivation of key time domain equations. Based on these equations, the analytical power flow expression, as well as the consequent output current one, is reached on an average basis.

Lastly, the average model of the converter is derived making use of the averaged equations, and validated using simulation results.

Then, a study is conducted for the alternative PWM schemes for modulating the DAB converter, discussing the main features of each that can be of interest for the specific application of this study.

To clarify the ideas presented, the chapter is also fortified with selected simulation results, whose main parameters are shown in Table 3. Two main power levels are undertaken for the study of the DAB converter, and later for the experimental validation of the constructed setup.

Table 3: Converter Simulation Parameters.

CIRCUIT PARAMETER	VALUE	
DC Link Capacitance	$1000\mu F$	
Switching Frequency	$20kHz$	
Dead time	$2\mu s$	
Transformer Turns-ratio (N_p/N_s)	$22:18$	
	AT LOW POWER	AT MAXIMUM POWER
Power Level	$50W$ - $300W$	$2kW$
DC Input Voltage	$60V$ - $200V$	$500V$
DC Output Voltage	$56V$ - $160V$	$350V$
Power Transfer Inductor	$600\mu H$, 1.397Ω	$600\mu H$, 0.166Ω
Load	76Ω - 100Ω	150Ω

3.1. Basic Characterization of DAB Converter

The section analyses the steady-state behavior of the DAB converter, deriving the expressions characterizing the topology [80].

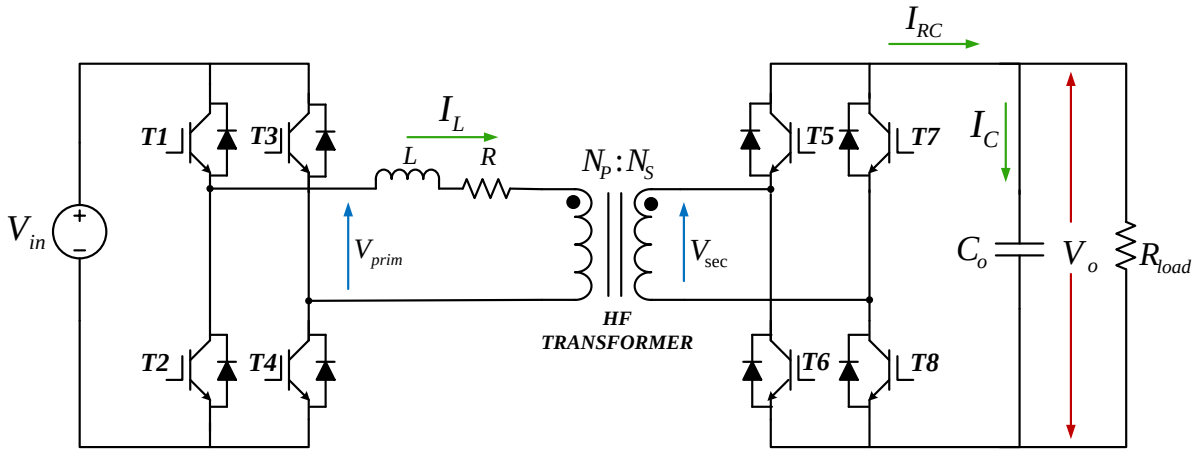


Figure 12: Dual-Active-Bridge Converter Topology.

The structure of the DAB converter is shown in Figure 12. The converter is composed of two full-bridge circuits connected across a power transfer inductor and a high frequency (HF) transformer. For achieving power transfer, the square-wave time varying voltages, V_{prim} and V_{sec}, must be provided by the full-bridges across the AC link, comprising the

inductor and the HF transformer. Then, the two full-bridges can be substituted by the corresponding voltage sources, V_1 and V_2. To keep simplicity, the study of converter principles is carried out under the following assumptions

1. All losses are neglected
2. Constant supply voltages, V_{in} and V_o, are considered.
3. The secondary side quantities are referred to the primary side.

The equivalent simple model that explains the converter operation can be seen in Figure 13.

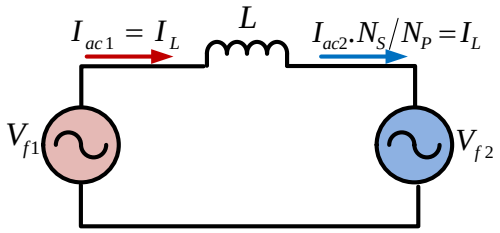


Figure 13: Dual-Active-Bridge Equivalent Model [6].

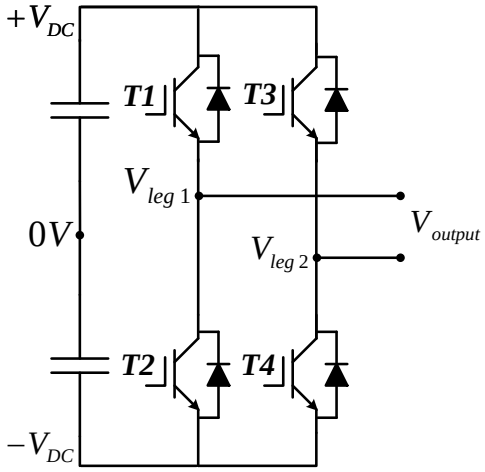


Figure 14: Simple H-Bridge Inverter Topology [7].

With an H-bridge circuit topology, as shown in Figure 14, three voltage levels are available for the output of primary or secondary bridges depending on the DC voltage levels of the input and output voltage sources respectively.

The voltage source representing the input bridge, hence, is defined by the four states

$$V_1(t) = \begin{cases} +V_{in} & \rightarrow \quad stateI \\ 0 & \rightarrow \quad stateII \ \& \ stateIII \\ -V_{in} & \rightarrow \quad stateIV \end{cases} \tag{1}$$

These states correspond to the full-bridge switches´ states clarified by Table III.

Table 4: States of an H-Bridge

State	S_1	S_2	V_{leg1}	V_{leg2}	V_{output}
II	0	0	$-V_{in}/2$	$-V_{in}/2$	0
IV	0	1	$-V_{in}/2$	$+V_{in}/2$	$-V_{in}$
I	1	0	$+V_{in}/2$	$-V_{in}/2$	$+V_{in}$
III	1	1	$+V_{in}/2$	$+V_{in}/2$	0

Similarly, the voltage source representing the output bridge, is defined by the same procedure, however, including the transformer turns-ratio for reference

$$V_2(t) = \begin{cases} +V_{out}.\dfrac{N_p}{N_s} & \rightarrow \quad stateI \\ 0 & \rightarrow \quad stateII \ \& \ stateIII \\ -V_{out}.\dfrac{N_p}{N_s} & \rightarrow \quad stateIV \end{cases} \tag{2}$$

These two phase shifted voltage waveforms, $V_1(t)$ and $V_2(t)$, generate a non-zero net voltage, $V_L(t)$, across the inductor

$$V_L(t) = V_1(t) - V_2(t) \tag{3}$$

This voltage applied to the power transfer inductor generates a current, I_L,

$$I_L(t_1) = I_L(t_0) + \frac{1}{L}.\int_{t_0}^{t_1} V_L(t).dt \tag{4}$$

at the time t_1, starting with an initial current $I_L(t_0)$ at time t_0.

The voltage sources, $V_1(t)$ and $V_2(t)$, thus generate or receive the respective instantaneous powers

$$P_1(t) = V_1(t).I_L(t) \text{ and } P_2(t) = V_2(t).I_L(t) \tag{5}$$

The average power over one switching cycle T_s, where $T_s = 1/f_s$, is finally calculated with

$$P_1 = \frac{1}{T_s}.\int_{t_0}^{t_0+T_s} p_1(t).dt \tag{6}$$

for the primary side, and

$$P_2 = \frac{1}{T_s} \cdot \int_{t_0}^{t_0+T_s} p_2(t).dt \tag{7}$$

for the secondary side.

Since the DAB model is lossless, thus

$$P_1 = P_2 \tag{8}$$

The power level of the DAB converter is thus typically adjusted using one or more out of four control parameters:

- The phase shift, θ, between the AC voltages, $V_1(t)$ and $V_2(t)$.

$$-\frac{\pi}{2} \le \theta \le +\frac{\pi}{2}$$

- The phase shift between legs of primary bridge, θ_P, or between legs of secondary bridge, θ_S [81].
- The duty cycle of AC voltage at primary bridge, D_1, or of AC voltage at secondary bridge, D_2,

$$0 < D_1, D_2 < \frac{1}{2}$$

- The switching frequency, f_S.

3.1.1.Phase Shift Modulation

The Phase Shift Modulation, also referred to as Single Phase Shift (SPS) Control, operates the DAB converter at constant switching frequency, with maximum duty cycles $D_1 = D_2 = 0.5$, it varies only the phase shift, θ, between the primary and secondary bridges to control the transferred power. With this control signals, the square-wave voltage, $V_1(t)$, at the primary bridge has two levels $\pm V_{in}$. And in a similar way, the square-wave voltage, $V_2(t)$, at the secondary bridge has two levels $\pm V_o . N_P / N_S$ .During steady-state operation, the voltages $V_1(t)$ and $V_2(t)$, and the inductor current repeat every half-cycle with reversed signs.

The firing pulses to a single bridge leg are a pair of a 50% duty cycle square wave signals that are offset 180° from each other, as shown in Figure 15.

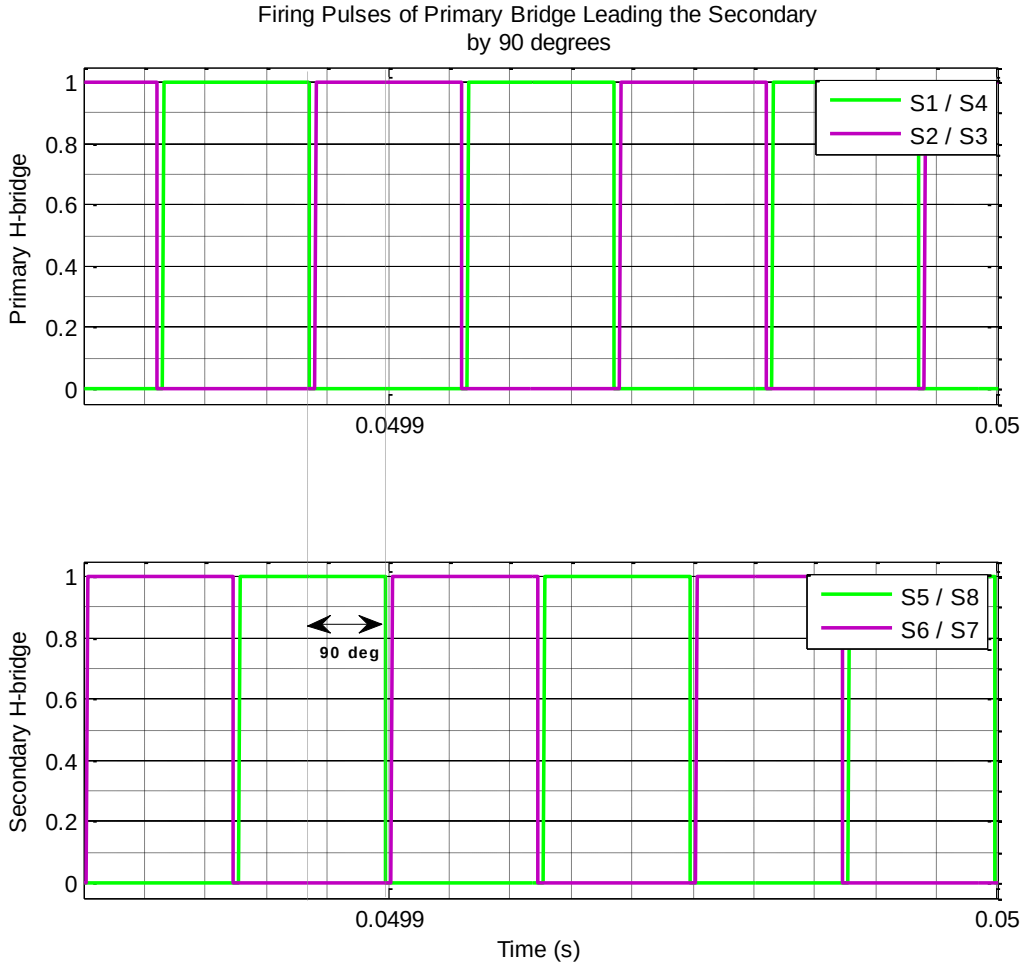


Figure 15: Phase Shift Modulation – The Primary Bridge and secondary Bridge Firing pulses Shifted by 90 Degrees.

Applying this modulation pulses to the primary and secondary bridges, with 90° phase shift between firing pulses, two AC square-voltage waveforms are generated at the outputs of each bridge, as shown in Figure 16 [80].

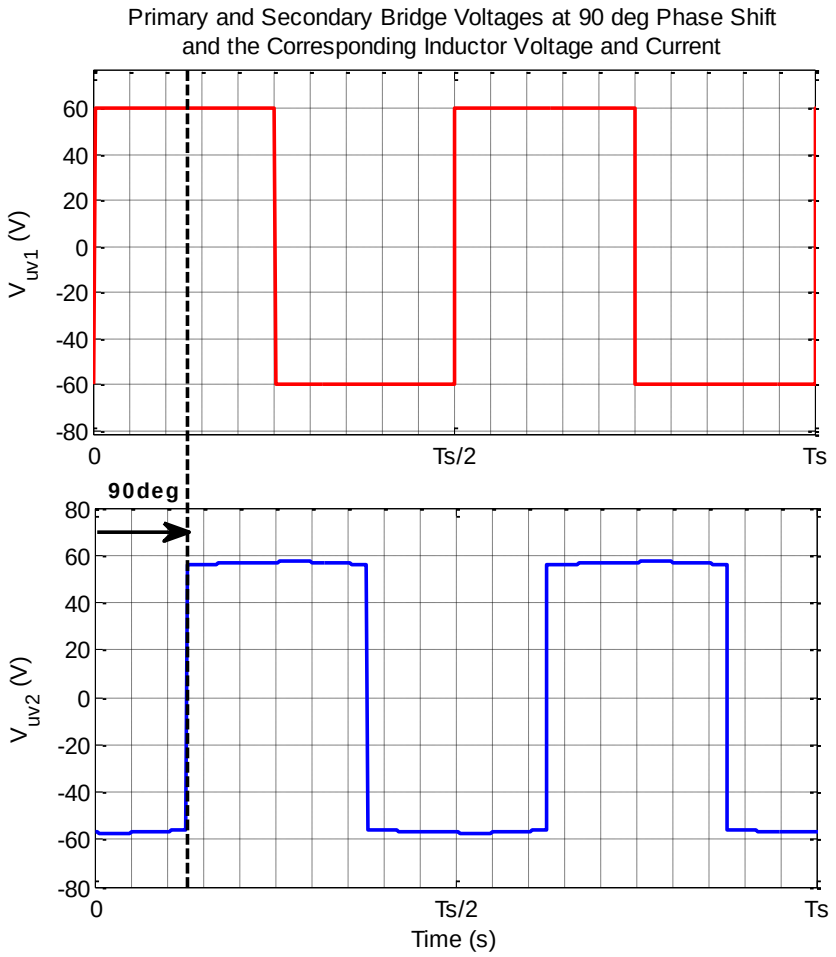


Figure 16: AC Output Voltage Waveforms at the Primary and Secondary Bridges.

As can be noted, the average values of $V_1(t)$ and $V_2(t)$ at steady state operation is zero, to avoid saturation of the transformer. These two phase shifted voltage waveforms, generate a non-zero net voltage, $V_L(t)$, across the inductor, resulting in a current I_L flowing through it. Figure 17 illustrates the converter characteristic waveforms. The waveforms clarify the equations discussed in the previous section, and validate them.

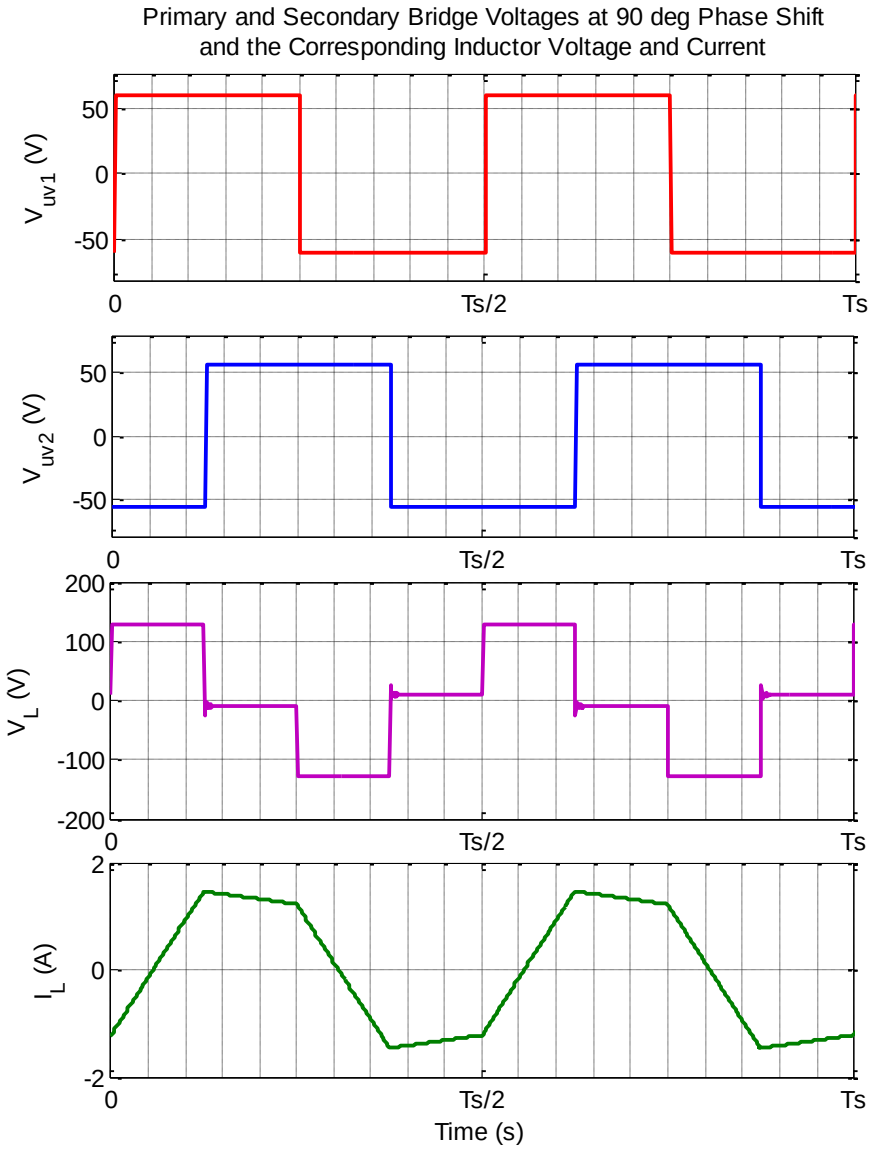
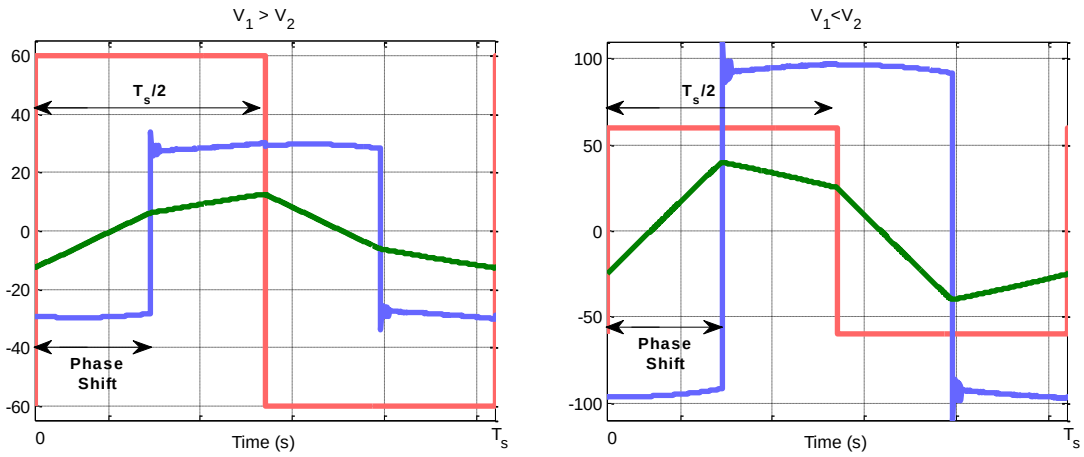


Figure 17: Dual-Active-Bridge Converter Operation Waveforms – AC Voltages at the output of Primary and Secondary Bridges Respectively, Voltage across the Inductor, and the Current through it.

3.1.1.1. DAB Inductor Current and Transferred Power

The shape of the inductor current depends on the magnitudes of the voltages across its terminals, $V_1(t)$ and $V_2(t)$, thus two main cases, Buck $V_1 > V_2$ or Boost $V_1 < V_2$, as clarified by Figure 18.



(a) (b)

Figure 18: Inductor Current Waveform – Two Operation Conditions: Boost State and Buck State.

Since the phase shift time, t_θ, and the DC supply voltages, V_{in} and V_{out}, remain the same during the first half-cycle, time intervals I, II, and during the second half-cycle, time intervals III, IV, as indicated in Figure 19, therefore, for the calculation of the transferred power, only the first half-cycle, intervals I and II, needs to be considered.

At $t_0 = 0$, Eq. (10) becomes

$$P_1 = \frac{1}{T_s}.\int_0^{T_s} p_1(t).dt = \frac{2}{T_s}.\int_0^{T_s/2} V_1(t).I_L(t)dt \tag{9}$$

Thus, in order to obtain an analytical expression for P_1, the current, $I_L(t)$, needs to be defined. During steady-state operation, a certain current, $I_{init} = I_L(t_0)$, is assumed.

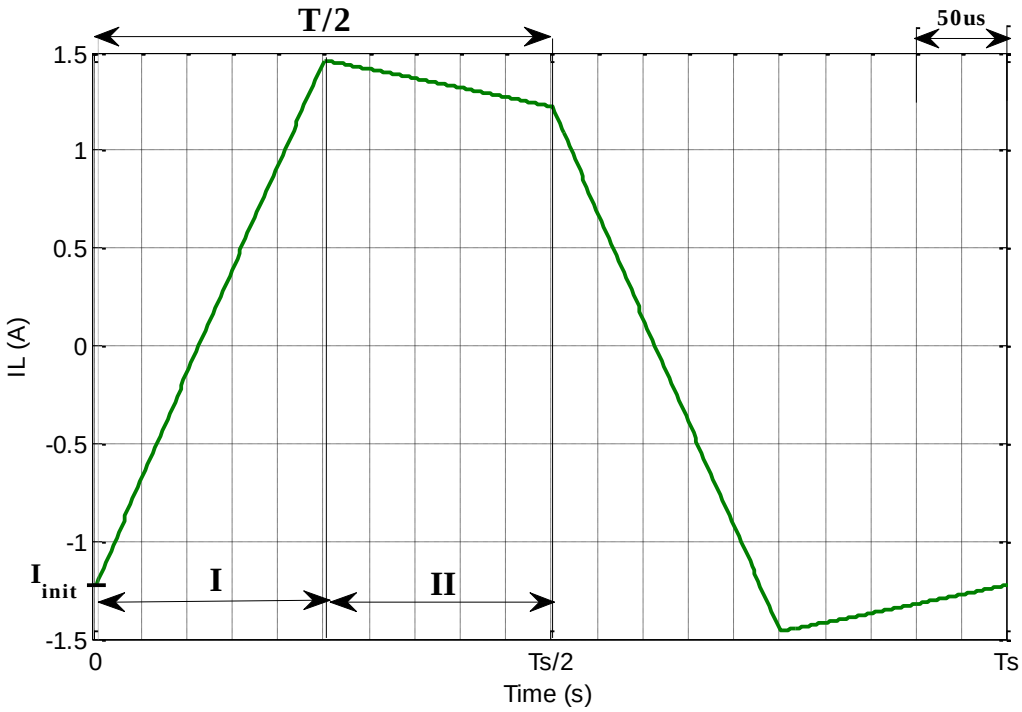


Figure 19: DAB Inductor Current resulting from Phase Shift modulation at Boost State.
Vin= 60V

The two different intervals, I and II, occur during $0 < t < T_S/2$. The inductor current expression is calculated for positive and negative phase shift angles, i.e. through the full phase shift range $-\pi/2 < \theta < \pi/2$, thus resulting in a power expression comprising both flow directions.

Power Flow in Forward Direction

First, on the assumption of positive phase shift, $0 < \theta < \pi/2$, the power is transferred from the leading H-bridge, i.e. primary, to the lagging H-bridge, i.e. secondary, the current expressions for the half cycle $0 < t < T_S/2$ are

$$i_L(t)\Big|_{0<t<\frac{T_s}{2}} = \begin{cases} \left[-I_{init} + \left(\frac{V_1+V_2}{L}\right).t\right] & \rightarrow \quad 0 \le t < \theta.\frac{T}{2.\pi} \\ \left[-I_{init} + \left(\frac{V_1+V_2}{L}\right).\frac{\theta.T}{2.\pi} + \frac{V_1-V_2}{L}.\left(t - \frac{\theta.T}{2.\pi}\right)\right] & \rightarrow \quad \theta.\frac{T}{2.\pi} \le t < \frac{T}{2} \end{cases} \tag{10}$$

Since, steady-state operation, the AC voltages $V_1(t)$ and $V_2(t)$, and the inductor current, $i_L(t)$, repeat every half-cycle with reversed signs,

$$V_1\left(t + \frac{T_s}{2}\right) = -V_1(t), \tag{11}$$

$$V_2\left(t+\frac{T_s}{2}\right)=-V_2(t)\text{, and} \tag{12}$$

$$i_L\left(t+\frac{T_s}{2}\right)=-i_L(t) \tag{13}$$

Similarly, the current expressions during the half cycle $T_S/2>t>T_S$ are

$$i_L(t)\Big|_{\frac{T_s}{2}>t>T_s}=\begin{cases}\left[I_{init}-\left(\frac{V_1+V_2}{L}\right).\left(t-\frac{T}{2}\right)\right] & \rightarrow \quad \frac{T}{2}\le t<\frac{T}{2}+\theta.\frac{T}{2.\pi}\\ \left[I_{init}-\left(\frac{V_1+V_2}{L}\right).\frac{\theta.T}{2.\pi}-\frac{V_1-V_2}{L}.\left(t-\frac{T}{2}-\frac{\theta.T}{2.\pi}\right)\right] & \rightarrow \quad \frac{T}{2}+\theta.\frac{T}{2.\pi}\le t<T\end{cases} \tag{14}$$

To calculate initial current component, and the phase shift;

At steady state,

$$I_{init}=-I_{init}+\frac{V_1+V_2}{L}.\frac{\theta.T}{2.\pi}+\frac{V_1-V_2}{L}.\left(\frac{T}{2}-\frac{\theta.T}{2.\pi}\right) \tag{15}$$

Simplifying the latter expression, therefore,

$$I_{init}=\frac{1}{X}.\left[V_2.\theta+(V_1-V_2).\frac{\pi}{2}\right] \tag{16}$$

Power Flow in Reverse Direction

A similar manner can be followed on the assumption of negative phase shift, $-\pi/2<\theta<0$, to depict the corresponding current expressions for both intervals as follows

$$i_L(t)\Big|_{0<t<\frac{T_s}{2}}=\begin{cases}\left[-I_{init}+\left(\frac{V_1-V_2}{L}\right).t\right] & \rightarrow \quad 0\le t<(\pi+\theta).\frac{T}{2.\pi}\\ \left[-I_{init}+\left(\frac{V_1-V_2}{L}\right).\frac{(\pi+\theta).T}{2.\pi}+\frac{V_1+V_2}{L}.\left(t-(\pi+\theta).\frac{T}{2.\pi}\right)\right] & \rightarrow (\pi+\theta).\frac{T}{2.\pi}\le t<\frac{T}{2}\end{cases}$$

$$i_L(t)\Big|_{\frac{T_s}{2}>t>T_s}=\begin{cases}\left[I_{init}-\left(\frac{V_1-V_2}{L}\right).\left(t-\frac{T}{2}\right)\right] & \rightarrow \quad \frac{T}{2}\le t<\frac{T}{2}+(\pi+\theta).\frac{T}{2.\pi}\\ \left[I_{init}-\left(\frac{V_1+V_2}{L}\right).\frac{\theta.T}{2.\pi}-\frac{V_1-V_2}{L}.\left(t-\frac{T}{2}-\frac{\theta.T}{2.\pi}\right)\right] & \rightarrow \quad \frac{T}{2}+(\pi+\theta).\frac{T}{2.\pi}\le t<T\end{cases} \tag{17}$$

To calculate initial current component, and the phase shift;

At steady state,

$$I_{init} = -I_{init} + \frac{V_1 - V_2}{L}.(\pi + \theta).\frac{.T}{2.\pi} + \frac{V_1 - V_2}{L}.\left(\frac{T}{2} - (\pi + \theta).\frac{T}{2.\pi}\right) \quad (18)$$

Simplifying the latter expression, therefore,

$$I_{init} = \frac{1}{X}.\left[-V_2.\theta + (V_1 - V_2).\frac{\pi}{2}\right] \quad (19)$$

Consequently, the initial current component expression can be put in a general form as follows,

$$I_{init} = \frac{1}{X}.\left[|V_2.\theta| + (V_1 - V_2).\frac{\pi}{2}\right] \quad (20)$$

Table 5 and Table 6 summarize the inductor current steady state expressions for forward and reverse power flow directions, respectively.

Table 5: Inductor Current Expression during Different Intervals – Forward Power Flow Direction.

Mode	Interval	Inductor Current at $0 < \theta < \pi/2$
I	$0 \le t < \theta.\frac{T}{2.\pi}$	$\left[-I_{init} + \left(\frac{V_1 - V_2}{L}\right).t\right]$
II	$\theta.\frac{T}{2.\pi} \le t < \frac{T}{2}$	$\left[-I_{init} + \left(\frac{V_1 - V_2}{L}\right).\frac{\theta.T}{2.\pi} + \frac{V_1 + V_2}{L}.\left(t - \frac{\theta.T}{2.\pi}\right)\right]$
III	$\frac{T}{2} \le t < \frac{T}{2} + \theta.\frac{T}{2.\pi}$	$\left[I_{init} - \left(\frac{V_1 + V_2}{L}\right).\left(t - \frac{T}{2}\right)\right]$
IV	$\frac{T}{2} + \theta.\frac{T}{2.\pi} \le t < T$	$\left[I_{init} - \left(\frac{V_1 + V_2}{L}\right).\frac{\theta.T}{2.\pi} - \frac{V_1 - V_2}{L}.\left(t - \frac{T}{2} - \frac{\theta.T}{2.\pi}\right)\right]$

Table 6: Inductor Current Expression during Different Intervals – Reverse Power Flow Direction.

Mode	Interval	Inductor Current at $-\pi/2 < \theta < 0$
I	$0 \le t < \theta.\frac{T}{2.\pi}$	$\left[-I_{init} + \left(\frac{V_1 - V_2}{L}\right).t\right]$

II	$\theta.\frac{T}{2.\pi} \le t < \frac{T}{2}$	$\left[-I_{init}+\left(\frac{V_1-V_2}{L}\right).\frac{(\pi+\theta).T}{2.\pi}+\frac{V_1+V_2}{L}.\left(t-(\pi+\theta).\frac{T}{2.\pi}\right)\right]$
III	$\frac{T}{2} \le t < \frac{T}{2}+\theta.\frac{T}{2.\pi}$	$\left[I_{init}-\left(\frac{V_1-V_2}{L}\right).\left(t-\frac{T}{2}\right)\right]$
IV	$\frac{T}{2}+\theta.\frac{T}{2.\pi} \le t < T$	$\left[I_{init}-\left(\frac{V_1-V_2}{L}\right).\frac{(\pi+\theta).T}{2.\pi}-\frac{V_1+V_2}{L}.\left(t-\frac{T}{2}-(\pi+\theta).\frac{T}{2.\pi}\right)\right]$

Analytical Power Flow Expression

Starting from the current expressions depicted concluded from the above analysis, an analytical expression for the power flow can be reached as mentioned below.

$$\therefore P = \frac{V_1.V_2}{X}.\theta.\left(1-\frac{|\theta|}{\pi}\right) \tag{21}$$

$$V_2 = V_o.\frac{N_p}{N_s}$$

$$\therefore P = \frac{N_p}{N_s}.\frac{V_{in}.V_o}{X}.\theta.\left(1-\frac{|\theta|}{\pi}\right) \tag{22}$$

This equation represents an expression for the power transferred from the primary bridge to the secondary one, thus it can be considered as the average output power delivered to the load.

It is of interest then to normalize this power expression and observe its evolution with variation of phase shift parameter. Considering that the input voltage, the inductor impedance, and the transformer turns ratio are fixed quantities, thus the ratio can be considered as a constant as defined below

$$K_n = \frac{N_p}{N_s}.\frac{V_{in}}{X} \tag{23}$$

For simplicity the transformer turns-ratio is given a notation, r_t, where

$$r_t = \frac{N_s}{N_p} \tag{24}$$

$$\therefore K_n = \frac{V_{in}}{X.r_t} \tag{25}$$

Thus, the normalized power transfer can be expressed as follows

$$P\big|_{norm} = \frac{P}{K_n} \tag{26}$$

$$\therefore P\big|_{norm} = V_o.\theta.\left(1 - \frac{|\theta|}{\pi}\right) \tag{27}$$

The normalized power transfer expression can hence be observed along with variation of phase shift for different output voltage levels, as seen in Figure 20. The maximum power transfer takes place at $\theta = \pm\pi/2$.

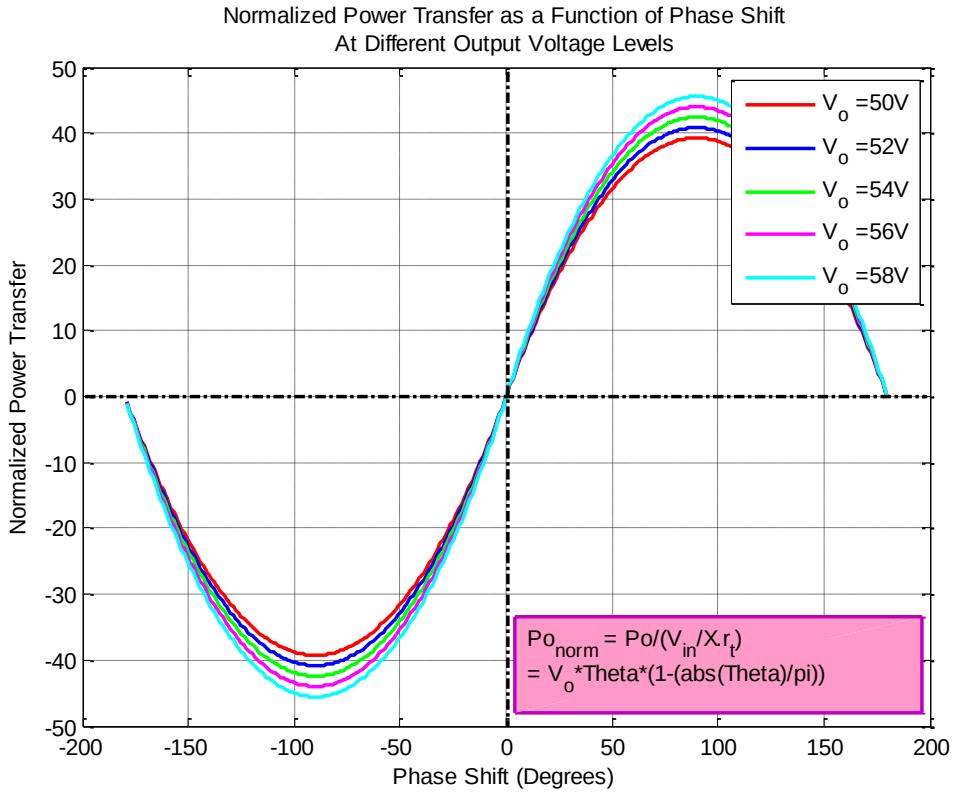


Figure 20: Power Transfer in DAB Converter against Phase Shift between Primary and Secondary Bridges.

Therefore also, an expression for the average output current can be depicted by following the next equations

$$P_{oavg} = V_o.I_{RCacg} \tag{28}$$

$$\therefore I_{RCavg} = \frac{V_{in}}{X.r_t}.\theta.\left(1 - \frac{|\theta|}{\pi}\right) \tag{29}$$

Using the normalization constant, K_n, assigned before, a normalized average output current can be expressed in terms of phase shift as follows

$$\therefore I_{RCavg}\Big|_{norm} = \frac{I_{RCavg}}{K_n} \tag{30}$$

$$\therefore I_{RCavg}\Big|_{norm} = \theta.\left(1 - \frac{|\theta|}{\pi}\right) \tag{31}$$

Figure 21 shows the latter normalized average output current expression plotted versus phase shift.

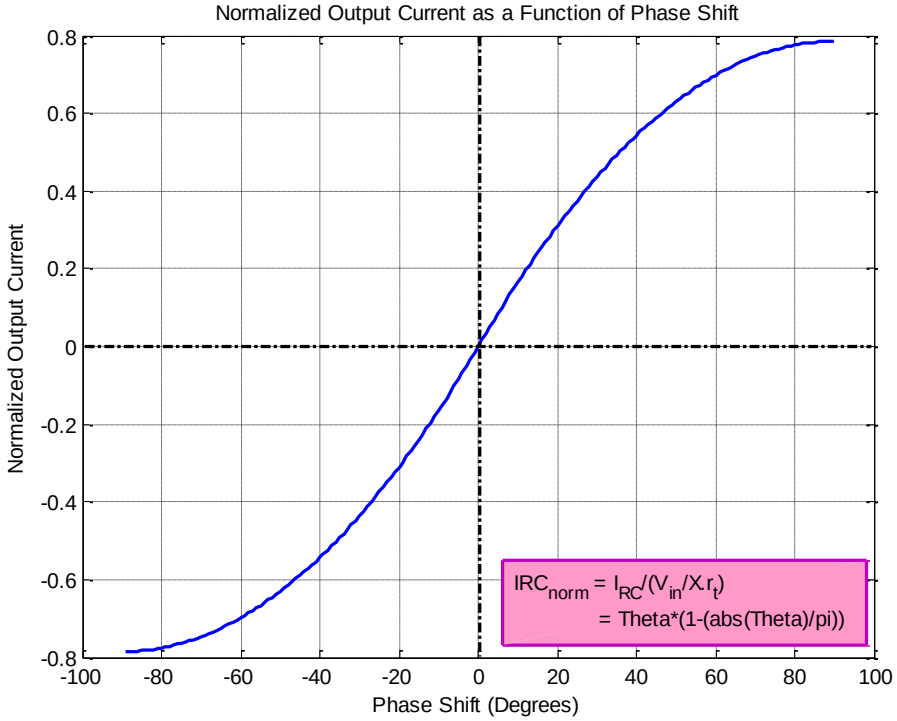


Figure 21: DAB converter Normalized Output Current in terms of Phase Shift between Primary and Secondary Bridges.

Fundamental Equivalent Power Flow Model

As explained previously, conceptually, the converter circuit can be viewed as an inductor, the series power transfer inductor, driven at either end by a controlled square-wave voltage source, as shown in Figure 22. The voltage sources are phase shifted from each other by a controlled angle, θ.

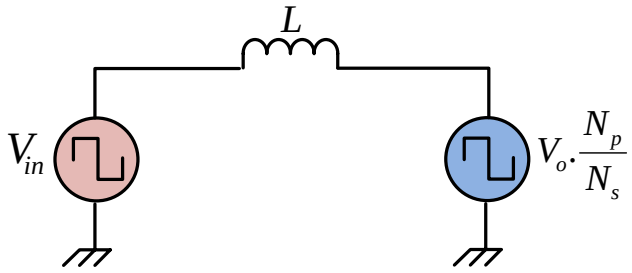


Figure 22: Exact model of DAB dc/dc converter

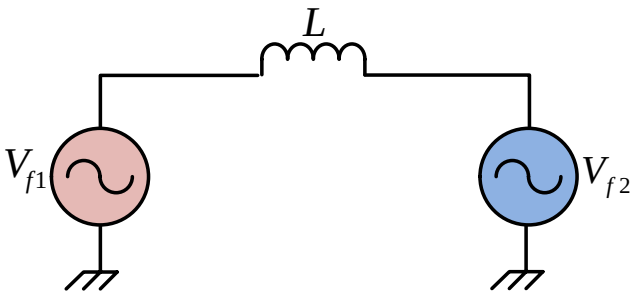


Figure 23: Fundamental model of DAB dc/dc converter

The fundamental power flow analysis proposes that the fundamental harmonic of the square-waves dominates, so the other, higher order, harmonics that make up the square wave can be ignored [7].

Thus the equivalent circuit, shown in Figure 22, can be further simplified, by replacing the square-wave voltage sources by their fundamental components as shown in Figure 23.Since all circuit quantities are sinusoidal at a single frequency, i.e. the switching frequency, a phasor analysis can be carried out;

The steady state inductor current vector is

$$\vec{I}_L = \frac{\vec{V}_{f1} - \vec{V}_{f2}}{\vec{X}} \tag{32}$$

$$\vec{V}_{f1} = V_{f1}\angle 0^\circ \tag{33}$$

$$\vec{V}_{f2} = V_{f2}\angle -\theta^\circ \tag{34}$$

$$\vec{X} = j.\omega.L \tag{35}$$

And the power flow in this fundamental equivalent circuit can be expressed using AC Phasor Theory as [18].

$$P = \mathrm{Re}[\vec{V}_{f2}.\vec{I}_L^{\,*}] \tag{36}$$

$$P = \frac{\vec{V}_{f1}.\vec{V}_{f2}}{\vec{X}}.\sin\theta \tag{37}$$

Where V_1 and V_2 are the RMS values of the two sinusoidal voltage sources, θ is the phase shift between the two sinusoidal voltage sources.

To validate this simplified power flow model, the fundamental harmonic component of the power transferred between the two bridges is calculated by first expressing the primary and secondary bridge voltages, V_{prim} and $V_{\sec}$, in terms of harmonics, applying Fourier Theory [82]. Therefore, the RMS magnitude of each harmonic can be extracted to be:

$$V_{prim})_{RMS} = \frac{1}{\sqrt{2}}\frac{4}{\pi}.V_{in}.\frac{1}{[2.n+1]} \tag{38}$$

$$V_{\sec})_{RMS} = \frac{1}{\sqrt{2}}\frac{4}{\pi}.V_{o}.\frac{1}{[2.n+1]} \tag{39}$$

Where V_{in} and V_o are the DC input and output voltages.

Thus the fundamental harmonic RMS voltages of primary bridge can be described as

$$\because V_{f1} = V_{prim}\big|_{n=0} = \frac{1}{\sqrt{2}}\frac{4}{\pi}.V_{in} \tag{40}$$

And, in order to eliminate the transformer, the secondary bridge voltage must be referred to the same point as the primary. For this reason, $V_{\sec}$ is multiplied by the turn ratio of the transformer, N_p/N_s , thus also the fundamental harmonic RMS voltages of secondary bridge can be described as

$$\because V_{f2} = \frac{N_p}{N_s}.V_{\sec}\Big|_{n=0} = \frac{1}{\sqrt{2}}\frac{4}{\pi}.V_o.\frac{N_p}{N_s} \tag{41}$$

The fundamental harmonic power flow model can be derived by substituting these RMS voltage components in Eq. (3) as follows

$$\therefore P_s = \frac{\frac{1}{\sqrt{2}}\frac{4}{\pi}.V_{in}.\frac{1}{\sqrt{2}}\frac{4}{\pi}.V_o.\frac{N_p}{N_s}}{X}.\sin\theta \tag{42}$$

$$\therefore P_s = \frac{8}{\pi^2}.\frac{V_{in}.V_o}{X}.\frac{N_p}{N_s}.\sin\theta \tag{43}$$

By comparing this simplified fundamental harmonic power flow expression to the analytical actual one, depicted in Eq. (21), it can be concluded that the power transferred by higher harmonics can be neglected compared to its fundamental component. As illustrated by Figure 24, a good correlation justifies the validity of the fundamental model.

[7] has proposed an accurate harmonic model for the converter, by choosing the number of harmonics, N, such that the difference between analytical and harmonic summation solutions are negligible.

Now, and while the fundamental power flow model has proofed an acceptably good match for the actual total power flow, the error between both models can compromised for the sake of depicting a helpful phasor diagram that clarifies the relation between voltage sources and inductor current.

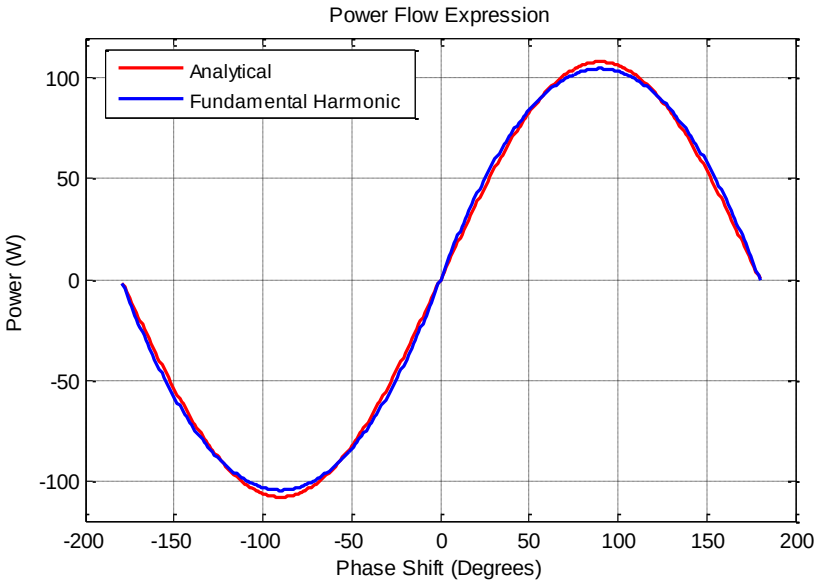


Figure 24: Fundamental versus Analytical Power Flow Waveforms against Phase Shift.

During the rest of the thesis study, the analytical model only will be considered, being the actual Power Flow model.

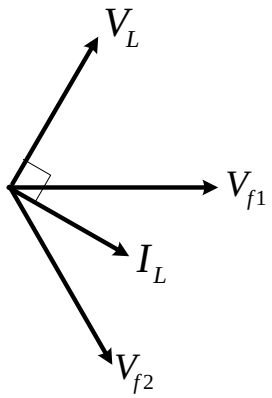


Figure 25: Phasor Diagram Showing AC Voltages at the Terminals of the Inductor, Voltage across and Current through it.

It is interesting thus to analyze the relation between voltage and current components in terms of phasors. As seen in Figure 25, for equal input and output voltage levels, as θ is varied over the range $0 \rightarrow \pi/2$, the current phasor, $\vec{I}_L$, always remains between the phasors $\vec{V}_{f1}$ and $\vec{V}_{f2}$, where it lags the input voltage, $\vec{V}_{f1}$, and leads the output voltage, $\vec{V}_{f2}$.

3.1.1.2. Ripple Analysis

It can be observed from Figure 26 that the output current, to the RC branch, matches the transformer secondary side current with double the frequency. Thus accounting for the transformer turns ratio, the output current peak-peak ripple can be identified by making use of the inductor current equations derived earlier through the analysis.

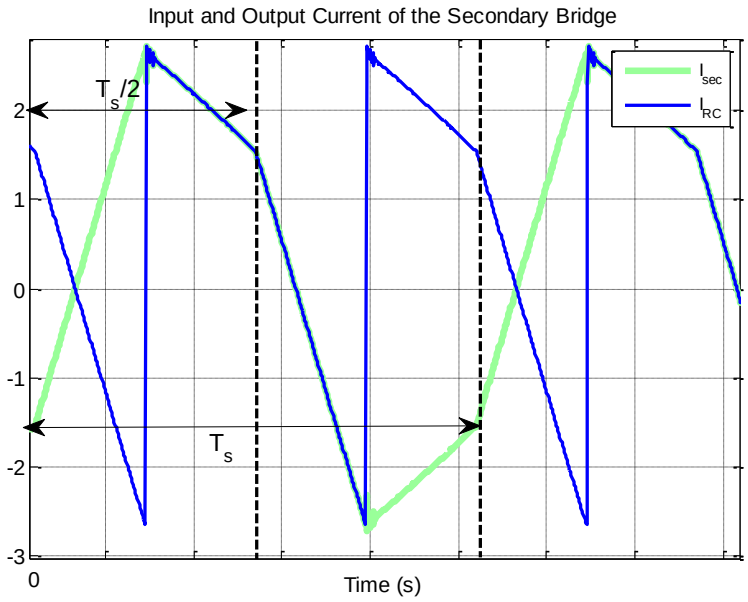


Figure 26: Ripple Current in Transformer Secondary Side of DAB Converter and Corresponding Ripple in Output Current.

Taking the boost state as the case, *V1<V2*, as seen in Figure 26, the peak-peak output current can be defined as double the peak inductor current. The peak inductor current in that case takes place at the phase shift θ, a corresponding time instant of

$$t = \frac{\theta}{2.\pi}.T$$
$$I_L\big|_{peak} = I_L\big|_{\theta} \tag{44}$$

The inductor current at this instant can be defined by substituting in Eq. (16),

$$I_L\big|_{\theta} = -I_{init} + \left(\frac{V_1 + V_2}{L}\right).\frac{\theta.T}{2.\pi} \tag{45}$$

Therefore, the peak-peak current can be described as

$$\Delta I_L\big|_{p-p} = 2.I_L\big|_{\theta} \tag{46}$$

$$\Delta I_L\big|_{p-p} = -2I_{init} + \left(\frac{V_1 + V_2}{L}\right).\frac{\theta.T}{\pi} \tag{47}$$

$$\Delta I_L\big|_{p-p} = -\frac{4}{X}.\left[|V_2.\theta| + (V_1 - V_2).\frac{\pi}{2}\right] + \left(\frac{V_1 + V_2}{L}\right).\frac{\theta.T}{\pi} \tag{48}$$

An expression for the transformer secondary side current can then be reached by scaling the inductor current through multiplying the transformer turns ratio

$$\Delta I_{Sec}\big|_{p-p} = \frac{N_p}{N_s}.\Delta I_L\big|_{p-p} \tag{49}$$

$$\Delta I_{RC}\big|_{p-p} = \Delta I_{Sec}\big|_{p-p} \tag{50}$$

$$\Delta I_{RC}\big|_{p-p} = -4.\frac{1}{X.r_t}.\left[|V_2.\theta| + (V_1 - V_2).\frac{\pi}{2}\right] + \left(\frac{V_1 + V_2}{L}\right).\frac{\theta.T}{\pi.r_t} \tag{51}$$

To represent the ripple in terms of DC input and output supply voltages, V_1 and V_2, are substituted by their corresponding supply voltages

$$\Delta I_{RC}\big|_{p-p} = -4.\frac{1}{X.r_t}.\left[\left|\frac{V_{out}}{r_t}.\theta\right| + (V_{in} - \frac{V_{out}}{r_t}).\frac{\pi}{2}\right] + \left(\frac{V_{in} + \frac{V_{out}}{r_t}}{L}\right).\frac{\theta.T}{\pi.r_t} \tag{52}$$

Furthermore, capacitor ripple current can thus be defined by subtracting the resistive branch current from total load current, thus

$$\therefore \Delta I_c\big|_{p-p} = -4.\frac{1}{X.r_t}.\left[\left|\frac{V_{out}}{r_t}.\theta\right| + (V_{in} - \frac{V_{out}}{r_t}).\frac{\pi}{2}\right] + \left(\frac{V_{in} + \frac{V_{out}}{r_t}}{L}\right).\frac{\theta.T}{\pi.r_t} - I_R \tag{53}$$

3.1.1.3. Advantages and Disadvantages of Phase Shift Modulation

The main advantage of phase shift modulation is its simplicity; according to Eq. (1), it can be seen that only one control parameter, the phase shift θ, is required to adjust the DAB power transfer level. Another advantage is the possibility of using half-bridge circuits to generate $V_1(t)$ and $V_2(t)$ high frequency AC voltages, instead of full-bridge ones. These two advantages are the reason of the wide use of this modulation scheme [6].

Conceptually, ZVS takes place during Phase-Shift Modulation, due to the leakage inductances of the transformer, the output AC current of each bridge lags its corresponding AC bridge output voltage, thus discharging the switch capacitances during dead times. However, if the voltage magnitudes across the transformer vary significantly, the load range over which ZVS occur is limited. A disadvantage of this modulation strategy, thus, is that it only achieves high converter efficiency for operating voltages close to $V1 \approx V2$, as will be verified by simulations in the next chapters. For $V1 << V2$ or $V1 >> V2$, the transformer RMS currents, the inductor and transformer copper losses, and the semiconductor conduction losses increase considerably [67]. Thus, specifically as the power level increases, for a higher efficiency converter, alternative modulation schemes should be employed [68].

For the initial characterization and practical verification of the converter operation, it is of interest, hence, to carry out the tests at the input and output operating voltages matching the transformer turns ratio.

3.1.2. Alternative Modulation Schemes

Motived by the previous discussion of the drawbacks of SPS control, other modulation strategies need to be explored.

3.1.2.1. Extended Phase Shift Modulation (EPS)

The EPS control [83] - [87] improves the SPS control by introducing an internal phase shift between the two legs of only one of the bridges while the other bridge legs are kept in complementary mode. Consequently, as clarified by Figure 27b, the output voltage at one bridge is a two-leveled AC waveform, while at the other is a three-level one. During zero voltage, hence, no circulating power. Also wider ZVS area can be achieved.

However, to decrease the circulating power, when the voltage levels are exchanged, $V1>V2$ or $V1<V2$, and the power flow directions are exchanged, forward or reverse directions, the operation states of both bridges should be exchanged.

This method thus employs the outer phase shift to control the power transfer, and the inner one to reduce circulating power and extend the range of ZVS [10].

3.1.2.2. Dual Phase Shift Modulation (DPS)

The DPS control [88] - [94] further improves the EPS control by employing the same additional internal phase shift for both bridges, instead of only one as in EPS control. Consequently, as clarified by Figure 27c, the output voltages at both bridges are three-leveled AC waveforms. Therefore, further expanding the ZVS, decreasing the circulating currents, minimizing the output capacitors, and improving the efficiency can be achieved.

The strategy offers symmetrical structure, thus easier implementation.

3.1.2.3. Triple Phase Shift Modulation (TPS)

The TPS control [74] [68] [81],[95] - [98] is similar to the DPS control, however, in this case the internal phase shift can be different from one bridge to the other.

The TPS strategy can be deemed the general form, from which SPS, EPS, and DPS can be described with one, two, or three control degrees of freedom respectively.

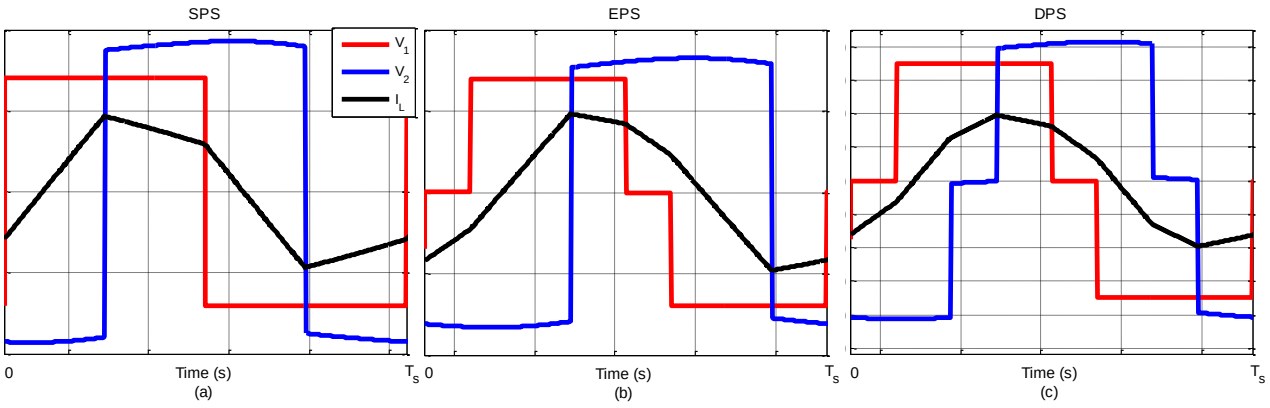


Figure 27: Modulation Control Strategies for DAB Converter Topology – SPS, EPS, and DPS.

3.2.Converter Average Model

Although accurate, the switching model is non-linear time-variant converter model, and since the ripple is inherent to the converter switching process, and is not caused by a controller input, hence it is not possible to design a controller that responds to this ripple.

A suitable approximate model can be developed using averaging procedure, it removes the complications involved in the switching behavior, and describes the essential low-frequency dynamics of the converter. Therefore, it sacrifices the converter switching behavior with a good tradeoff for the simplicity of the model as well as the control system analysis.

Taking advantage that there is no switching frequency ripple, and consequently the simulation time required by averaged model is much lower than that required by switched model. It gives a sufficiently accurate view of the configuration of variations, so it is called Large Signal AC Model.

During the previous analysis, the states of the inductor current have been defined, from which an expression for the average output current has been derived, stated below for convenience,

$$I_{RCavg} = \frac{V_{in}}{X.r_t}.\theta.\left(1-\frac{|\theta|}{\pi}\right) \tag{54}$$

This expression defines the current injected in the output plant, RC. Similarly, the average input current can be derived to be

$$I_{Lavg} = \frac{V_o}{X.r_t}.\theta.\left(1-\frac{|\theta|}{\pi}\right) \tag{55}$$

Using the input and output current expressions, while omitting the transformer and accounting for its turns ratio, the average model of the DAB converter can be simplified from the form shown in Figure 28 to that in Figure 29.

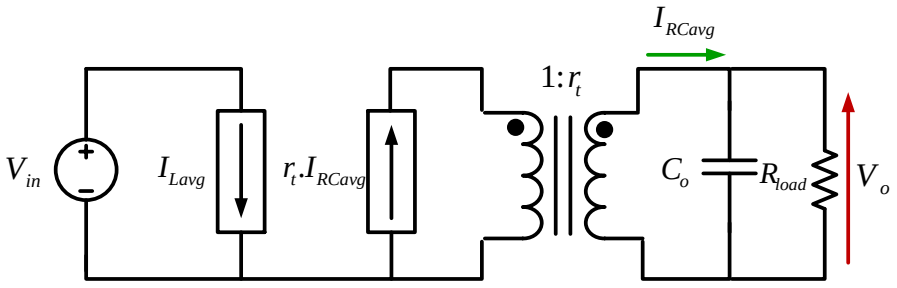


Figure 28: DAB Converter Average Model – With Transformer.

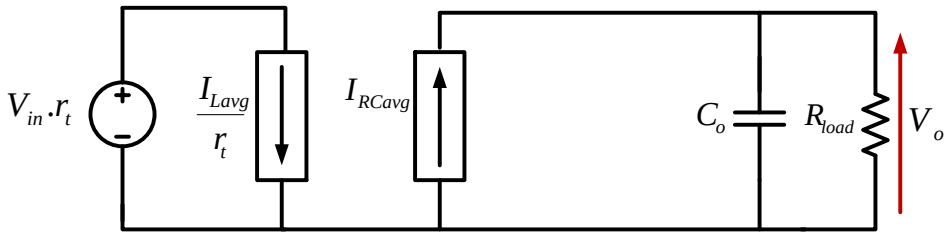


Figure 29: DAB Converter Average Model – Omitting Transformer and Accounting for Turns Ratio.

Since the actual model of the transformer is employed for constructing the switching model, thus to improve the average one, the transformer model is added. This is realized by accounting for the primary and the secondary transformer leakage inductances and series resistances, while all the impedances are referred to the secondary side of the transformer by multiplying by the corresponding turns ratio. The full average model of the DAB converter can thus be depicted in Figure 30.

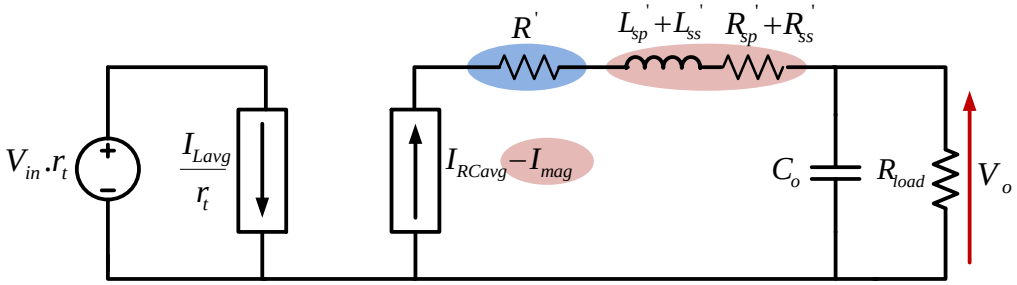


Figure 30: Full Average Model of DAB Converter.

To verify the validity of the average model, its response to a step change in θ is compared to that of the switched simulation. Figure 31 shows this response. It can be seen that the resulting average model is able to predict system dynamics.

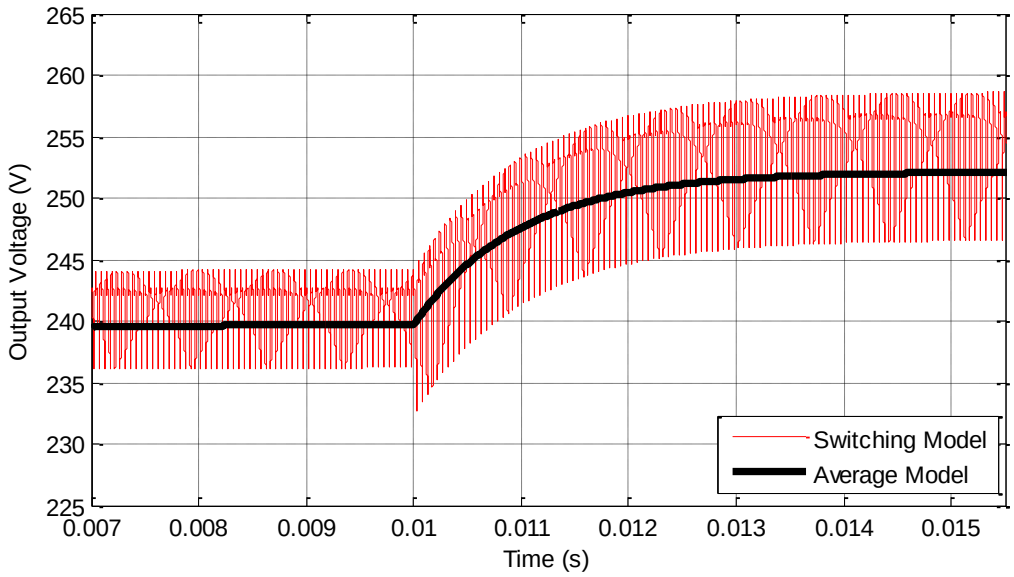


Figure 31: Average Model Verification – Open Loop Converter Response to a Phase Shift Step.

Chapter Four

4. Closed Loop Control

Power electronic converters need closed loop regulation to ensure that the correct output is maintained irrespective of operating conditions, as well as to guarantee stability and fast recovery in the face of transient events. There are two basic types of transient that affect this class of system, i.e. variations in reference command and changes in load condition.

As an initial solution to simplify control problem, open loop regulation was regarded. This method involves a pre-calculated lookup table that generates the control signal for a DAB converter based on the desired output power, as is proposed by Akagi et al. in [79]. Although simple, open loop control is not robust to variations in operation conditions, moreover, at certain operating point it cannot guarantee transient performance. So it is not of interest for this review.

The DAB converter is to be used in a Smart Grid application, with a load resistance or inverter, thus the most effective control strategy in this context is the converter output voltage regulation. For this specific converter application, the power transfer direction during steady state operation is assigned to be from the input H-bridge to the output one, connected to the load, i.e. the forward power flow direction discussed earlier during the DAB analysis.

The basic closed loop block diagram of the DAB converter is shown in Figure 32, all the system characteristic transfer functions are given in LaPlace domain. The plant is considered to have one input which is the current, i_o ,and one output which is the load voltage, V_o .The controller is used to regulate the output voltage by varying the plant input current, which justifies the choice of the single-loop controller structure.

However, considering that the DAB converter controllable quantity is the phase shift between the two bridges. This implies that the controller action, represented in the load current reference, needs to be translated to the corresponding phase shift reference, as clarified by the intermediate $i_o^* \rightarrow \theta^*$ block clarified in the block diagram in Figure 32.

The sought relation that ties the phase shift with the plant current, as will be seen, is completely non-linear putting complications on the control problem, thus attempts to simplify this relation into a linear one are presented in context of this chapter.

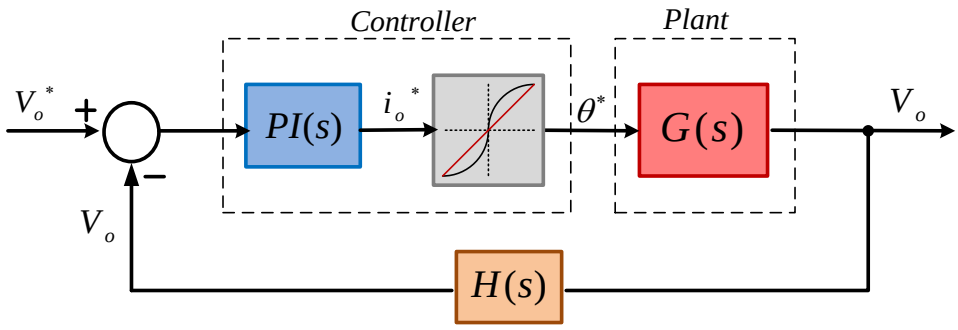


Figure 32: Basic Closed Loop Block Diagram – The diagram shows Single-Loop Controller Structure for Controlling the Output Voltage of DAB Converter.

4.1. Control Structure

The control structure used to regulate the DAB converter is designed to realize two essential functions:

a) Good tracking of the reference command.
b) Rejection of disturbance caused by uncontrollable load condition.

These two main properties should be guaranteed with no steady-state error, as well as relatively fast transient response.

Based on this, the control system design is developed in two stages:

- First, assuming a fixed load condition, thus the considered plant is an RC load, the converter output DC link capacitor in parallel with a known resistive load. This creates an appropriate condition for studying the reference tracking. Figure 33 shows the block diagram for this control structure.

$$G_r(s) = \frac{1}{C.s + 1/R} \tag{56}$$

- Then, the load condition is assumed to be unknown thus uncontrollable, which is the case for this class of applications. Thus the plant is transformed to a C load, only converter output DC link capacitor is considered, while defining the load current input, i_{load}, as a disturbance input. This creates an appropriate condition for studying the disturbance rejection. Figure 34 shows the block diagram for this control structure.

$$G_d(s) = \frac{1}{C.s} \tag{57}$$

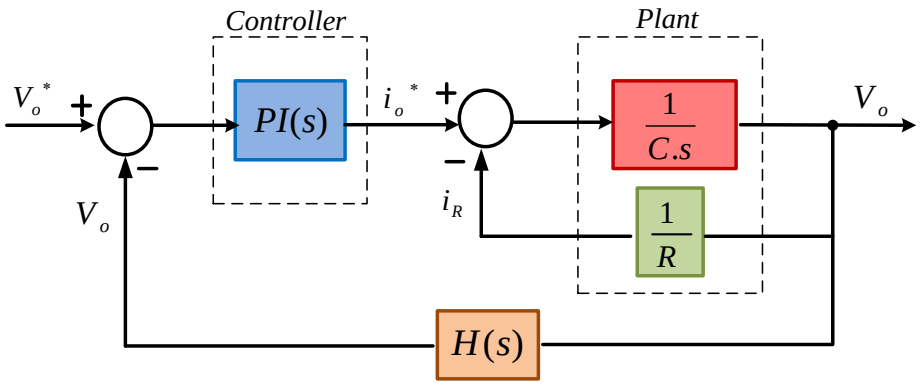


Figure 33: Closed-Loop-Controller Structure assuming Fixed Load Condition for Studying Controller Response to a Transient Variation of Reference Output Voltage.

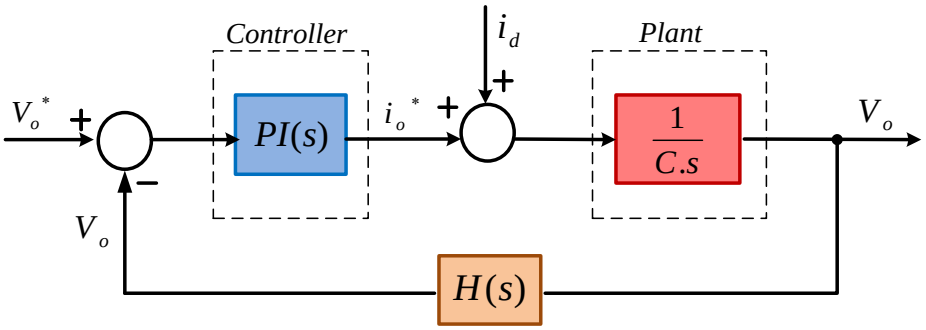


Figure 34: Closed-Loop-Controller Structure for Studying Controller Response to a Transient Variation of Load Condition.

4.2. Controller Design

As seen from Eq. (56) and Eq. (57), the plant model is first-order in nature and the regulator needs to regulate a DC quantity, converter output voltage, thus a Proportional-Integral (PI) structure should be sufficient to achieve high performance output voltage regulation. The transfer function of a PI controller was mentioned in the Literature Review.

To justify the choice of such controller, and tune its parameters, the system is designed following the two previously mentioned stages, starting by analyzing reference tracking property, then disturbance rejection.

- *Reference Tracking (Steady State Error)*

To justify the choice of such a simple controller for reference tracking, the PI-regulated system, depicted in Figure 33, is derived below, considering that the sensor has no dynamics, i.e. $H(s)=1$.

$$\frac{V_o}{V_o^*}=\frac{PI(s).G_r(s)}{1+PI(s).G_r(s)} \tag{58}$$

$$\frac{V_o}{V_o^*} = \frac{K_p.(T_i.s+1)}{T_i.C.s^2 + K_p.(T_i.s+1)} \tag{59}$$

Since the system output voltage is hence described as

$$V_o = \left[\frac{V_o}{V_o^*}\right]_{T.F} \times V_o^* \tag{60}$$

The PI controller gives the forward path a pole at the origin. This makes the forward path gain asymptote to infinity as the system frequency approaches DC ($s \to 0$). This large gain eliminates steady state error, ensuring good tracking of the DC reference. This system is it is unconditionally stable, regardless of controller gains. There is therefore no theoretical limit on controller gains, so a very high controller bandwidth and a very fast transient response can be achieved [7].

The PI controller is thus tuned for zero-pole cancellation [69], the system plant, defined by Eq. (56), has a pole at

$$T_p = -\frac{1}{R.C} \tag{61}$$

Consequently, if the integrator time constant is adjusted to the location of that pole, the controller can guarantee to cancel the system pole by the integrator zero. Assuming this, the system transfer function can be put to the next form

$$\frac{V_o}{V_o^*} = \frac{K_p.\left(\frac{s+\frac{1}{T_i}}{s}\right).\left(\frac{C}{s+\frac{1}{R_L.C}}\right)}{1+K_p.\left(\frac{s+\frac{1}{T_i}}{s}\right).\left(\frac{C}{s+\frac{1}{R_L.C}}\right)} \tag{62}$$

$$\because \left(s+\frac{1}{T_i}\right) = \left(s+\frac{1}{R_L.C}\right) \tag{63}$$

$$\frac{V_o}{V_o^*} = \frac{\left(\frac{K_p.C}{s}\right)}{1+\left(\frac{K_p.C}{s}\right)} \tag{64}$$

$$\frac{V_o}{V_o^*} = \frac{K_p.C}{s+K_p.C} \tag{65}$$

The controller gains are thus defined based on system to be

$$K_p = 2.\pi.BW.C \tag{66}$$

$$T_i = -\frac{1}{T_p} = R.C \tag{67}$$

The bandwidth defines the speed of the controller. Thus a larger bandwidth implies a faster response to transient events, which implies a larger overshoot component. This may cause saturation to the defined limits, thus in reverse slowing down the response.

A typical value for the application is, hence, 50Hz, and can be reduced further more to 30Hz for characterization of converter operation at higher power.

Based on the parameters defined for the system at low power, Table 3, the controller gains are calculated based on this analysis to be

$$K_p = 2 \times \pi \times 50 \times 1000^{-6} = 0.3141592 \tag{68}$$

$$T_i = 100 \times 1000^{-6} = 0.1 \tag{69}$$

It is of interest then to study the characteristics of the system transfer function, defined by Eq. (59), being a second order system can thus be compared in analogy to the canonical second order transfer function.

$$TF(s) = \frac{{w_n}^2}{s^2 + 2.\zeta.w_n.s + {w_n}^2} \tag{70}$$

where w_n is the natural frequency of the system, and ζ is the damping ratio.

As a response to a unity step response, the behavior of the system differs according to three distinct conditions.

$$\zeta = \begin{cases} <1 & Overdamped \\ =0 & Critically-Damped \\ >1 & Underdamped \end{cases}$$

Since the control action is the output current, while the final controlled quantity is the converter output voltage, the choice of damping ratio should be decided by observing the response of the output voltage to variations in reference command. This can be studied by introducing a step in the controller output voltage reference and testing the voltage response for different damping ratios.

The damping ratio affects the controller integral time constant, the relation between both parameters can thus be concluded by comparing the system transfer function, Eq. (59), to the second order canonical second order equation, Eq. (70), as follows.

$$2.\zeta.w_n = \frac{K_p}{C} \tag{71}$$

$$\zeta^2 = \frac{2.\pi.BW}{4.K_i} \tag{72}$$

Figure 35 illustrates the response of the output voltage to a step variation of reference voltage. The studies are carried out for the simulated system at maximum power (parameters stated in Table 3).

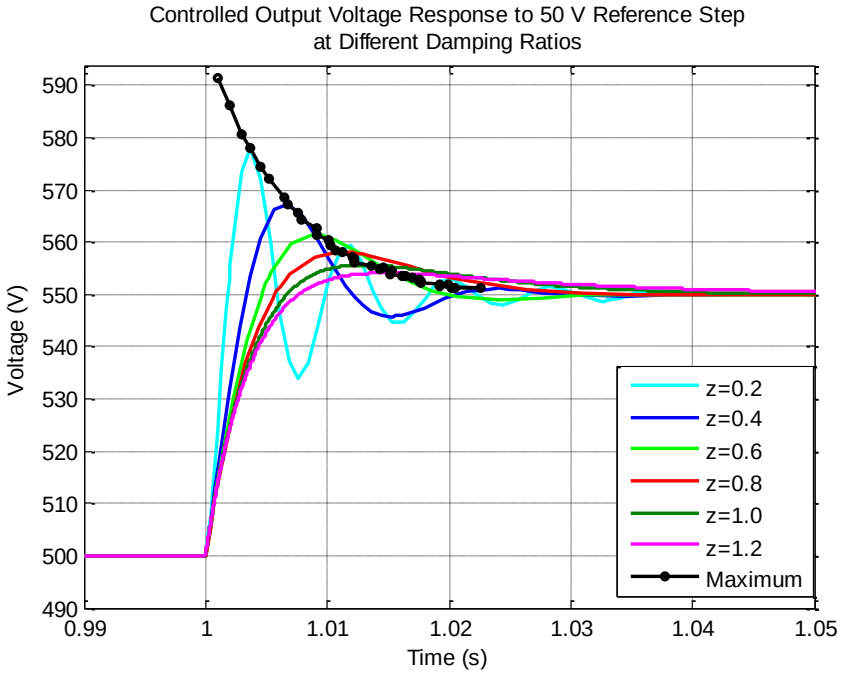


Figure 35: Output Voltage Response to a 50V Reference Voltage Step under Different Damping Ratios – Maximum Overshoot of Resulting Curves is Recorded and Clarified by the Black Maximum Envelope.

The maximum overshoot envelope indicated in the figure thus can be repeated for different voltage steps resulting in a set of curves, Figure 36, additionally explaining the voltage step effect on the maximum overshoot values.

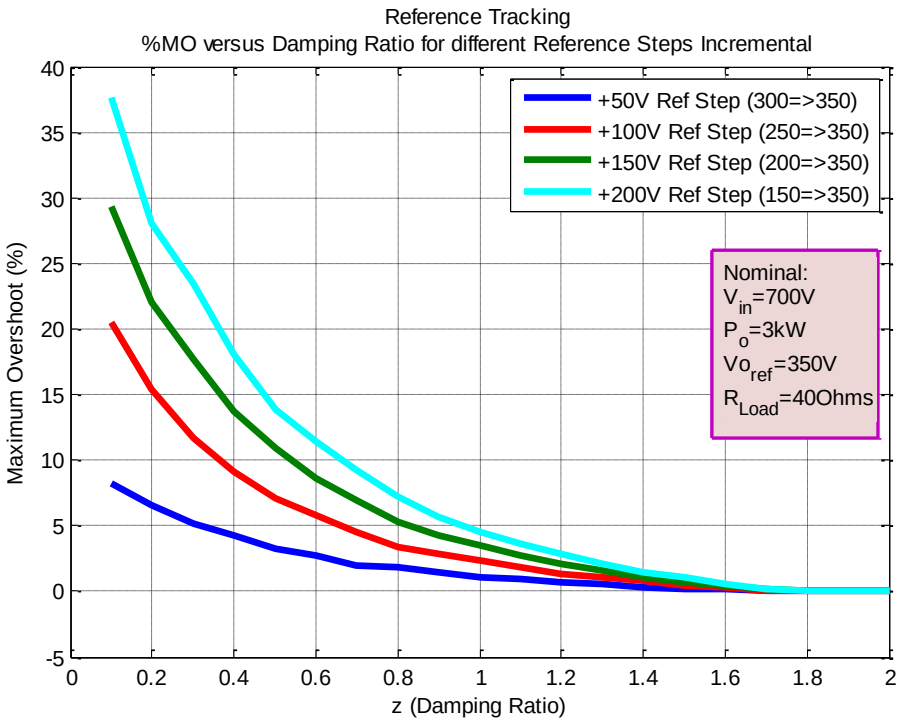


Figure 36: Percentage Maximum Overshoot against damping Ratio for Different Voltage Steps.

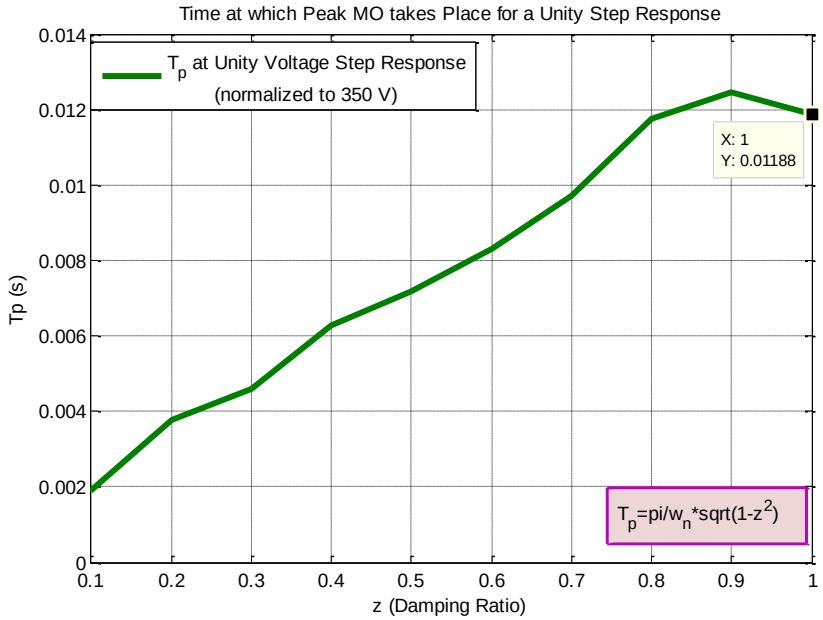


Figure 37: Overshoot Time – Time at which Maximum Overshoot takes place against the Damping Ratio – Measurement is done from the simulated system at maximum power.

As can be observed, and further clarified by curve shown in Figure 37, the larger the damping ratio, the lower the magnitude of maximum overshoot, but the larger is the time at which the maximum overshoot takes place, and the larger the settling time, i.e. the slower the system.

- *Disturbance Rejection*

Disturbance Rejection is the immunity of the system to disturbances; the term indicates the capability of the system to tolerate unbalances/distortion without being affected. Since DAB converters commonly face changing load conditions, the closed loop controller must provide good load transient regulation. In fact, a high performance controller should provide equivalent performance for both reference and load transients.

Similarly, to justify the choice of the controller for disturbance rejection, the PI-regulated system, depicted in Figure 34, is derived below, considering also that the sensor has no dynamics, i.e. $H(s)=1$.

$$V_o = \left[\frac{V_o}{V_o^*}\right]_{T.F} \times V_o^* + \left[\frac{V_o}{i_d}\right]_{T.F} \times i_d \tag{73}$$

$$\frac{V_o}{V_o^*} = \frac{PI(s).G_d(s)}{1+PI(s).G_d(s)} \tag{74}$$

$$\frac{V_o}{V_o^*} = \frac{K_p.(T_i.s+1)}{T_i.C.s^2 + K_p.(T_i.s+1)} \tag{75}$$

$$\frac{V_o}{i_d} = \frac{G_d(s)}{1+G_d(s).PI(s)} \tag{76}$$

$$\frac{V_o}{i_d} = \frac{T_i.s}{T_i.C.s^2 + K_p(T_i.s+1)} \tag{77}$$

In this case, the controller proportional gain can still be tuned for the DC link capacitance, however, the integral time constant cannot be sufficiently tuned for zero pole cancellation due to variation of system pole corresponding to load disturbance condition. The integrator gain, T_i, can be tuned based on the desired system behavior, namely the allowable maximum overshoot.

As can be understood from the later system analysis, the tuning process is a compromise. If the process favors fast response to dynamic variations in reference, then the system will suffer larger magnitudes of maximum overshoot and oscillations thus leaving the controller struggling to reject disturbances. On the other hand, if the process trades off fast response thus it has a smoother rejection of disturbances in terms of smaller magnitudes of oscillations. In conclusion, with the presence of disturbances and pollution in terms of load variations, the tuning of a PI controller is a critical process. For a closed loop regulator maximally tuned for reference tracking, the load transient will be sluggish compared to its reference step counterpart.

For choosing the integrator time constant, hence, a study similar to the one performed for reference tracking is carried out. By introducing a disturbance in the load condition and testing the voltage response for different damping ratios. Figure 38 illustrates the latter mentioned response.

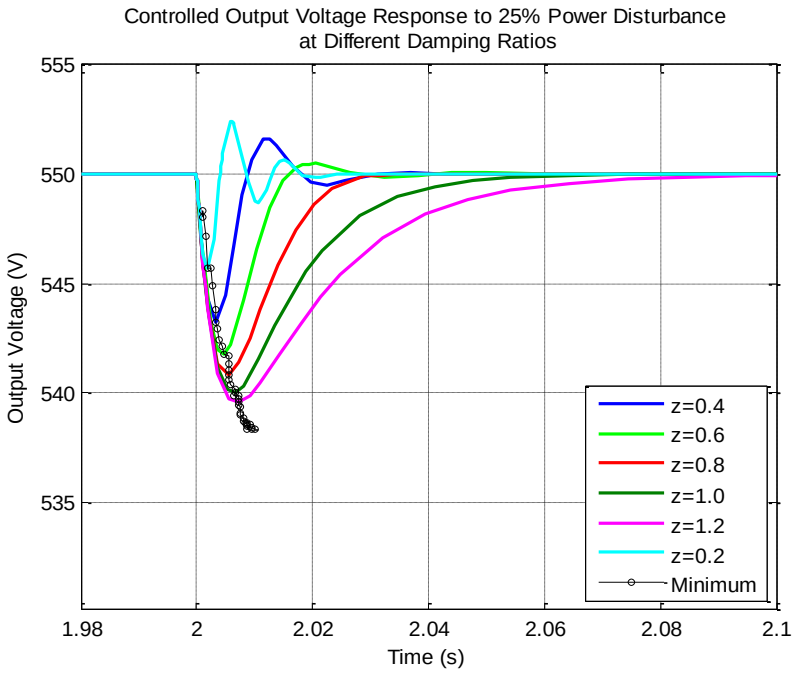


Figure 38: Output Voltage Response to 25% Power Step due Load Disturbance under Different Damping Ratios – Maximum Overshoot of Resulting Curves is Recorded and Clarified by the Black Minimum Envelope.

Hence, the overshoot envelope indicated in the figure thus can be repeated for different power steps resulting in a set of curves, Figure 39, additionally explaining the load disturbance effect on the overshoot values.

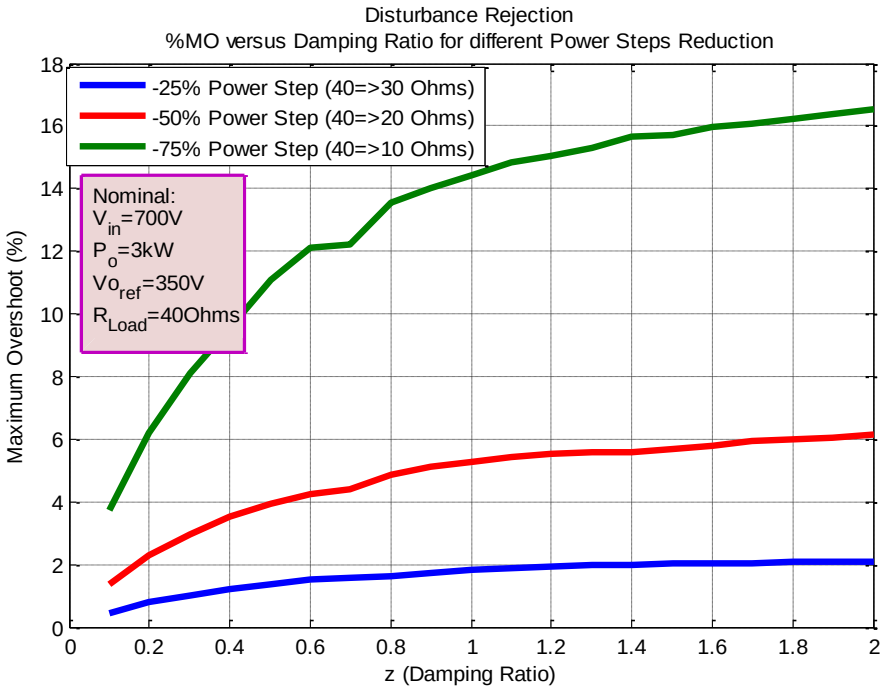


Figure 39: Percentage Maximum Overshoot against damping Ratio for Different Power Steps.

Similar curves can be constructed for any power level to choose the integral gain of the controller, the Simulink block diagram along with the Matlab scripts are consulted.

Comparing the percentage overshoot as a response to different damping ratios with its corresponding disturbance rejection response at the same damping ratios, Figure 40 illustrates the resulting curves. It can be seen that the higher the damping the higher the magnitude of voltage during riding through a load disturbance, while it is completely the opposite for the case of the response to variation of the reference voltage. This leaves a region of good compromise between both transient responses. Thus the damping ratio is selected within region to be

$$\zeta = 0.8 \tag{78}$$

Substituting in Eq. (72), this damping ratio translates to the controller integral gain.

$$K_i = \frac{2.\pi.BW}{4.\zeta^2} \tag{79}$$

$$K_i = \frac{2*\pi*50}{4*0.8*0.8} = 122.718Hz \tag{80}$$

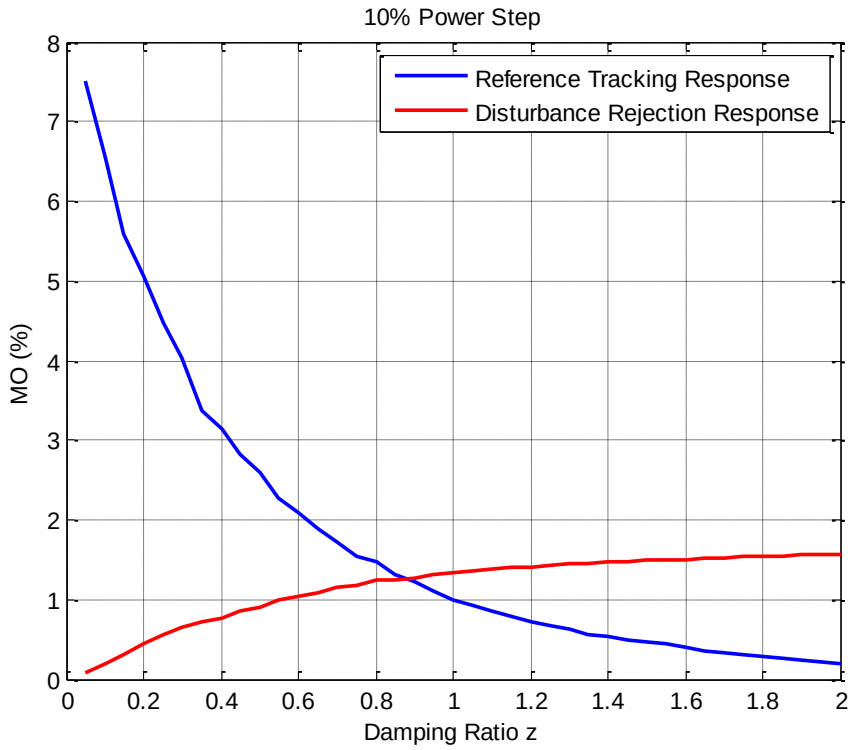


Figure 40: Reference Tracking versus Disturbance Rejection Controller Percentage Overshoot.

4.3. Current-to-Phase Relation

4.3.1. Initial Simple Approach

The relation between the load current and the phase shift can be derived starting by analytical power expression depicted in Eq. (21), stated here for convenience

$$\therefore P = \frac{N_p}{N_s}.\frac{V_{in}.V_o}{X}.\theta.\left(1-\frac{|\theta|}{\pi}\right) \tag{81}$$

For simplicity, the turns-ratio is assigned the following notation

$$r_t = \frac{N_s}{N_p} \tag{82}$$

$$\therefore P = \frac{V_{in}.V_o}{X.r_t}.\theta.\left(1-\frac{|\theta|}{\pi}\right) \tag{83}$$

Since the DAB converter is considered to send power to the load, therefore the phase shift during steady state operation is positive, thus complying with the case $\theta > 0$. The power transfer expression in this case simplifies to

$$\therefore P = \frac{V_{in}.V_o}{X.r_t}.\theta.\left(1-\frac{\theta}{\pi}\right) \tag{84}$$

The average output current calculated during the previous analysis, for $\theta > 0$, is

$$I_{RCavg} = \frac{V_{in}}{X.r_t}.\theta.\left(1-\frac{\theta}{\pi}\right) \tag{85}$$

$$\frac{I_{RCavg}.X.r_t}{V_{in}} = \theta - \frac{\theta^2}{\pi} \tag{86}$$

$$\frac{I_{RCavg}.X.r_t.\pi}{V_{in}} = \pi\theta - \theta^2 \tag{87}$$

$$\theta^2 - \pi\theta + \frac{I_{RCavg}.X.r_t.\pi}{V_{in}} = 0 \tag{88}$$

$$\theta = \frac{\pi \pm \sqrt{\pi^2 - 4.\frac{I_{RCavg}.X.r_t.\pi}{V_{in}}}}{2} \tag{89}$$

$$\theta = \frac{\pi}{2} \pm \frac{\pi}{2}.\sqrt{1-4.\frac{I_{RCavg}.X.r_t}{V_{in}.\pi}} \tag{90}$$

$$\theta = \frac{\pi}{2}\left(1 \pm \sqrt{1-4.\frac{I_{RCavg}.X.r_t}{V_{in}.\pi}}\right) \tag{91}$$

Since the DAB is employed in this context to send power from the input voltage source to the load, then it is necessary to define the maximum power that can be transferred at certain operation parameters, which in turn identifies the limit for the output current that can be supplied to the load.

Maximum power transfer takes place when input bridge leads the output one by 90 degrees, thus the maximum power transfer can be derived from the analytical power expression in Eq. (21) to be

$$\therefore P_{\max} = \frac{V_{in}.V_o}{X.r_t}.\frac{\pi}{2}.\left(1-\frac{1}{2}\right) \tag{92}$$

$$\therefore P_{\max} = \frac{V_{in}.V_o}{X.r_t}.\frac{\pi}{4} \tag{93}$$

The average output power transferred to the load can be expressed in terms of load voltage and average output current as,

$$P = I_{RCavg}.V_o \tag{94}$$

Thus the ratio of the output power to the maximum is

$$\therefore \frac{P}{P_{\max}} = \frac{I_{RCavg}.V_o}{\pi.V_{in}.V_o/4.X.r_t} \tag{95}$$

$$\therefore \frac{P}{P_{\max}} = \frac{4.I_{RCavg}.X.r_t}{V_{in}.\pi} \tag{96}$$

Now, the final phase shift expression as a function of the output current can be reached by substituting this power ratio into Eq. (10)

$$\theta = \frac{\pi}{2}\left(1-\sqrt{1-\frac{P}{P_{\max}}}\right) \tag{97}$$

Therefore, it can be assured that for valid operation

$$1-\frac{P}{P_{\max}} \geq 0$$

Thus the condition that should be fulfilled is

$$P \leq P_{\max}$$

This analysis implies that the control action of the regulated represented in the commanded output current should be limited to the maximum achievable current specific to the operation parameters.

However, by studying the resulting current-to-phase relation, it can be concluded that the equation is non-linear representing the result of a square root function, thus linearization is necessary for improving the development of the reference phase shift angle from the corresponding load current control action.

4.3.2. Linearization

Linearization can be carried out in several manners, the most simple of which is the line approximation,

3.3.2.1. Line Approximation

Starting from the average output current calculated for the assumption of positive phase shift, $\theta > 0$,

$$I_{RCavg} = \frac{V_{in}}{X.r_t}.\theta.\left(1-\frac{\theta}{\pi}\right) \tag{98}$$

It is noticed that the output current is a function of the input voltage and the phase shift angle, thus for a certain fixed input voltage value, the average output current can be plotted as a function of phase shift angle, as was seen in Section 3.1.1.1, in Figure 41.

It is interesting in this context to plot the output current expression, Eq. (98), versus the phase shift for the exact test conditions, to attempt to reach a linearized equation that depicts the phase shift corresponding to a certain output current value.

Fig. 5 shows the variation of average output current depending on phase shift angle for 60 V input voltage level. This voltage level will be used for the initial tests of DAB converter under low power level, as will be explained ahead.

Studying the current waveform, an attempt to approximate that non-linear curve is to construct a straight line relationship. Conditions for this straight line are a zero phase shift at a zero output current, and 77 degrees phase shift for an output current of 0.7466 A, thus keeping a margin of around 15% from the maximum phase shift of 90 degrees. The line approximation is shown on the same figure, Figure 41, for clarification, and its equation is defined as follows.

$$\theta^* = \begin{cases} 0^\circ \rightarrow & I_{RCavg}{}^* = 0A \\ 77^\circ \rightarrow & I_{RCavg}{}^* = 0.7466A \end{cases} \tag{100}$$

$$\theta^* = I_{RCavg}{}^* . \frac{77}{0.7466} \tag{101}$$

$$\theta^* = 103.134 I_{RCavg}{}^* \tag{102}$$

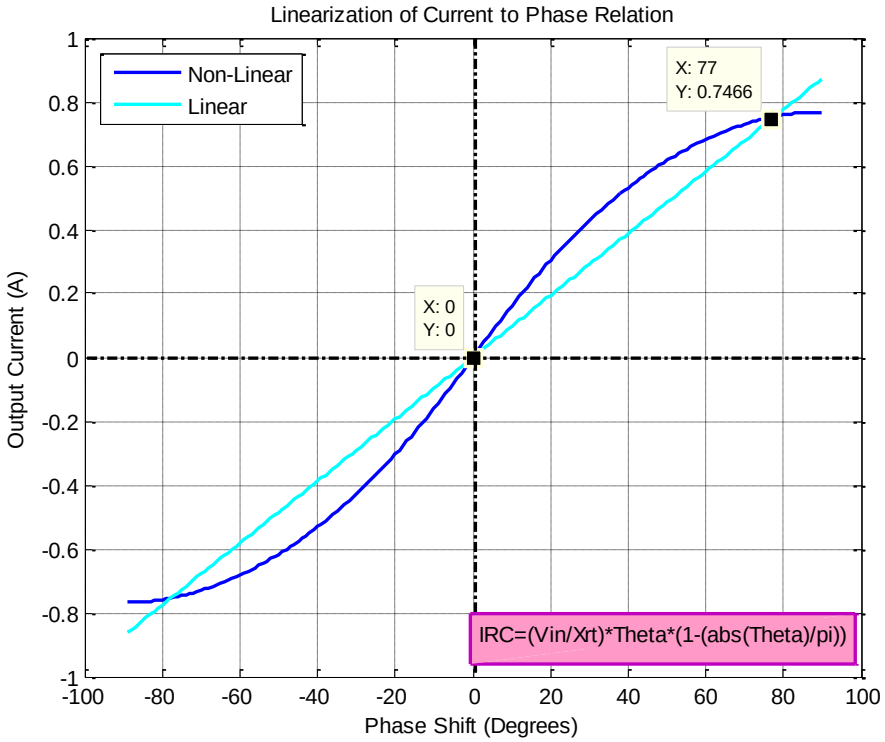


Figure 41: DAB Converter Calculated Output Current against Phase Shift and Linearization of the Curve Using Line-Approximation.

However, as can be seen observing Figure 42, the line approximated relation will always be dependent on the input voltage condition, thus an improved approach is to normalize the relation in the form that was introduced earlier through the analysis, Section 3.1.1.1, and stated here for convenience

$$I_{RCavg}\Big|_{norm} = \theta.\left(1 - \frac{|\theta|}{\pi}\right) \tag{103}$$

Line approximation is thus modified to the curve shown in Figure 43.

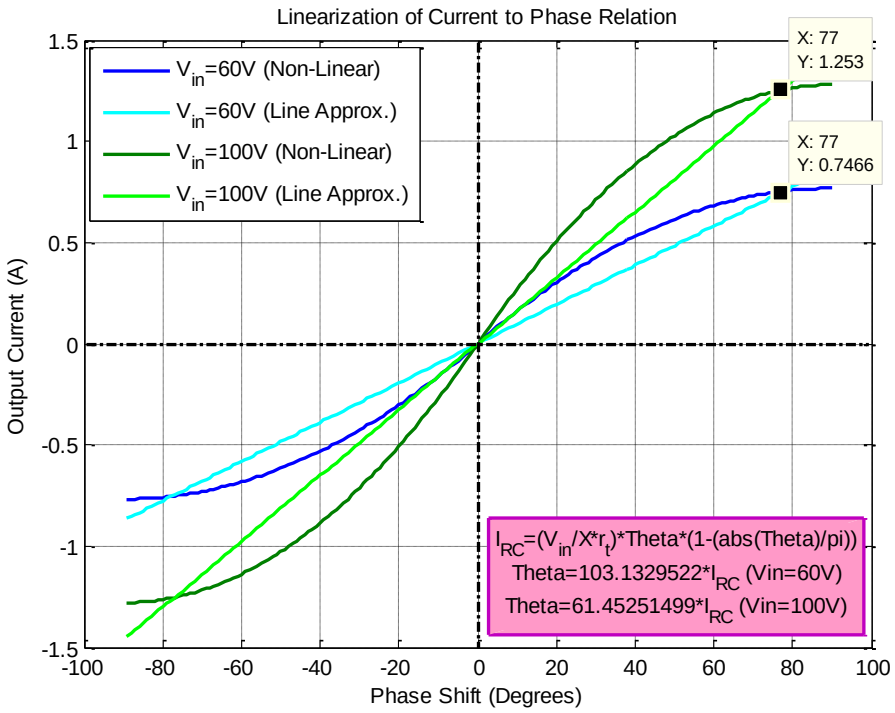


Figure 42: DAB Converter Calculated Output Current against Phase Shift and Linearization of the Curve Using Line-Approximation – Different DC Input Voltage Levels.

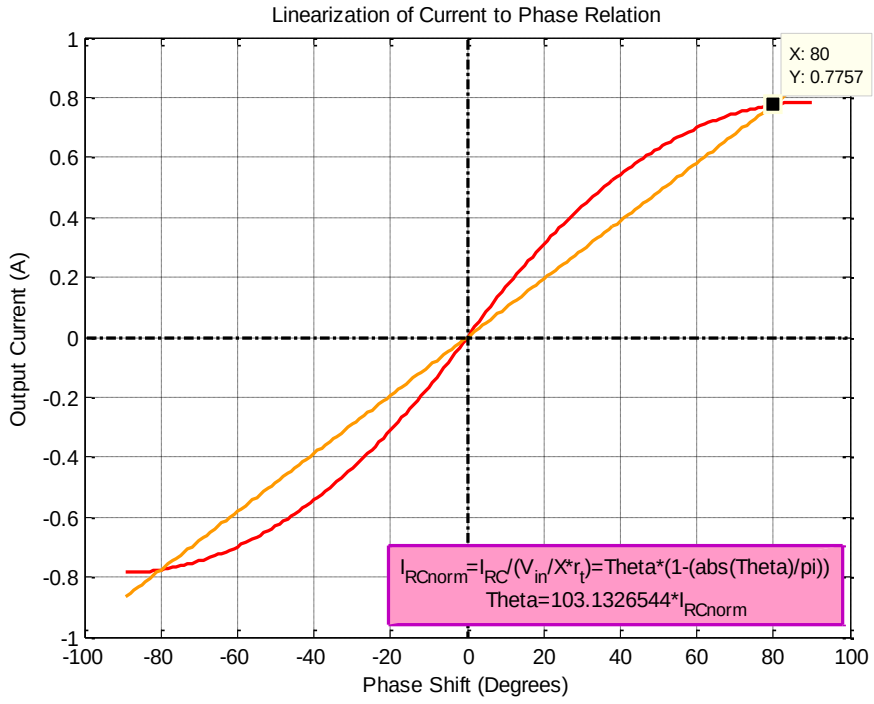


Figure 43: DAB Converter Normalized Output Current against Phase Shift and Linearization of the Curve Using Line-Approximation.

The line approximation is valid and allowable since the current-to-phase relation is regarded as a feed forward, which is simply a gain that assists the controller to track its reference quantity.

But although the line approximation spears the digital controller from suffering oscillations and unbalance due to computations of non-linear equations, on the other hand, it sacrifices the controller accurate reaction to fine variations.

It can be observed from Figure 44 and Figure 45 that the linearization solution reacts differently in both cases of transients. Thus another linear controller structure needs to be studied, namely the feed forward controller described by the diagram clarified by Figure 46.

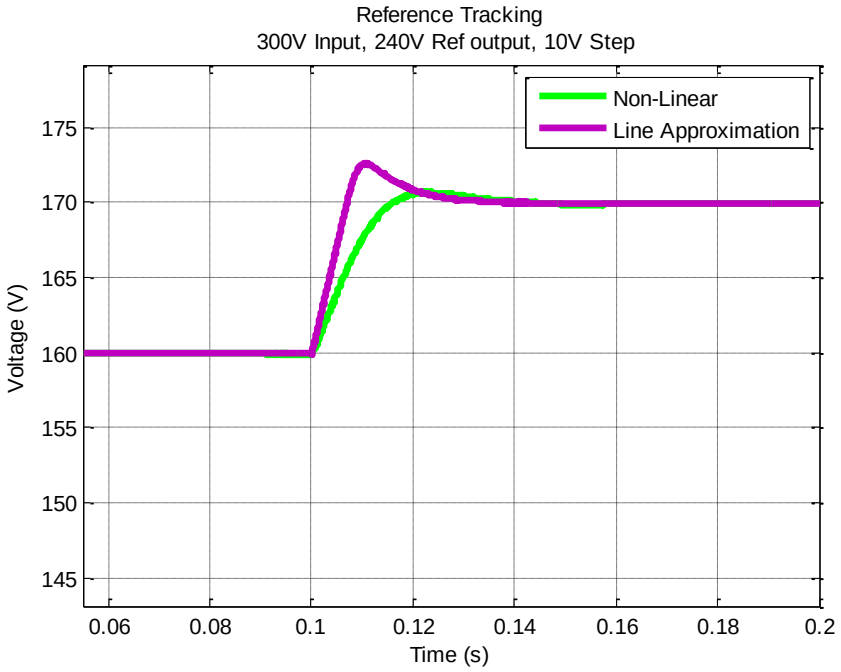


Figure 44: Non-linear Controller versus Linear controller Responses to a Step Variation of Voltage Reference.

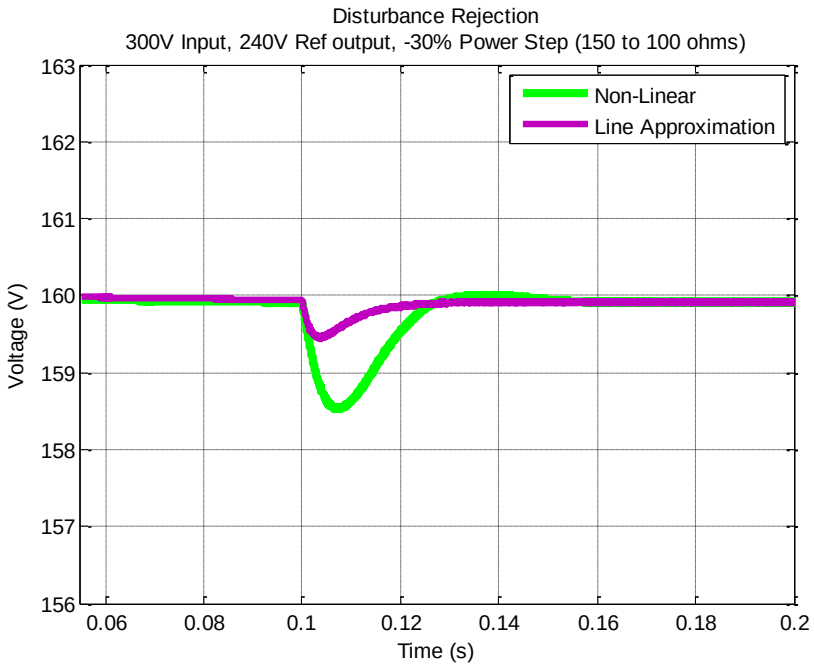


Figure 45: Non-linear Controller versus Linear controller Responses to a Load Disturbance.

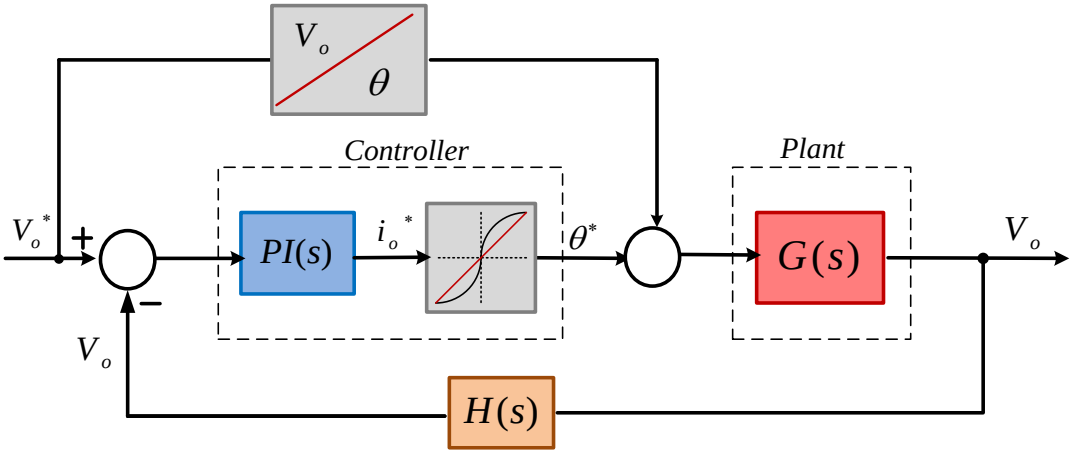


Figure 46: Feed-Forward Controller.

4.4.Controller Performance

After tuning the controller to the previously discussed design, it is of interest to assess the performance of the controller to transient events. The following sections study waveforms from the simulated switching model of the DAB converter topology under the discussed control strategy. The two previously discussed transient variations; variation of reference voltage and variation of load condition, are considered. The simulated operation conditions are matching those of the experimental ones discussed in Section 7.3.1, for the ease of comparison.

4.4.1. Reference Tracking

Figure 47 shows the output voltage response to a 10V increased step in reference voltage command. Observing the figure, the system voltage is seen to track the commanded reference with zero steady state error. The voltage response follows the selected bandwidth, 30 Hz in this case.

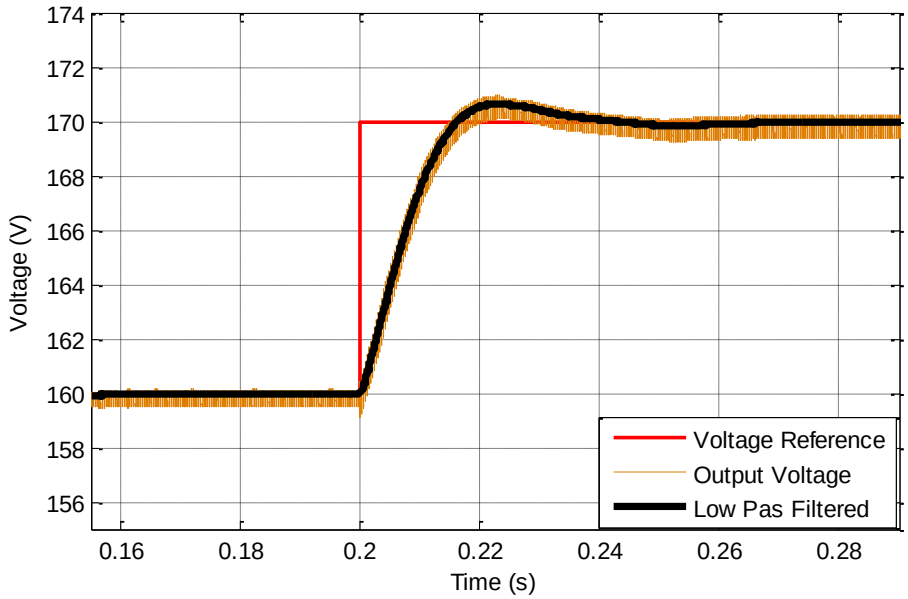


Figure 47: Reference Tracking – The Output Voltage Transient Response to a 10 V Step Variation in Reference Command.

4.4.2. Disturbance Rejection

Figure 48 illustrates the measured output voltage compared to the reference one as a response to disturbance introduced by varying the load condition. The controller is expected to fix the output voltage to the commanded reference.

The system is seen to ride-through the disturbance, encountering a relatively slight voltage drop while the controller successfully holds on the output voltage to the reference one.

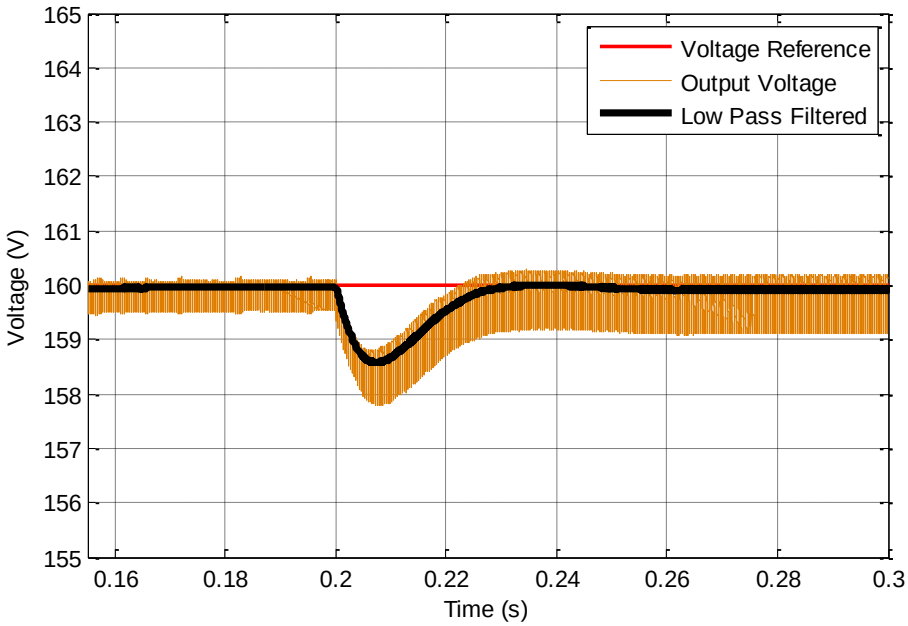


Figure 48: Disturbance Rejection – The Output Voltage Transient Response to a 30% Power Step due to Load Disturbance.

Chapter Five

5. Description of Simulation

Before validation on the experimental setup, the discussed principles are explored using simulations. Therefore, this chapter is dedicated to the simulations description, followed by another chapter to explain the design of experimental setup, together with some simulation results, which are employed to select the appropriate system components.

To simulate the behavior of the DAB converter, the simulation package PowerSim and Simulink from MATLAB were used.

It is necessary to precede some experimental tests with simulations of the physical tested system. This is desirable to accurately predict the behavior of system, and to allow exploration of applied modulation and control strategies, thus ensuring that equivalent results will be expected in practice. This saves time, and has significant safety benefits as well.

This section presents an overview of the simulation arrangement, along with some selected simulation results that serves as an initial examination of topology operation.

First, an ideal simulation was constructed, assuming all components are lossless. This simulation is basically used to study the behavior of the converter, its principles of operation, and to depict typical topology waveforms, which have also been introduced in previous sections for characterizing the topology.

The ideal simulation has also been employed to conduct the closed loop control ideas discussed in previous chapters, and thus predict the converter behavior under reference tracking as well as disturbance rejection.

After simulating the system under ideal conditions, it has been of interest then to develop the final simulation to be of closest match to the designed experimental system for the sake of comparing practical results with simulation ones thus validation of the constructed DAB converter.

Basically, the simulated system is composed of three main parts, i.e.:

a) Power Stage
b) Modulators
c) Closed Loop Controllers

5.1.Open Loop Ideal Simulation

The simulated power stage is divided into the DAB converter and the load, as shown in Figure 49. The DAB converter consists of two H-bridges, primary and secondary, with a

high frequency transformer as a link between both bridges. The real model of the transformer is implemented as shown in Figure 50. The converter is fed from an input DC voltage source, and transfers power to an output RC load, including the DC link capacitor of secondary H-bridge.

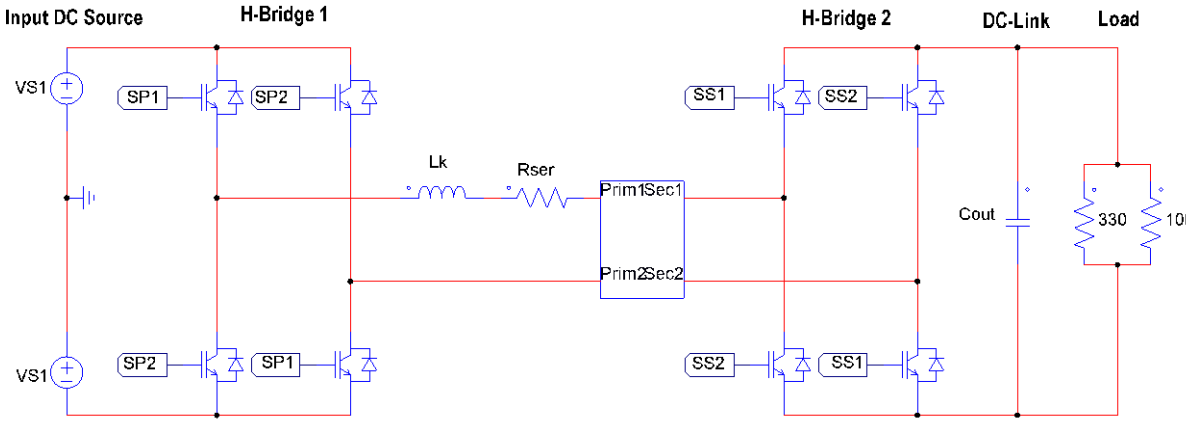


Figure 49: Dual-Active-Bridge Converter Switching Model.

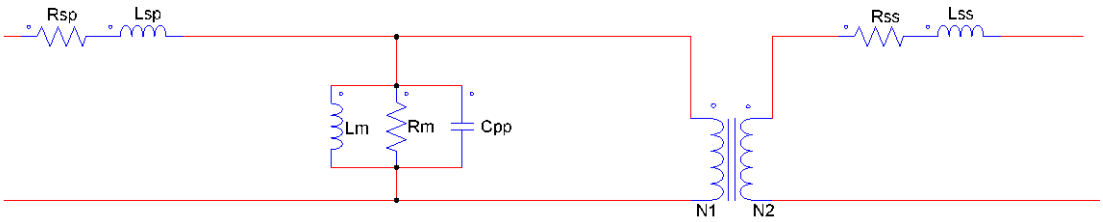


Figure 50: Real Transformer Model.

The firing pulses for the converter switches are generated by a modulator circuit. There are two bridges, and power transfer is achieved by shifting one bridge from the other, thus it is of interest then to have a modulator circuit for each bridge. The circuit consists of a comparator to compare the input modulation reference signal, to a triangular wave carrier signal of same frequency as the required switching frequency of the converter, as seen in Figure 51. Thus it gives rise to two firing complementary pulses for an H-bridge leg. The dead time is also generated between complementary signals, to include its effect on converter operation. The modulator circuit is shown in Figure 52.

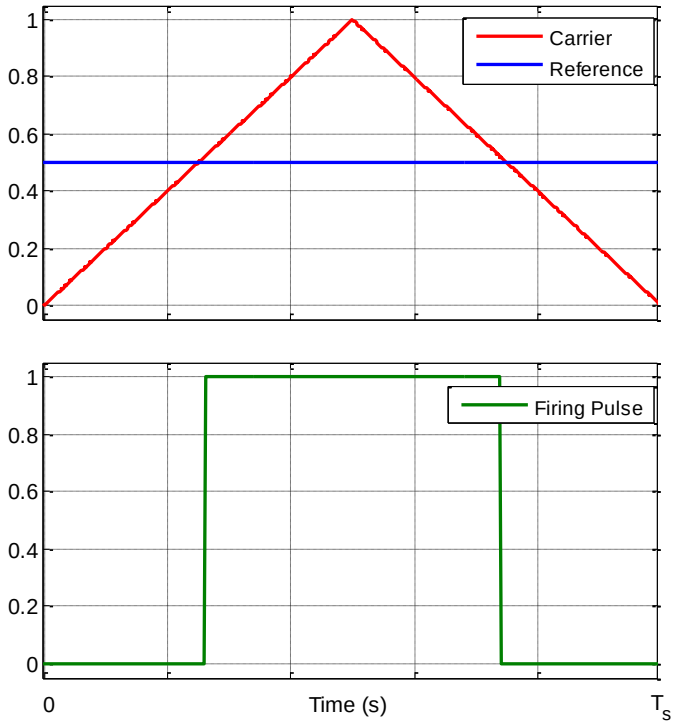


Figure 51: Block Modulation of DAB Converter – Generation of Firing Pulses for Modulation of Switches.

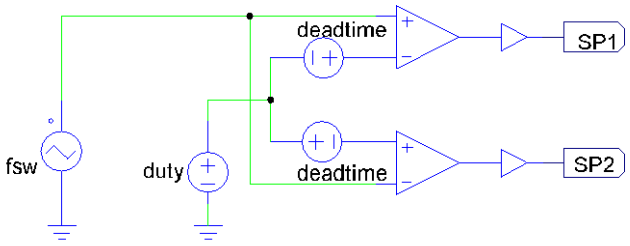


Figure 52: H-bridge Modulator.

5.2. Closed Loop Control Simulation

The previous chapter explained the structure of the closed loop control, and correspondingly, the PI controller is implemented in simulation as illustrated by Figure 53. Since the controlled parameter is the output voltage, thus it is measured and fed to the controller, while comparing with a commanded reference. The controller tuning parameters are adjusted with the values stated during the design, and the output control action (CA) is naturally the reference output current to the load.

The limitation signals, which indicate if the current exceeded the maximum value, are employed to reset the integrator each time a limit is hit. Those signals are generated by calculating the maximum output power, and consequently the maximum output current, then comparing the reference current to this value, as illustrated by Figure 54.

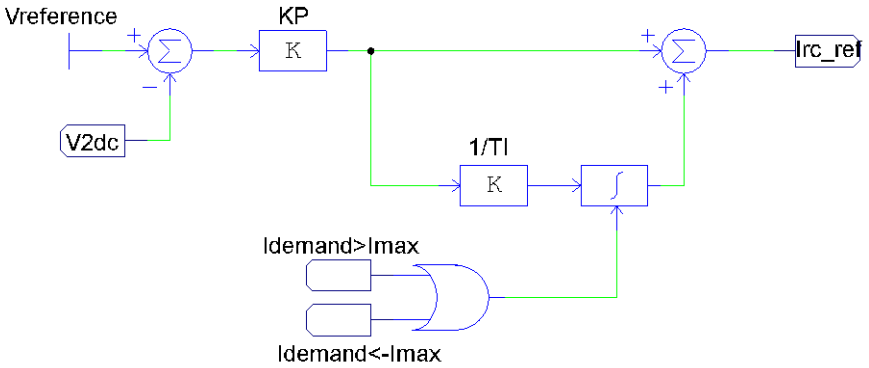


Figure 53: Closed-Loop Controller Implementation as Single-Loop Structure to Control the DAB Converter Output Voltage.

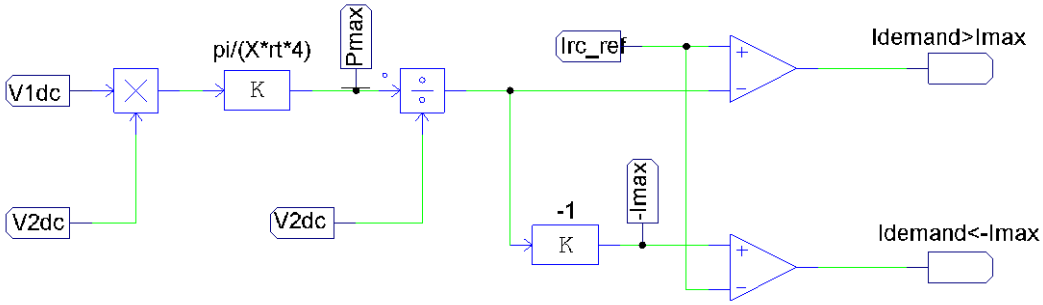


Figure 54: Calculation of Maximum Current.

The limitation signals are thus binary ones thus can be easily processed using a simplified C block, as seen in Figure 55 to select the reference current value, similar to a multiplexer block.

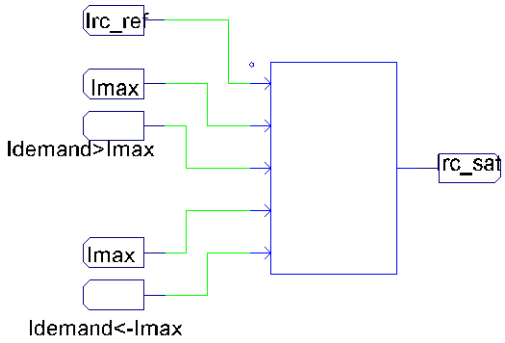


Figure 55: Saturation of Current Command to the Maximum Current Value.

The current reference is then transformed to a phase shift command through the previously derived expression, Section 4.3.1 Eq. (97), stated hereafter for convenience, and implemented as seen in Figure 56.

$$\theta = \frac{\pi}{2}\left(1 - \sqrt{1 - \frac{P}{P_{\max}}}\right)$$

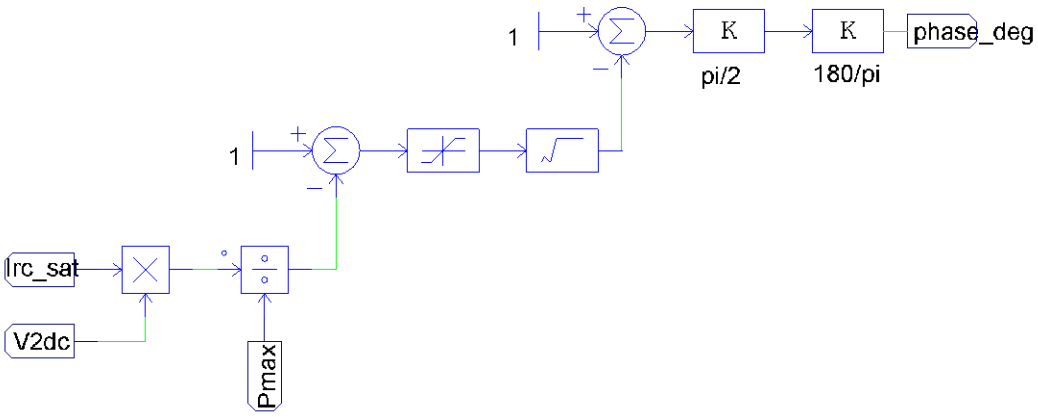


Figure 56: Non-Linear Current-to-Phase Relation.

The linearization mentioned in Section 1, is also implemented for the interest of comparison with non-linear one, as seen in Figure 57.

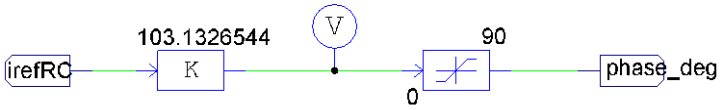


Figure 57: Current-to-Phase Relation – Linearization.

5.3. Real Simulation

The simulation model is sought to be of the most achievable match to experimental setup. This allows for accurate matching and validation of experimental results with simulation ones.

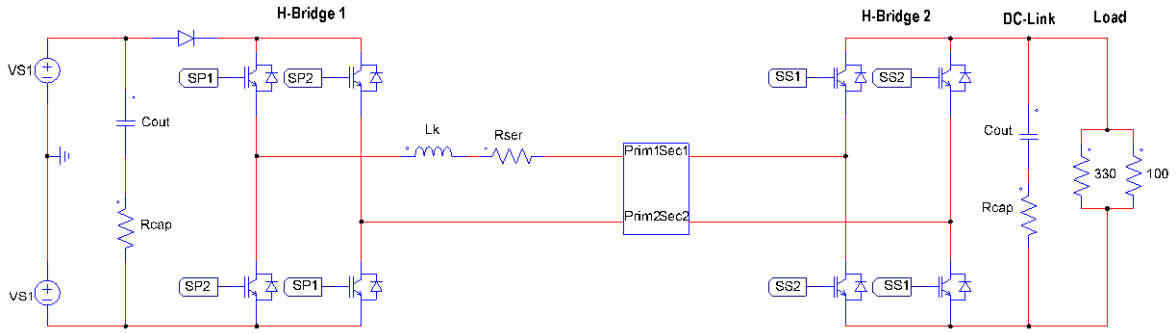


Figure 58: Real DAB Converter Switching Model – Model seeks to account for Losses that are expected to occur in practical converter, mainly inherent to IGBTs and Series Resistance of DC Links

Some loss elements in the model are further characterized with their accurate specification. IGBTs are employed with a freewheeling diode adjusted to the actual forward voltage specified for the experimental ones. A series resistance is added to the ideal capacitor banks to accurately emulate the experimental dc link capacitor banks. The modified model is shown in Figure 58.

Table 7: Real Converter Parameters

CIRCUIT PARAMETER	VALUE
Inverter IGBT Collector-emitter saturation voltage V_{CEsat}	$2.94V$
Free-wheeling Diode Forward Voltage V_F	$2.27V$
DC Link Capacitor Series Resistance ESR	$166m\Omega$
Rectifier Bridge Diode Forward Voltage V_F	$1.21V$

Also controller digital implementation imposes delays, which will be discussed later in the digital implementation, it is necessary then to account for those delays to result in a real controller behavior.

5.4.Simulation Based Analysis

5.4.1. Active and Reactive Power Variation with Phase Shift

Since power transfer takes place due to interaction between primary and secondary bridge AC voltages through a power transfer inductor, therefore, the inductor current phase angle does not always match that of the primary voltage. During one switching cycle, thus, an amount of the power is consumed by the load while the other amount is sent back to the source defining a reactive power component [89].

Similar to the fundamental active power flow equation, Eq. (21), the reactive power can be defined by AC phasor Theory to be

$$Q = \frac{\vec{V}_{f2}}{\vec{X}}.\left(\vec{V}_{f1}\cos\theta - \vec{V}_{f2}\right) \tag{104}$$

where is also the phase shift between the two bridges in a SPS modulation.

Thus, inevitably, as active power transfer takes place between the two bridges, also reactive power transfer will take place. Figure 59 shows the active and reactive power components with the variation of phase shift between bridges extracted from the converter simulation model.

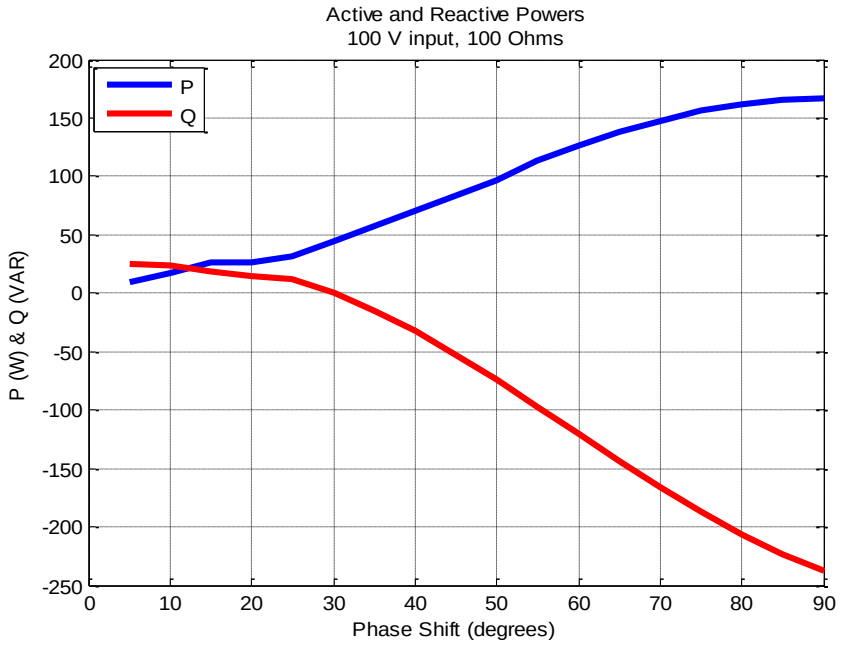


Figure 59: Simulation Results – Active and Reactive Power components for Different Phase Shifts.

Reactive power component is a lost power that must be minimized, thus the two following sections addresses two issues that affect reactive power within the converter.

4.4.2 Circulating Currents

For voltage magnitudes not matching transformer, $V1 << V2$ or $V1 >> V2$, circulating currents take place, and thus resulting in circulating power whose amount which depends

on the extent of mismatch. Figure 60 compares two cases; one is the ideal case with the voltages across the transformer are defined by the turns ratio, Figure 60a, and the other is a 60% mismatch between voltage magnitudes, Figure 60b.

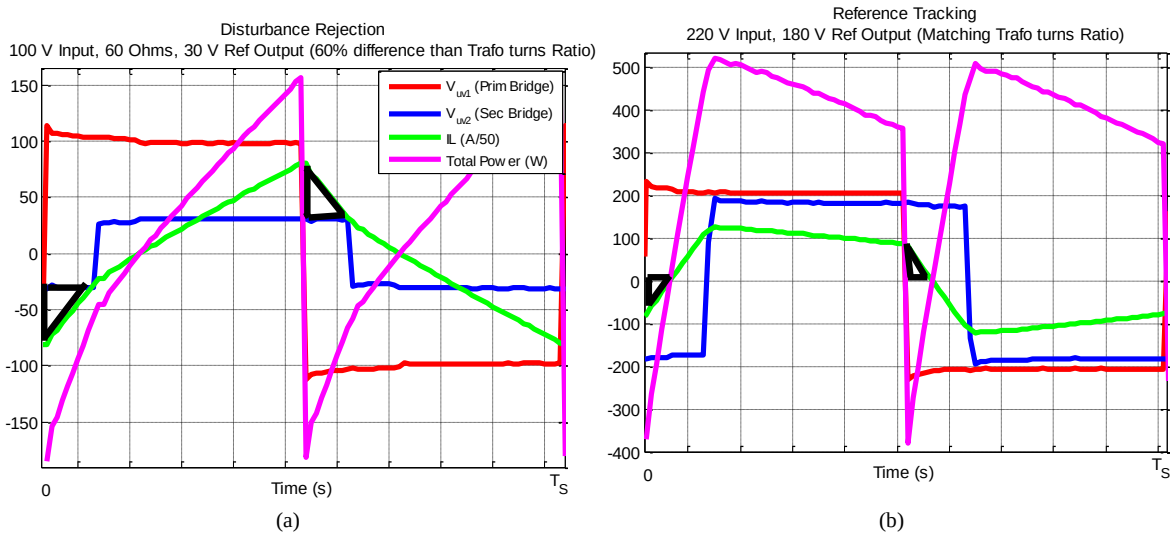


Figure 60: Output Voltages of Primary and Secondary Bridges, Inductor current, and Total Power transfer of DAB Converter for Two Operation Conditions, $V1 \ll V2$ or $V1 \gg V2$, indicating circulating Currents for both Cases, in Black.

In Figure 60a it can be seen that reduced phase shift results. This is due to lower transferred power than the ideal condition. Since the magnitudes of currents are hardly comparable by observing the plots, it is interesting to calculate, hence, the reactive power, and compare both cases. Figure 61 illustrates the total power calculated by multiplying AC voltage at the primary side of the inductor with the inductor current. Observing both accumulative areas it can be seen that the case of 60% mismatch it about 1.5 times that of exact match.

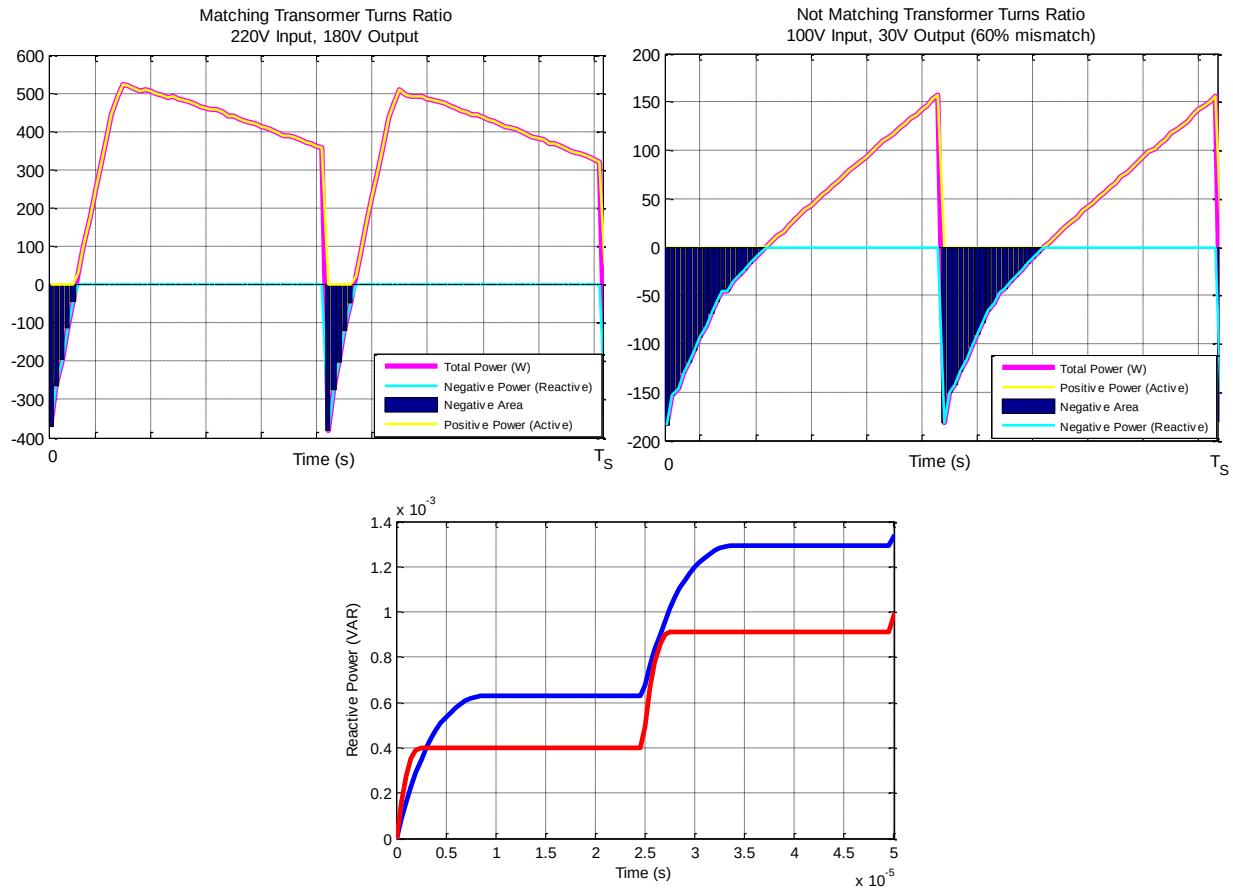


Figure 61: Total Power transfer of DAB Converter for Two Operation Conditions, $V1<<V2$ or $V1>>V2$, Comparing the Amount of Reactive power, indicating by the Blue area.

This study implies that the best ratio between the input and output voltage magnitudes is the transformer turns ratio. This latter conclusion sets a basis for a number of design criteria that will be followed in the next sections for practical system design.

4.4.3 Dead Time Effect on Power Transfer

The basic characterization of the DAB converter in the previous chapters did not consider the effect of the dead time. In practical implementation, the dead time is necessary to be introduced between switches of the same leg, to avoid shorting on the supply. Literatures [99] - [102] discussed the dead time effect, as well as its control methods to increase efficiency. In principle, two main effects are caused by dead time, voltage polarity reversal, and voltage sag. The power transfer characterization is thus deformed from the ideal case, as shown in Figure 62. Also Figure 63 shows bidirectional power transfer for a higher power level. Later on, in Section 7.3.2, the practical DAB converter is put under different dead times to study the dead time effect on reactive power level.

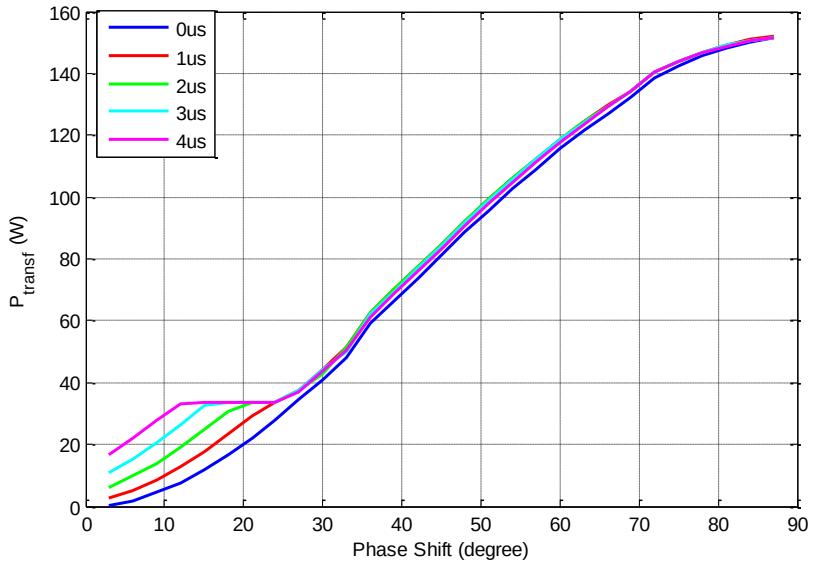


Figure 62: Power Transfer of Simulated DAB Converter against Phase Shift for Different Dead Times.

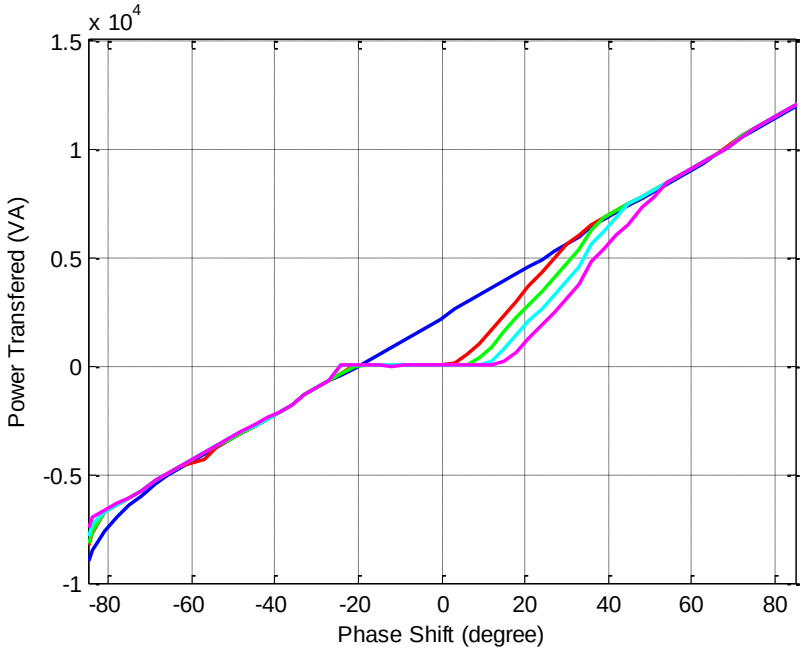


Figure 63: Power Transfer of Simulated DAB Converter against Phase Shift for Different Dead Times – Bidirectional Power flow.

Chapter Six

6. Experimental System Design

After implementation of the simulation platforms, and verification of the studied concepts, the design of the DAB converter prototype can be carried out in the light of the derived system equations and backed by the required simulation results.

Figure 64 shows a circuit diagram of the constructed converter platform. The constructed platform can be mainly divided into the power stage, the programmer software, and the programmer hardware. Each of these will be discussed in detail throughout the chapter. Also Figure 65 illustrates the final constructed experimental platform for practical testing of the DAB converter, and validating its operation against the analytical studied concepts.

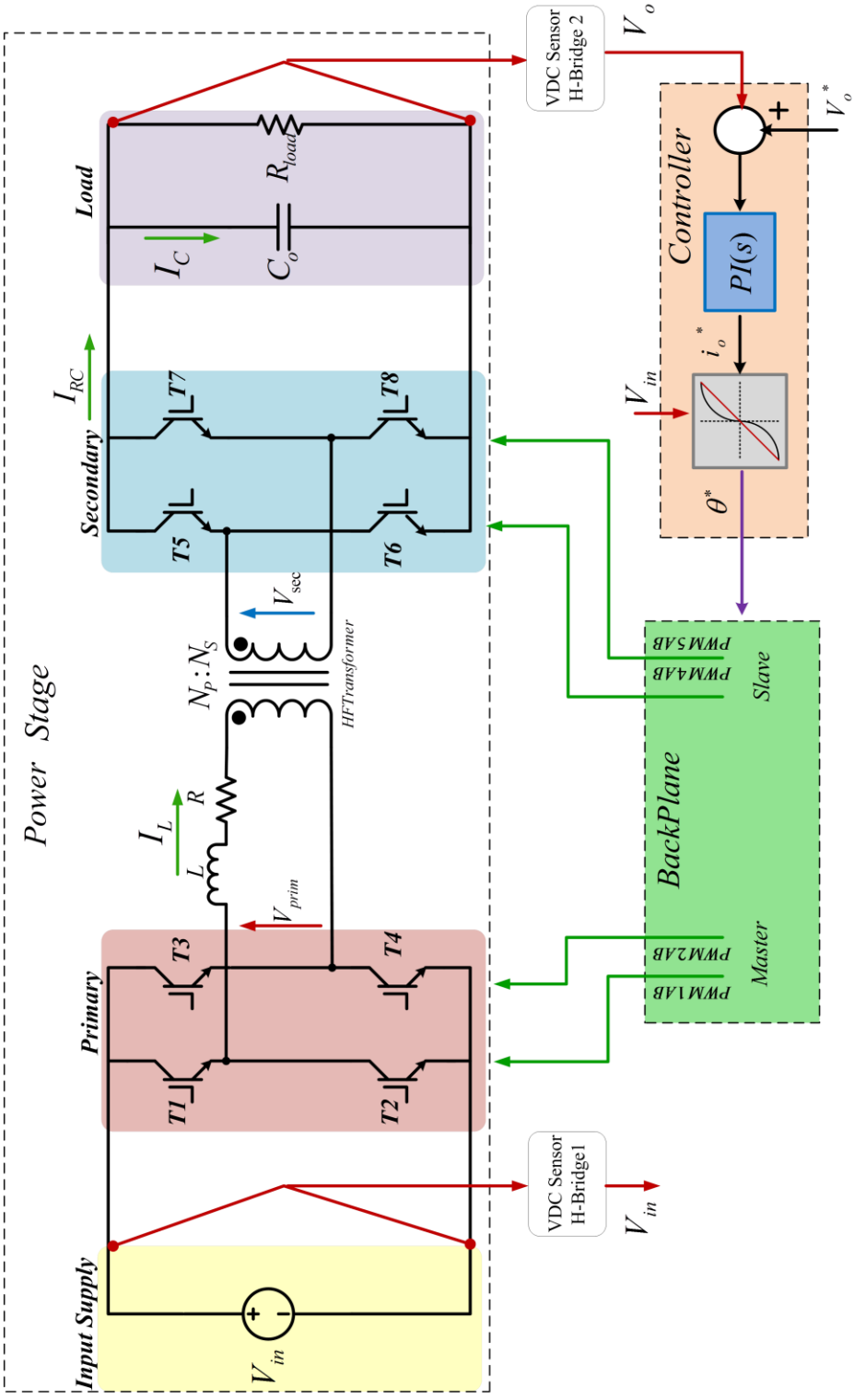


Figure 64: DAB Converter System Diagram.

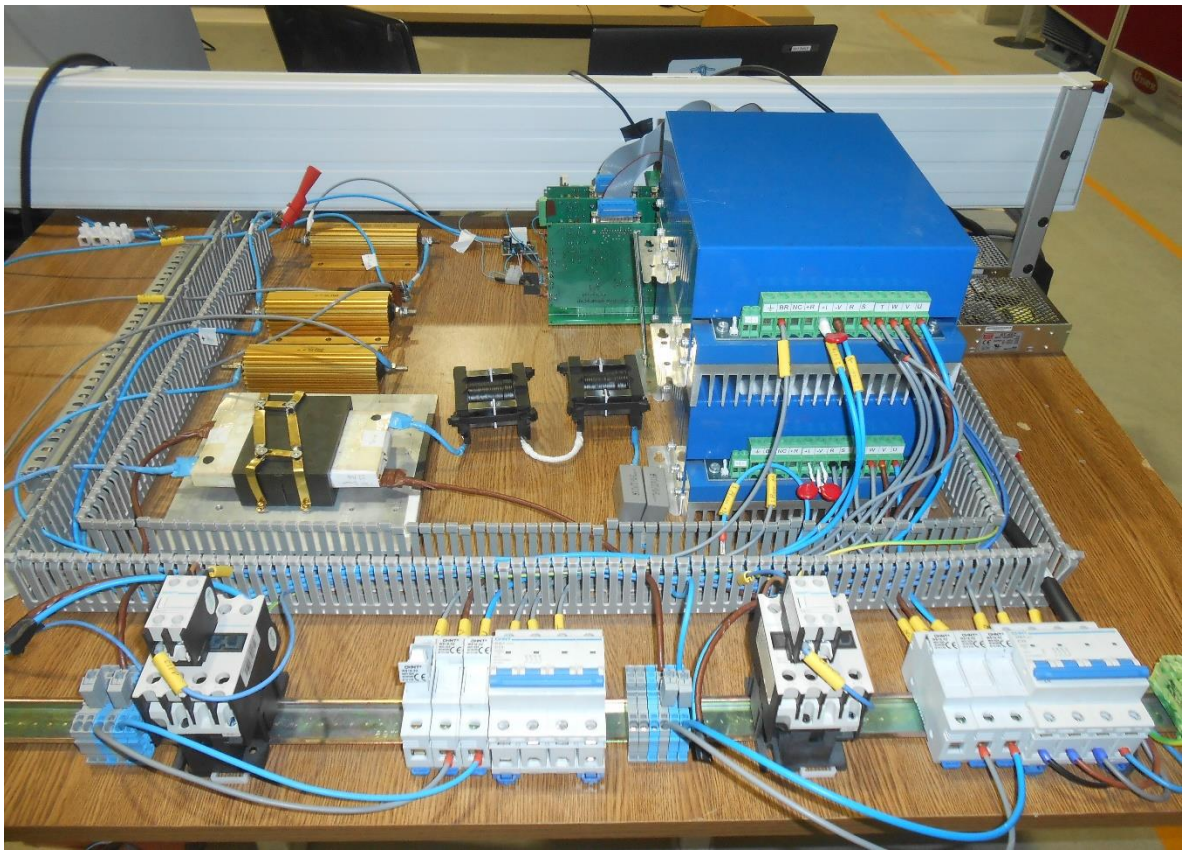


Figure 65: Constructed Experimental Platform for Practical Test of DAB Converter.

The converter is tested on two power levels; first, low power transfer, up to 300 W, and second, higher power transfer, up to 2kW. The low power test serves as an initial test stage for analyzing the real converter principle waveforms, and verifying the studied simulation models.

6.1. Power Stage

6.1.1. Input Supply

For the tests performed at low power levels, the power supply used was a *BK PRECISION* 1672 DC supply with a maximum of 66 V, shown in Figure 66. The power supply provides a current of maximum 3 A. Initially, the supply is adjusted for 60 V, for clarity of calculation figures and simplicity of observing results.

Figure 66: *BK PRECISION* DC supply with a Maximum of 66 V.

For higher VDC and power levels experiments (above 60V/3A) an autotransformer is employed. The autotransformer ratings correspond to a nominal phase-to-phase RMS voltage of 440V. Employing the autotransformer with a three-phase 6-diode rectifier bridge within the inverter stack, a maximum DC voltage of 620V can be obtained at the output of the bridge.

6.1.2. Power Converter

This section describes the converter main components, namely the input and output H-bridge inverters, the power transfer series inductor, as well as the HF transformer. Then, since a real converter implementation always implies losses in several system components, an estimation for these losses is provided, to allow for a better design process. And finally, employing this loss estimation and considering other safety and topological limitations, a study is performed to define the maximum power that can be transferred by the constructed converter.

6.1.3. Converter Main Components

6.1.3.1. Input and Output H-Bridges

The DAB power converter topology is constructed using two GUASCH*MTL-CBI0010N12IXFE* Converter-Brake-Inverter power stacks, shown in Figure 67, each inverter consists of a 3-phase diode bridge, a capacitor bank, and a 3-phase bridge inverter. Figure 68 shows the circuit diagram of the device. The power stack general specifications are stated in Table 8.

Figure 67: GUASCH *MTL-CBI0010N12IXFE* Converter-Brake-Inverter Power Stack.

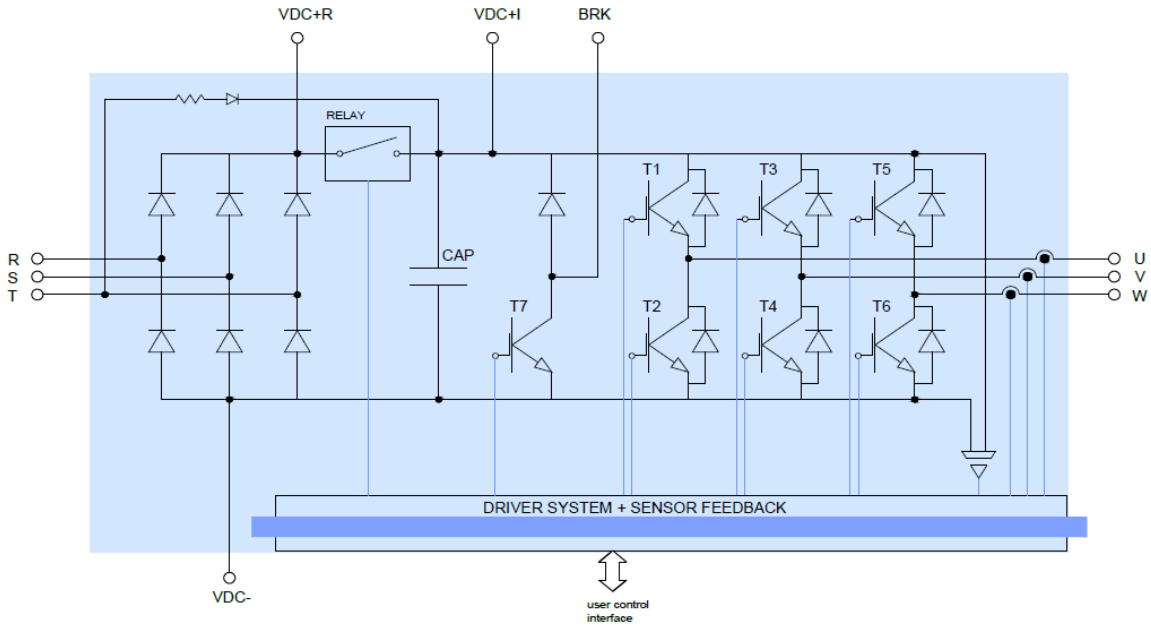


Figure 68: The circuit diagram of the Inverter Stack.

Table 8: GUASCH Inverter Specifications

SPECIFICATION	VALUE
Manufacturer	GUASCH
Maximum Input AC RMS voltage	460V
Maximum DC Bus Voltage	750V
Output RMS Current per Phase (f_{sw}=10kHz, 400V, f_o=50Hz)	9A

The maximum power that can be handled by the inverter power stack can, thus, be calculated from its manufacturer's specifications, depicted in Table 8, as follows.

$$S_{\max} = \sqrt{3}.V_{PH-PH}\big|_{rms}.I_{rms} \tag{105}$$

The maximum phase-to-phase RMS converter voltage can be defined based on the maximum converter DC-Bus voltage to be

$$V_{PH-PH} = \frac{V_{DC-Bus}}{2}.\frac{\sqrt{3}}{\sqrt{2}} = \frac{750}{2}.\frac{\sqrt{3}}{\sqrt{2}} = 459.3V \tag{106}$$

While also the maximum output RMS current per phase is given to be

$$I_{\max}\big|_{rms} = 9A$$

$$\therefore S_{\max} = \sqrt{3} * 459.3 * 9 = 7159.7W$$

The maximum power that can be handled by each inverter can, hence, be approximated to 7kW.

From each of the two power stacks, for initial low power tests the rectifier bridge is bypassed, thus each inverter bridge contributes by two legs to form the topology input and output H-bridges. Also for protecting the input power supply, the DC link capacitor of the inverter bridge is fed via one diode leg, namely *R* phase, instead of directly charging through the access terminals, *VDC+R* and *VDC-*, shown in Figure 68.

6.1.3.2. High Frequency Transformer

The High frequency link is achieved by the use of HIMAG High Frequency Planar Transformer, Figure 69, the main specifications of which is stated in Table 9.

Figure 69: HIMAG High Frequency Planar Transformer.

Table 9: High Frequency Planar Transformer

CIRCUIT PARAMETER	VALUE
Manufacturer	HIMAG
Total Output Power	10kW
Switching Frequency	20kHz
Turns Ratio (Prim:Sec)	22:18

The transformer was put under two tests for identifying its impedance model, and the estimation of its parameters, a no-load test, and a short circuit test using an impedance analyzer.

Only the final impedance model along with the estimated model parameters are stated in Figure 70, and Table 10 respectively.

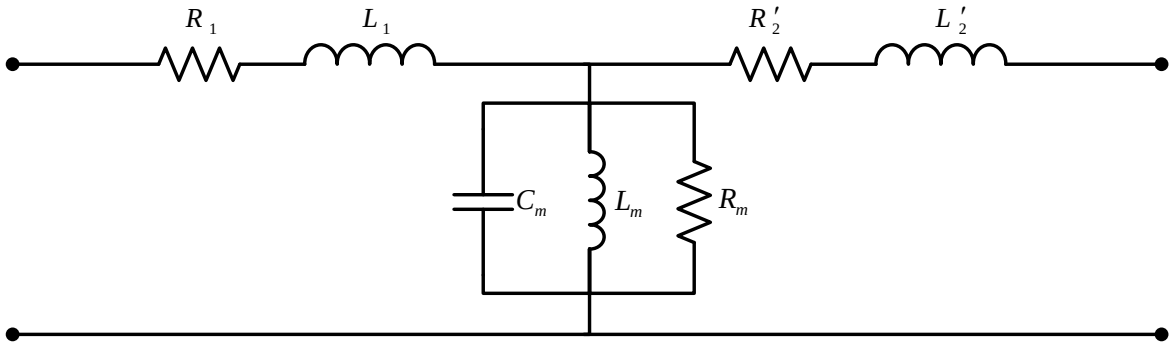


Figure 70: Impedance Model of the High Frequency Transformer.

Table 10: Estimated Parameters of High Frequency Transformer Model

CIRCUIT PARAMETER	VALUE
R_1	0.2Ω
L_1	$2.5\mu H$
R'_2	0.2Ω
L'_2	$2.5\mu H$
R_m	$188.2k\Omega$
L_m	$7.044mH$
C_m	$0.2388nF$

Moreover, the transformer is fixed to a heat sink for two reasons, tightly holding the transformer to avoid any vibration resulting in ringing sound, as well as increasing heat transfer surface thus cooling the transformer.

Magnetic Core Saturation of high frequency Transformer

During simulation, no system asymmetry could be detected, however, when regarding practical converter implementation, the problem of saturation must be addressed and avoided.

In isolated DC/DC converters, with the semiconductor switches tolerances, many reasons can provide excitation to a transformer, such as [103]:

- unmatched turn-on/turn-off times,
- semiconductor forward voltage drop,
- gate driving signal delays,
- insufficient pulse width modulation (PWM) resolution, or
- Pulsating load.

Figure 71 illustrated two AC waveforms mismatch conditions compared to the ideal case. Additionally, there is an increased motivation to address this issue since the adopted control strategy is an output voltage control, thus cannot assure a fixed amount of DC inductor current, thus more likely to have a DC component of magnetic flux.

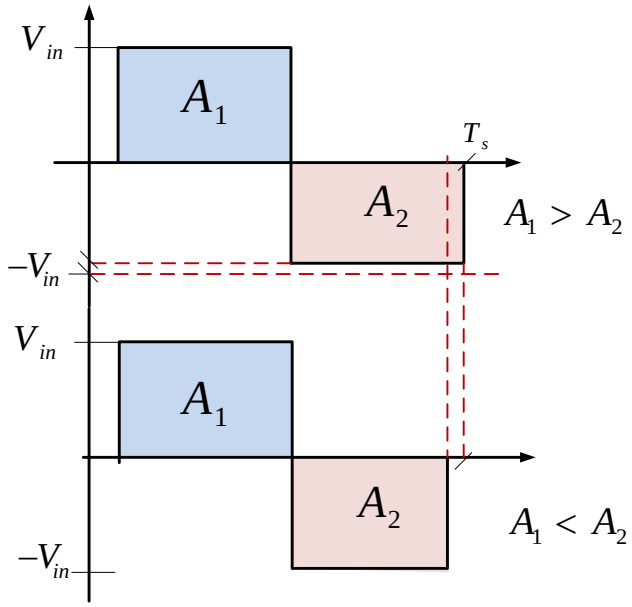


Figure 71: Two AC waveforms mismatch conditions due to asymmetries in a Practical Converter.

These phenomena among others can cause differences in the positive and negative volts–seconds applied to the transformer. This result in a dc-voltage component at the transformer terminals, which is translated into an undesired dc magnetic flux density component in the transformer core, however small this component might be, flux could build up driving the magnetic core to saturation [77] [103], as clarified by Figure 72.

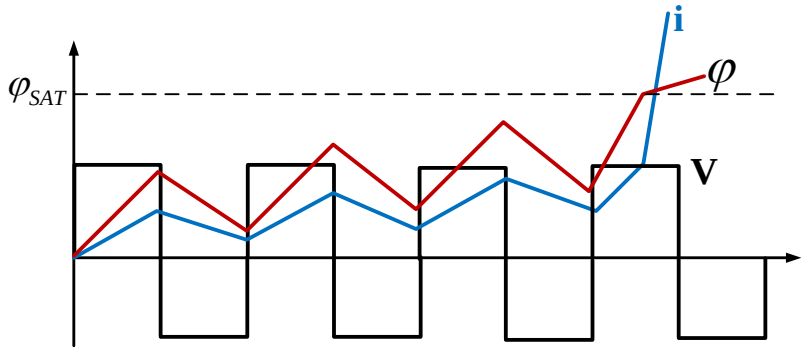


Figure 72: Flux DC Bias Leading to Saturation [77].

To show the relation between this voltage and magnetic flux density dc components, Ortiz et al. studied the case of a DAB converter depicting an equivalent model of the converter with independent dc and ac voltage sources.

This DC magnetization is limited by the equivalent series resistance of the circuit. And as efficiency is a key aspect in high-power applications, a small equivalent series resistance is desired in order to reduce losses. This in turn increases the risk of reaching high DC magnetization in the core and thus driving it into saturation.

Moreover, it is not always a risk of saturation, since the flux density in the core can still be biased without being saturated, and therefore, the core losses are increased. Thus the issue is of interest to study, and select a technique to avoid its effect.

A. Measurement and Detection Techniques

1. Detection of Saturation

Some previous concepts were proposed to detect saturation, such as using an *E-core with air gap in external leg*, studied in [104]. Also, in [105], *reduced cross-section and additional magnetic path* was used.

2. Dynamic Flux Measurement

This method was proposed in [106], which detects dynamic variations of flux by performing integration for the applied voltage in an additional RC network.

3. Continuous Measurement of Flux Density

This method is based on sensing of flux behavior, which has a vast fortune of research literature. In [103], a brief review of the main sensing and measurements techniques has been given pointing out the main advantages and disadvantages of each. The most direct method is the use of a Hall sensor in the path of the magnetic path [107]. Also by measuring the magnetizing current, the status of the core flux density can be detected [108].

However, another way is to process the measured currents at either sides of the transformer in terms of Fourier components, which are then feedback to balance the flux [109].

B. Solutions

1. Passive balancing

The passive balancing indicates a technique that does not update the converter switching signals for assuring limited transformer flux. The main passive balancing techniques are:

- Adding a series capacitor to the transformer blocks any DC voltage component from the transformer.
- Employing modulation techniques to ensure a ZVS, thus compensating a part of the mismatch in volt-seconds applied to the transformer [110] [111].
- Adding an Air-gap in the magnetic path reduces the equivalent permeability of the core. Therefore, a DC component in the magnetizing current generates a smaller DC flux density component.

2. Active Feedback Control of Flux

The main active feedback concepts have been proposed in [106] [112] [113] [107] [114], a signal proportional to the core flux density is necessary, depending on which an active modification of volt-second applied to the transformer can be achieved.

Figure 73 shows a typical waveform due to saturation problem caused by asymmetry of AC voltage waveforms, leading to an obvious DC current component, thus the flux builds up until saturation.

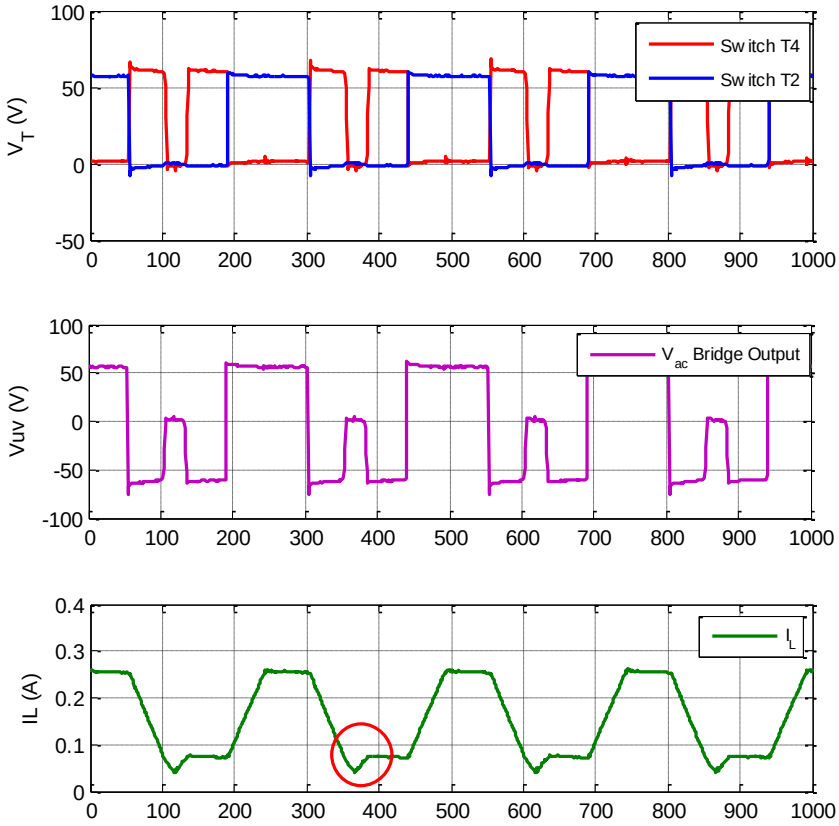


Figure 73: Magnetic Core Saturation.

To tackle the probable danger of saturation of high-frequency transformer, the simplest solution of adding a series capacitor is employed. This capacitor blocks any DC voltage value from reaching the transformer, thus ensuring no saturation takes place. The capacitance value is selected to be relatively high to assure no resonance takes place within the circuit defined by the series capacitor and inductor, and the magnetizing inductance of the transformer. Designing a resonant converter is a future step to be taken, for its possible benefits discussed in Section 2.1.1.

6.1.3.3. Power Transfer Inductor

Since the inductor is custom made for the application, the process targets an optimum design, minimizing size and losses.

Losses can be mainly divided to Low-Frequency (LF) and High-Frequency (HF) copper losses. Minimizing LF losses implies a larger wire diameter, thus making use of the maximum core window area.

On the other hand, HF losses due to skin effect, clarified by Figure 74, imposes a condition that any wire diameter should not exceed twice the skin depth, thus invalidating the solution of increasing the wire diameter, pushing forward another solution of using Litz wire, thus each turn is split into several wires in parallel, thus keeping the skin depth

condition. While also HF losses due to proximity effect, clarified by Figure 75, implies that losses due to external magnetic fields increase exponentially with the number of layers in a winding, thus invalidating the solution of using maximum core window area [77], and favors larger core size.

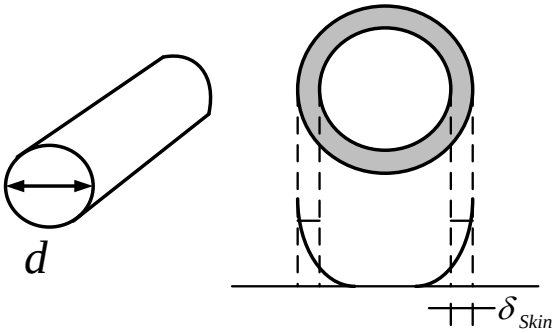


Figure 74: Inductor Design – Skin Effect.

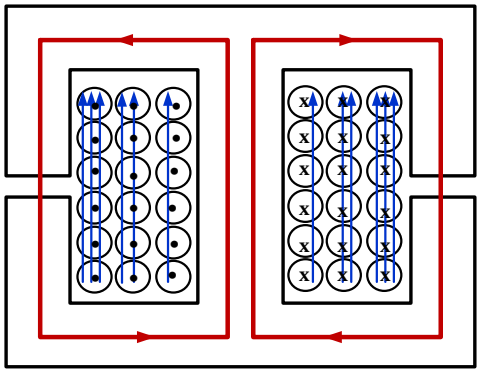


Figure 75: Inductor Design – Proximity Effect, in *Red* is the Magnetic Flux, and in *Blue* the Induced Field in the Windings.

Taking this discussion into consideration, the direction for decreasing the total losses is concluded to be a compromise between LF, HF losses, and core size. As proximity effect is responsible for the major amount of HF losses, a general procedure, hence, is to use smaller wire diameter, thus reducing the number of winding layers, and allowing for a minimized core size, while compromising a little higher LF losses.

As mentioned before, the practical tests are carried out on two power levels, thus for the initial lower power tests *a Single Core Inductor with Multilayer winding* is designed, and for the higher power tests a *Two-Core Split Inductor* is designed, which is also favored for future application where bi-directional power flows, thus a better power handling by placing each inductor at primary and secondary transformer sides.

In the latter case of a two-core inductor design, it can thus be interesting to compare two design options: a *Single-wired One-layer inductor*, and *a Litz-wired Multi-layer inductor*, Figure 76. Then, concluding the best combination in terms of least total losses.

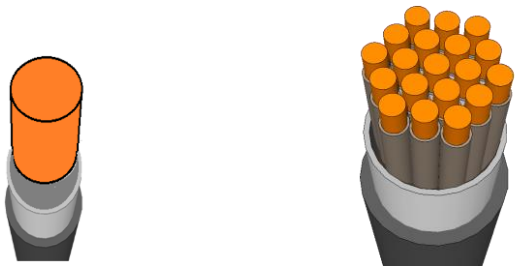


Figure 76: Inductor Design – Single versus Litz Wire.

In both cases, the design procedure is the same, and the objective design parameters are specified based on the application requirements as explained below.

The inductance is chosen to allow for the maximum power to be transferred, thus calculated as follows. Making use of the ac power transfer equation for the DAB converter, Eq. (37),

$$P = \frac{V_{in}.V_o}{X.r_t}.\sin\theta$$

$$\therefore P_{\max} = \frac{V_{in}.V_o}{X.r_t} \tag{107}$$

Recalling that the best ratio for minimizing reactive power was concluded to be the transformer's turns ratio, thus the voltage across inductor terminals is considered to be equal yielding the final equation of

$$P_{\max} = \frac{V_{in}\big|_{\max}^{2}}{X} \tag{108}$$

$$7159.7 = \frac{750^2}{X}$$

$$X = 78.56\Omega$$

Under a switching frequency of $20kHz$, the resulting inductance can be depicted as follows.

$$w.L = 78.56\Omega$$

$$L = \frac{78.56}{2*\pi*20000} = 625\mu H$$

Therefore, the inductor input design parameters are similar for both compared options, and are stated in Table 11. A general design procedure is followed as clarified by Figure 77.

Table 11: Input Design Requirements OF Power Transfer Inductor

SPECIFICATION	VALUE
Inductance L	$600\mu H$
Power Level	$7kW$
Maximum Inductor Current Ripple	$20A$
Operation Frequency	$20kHz$
Core Material	$3C85$

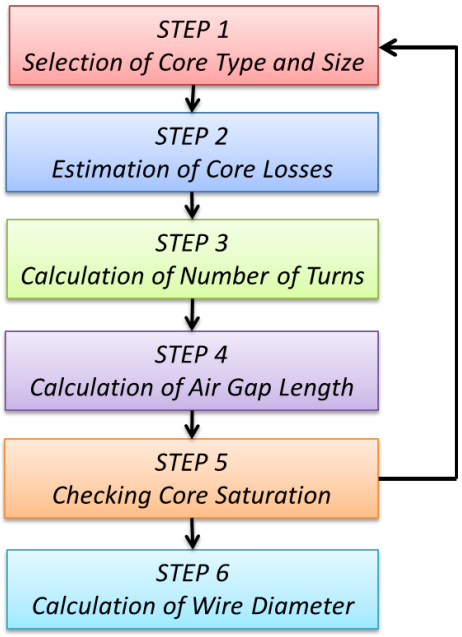


Figure 77: Inductor General Design Procedure.

(a) Single Core Inductor

Following the design procedure depicted in Figure 77, a summary of the design output was an inductance of $597\mu H$ with an equivalent series resistance of 1.397Ω.Thus the total impedance of the inductor

$$Z = \sqrt{X^2 + R_{ser}^2} \tag{109}$$

$$Z = \sqrt{(2 * \pi * 20000 * 597e^{-6})^2 + (1.397)^2}$$

$$Z = \sqrt{(75.021)^2 + (1.397)^2}$$

$$Z = 75.034\Omega$$

It can be seen that the inductor series resistance can be neglected compared to the inductor total impedance, thus during the following calculations the inductor impedance is denoted by X, and given the value 75Ω.

The inductor design outputs are stated in Table 12, and the final design is illustrated in Figure 78.

Table 12: Output Design Specifications OF Power Transfer Inductor

SPECIFICATION	VALUE
Inductance L	$597\mu H$
Core Type	ETD59
Number of Turns	88 turns
Number of Layers	2 layer
Equivalent Series Resistance	1.379Ω

This inductor design presents relatively high resistive losses, which are acceptable at lower power level. However, as the power level increases these losses becomes significant causing heating of the inductor, and reduce the efficiency of the converter.

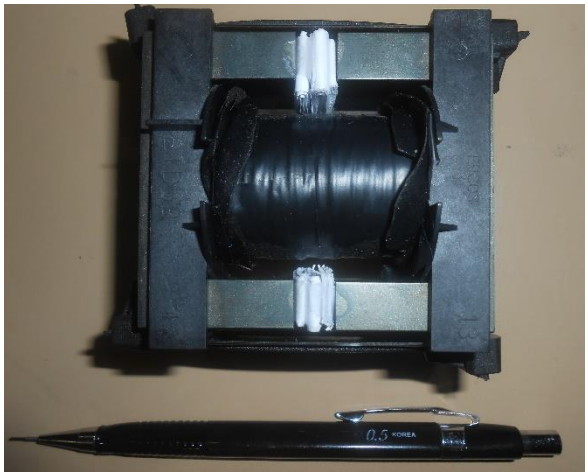


Figure 78: Designed High Frequency Inductor – Single Core.

(b) Two Core Inductor

Similarly, the design procedure depicted in Figure 77 is followed, targeting the same input design requirements, however, splitting the design on two cores that are intended to be in series, i.e. 300uH each. For this case, it interesting to compare two design options, being the single wire, and the Litz wire. Then based on the comparison, the best combination of both options are undertaken for implementation.

Single-wire Wound Inductor

Output design parameters are depicted in Table 13.

Table 13: Output Design Specifications OF Power Transfer Inductor.

SPECIFICATION	VALUE
Inductance L	$300\mu H$
Core Type	ETD59
Number of Turns	35 turns
Number of Layers	1 layer
Equivalent Series Resistance	0.2664Ω

Litz-wire Wound Inductor

Output design parameters are depicted in Table 14. And the constructed Inductor is shown in Figure 79.

Table 14: Output Design Specifications OF Power Transfer Inductor.

SPECIFICATION	VALUE
Inductance L	$300\mu H$
Core Type	ETD59
Number of Turns	35 turns
Number of Layers	1.2 layers
Equivalent Series Resistance	0.07751Ω

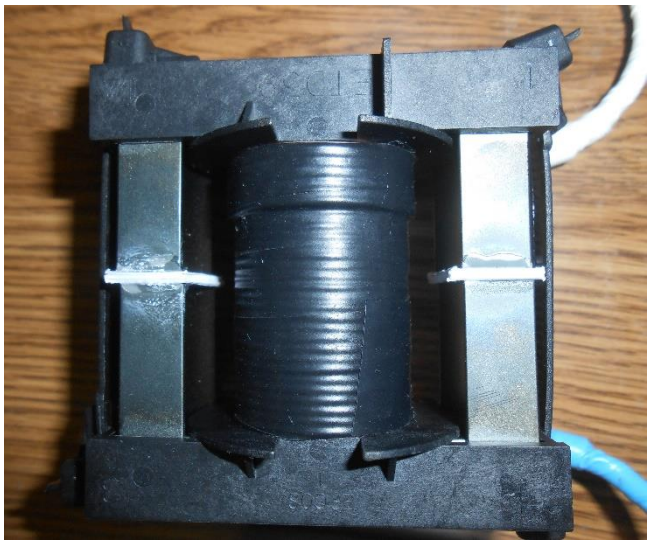


Figure 79: Designed High Frequency Inductor.

Comparing both wire types, Figure 80 shows the ohmic losses of the windings for each wire type, before mounting the magnetic core, based on the previous discussion, and provided that similar designs are implemented especially with equal number of turns, a comparison can be performed.

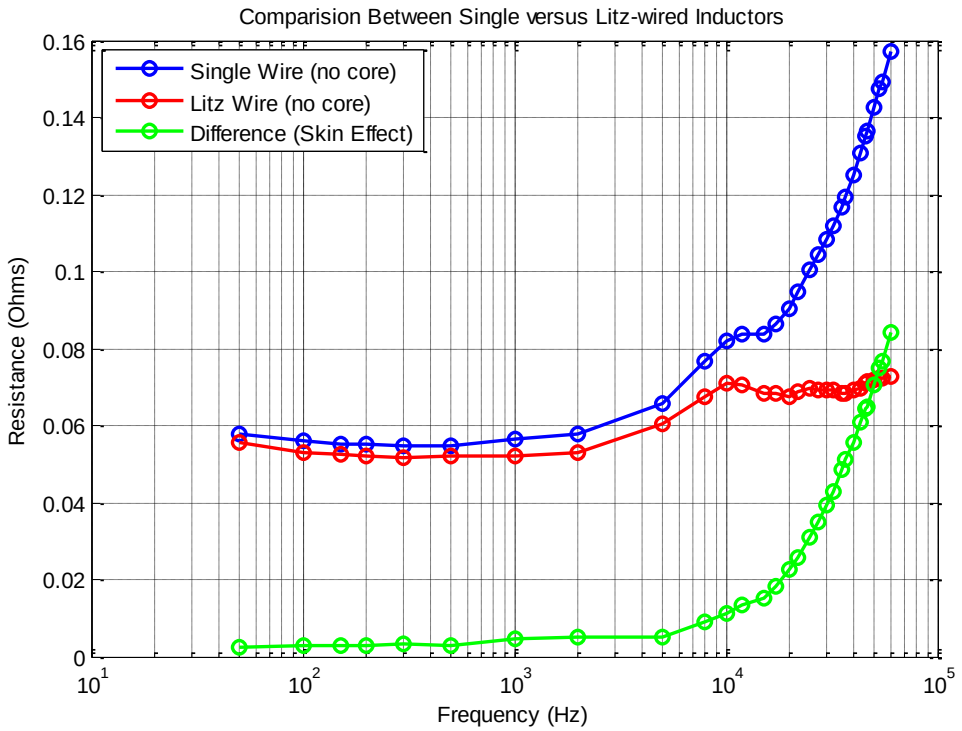


Figure 80: Single versus Litz Wire – Without Magnetic Core.

Observing the figure, it can be seen that for a single wire inductor, the ohmic losses is significantly increasing with the increase of frequency relative to a litz wire inductor. The curve showing the difference between both losses is seen to be nearly negligible at low frequencies, it increases rapidly for higher ones. The extra losses encountered by the single wire are thus attributed to the skin effect.

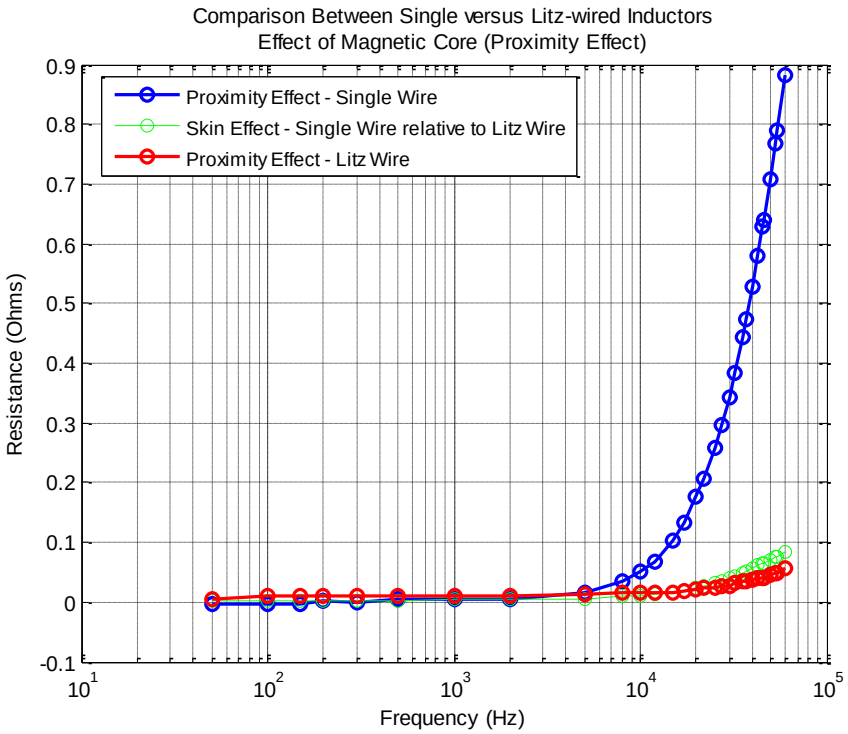


Figure 81: Single versus Litz Wire – With Magnetic Core.

It is also intersting to observe the proximity effect. Although the proximity effect appears in a significant manner for multi-layer design, it exists for a one-layer design due to external magnetic field. Therefore, comparing the losses without core to those with a magnetic core, a difference mainly, not totally, related to proximity effect appears, as seen in Figure 81. It can be seen that losses due to magnetic core are high in case of a single wire relative to its counter litz wire design. Comparing HF losses due to proximity to those due to skin effect, clarified on the same figure for ease of comparison, it is observed that proximity has higher contribution to HF losses than skin effect.

To compare between the two performed designs, Figure 82 shows the resistive losses in the case of a single core inductor design, and those in case of splitting the inductor to a two-core design. It is obvious that the two-inductor design is the best in terms of losses. So the latter solution is implemented.

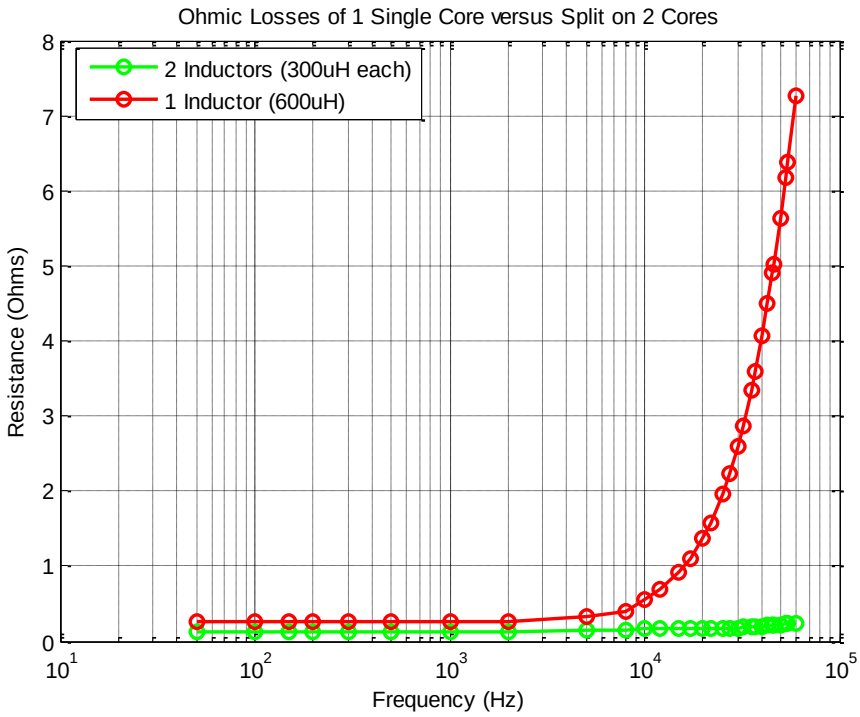


Figure 82: One versus Two Core Design.

6.1.3.4. Losses in Real System

The real converter suffers losses that can mainly be confined to a number of system components, as stated below.

a. IGBT Switches,

The switch collector-emitter saturation voltage, which is the conduction voltage drop when the transistor is ON, defined by the inverter datasheet to be typically 2.94 V. Also, the forward-voltage drop of the free-wheeling diode, which is defined by the inverter datasheet to be 2.27 V. However, it should be noted that these voltage drop levels are estimated for the converter operation under rated power condition, thus will differ with different operation condition.

Therefore, a total of 10 V drop per leg, since two switches conduct in series at a time.

b. Resistive Losses Power Transfer Inductor

As mentioned during the characterization of the inductor design, an equivalent series resistance of 0.166 Ohms results of which, consequently. This resistance represents a power loss in the inductor whose amount differs according to the level of power transferred by the inductor.

c. Transformer Series Resistances (Efficiency)

Based on the characterized transformer impedance model, a series resistance exists for each of the primary and secondary transformer windings, recalling the measured values, a total of 0.4Ω results, referred to the primary side of the transformer.

d. DC-Link Capacitor

An equivalent series resistance is associated with each capacitor forming the DC-link structure, later clarified in context in Figure 83, a given estimated value of $166m\Omega$ is considered, thus also a total value of $166m\Omega$ due to the three-leg symmetric structure of the capacitors' bank.

6.1.3.5. Maximum Power Calculation and Limitations of Power Transfer

The maximum power that can be handled by each constructed H-bridge converter was previously calculated to be7kW.However, this power rating cannot be fully used; it is limited by safety operation margins, the DAB topology structure, and its characteristics of operation. These three main issues imposing limitations are thus discussed below.

Safety Operation Margins

DC-Bus maximum voltage is defined to be 750 V. However, considering a overshoot during control process, it is preferable to set this limit down by an acceptable percentage. Assuming a safe margin of 6-7%, a reachable maximum voltage of 700V is thus defined.

Transformer Turns Ratio

During the study of the best input and output voltages magnitudes, the best ratio for minimizing reactive power was concluded to be the transformer's turns ratio, thus provided the case that the transformer is employed as a step down transformer, i.e. 22:18, then the maximum output voltage is

$$V_o\big|_{\max} = V_{in}\big|_{\max} . r_t \tag{110}$$

Following the maximum power expression, Eq. (93), which is stated here for convenience,

$$P_{\max} = \frac{V_{in} . V_o}{X . r_t} . \frac{\pi}{4}$$

$$P_{\max} = \frac{V_{in}\big|_{\max}{}^2}{X} . \frac{\pi}{4}$$

$$P_{\max} = \frac{700^2}{75} . \frac{\pi}{4} = 5131.3W$$

Thus maximum power until this stage can, hence, be approximated to 5kW.

DC Link Capacitor

The power density levels that can be reached with an H-bridge are limited by peak and average device-switching losses, transformer leakage inductances, series inductor and freewheeling diodes reverse recovery [18]. As mentioned before, the maximum power of the used commercial inverter was calculated to be 7kW, however, for the DAB topology specifically the DC link capacitors are exposed to large ripple currents, as the full AC inductor current, iL, must flow through them during operation [11][12][13], this puts limits for the power that can be handled safely by the inverter.

Thus the power rating of this inverter is much less when employed for a DAB application. It is of interest then to calculate the limit for power transfer level that can be sustained by the DC link capacitors included in the inverter stack, to reach a defined safe maximum power transfer level for the power stage.

The GUASCH Inverter stack has an internal DC link capacitor bank, the bank is constructed by three parallel branches each consists of three series capacitors of 1000uF capacitance each, thus a total capacitance of 1000uF, and 250V rated voltage each, thus a total voltage rating of 750V. The structure is illustrated by the circuit diagram in Figure 83.

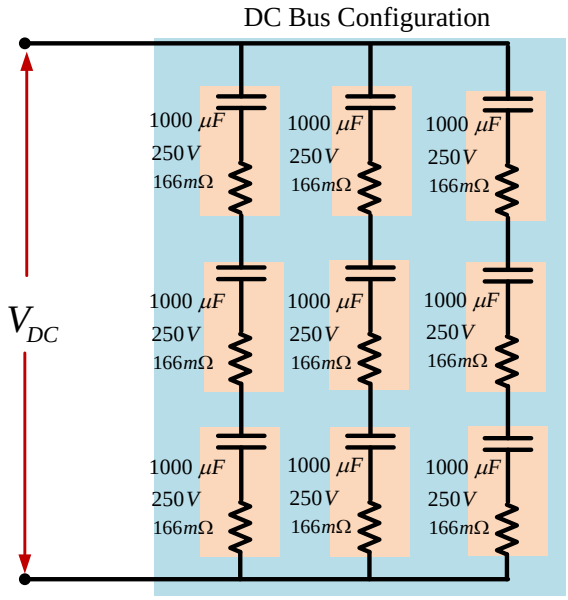


Figure 83: Circuit Diagram of DC-Link Capacitor Connections.

The datasheet of the inverter unit capacitor, 1000uF 250V, indicates a maximum tolerable ripple of 2.2A RMS, with frequency correction factor of 1.4 for frequencies higher than 10 kHz. Taking into account the capacitor bank configuration, of 3 parallel branches, then the maximum ripple current that can be sustained by the inverter DC link can be calculated as follows,

$$I_{cRMS} = 2.2Ar.m.s \times 3 = 6.6Ar.m.s$$

$$I_{cRMS}\big|_{20kHz} = 6.6Ar.m.s \times 1.4 = 9.24Ar.m.s$$

Thus 9.24Arms is the maximum ripple that can be sustained by the capacitor bank.

In order to find the maximum power that the practical DAB converter can withstand, it is necessary then to study the power level at which the maximum capacitor RMS ripple, $9.24 Ar.m.s$, takes place.

Figure 84 shows the ripple current in the DC link capacitor of the converter under the safe maximum power of 5kW. Calculating the RMS value of that component, I_{cRMS}, the current is $14 Ar.m.s$, which is beyond the acceptable limit.

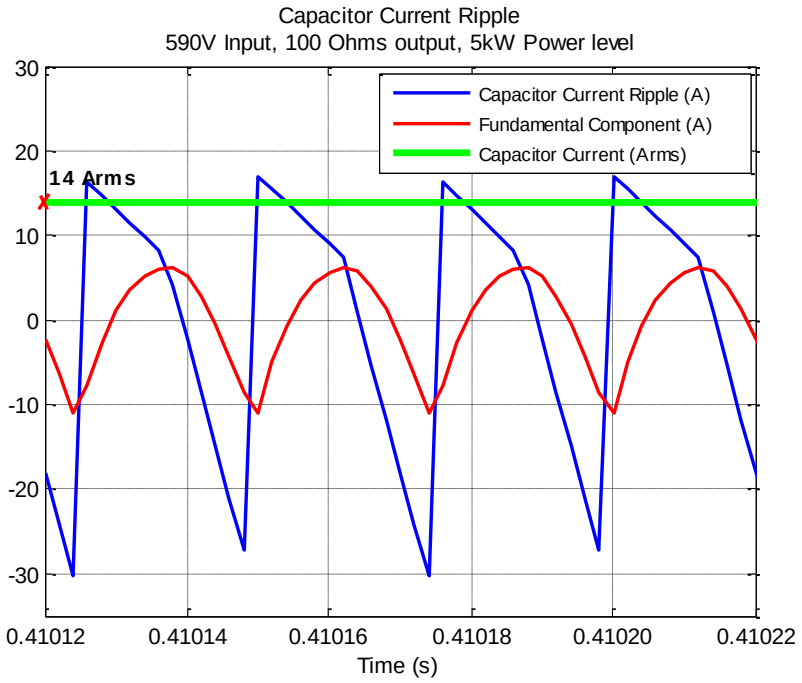


Figure 84: Current Ripple in DC Link Capacitor of the Simulated DAB Converter at 5kW Power Level.

To get the acceptable power level thus I_{cRMS} is plotted for different input voltage levels, i.e. different power levels. Figure 85 shows the RMS capacitor current recorded against input voltage. The curves are taken for different load conditions, to make the study consistent with the load analysis that will be done, Section 6.1.4, and also to allow variety of data to be ready for converter experimental testing.

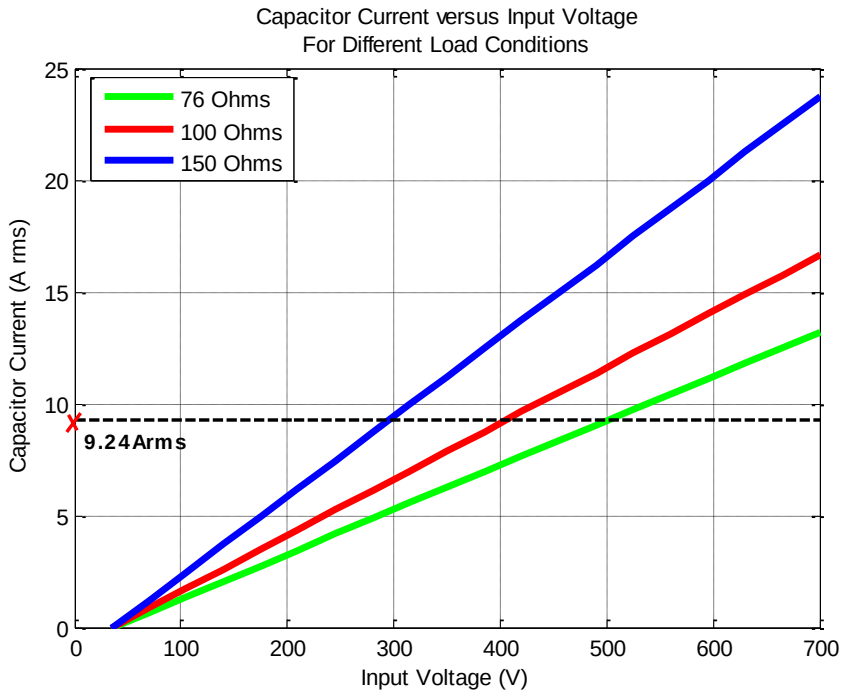


Figure 85: RMS Capacitor Current of the Simulated DAB Converter against Input Voltage for Different Load Conditions.

Figure 86 further adds a third dimension to the curves to indicate the corresponding maximum output power, and therefore the RMS capacitor current limit, 9.24A, sets the power limit, which the intersection with different load curves. The maximum power level can thus be observed from the curves to be 2kW.

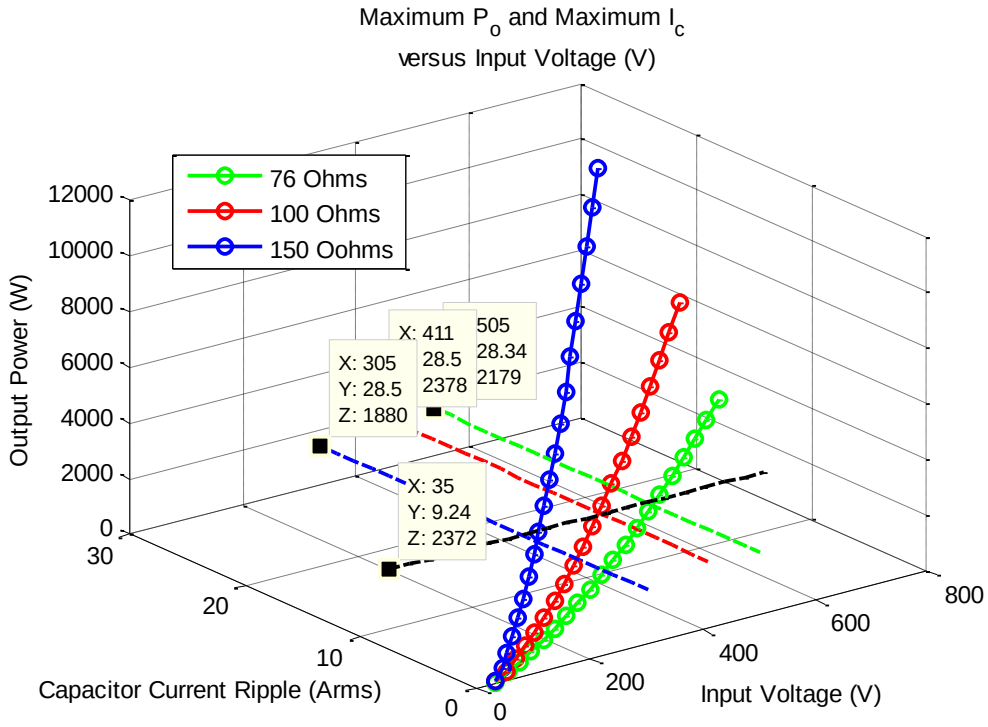


Figure 86: RMS Capacitor Current of the Simulated DAB Converter against Input Voltage and Output Power Level for Different Load Conditions.

This study implies that the DC link capacitor of the inverter stack imposes the largest limitation due to the DAB converter topology limiting the power to more than half the rated power of the stack, thus a maximum of 2kW power transfer level can be handled by the implemented DAB converter.

6.1.4. Load

The input H-bridge is capable of sending power to charge the DC link capacitor of the output H-bridge to infinity, however, the load demands a fixed power consumption, thus fixes the voltage over its terminals.

In other words, at a certain load condition, for each specific input operation voltage, there is a maximum voltage that can be achieved at the load terminals, i.e. a maximum power level. Therefore, in principle, the resistive load value is selected in order to achieve a certain maximum power transfer at the current operation conditions.

An approach to select the load is based on the required ratio between input and output voltage levels assuming maximum power transfer, i.e. 90 degrees phase shift. Recalling the previous analysis on reactive power levels associated with different input-to-output voltage ratios, the best case was concluded to be operation exactly at the transformer turns ratio. The load can, hence, be selected to ensure the open loop operation at this specific ratio for maximum power transfer.

Derivation equation defining resistive load at these conditions is as follows.

Starting from the maximum power that can be transferred by the DAB, following Eq. (93), which is stated here for convenience,

$$P_{\max} = \frac{V_{in}.V_o}{X.r_t}.\frac{\pi}{4}$$

Assuming an output voltage matching the turns ratio thus

$$V_o = r_t.V_{in}$$

$$\therefore P_{\max} = \frac{{V_o}^2}{X.{r_t}^2}.\frac{\pi}{4}$$

Thus the load resistance is thus selected depending on the maximum power it consumes as follows

$$R = \frac{{V_o}^2}{P_{\max}}$$

Assuming the total power is transferred to the load, i.e. neglecting losses, the load resistance is, hence, calculated as follows

$$R = \frac{{V_o}^2}{\frac{{V_o}^2}{X.{r_t}^2}.\frac{\pi}{4}}$$

$$R\big|_{P\max} = \frac{4X.{r_t}^2}{\pi}$$

$$R\big|_{P\max} = \frac{4 * 75 * (18/22)^2}{\pi} = 64\Omega$$

Taking into consideration the loss estimation carried out in the previous section, it is preferable, thus, to choose a higher resistance value in order to provide a margin that ensures that the target output voltage fulfilling the transformer turns ratio can be reached.

The simulation system is then consulted for the load conditions of interest for this study, i.e. different power levels. The curves illustrated in Figure 87 show the maximum output voltage that can be reached against the input voltage, for different load conditions.

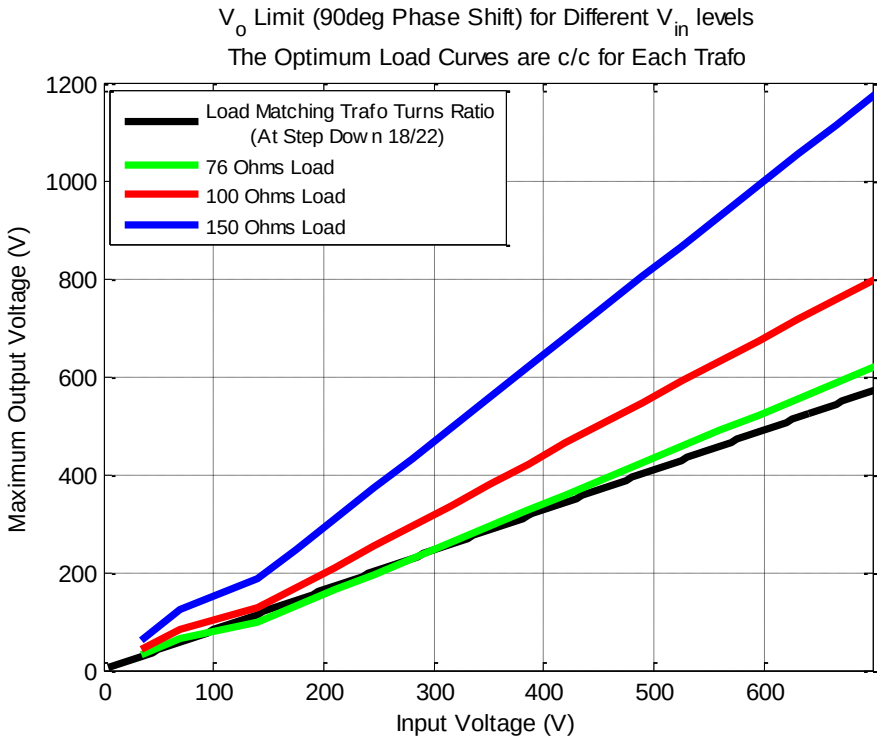


Figure 87: Maximum Achievable Output Voltage versus Input Voltage for the Simulated DAB Converter.

It can be seen, then, that a higher load resistance increases the output voltage limit, but for a certain output voltage condition decreases the power level under test, as clarified by Figure 88, which visualizes the variation of transferred power against input voltage. However, considering that the control loop will always assure the output operation voltage that match the transformer turns ratio, this load choice is considered to be a good compromise.

The higher load value is selected to be 100 Ohms, for two main reasons; first, availability of this load for test under the sought power level, and second, observing the curves in Figure 87, it can be seen that for a 100 Ohms-load the output voltage can be easily expected during open loop converter tests to be nearly equal to the input one.

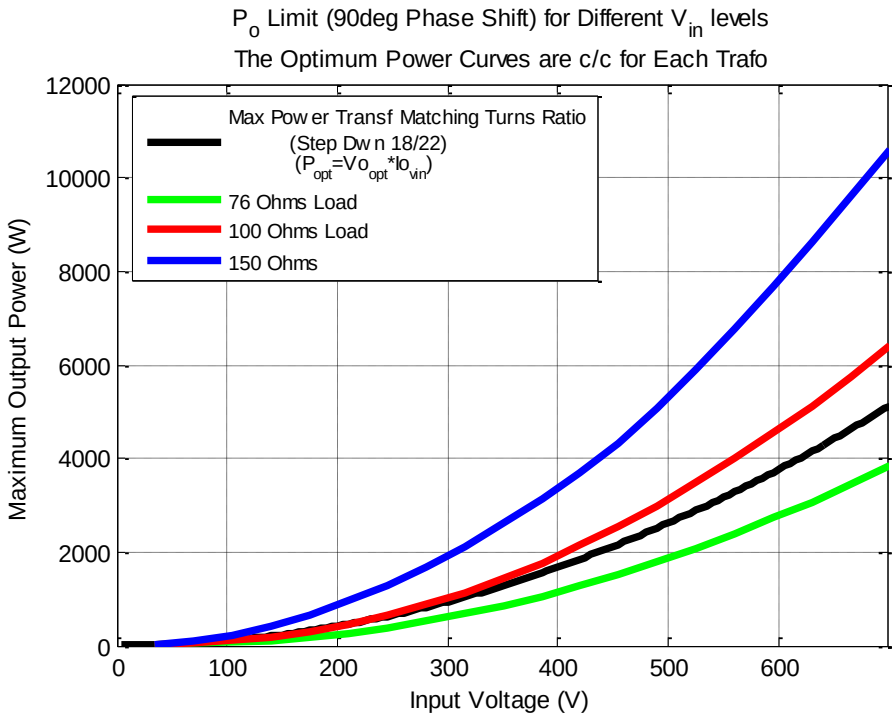


Figure 88: Maximum Achievable Output Power versus Input Voltage for the Simulated DAB Converter.

For the lower power level, defined in Table 3, to be 300W resistors, with 300W rated power are used to construct the load. However, at a higher power, a fan, shown in Figure 89, is employed to be used as a load, with rated power 3kW. The fan is structured by three separate resistors of 50 Ohms each, thus these resistors are accessed by modifying the device connections, so that any load configuration using these three resistors is made possible. A load of a higher value, 150 Ohms, is selected for higher power to assure an output voltage matching the turns ratio.

Figure 89: Fan Employed as the Resistive Load to be Fed by the DAB Converter.

6.2. Programmer Hardware

The interface between the programmer software and the power stage is a backplane structured board consisting of four connection tracks to integrate four boards, Figure 90, The backplane structure of boards performs three basic functions, i.e.:

Driving Power Switches

Driving the IGBT switches in the power stage takes specialized gate drive circuitry, this is provided by the Driver Boards.

Sensing and Signal Adaptation

All voltage and current measurements link to the analog measurement circuitry in the GUASCH inverter. This measurement circuitry is primarily made up of op-amp based differential amplifiers, and is used to scale the incoming analog measurements, from the inverter sensors, to levels that the Analogue-to-Digital Converters (ADCs) on the DSP can safely read, namely 0 to 3.3 V. Translating these ADC results back into sensible voltage readings is then done inside the programmer software.

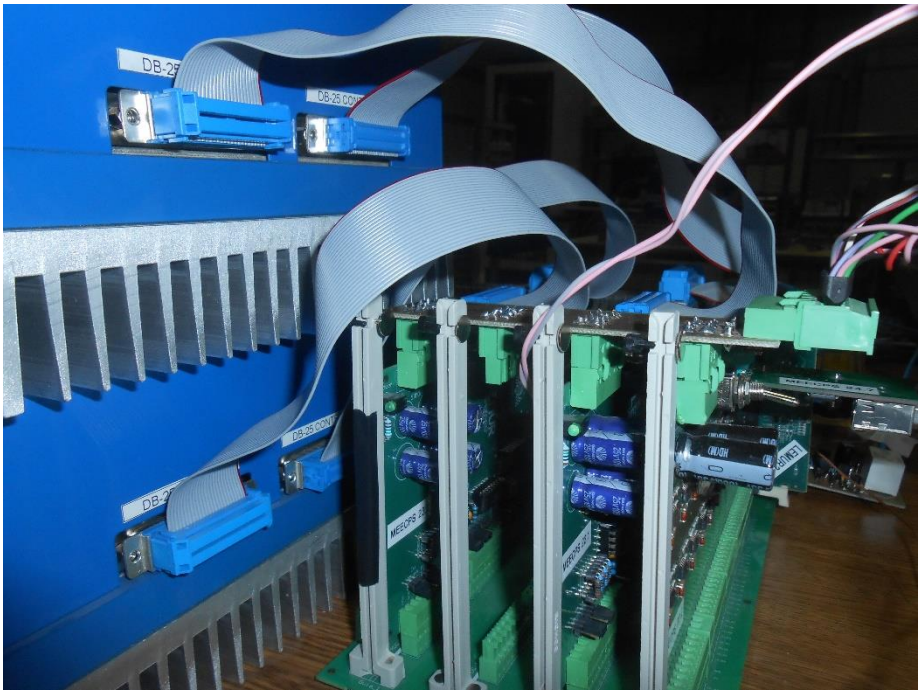


Figure 90: Backplane Structured Boards serve as the Programmer Hardware Interfacing the DAB Converter Power Stage with its Programmer Software.

A detailed review of the main components of this hardware structure along with the functionality of each is described in the next sections.

6.2.1. DC Supply

Two DC supplies are included. These supplies convert the incoming AC mains, 240V RMS, and into the four different DC voltage levels required by the four boards, namely 5 V, 12 V, 15 V, and -15 V. The supplies are shown in Figure 91, and Figure 92.

Figure 91: DC Supply 15V, -15V, +5V – Mean Well (RT-65C).

Figure 92: DC Supply 12V, -12V – Mean Well (RS-35-12).

6.2.2. Digital Signal Controller Board

Digital Signal Controller

The Digital Signal Controller (DSC) employed is the TMS320F28335 with C2000 Microcontroller, which is a product of Texas Instruments. It is operated with a clock frequency of 150MHz. The technical guide and the necessary documentation are available on website. It includes many features which include,

a) Interface to current and voltage measurement peripherals (analogue-to-digital converters).
b) Communicates the control PC with the converter.

The commercial C2000 Peripheral Explorer Kit is shown in Figure 93. It consists of two main partitions integrated via a 100-pin DIMM socket; *F28335 Control Card*, and *Base Board* with necessary interaction hardware.

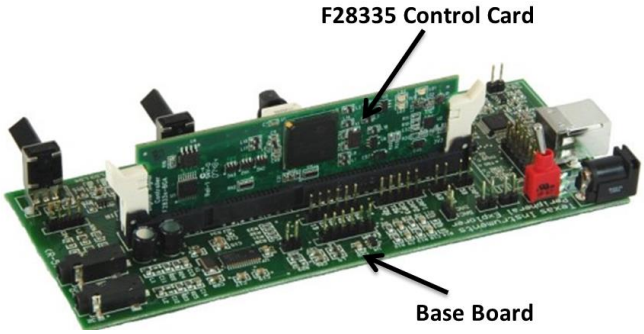


Figure 93: C2000 Peripheral Explorer Kit from Texas Instruments.

The *Control Card* is employed for use in this study, however, the *Base Board* is redesigned and manufactured as a previous project. This is done mainly because it performs several functions that can be compromised for the sake of cutting down the expenses, in terms of the cost of purchasing the board, as well as for the ability of integration of the full DSC board into a Backplane structure, thus reducing wiring system.

Channels Board

This is mainly the measurement peripherals, it performs two basic tasks;

a) Analogue-to-digital conversion of the measurement signals
b) Signal adaptation for safe read by DSC

6.2.3. GUASCH Inverter Interface Board (Driver)

Firing pulses OFF state and ON state leveled 0 V and 15 V.

Since the power stage is composed of two converters, i.e. two H-bridges, thus 8 power switches need to be driven. Basically, each leg is fired by a pulse and its complementary one, thus concluding that 4 pulse-width-modulated signals are necessary for driving the switches of the whole topology.

Design of Hysteresis Comparator

Hysteresis comparator circuit sets a window of safe operation for the DC voltage levels applied to the inverters' DC link capacitors. Exceeding the maximum an output signal triggers the breaking resistor to consume the excess voltage.

The driver boards are equipped with a hysteresis comparator circuit, Figure 94, with implemented using changeable insertion resistors, thus the design is modified for the voltage levels of operation.

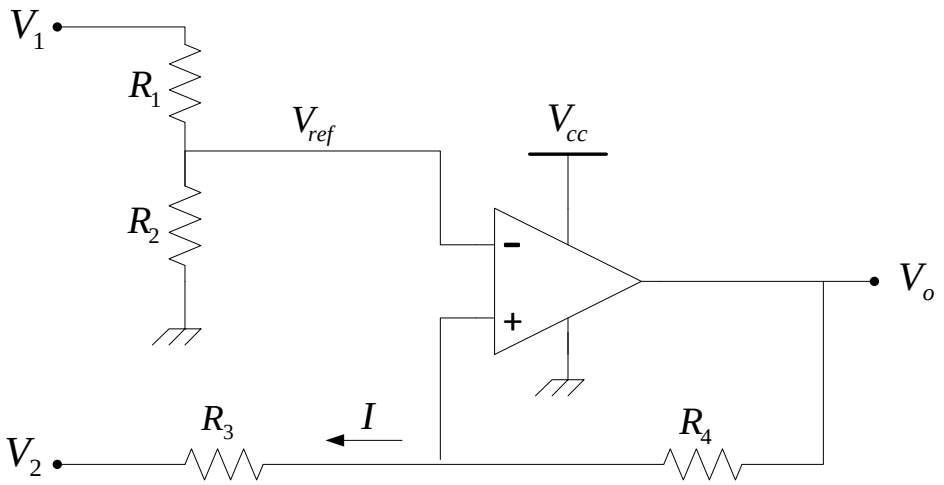


Figure 94: Hysteresis Comparator Circuit Design Implemented on the Driver Boards to adjust a safe window for DC Voltage Levels applied to the Inverter DC-Links.

Below are the calculations followed for the design, applied on an example design for low power test.

$$R_1 = 103300\Omega, R_2 = 2700\Omega,\ R_3 = 3000\Omega, \text{ and } R_4 = 47000\Omega$$

$$V_1 = 15V$$

$$V_{cc} = 5V$$

$$V_{dc}(V_2) = 100.\frac{3.2}{2}.V_2$$

$$V_{ref} = \frac{R_2}{R_1 + R_2}.V_1$$

$$\therefore V_{ref} = 0.382V$$

Dc bus voltage value to trigger the safety load, allowing for overvoltage protection (OVG) is

$$V_2|_{OVG} = \frac{R_3 + R_4}{R_4}.V_{ref}$$

$$V_2|_{OVG} = 0.406V$$

$$V_{dc}(V_2|_{OVG}) = 100.\frac{3.2}{2}.V_2|_{OVG} = 65.034V$$

Dc bus voltage value to bypass the safety load, allowing for under voltage limit (UVG) is

$$V_2|_{UVG} = \left(V_{ref} - V_{cc}.\frac{R_3}{R_3 + R_4}\right).\frac{R_3 + R_4}{R_4}$$

Dc bus voltage value to reset the Dc bus voltage

$$\therefore V_2|_{RESET} = V_2|_{UVG} - V_{cc}.\frac{R_3}{R_4}$$

$$\therefore V_2|_{RESET} = 0.087V$$

$$\therefore V_{dc}(V_2|_{RESET}) = 100.\frac{3.2}{2}.V_2|_{RESET} = 13.97V$$

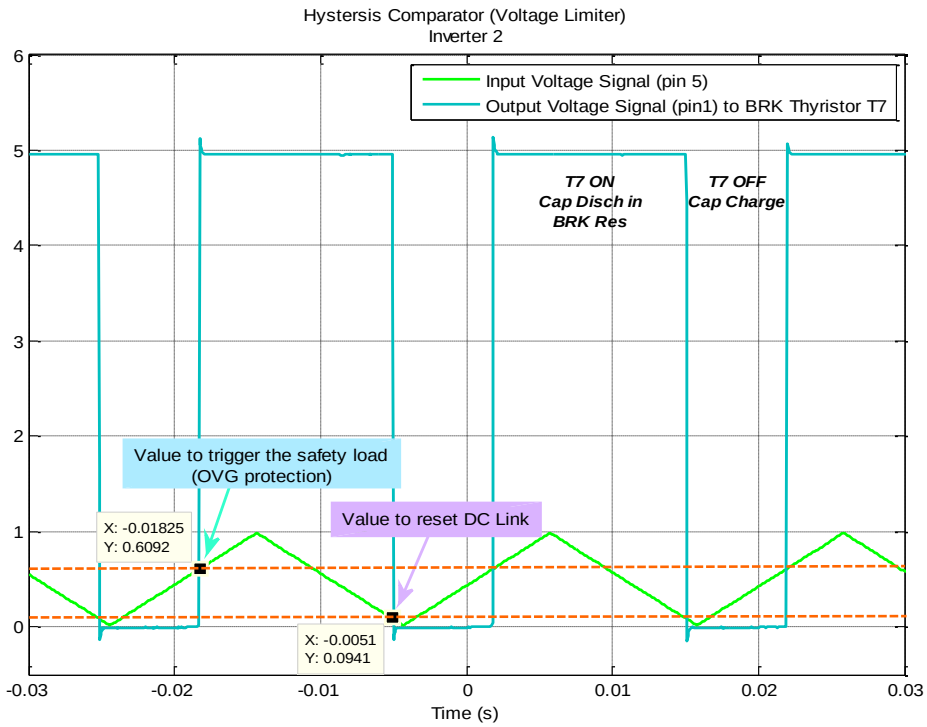


Figure 95: Operation of Hysteresis Comparator for a Window of 65 V Maximum and 13 V Minimum.

6.2.4. Relay Board

During closed loop control test, in order to test the disturbance rejection performance, it is necessary to introduce a variation in the load condition. This can be done by inserting an additional load in parallel with the system load. Therefore, a relay is needed to connect or disconnect the additional disturbance load. A circuit design for the relay board was already available as a part of a previous project, thus modification of this circuit is carried out, along with developing a dedicated Printed Circuit board (PCB) for that purpose as seen in Figure 96.

The circuit input signal is given by one GPIO (General Pin Input Output) from the DSC. Since the voltage range from the DSC board is defined to be from 0V to 3.3V, the relay circuit thus adapts the input signal to operate the relay. A low level, 0V, opens the relay, and a high level, 3.3V, closes it, i.e. connects the parallel disturbance load.

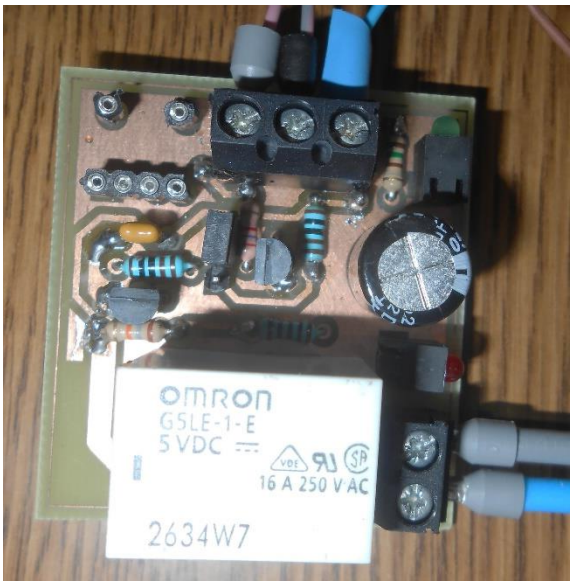


Figure 96: Relay Board.

6.3.Programmer Software (coding)

The software is implemented in the computer language C using Code Composer Studio (CCS v6) platform. In principle, the software code is realized to modulate the converter switching devices, monitor the DAB converter voltage and current measurements, assure safe converter operation, and control of the output voltage by varying phase shift between primary and secondary bridges.

(a) Structure of the Programmer Code

The main skeleton of the programmer code is shown in Figure 97.

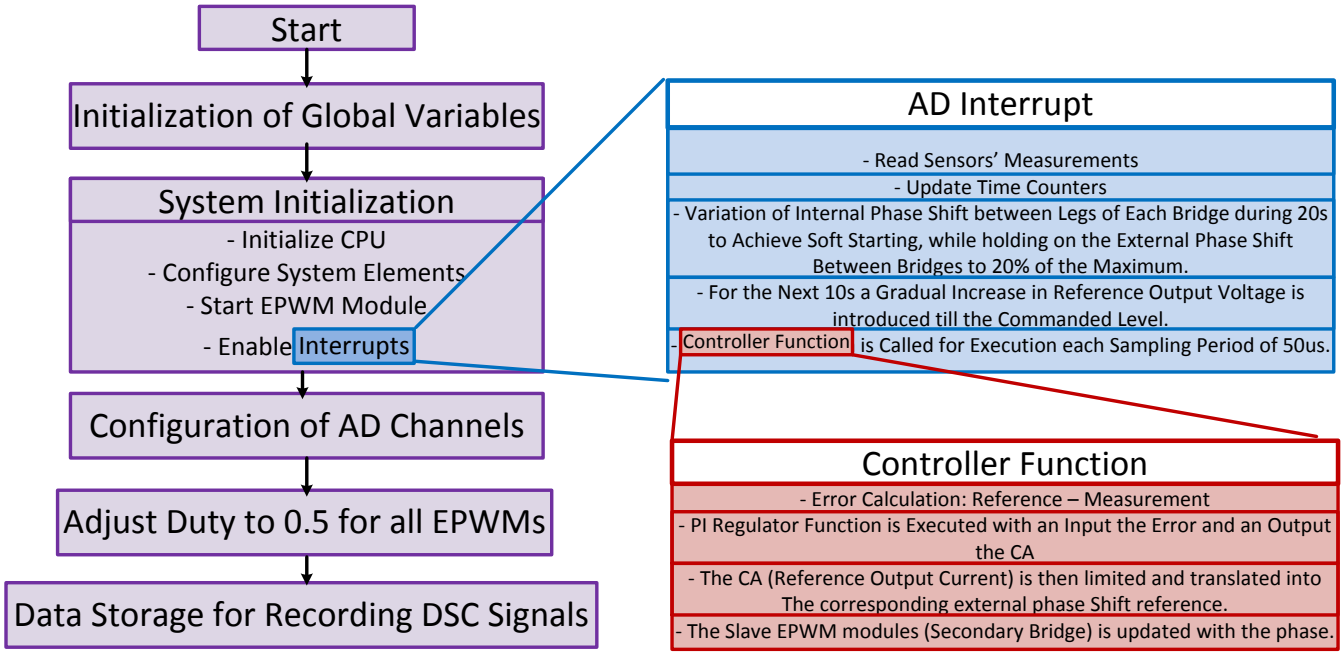


Figure 97: Flow Chart Explaining the Structure of the DAB Converter Programmer Software.

(b) Controller Digital Implementation

The output voltage of the DAB converter has a high frequency ripple component, due to the switching behavior, as well as an average DC value. As it is the average DC value that must be controlled by the closed-loop regulator, it is essential to ensure that only this value is fed to the controller. This spares the control signal from oscillations [7].

A way to achieve this is by synchronous sampling, thus timing the sampling instant to be at the same point of the waveform each cycle. This instant is selected to be at each period, known as symmetrical sampling. It is necessary then to point out that two primary delay mechanisms relevant to the design arise, which are:

Sampling Delay

Using a ZOH for sampling, the average of the sampled system lags that of actual one by half a sample period. Since Symmetric Sampling is employed, sample rate equals to carrier rate, thus half sample period equals half the switching period.

Computational Delay

Control reference, and thus phase shift modulation command, is updated each sample, in this case the reference is sent to the controller half a sample cycle later, which is again half the switching period.

Thus a total of one period transport delay results. Hence, for matching any experimental results with simulation ones, the simulations of the system should be updated with those delays to account for their effect.

Chapter Seven

7. Simulation and Experimental System Results

This chapter presents the simulation results of interest and their match with experimental results.

As mentioned previously, the power stage is composed of two H-bridge converters, with a high frequency transformer in between, and a series inductor at the primary side of the transformer for management of power transfer, and a load in parallel with the DC link of the second H-bridge. The summary of converter parameters is given in Table 15. The input supply DC level, and the load resistance are selected to achieve a certain power transfer level, i.e. low or high power tests.

Table 15: Summary of Experimental Converter Parameters

CIRCUIT PARAMETER	VALUE
Switching Frequency	$20kHz$
Dead time	$2\mu s$
Power Transfer Inductor	$600\mu H$
Transformer Turns-ratio (N_p/N_s)	$22:18$
DC Link Capacitance	$1000\mu F$

Prior to recording any experimental results, some tests have been carried out for validating the correct functionality of the interface backplane, and calibration of the used sensors. This is essential to assure accurate measurements, and correct feedback necessary for closed loop control test.

Then the topology has been powered under open loop test condition to match some studied simulation results and topology principles. Following this tests, and after validation of the operation of constructed power stage, the closed loop control has been applied to the converter.

Then it has been of interest to push the power level up to 2kW for approaching its design purpose for Micro-grid application.

7.1.Calibration Tests

A prior step to any measurement process is to calibrate the employed sensors for identification of correct sensor equation. Consequently, an accurate translation of sensor measurement to the real quantity measured can be assured.

Inverter Internal Sensors

The GUASCH inverter stack is equipped with internal sensors for DC bus voltage, and currents in inverter output phases. For the two stacks used, as primary and secondary bridges, sensors for the DC bus voltages of the two bridges are the ones in use.

The calibration process is carried out by recording several measurement points for the voltage measured by the sensor, and the corresponding bits resulting from the A/D conversion.

7.1.1. Input DC Bus Voltage Sensor

This is used mainly to monitor the input voltage, also the measured value is included in controller computations. The calibration curve is shown in Figure 98a.The resulting expression tying the real voltage quantity to the digital bits is

$$V_{dc}\big|_{in} = 0.183035714 * \mathrm{N}_{\mathrm{bits}} + 3.8$$

7.1.2. Output DC Bus Voltage Sensor

This is of major importance since it monitors the controlled quantity, which is the output voltage. The calibration curve is shown in Figure 98b. The resulting expression tying the real voltage quantity to the digital bits is

$$V_{dc}\big|_{out} = 0.1818182 * \mathrm{N}_{\mathrm{bits}} + 15.6385$$

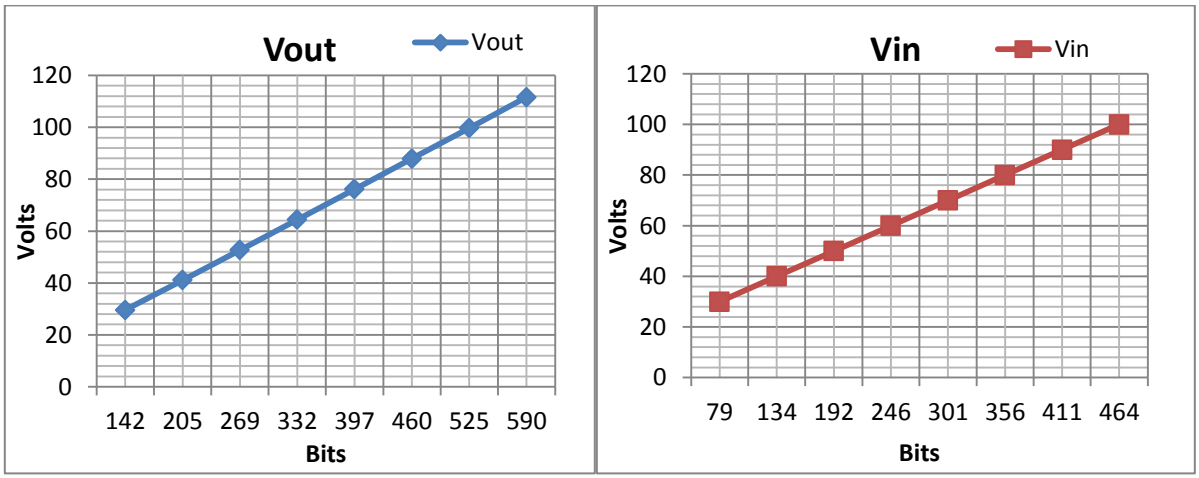


Figure 98: DC Bus Voltage Sensors Calibration.

7.2. Steady State Operation Waveforms

This section presents the principle switching waveforms of the constructed DAB converter. This characterization is carried out at low safe power level. The simulation results presented through the previous chapters are recalled for matching with the experimental ones presented in this chapter.

Figure 99 shows the output AC voltage at the primary and secondary H-bridge converters, along with the corresponding voltage across the inductor and the current through it. These waveforms are captured from the oscilloscope measured from the experimental power stage. In analogy with these experimental waveforms, similar ones are recorded from the simulations, for the sake of comparison. The waveforms under ideal simulation conditions are shown in Figure 100.

A phase shift of 90 degrees is clearly visible between the resulting voltage waveforms at the output of primary and secondary H-bridges, with the primary bridge leading the secondary one. This matches well with the simulated results.

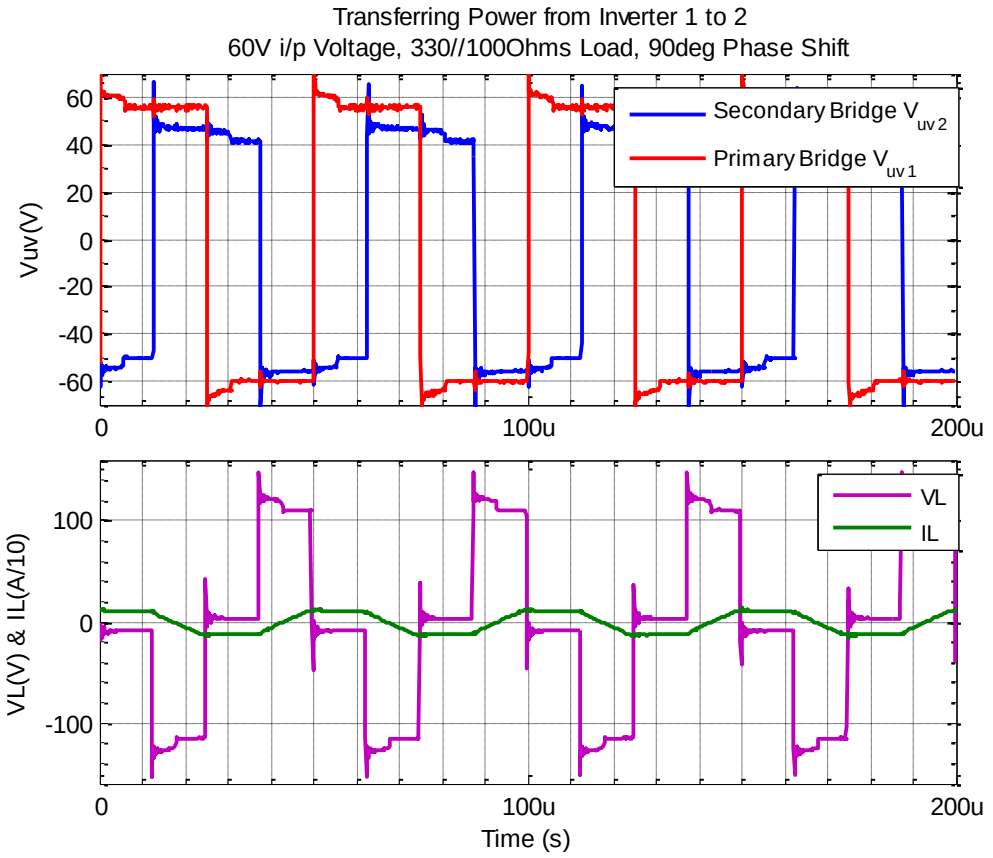


Figure 99: Experimental Results of DAB Converter – AC Output Voltages at the Primary and Secondary H-bridges, and the corresponding Voltage across the Inductor and the Current through it.

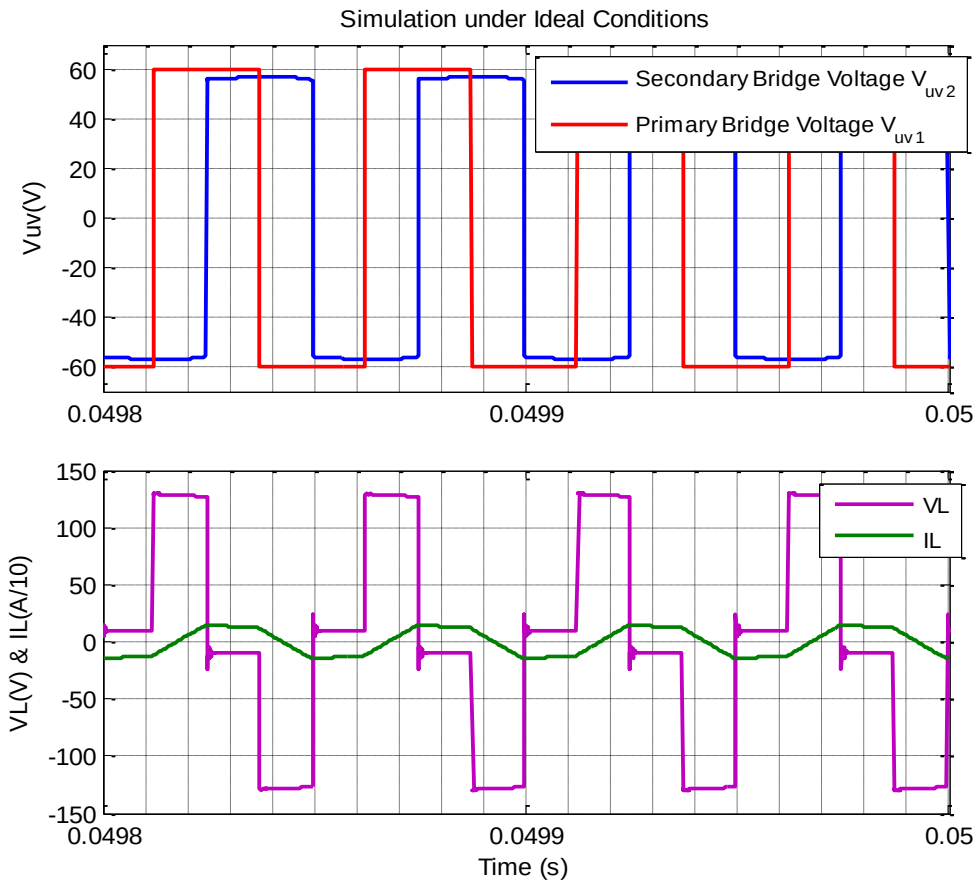


Figure 100: Ideal Simulation Results of DAB Converter – AC Output Voltages at the Primary and Secondary H-bridges, and the corresponding Voltage across the Inductor and the Current through it.

However, the ideal simulation does not justify the voltage sags taking place during switching, as marked on the plots. Thus the real simulation, earlier disscussed in Section 5.3, is consulted for the same switching waveforms, shown in Figure 101. The conduction voltage drop when the transistor is ON, i.e. the IGBT saturation voltage, defines the magnitude of voltage sag taking place, as clarified by Figure 102b. While also the threshold voltage drop associated with the the free-wheeling diode is responsible for the slight overshoot encountered in the voltage waveform, as clarified by Figure 102a.

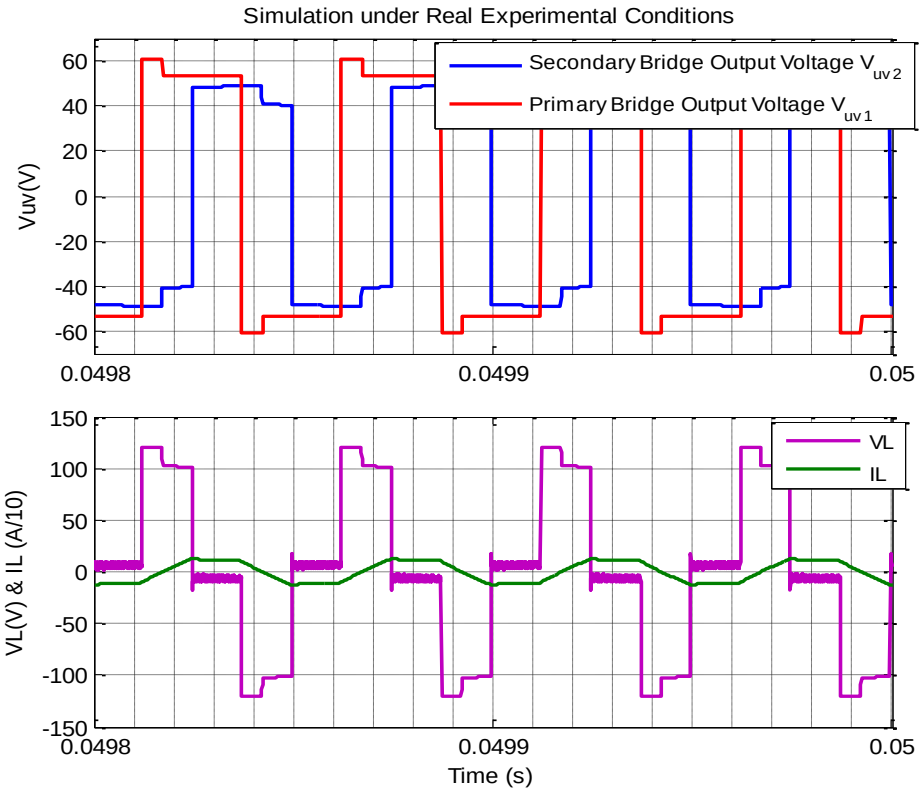
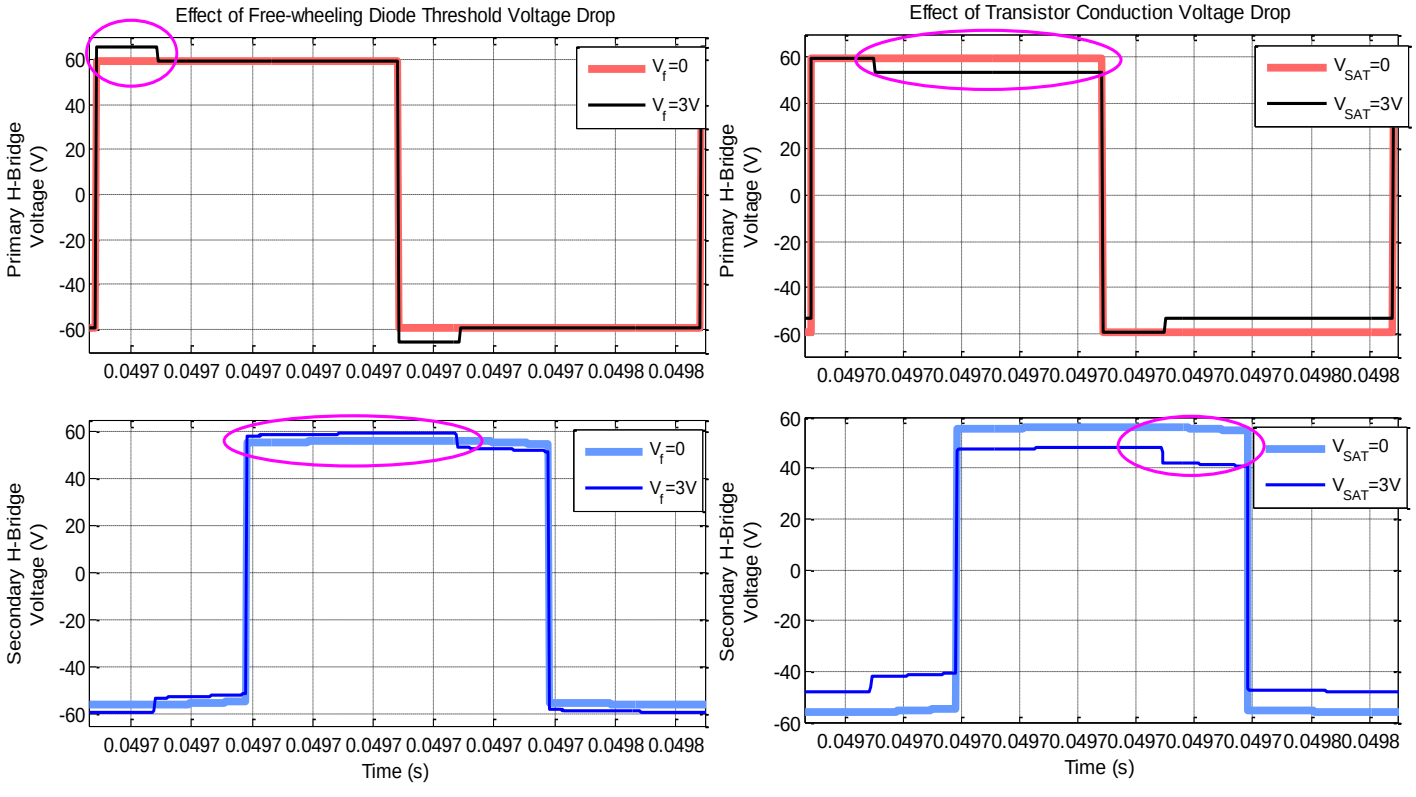


Figure 101: Real Simulation Results of DAB Converter – AC Output Voltages at the Primary and Secondary H-bridges,



(a) (b)

Figure 102: Real Simulation Results – Effect of Free-wheeling Diode Threshold Voltage Drop, and Transistor Conduction Voltage Drop on the AC Output Voltages at Primary and Secondary H-Bridges.

It is interesting also to put the experimental waveforms, previously depicted in Figure 99, all together on the same plot to observe the phase shift effect on the voltage and current shapes, as seen in Figure 103.

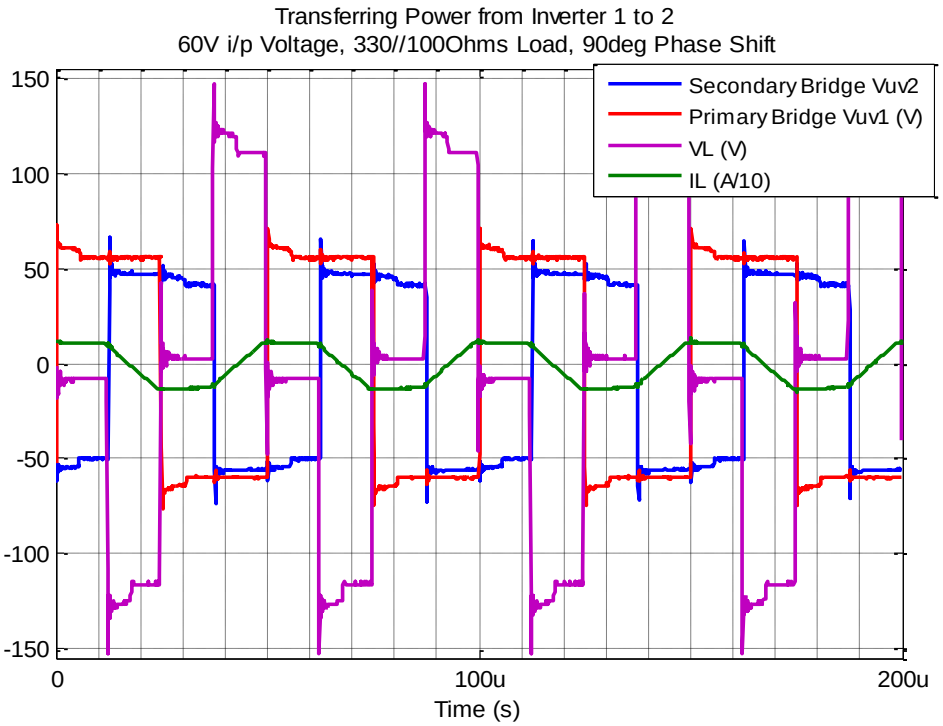


Figure 103: Principle DAB Converter Waveforms – AC Output Voltages at the Primary and Secondary H-bridges, and the corresponding Voltage across the Inductor and the Current through it.

To further compare results the inductor current waveforms at 90 degrees phase shift are, hence, shown in Figure 104 for the three mentioned cases. It can be seen that the practical measured current shows slight difference from that under ideal simulation conditions, but nearly the same as that under real system simulation.

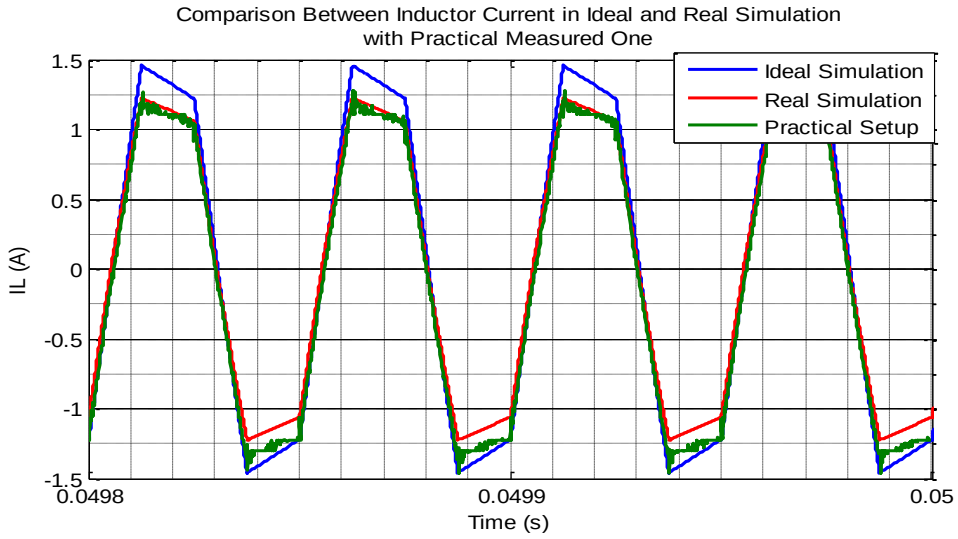


Figure 104: DAB Converter Inductor Current Waveform at Maximum Power Transfer – Comparison of Ideal and Real Simulation with the Experimental Results.

Since the phase shift between bridges defines the amount of power to be transferred, thus also the applied voltage at the load terminals during open loop. Figure 105 shows the output measured output voltage of the DAB converter recorded by the DSC against phase shift angle. Also since the load condition decides the output voltage level for a given input one, it can be observed that for the same phase shift, a 100 Ohms-load can provide a higher maximum output voltage than a 76 Ohms-load. During this test the phase shift is varied in steps of 0.025, which assures that the corresponding output voltage has reached steady state value. The voltage is thus observed to increase gradually.

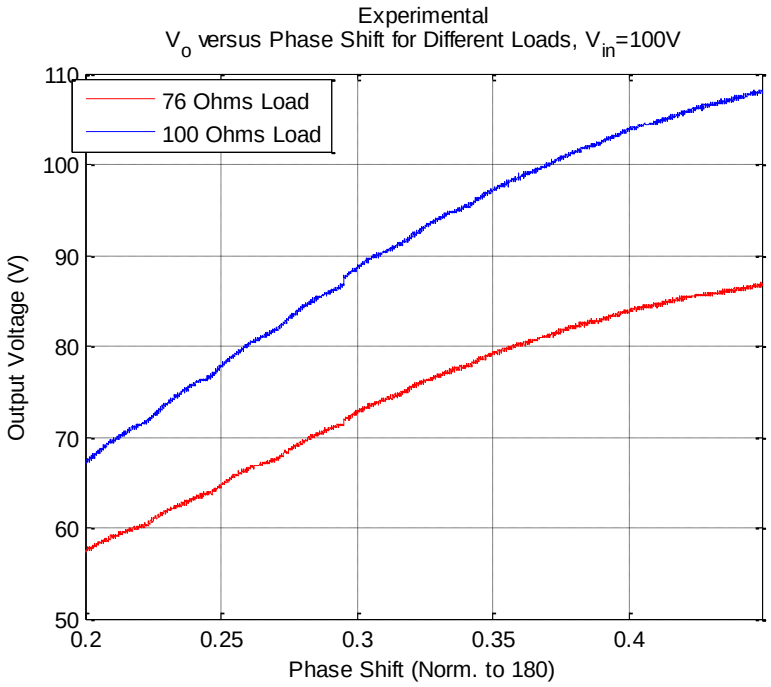


Figure 105: DAB Converter Output Voltage against Phase Shift for Different Load Conditions.

7.3. Closed Loop Control Performance

As mentioned before, in Section 6.1.4, at a certain load condition, for each specific input operation voltage, there is a maximum output voltage at the load terminals, i.e. a maximum power level.

During the control process, to demand a certain output voltage reference, it is necessary thus to take into consideration the maximum voltage that can be reached deploying a certain load at the current input voltage level.

7.3.1. Performance Verification

The closed loop performance is checked at an input voltage of 200V. The output commanded voltage reference is set to match the transformer turns ratio, i.e. 160V, in order to minimize circulating currents. The employed load is a 150 Ohms-load, thus an output power level of around 200 W.

7.3.1.1. Disturbance Rejection

A disturbance is introduced by varying the load condition from 150 Ohms to 100 Ohms. The controller is expected to fix the output voltage to the command reference of 160V. Thus, since the load decreases while keeping the voltage constant a step increase in power by 33% step takes place.

Digital Controller Signals

To assess the implemented digital controller performance, it is interesting to save and extract the signals processed by the programmer software, i.e. data from the point of view of DSC.

Figure 106a illustrates the measured output voltage compared to the reference one. It can be noticed that a voltage drop of 1.3 V is suffered during the transient load variation. Referred to the reference voltage level of 160V, this drop is 0.8%. Compromising this drop with the time the controller takes to recover the voltage reference, this is a good response.

The error input to the PI regulator is thus shown in Figure 106b, being zero at steady state where the measured voltage is equal to the reference one, and shows a value greater than zero during transient.

The reference current is observed, in Figure 106c, to increase by a step of nearly 33% and consequently resulting in the expected power step.

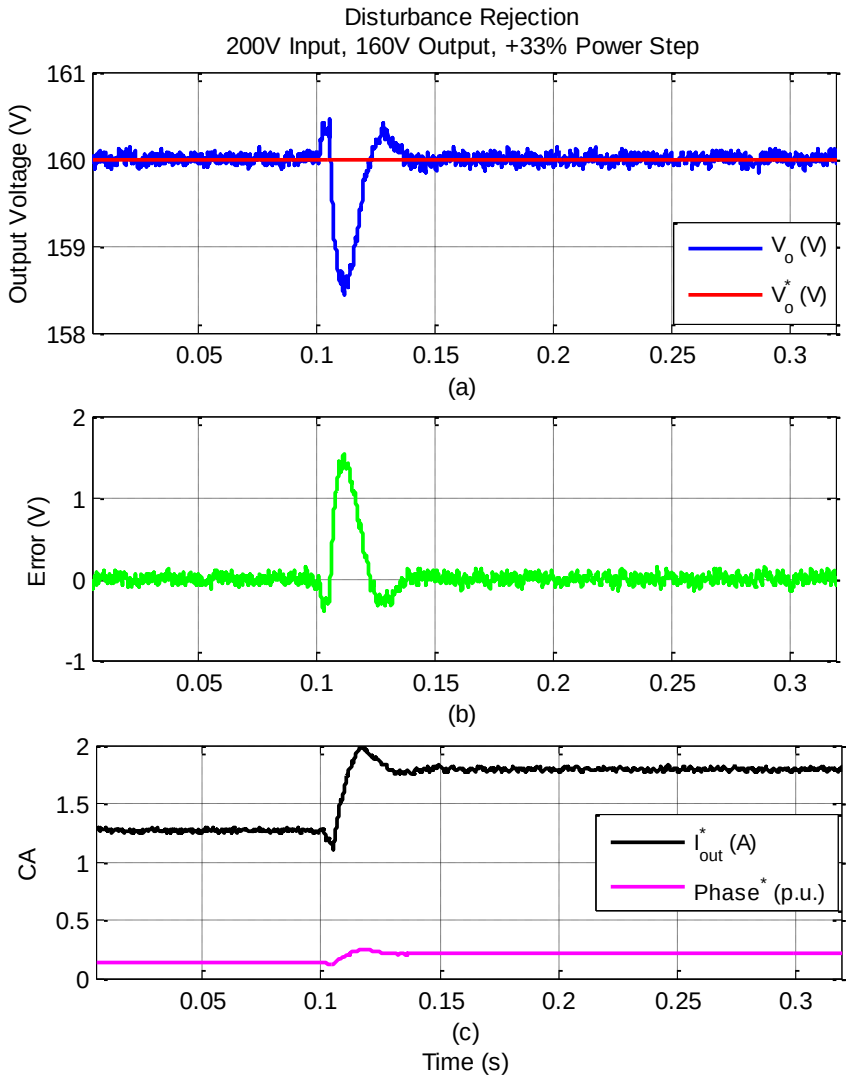


Figure 106: Disturbance Rejection Waveforms Recorded from DSC – DAB Converter Response to a 33% Increase in Power, due to Load Variation, at a Nominal Power level of 170W.

Converter Measured Waveforms

The measured waveforms are captured from the oscilloscope and are depicted in Figure 107. The output voltage waveform is seen to ride through the transient load variation to return to the commanded output voltage reference. A zoom is also presented to observe the shape of the primary and secondary bridges' AC voltages during the transient event.

The current in the inductor and the corresponding current in the transformer secondary side are also shown. Observing the currents envelopes, they are similar to the ones captured by the digital controller, previously shown in Figure 106c.

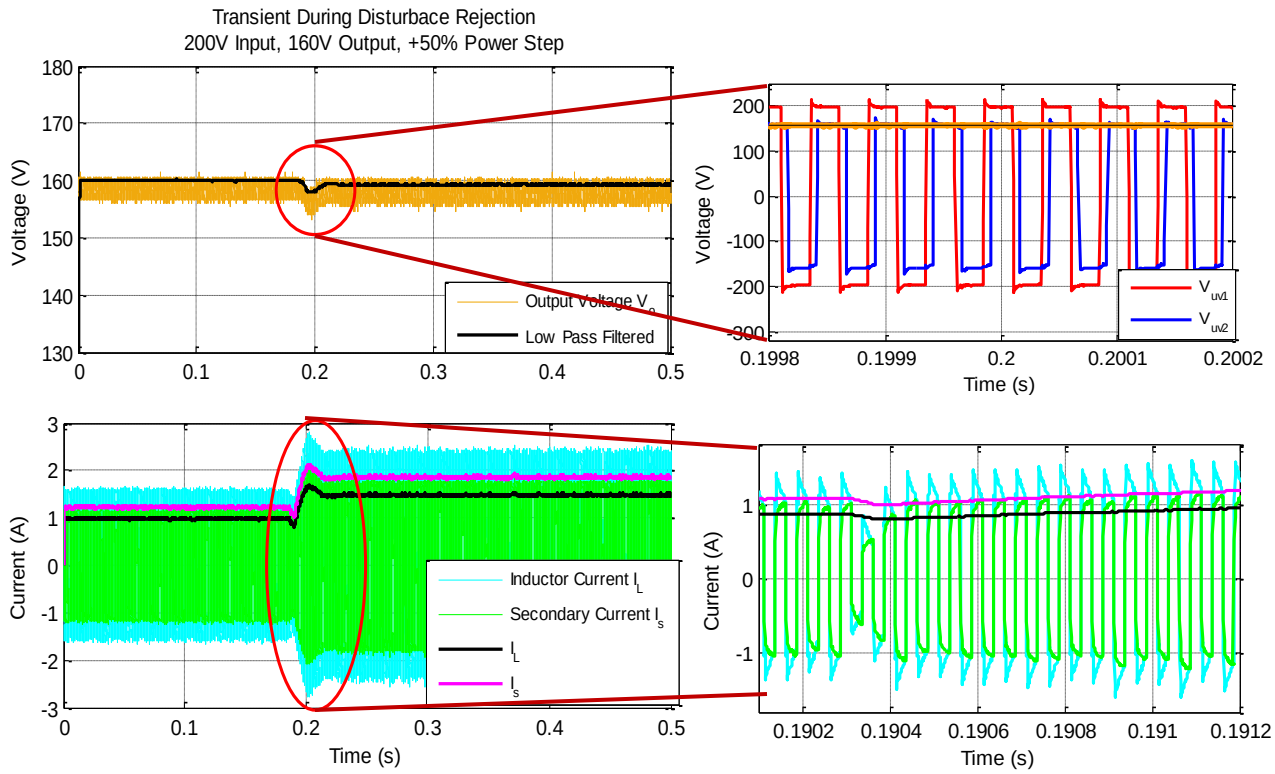


Figure 107: Disturbance Rejection Waveforms Recorded from Oscilloscope – DAB Converter Response to a 33% Increase in Power, due to Load Variation, , at a Nominal Power level of 170W.

Matching with Simulation Results

It is interesting then to compare the transient system response to load variation with the analogous simulated one. Figure 108 shows the simulation response of the system, under the same experimental test conditions, versus the experimental response.

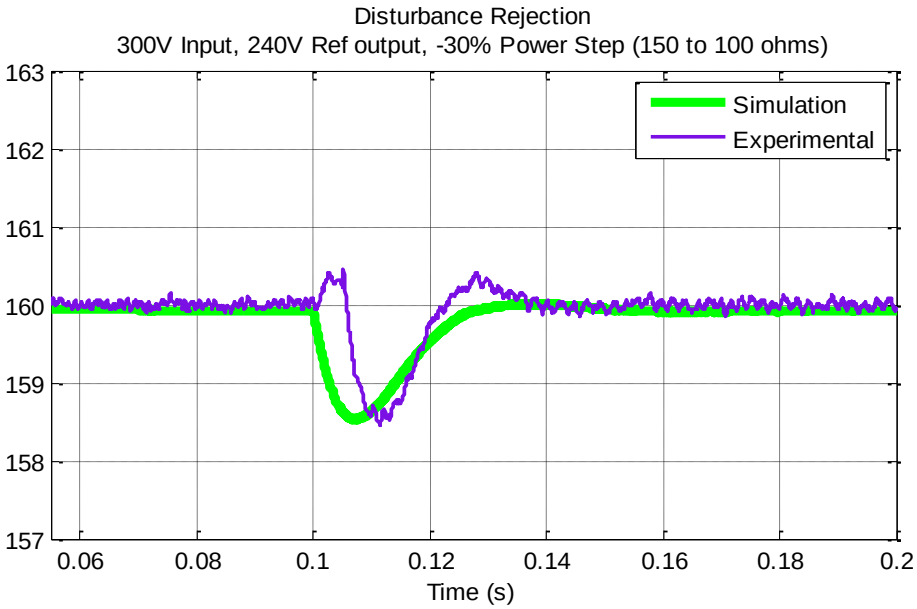


Figure 108: Disturbance Rejection Response for 33% Increase in Power – Experimental versus Simulation.

7.3.1.2. Reference Tracking

A variation in the commanded output voltage reference is introduced from 160V to 170V, thus a 10V step. The controller is expected to track the reference voltage command with zero steady state error.

Digital Controller Signals

Similar to the previous test, the digital signals processed by the programmer software are extracted to assess the implemented digital controller performance. Figure 109a illustrates the measured output voltage compared to the reference one. It can be noticed that an overshoot of nearly 2.5% percent is experienced during the transient event. This overshoot is acceptable taking into consideration the compromise carried out in tuning the controller for both types of transient events.

Similarly also, Figure 109b clarifies that the steady state error is zero while the measured voltage differ from the reference one only during the transient. While in the reference current is seen to be limited, during the transient event, to the maximum allowed by the current operation condition, as can also be verified by observing the phase shift at a maximum value of 0.5, normalized to 180.

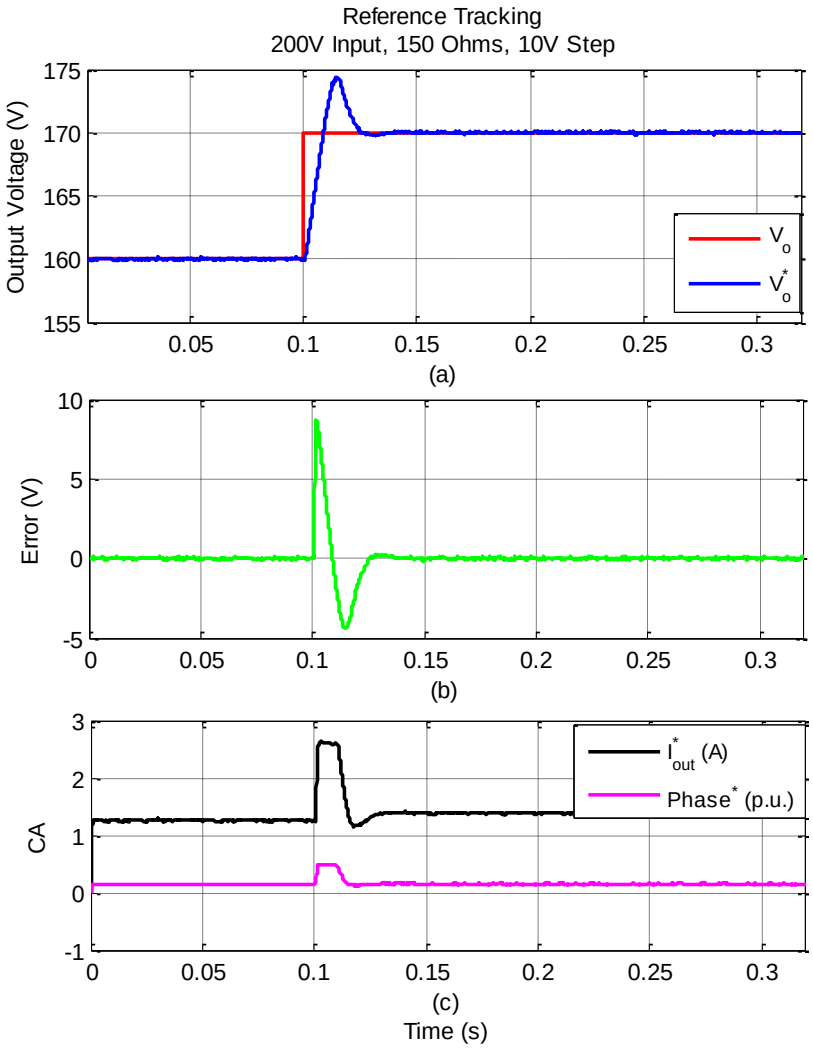


Figure 109: Reference Tracking Waveforms Recorded from DSC – DAB Converter Response to a 10V Step of Commanded Voltage reference, at a Nominal Power level of 170W.

Converter Measured Waveforms

Similarly, also the measured waveforms are captured from the oscilloscope and are depicted in Figure 110.

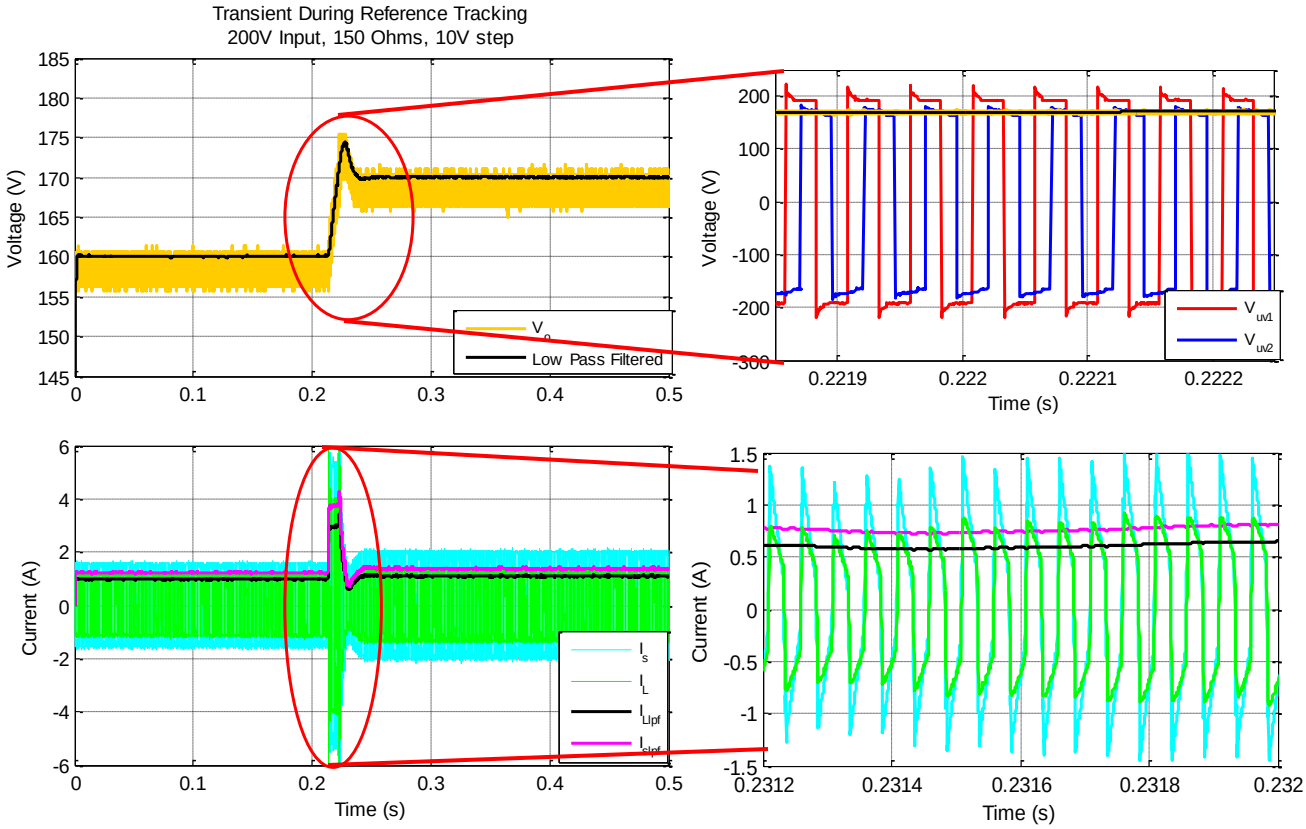


Figure 110: Reference Tracking Waveforms Recorded from Oscilloscope – DAB Converter Response to a 10V Step of Commanded Voltage reference, at a Nominal Power level of 170W.

7.3.2. Control-based Tests

After verification of controller operation, the closed loop control is then used to fix the output voltage applied to the load.

In this case, it is of interest to perform a side study of the dead time effect on practical converter. The input voltage level employed for this test is 220V. The output voltage is commanded to be of exact match to transformer turns ratio, i.e. 180V. By this, the circulating currents, discussed in Section 3, can be minimized, so that the major effect on reactive power is due to dead time. Similar analysis carried out in the latter mentioned section is adopted hereafter to calculate the reactive power in each case of dead time variation, and finally compare between different cases.

Figure 111, plots arranged from top to bottom, illustrates the AC voltage at the primary bridge and the corresponding inductor current. For larger dead times, 3us and 4us, the voltage reversal effect can be noticed.

The second row of plots shows the total power resulting by multiplication of voltage and current. This power is then analyzed into active power component, positive, and reactive power component, negative. Negative areas marked indicates the reactive power, thus by

cumulative trapezoidal integration, the total reactive power during one switching cycle can be computed, as clarified by the third row of plots. The final plot is thus a comparison between the three dead time cases in terms of reactive power.

This study concludes dead time causes a reactive power component that increases with the increase of inserted dead time.

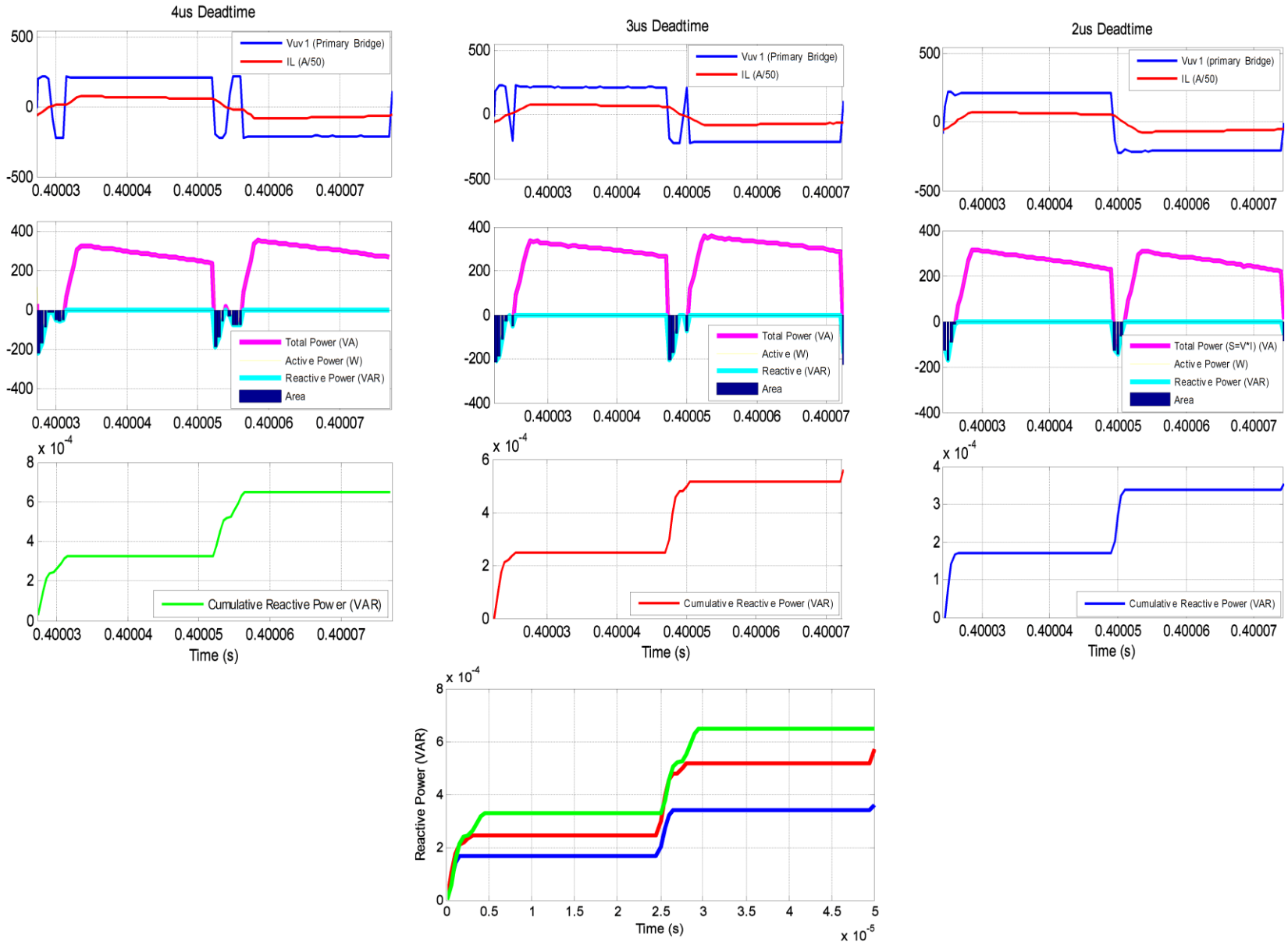


Figure 111: Dead Time Effect on Practical DAB Converter – Different Cases of 2us, 3us, and 4us are compared.

7.4.Higher Power Tests

As mentioned before through the design process, Chapter 6, there are some design modifications for the higher power level tests. The modifications are summarized hereafter as a start to the tests at this level.

- Input supply is an autotransformer a maximum DC voltage of 620V which can be supplied through a rectifier stage.
- Inductor Design is split into a two-core Litz wired design output, which targets minimization of overall losses.
- The normal 300W resistive loads are replaced by a fan whose rated power is 3kW to withstand the power level of the tests.

During the real transformer characterization, presented in Section 6.1.2, the saturation of the magnetic has been brought about, selecting the passive solution of introducing series capacitors to block any DC voltage component. However, also to avoid any asymmetry in voltages applied to the transformer primary and secondary sides, two techniques have been developed and digitally implemented using software code.

Soft Starting

First, a soft starting technique has been implemented. It depends, in principle, on inserting the same internal phase between legs of the each H-bridge converter, which is the DPS modulation strategy discussed previously, in Section 3.1.2.2. This modulation is applied to both primary and secondary bridge converters for the first seconds of converter operation to insure smooth variation of applied voltage, and consequently current. Figure 112 shows the waveforms captured during soft starting modulation from the experimental converter.

Figure 113 also illustrates the soft starting during an enough period of time to see the evolution of waveforms. The plot is directly snapped from the oscilloscope without data processing due to large data size. The internal phase shift is increased by 9 degrees each step until a maximum of 180 degrees, i.e. the normal 50% modulated waveforms. The soft starting is done while fixing the phase shift between the bridges to a constant value, 90 degrees in this case.

However, the phase shift during the open loop soft starting process is adjusted to be consistent with the output voltage reference command sought to be achieved during control process. Keeping the phase shift to zero, i.e. zero output voltage, during soft starting implies that the input current ripple increases with the increase of the applied input voltage as clarified by Figure 114. Also, recalling the maximum power study presented in Section 6.1.3.5, the power limitation imposed by the maximum current ripple that the DC link capacitor can withstand, 2kW, should be the boundary. Thus there is a limitation for the maximum phase shift that can be applied also.

Therefore, the phase shift during soft starting is selected to be at 20% between minimum and maximum boundaries, thus 18 degrees.

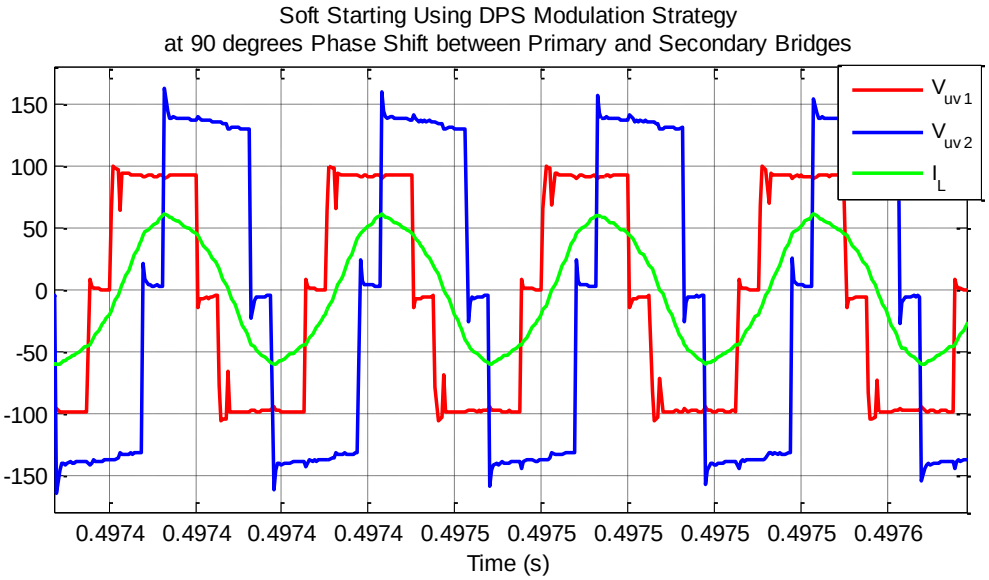


Figure 112: Soft Starting – DPS Modulation Strategy at 90 External Phase Shift between Primary and Secondary Bridges.

Figure 113: Soft Starting – Evolution of DPS Modulation Strategy a 9 degrees step increase Internal Phase until a Maximum of 180 degrees. The External Phase Shift is 90 degrees between Primary and Secondary Bridges.

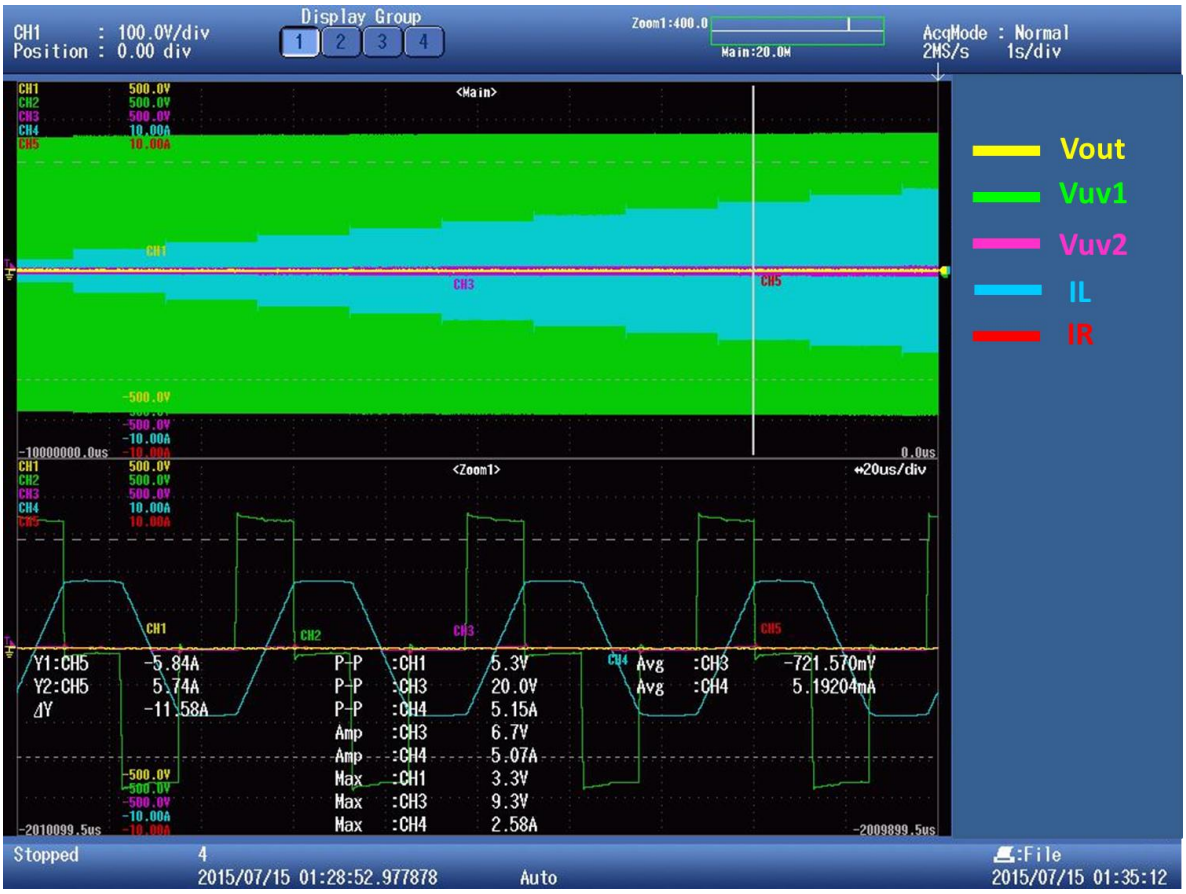


Figure 114: Soft Starting – Evolution of DPS Modulation Strategy a 9 degrees step increase Internal Phase until a Maximum of 180 degrees. The External Phase Shift is 0 degrees between Primary and Secondary Bridges.

Gradual Reference Voltage Command

Second, with the start of the control process, the regulator takes control of the phase shift angle between bridges, adjusting it to reach the commanded output voltage reference. The reference output voltage is also adjusted to increase in steps to the commanded reference output voltage. The process can be observed in Figure 115.

Figure 115: Gradual Increase of Voltage Reference Command, and Corresponding Reduction in Current Ripple as Output Voltage Increases in Response to the Reference.

7.4.1. Open Loop Test

Characteristic Waveforms

The test is carried out at a power level of 1.7kW. To achieve this power level, a 150 ohms load is employed at an input DC voltage level of 350 V. Soft starting is used to gradually increase the applied input voltage, at 18 degrees phase shift between primary and secondary bridges, and thus gradually increasing the output voltage. After soft starting, the phase shift between bridges is continued to be increased gradually until the maximum, 90 degrees. The resulting converter characteristic waveforms are depicted in Figure 116 as measured from the power stage.

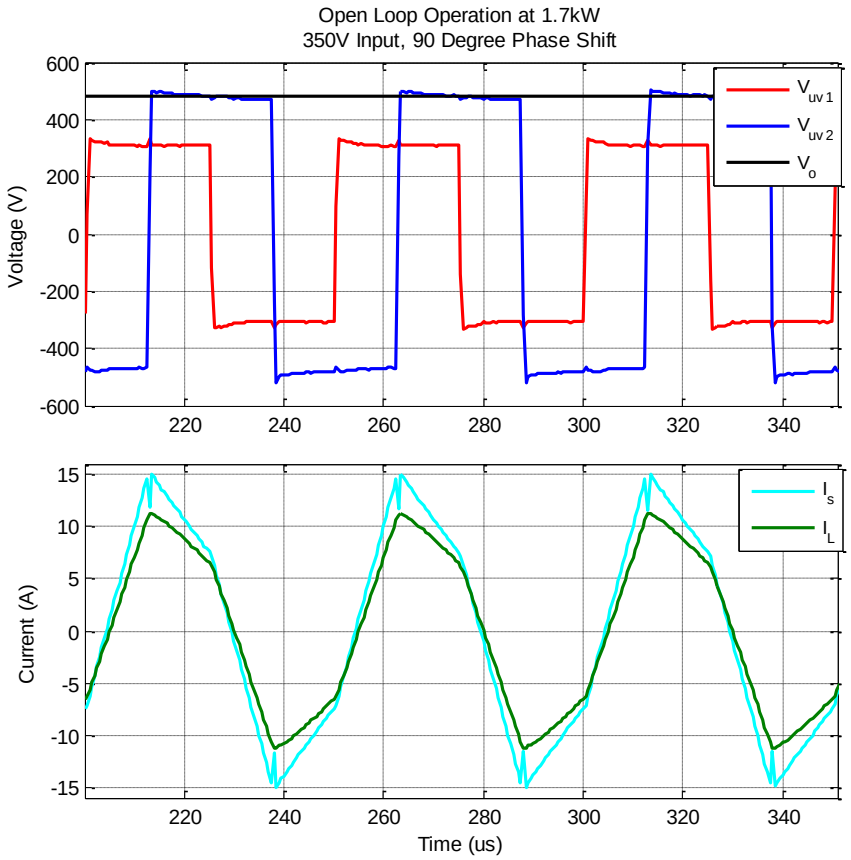


Figure 116: Dual-Active-Bridge Converter Open Loop Operation Waveforms – AC Voltages at the output of Primary and Secondary and Current waveforms at the Primary and Secondary Transformer Sides.

Open Loop Transient

Varying the external phase shift between primary and secondary bridges, varies the power transferred from the primary to the secondary. Therefore, it is interesting to observe system response to a step change in phase shift as observed in Figure 117.

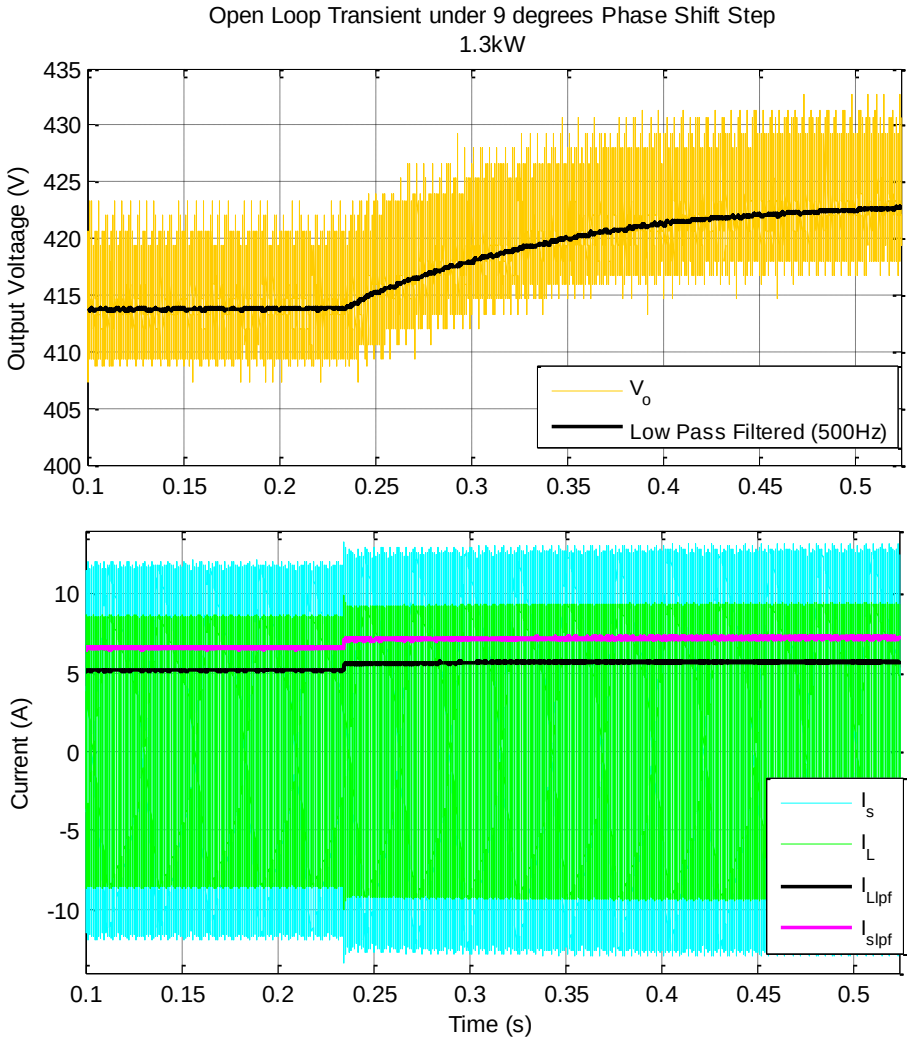


Figure 117: Dual-Active-Bridge Converter Open Loop Transient Response to 9 Degrees Step Change in Phase Shift – Output Voltage and Current waveforms at the Primary and Secondary Transformer Sides.

7.4.2. Closed Loop Control Test

Similar to the previous closed loop controller performance assessment during transients, disturbance rejection is again checked for validating controller performance at a higher power level.

The test is carried out at an input voltage of 500V. The output commanded voltage reference is set to 330V. The employed load is a 150 Ohms-load, thus an output power level of around 1kW.

The measured waveforms are captured from the oscilloscope and are depicted in Figure 118. The top figure illustrates the measured output voltage compared to the reference one. A zoom is also presented to observe the shape of the primary and secondary bridges' AC voltages during the transient event. Compromising the drop in voltage, observed to be 1%, during transient ride-through with the time the controller takes to recover the voltage reference, this is a good response.

The current in the inductor and the corresponding current in the transformer secondary side are also shown in the bottom figure. Observing the current envelope the curve is seen to increase by a step and thus an expected power step of nearly 33% is encountered while successfully holding on the system output voltage to the commanded reference.

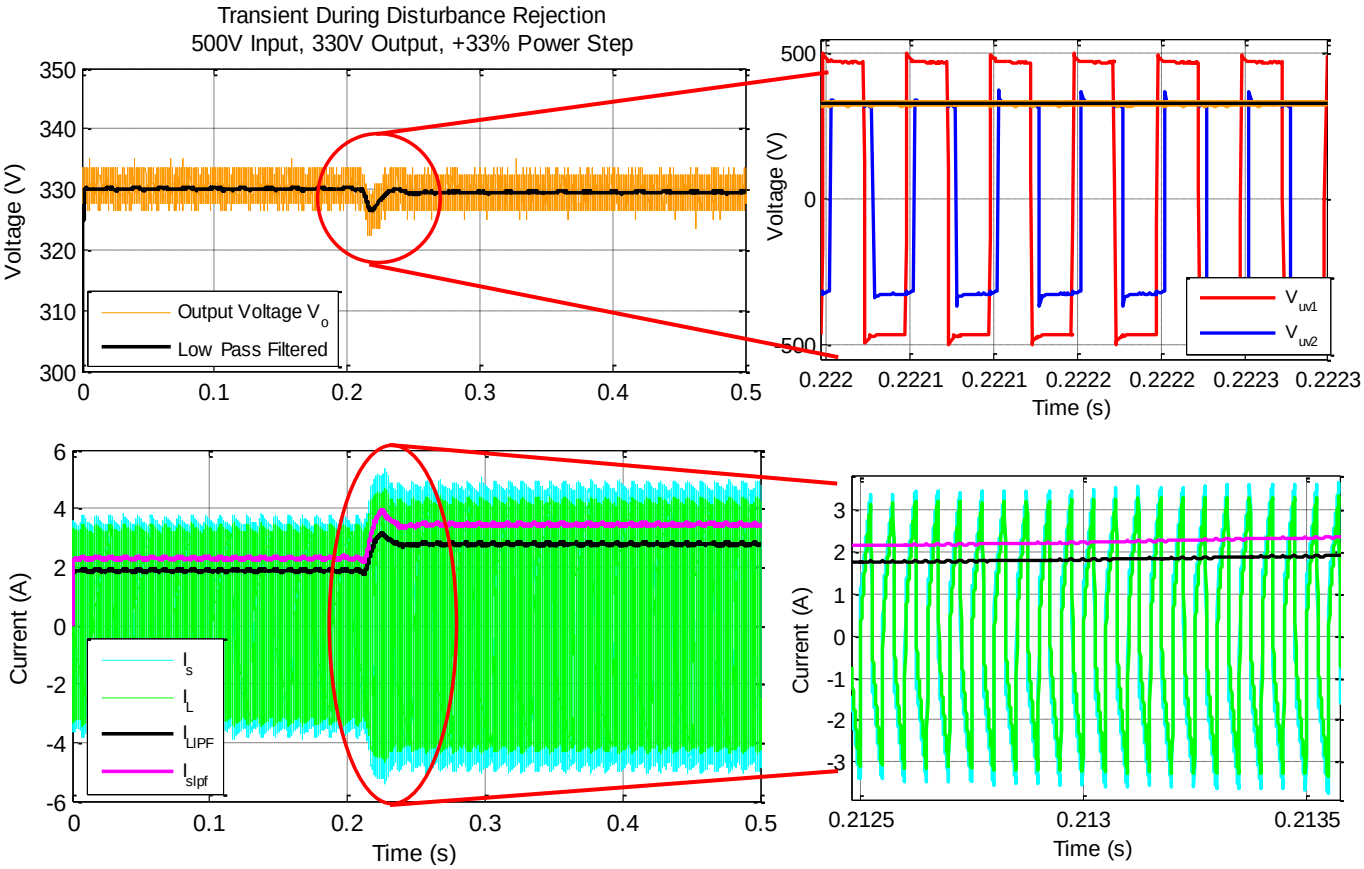


Figure 118: Disturbance Rejection Waveforms Recorded from Oscilloscope – DAB Converter Response to a 33% Increase in Power, due to Load Variation, at a Nominal Power level of 800W.

7.4.3. Power Breakout and Efficiency Estimation

Referring to Section 6.1.3.4, losses discussed can be further estimated accurately by studying real converter waveforms.

It is noteworthy to mention that prior to any efficiency study the measurement system, represented in voltage and current probes, should be precisely adjusted. This is necessary to avoid any DC offset imposed on the measurements.

The study is concerned with the main elements marked on Figure 119.

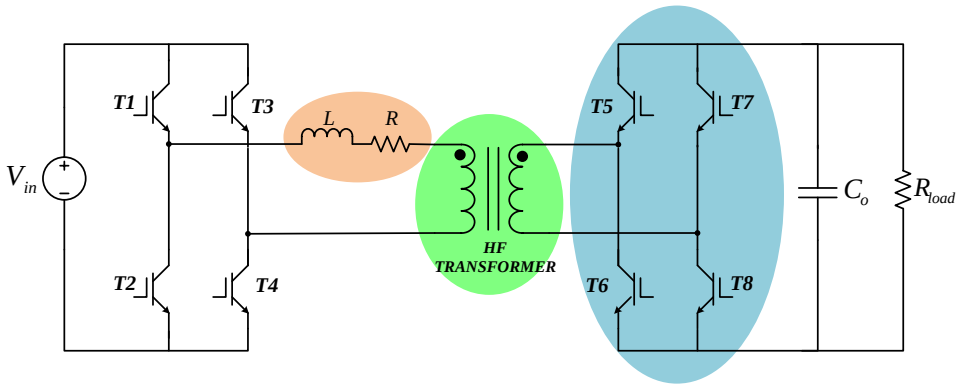


Figure 119: DAB Converter Main Loss Elements.

The test is carried out at 500V input voltage, and controlling the output voltage to 350V, while employing a 150 Ohms-load thus an approximate power level of 800 W.

To estimate the power loss in each of the marked elements, the same procedure is followed. First, the voltage and the current components at the input and the output of the element are measured and multiplied to get the corresponding input and output power components.

Then, averaging each power component, and subtracting output from input one, a power loss component results. Also to get the efficiency, the output power component is taken as percentage of total power, as seen below.

$$\eta = \frac{P_o|_{avg}}{P_i|_{avg}}$$

The efficiency calculations are performed by recording a measurement window of 50ms.

Power Transfer Inductor

In the case of the power transfer inductor, the power loss is expected to be relatively low, since the equivalent series resistance is recorded during the design process for the final inductor to be 0.166 Ohms. The voltage and current measurement probes, while accurately calibrated, still have some filtering on the signals. Therefore, similar comparison of input and output powers using this method renders an appreciable error.

The power loss can then be estimated by taking only the fundamental equivalent resistance at the switching frequency of 20 kHz is considered, to estimate the losses at this operation frequency following the relation.

$$P_{loss} = I_L{}^2 . R_{ser}$$

Figure 120 shows the power loss calculated following this equation, indicating the average and RMS values. An average power loss of 0.77W is recorded.

The average input power is recorded to be 823.65 W, thus the efficiency

$$\eta_{Inductor} = \frac{823.65 - 0.77}{823.65} = 99.99\%$$

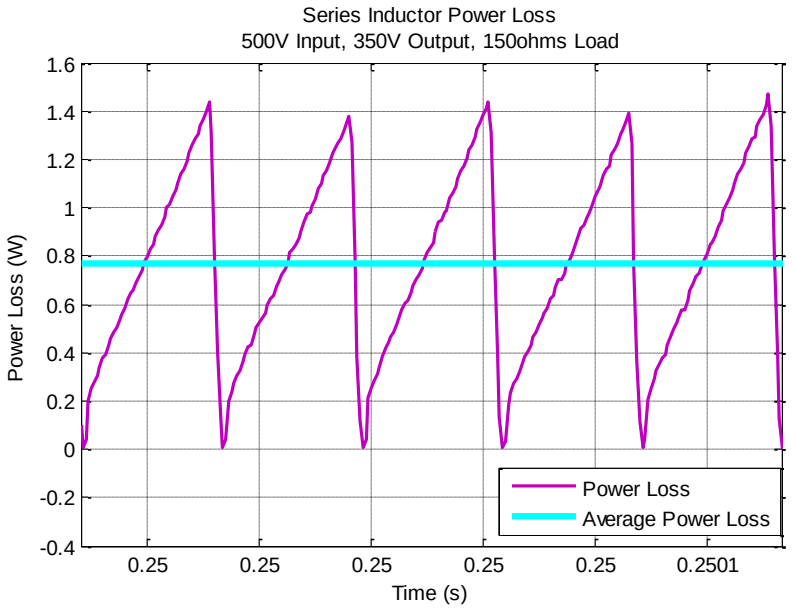


Figure 120: Power Loss of the Real Power Transfer Inductor in the DAB Converter Prototype.

High Frequency Transformer

Similarly, the formerly mentioned procedure is followed with the DAB converter. Figure 121 shows the total input power to the transformer and the output power from it, the average of these powers are also indicated on the plot. However, the values are very close to point out the difference, which is recorded to be exactly 4.57W.

The efficiency of the transformer is thus calculated to be

$$\eta_{Transforme} = \frac{849.43}{853.99} = 99.465\%$$

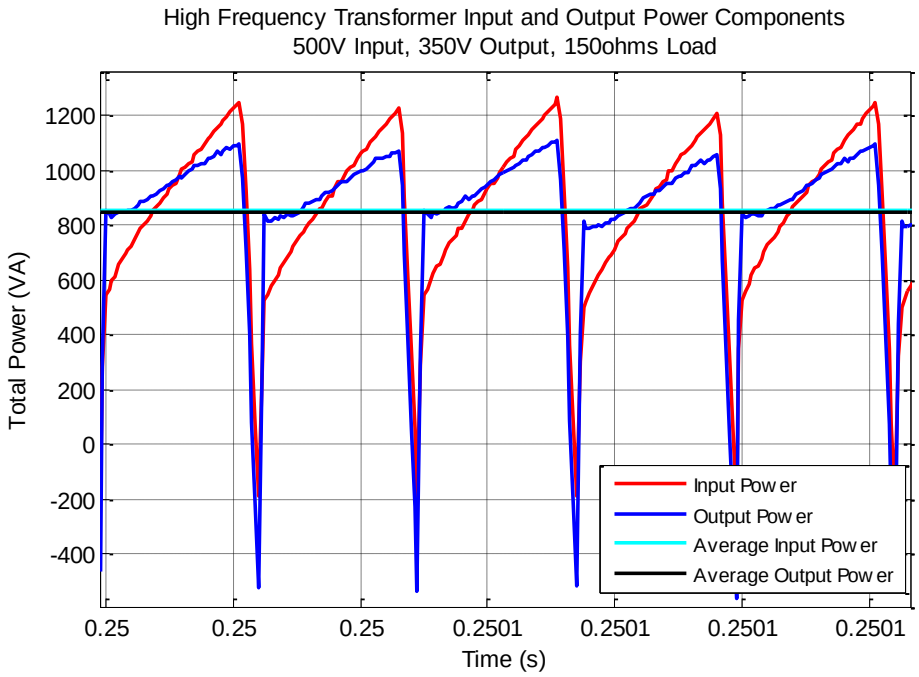


Figure 121: Total Input and Output Power Components of the Real High Frequency Transformer in the DAB Converter Prototype.

H-Bridge Converter

To ease estimation of frequency, the primary and the secondary bridge converters are assumed to be similar. This assumption is due to the difficulty of accessing the input current to the primary bridge, since the inverter stack has no internal sensor available for the purpose. In addition it is infeasible to open the inverter at this stage of test and place an external sensor. Also since the inverter stacks are of the same manufacturer and differences in behavior can be neglected.

Figure 122 shows the total input power to the Secondary H-bridge converter and the output power from it, the average of these powers are also indicated on the plot. In this case, the values difference is relatively differentiable, which is recorded to be exactly 43.15W.

The efficiency of the transformer is thus calculated to be

$$\eta_{Bridge} = \frac{806.22}{849.37} = 94.92\%$$

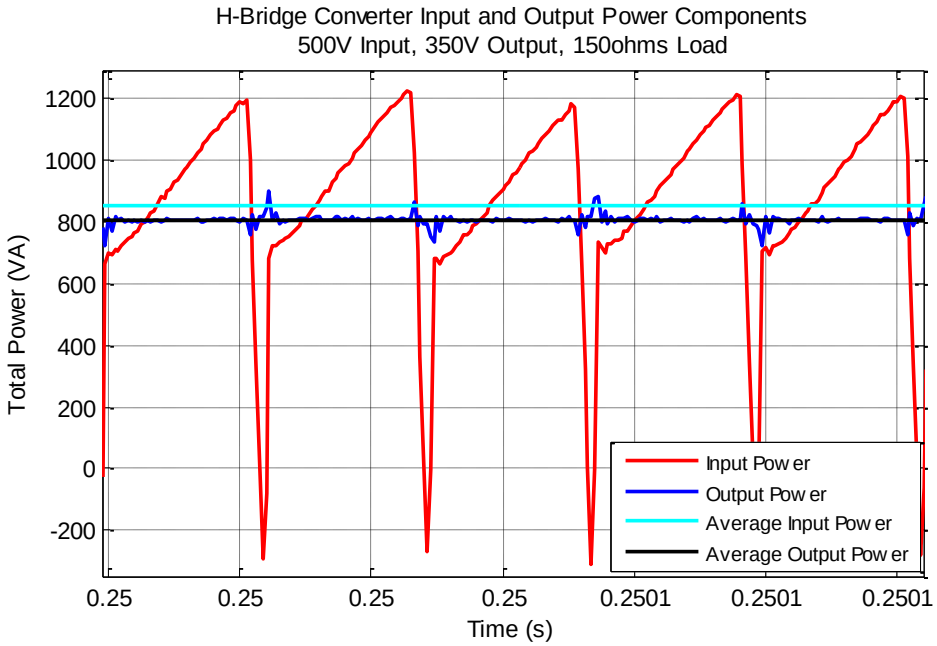


Figure 122: Total Input and Output Power Components of the Real H-Bridge Converter in the DAB Converter Prototype.

The overall efficiency of the system is thus calculated to be 98.13%. It is concluded that the efficiency of the high frequency transformer is the highest in the system. The HF transformer causes 0.5% drop in efficiency, while the inductor causes a relatively negligible drop, and the highest drop is caused by the bridge converter.

Thus is essential to target a more efficient bridge converter, by deploying an alternative modulation, discussed in Section 3.1.2. These modulation schemes besides reducing the circulating currents, but also allows and extends the ZVS range of operation, cutting down the switching losses associated with IGBT devices, which becomes more important as the switching frequency increases.

Chapter Eight

8. Conclusions and Outlook

This chapter presents the main conclusions reached out of the work, and puts the light on the main covered issues and the present work situation. Then an outlook is proposed for the future work.

8.1.Conclusions

The DAB converter topology is analyzed, simulated, and practically implemented. An approach for the study has been to employ the converter in an application to feed a resistive load. In general, the DAB converter is concluded to be an efficient power electronic converter with many optimization aspects available for enhancing its deployment in tying ESS to the grid.

The following points are the main aspects that have been studied and conclusions reached in each.

- The DAB converter topology has been analytically studied, deriving the characteristic equations that define its operation. In this aspect the analytical power low expression, depicted from derivation of current of current expression along different intervals of operation, has been compared to the fundamental harmonic approach, and found to accurately describe the power transfer within the converter.

- The control of the DAB has been structured and designed for suiting the application under test. In this aspect, an output voltage control with a single-loop structure was adopted, and the tuning process was carried out as a compromise between the controller performance to reference tracking and disturbance rejection. This gave rise to 0.8 damping ratio, which translates to 122 Hz integral gain at 50 Hz bandwidth.

- A simulation platform has been implemented for the DAB converter prior to constructing the experimental one. Using simulations, the studied concepts have been validated for correct prediction of converter behavior, thus basing the experimental work on expected waveforms and verified analysis. In this aspect, the ideal simulation has been additionally equipped with some loss elements of the real system, to assure as close match as possible with practical results.

- The DAB converter experimental test platform has been designed, and constructed. The design has been targeted towards three main components, the power stage, the programmer hardware, and the programmer software. In the design of the power stage, a special focus has been given to the design of the power transfer inductor, taking the opportunity of testing two designs, single wire and Litz wire. Moreover, in the characterization of the HF transformer, the saturation problem of magnetic cores has been discussed. The solution of adding a series capacitance has been selected to block any DC voltage component from being applied to the transformer. The design also discussed the main loss elements in the system, pushing forward a study for power limitations under the designed platform, which was concluded to be 2kW.

- As a final step, after the construction of the DAB converter system, tests have been carried out to validate its practical operation under the employed design and control concepts. Initially, low power tests were performed to characterize the steady state converter operation waveforms, and match those with the simulation ones. Then, an approach to increase the power has been taken, starting by developing a soft starting technique and gradual increase of reference command. The converter was verified for operation at open loop under a 1.7 kW power level, checking the system open loop transient response to a step change in phase shift. Then, the controller performance has been tested under load disturbance and found to ride-through the disturbance with a good transient response while successfully holding the system output voltage to the commanded reference one.

8.2.Future Work

Specific to the bidirectional DAB converter topology, many issues show motivations for study and implementation, among these issues are the following:

- The study and employment of the different modulation strategies discussed in Section 3.1.2, starting by DPS which was practical deployed for soft starting of the converter operation. These modulation strategies allow for a more efficient and optimized converter operation under wide load range.

- Replacing the resistive load by an ESS at the secondary bridge converter. All the presented study is expected to keep its validity for the forward power flow direction, however, the reverse direction will be a new possibility to further study.

- The study and implementation of a Multiport structure for integration of additional ESS via multiport transformer, allowing energy to be exchanged from and to all ports.

- Adopting a control strategy that targets the inductor current. This calls for an accurate complex sampling procedure to predict current slope during its different intervals of operation. However, controlling the primary side transformer current will fix the applied voltage to the transformer, thus avoiding any risk of core saturation.

- Studying and practical deployment of the Feed-Forward Controller as an approach for linearization of the relation between output current and phase shift that translates the controller CA to the system input being the external phase shift between primary and secondary bridges.

References

[1] L. Heinemann and G. Mauthe, “The Universal Power Electronics Based Distribution Transformer, an Unified Approach,” in IEEE Power Electronics Specialists Conference (PESC), 2001, pp. 504–509.

[2] UNIFLEX, “UNIFLEX Project,” 2013. [Online]. Available: http://www.eee.nott.ac.uk/uniflex/Project.htm

[3] M. Simoes, R. Roche, E. Kyriakides, A. Miraoui, B. Blunier, K. McBee, S. Suryanarayanan, P. Nguyen, and P. Ribeiro, “Smart-Grid Technologies and Progress in Europe and the USA,” in *IEEE Energy Conversion Congress and Exposition (ECCE)*, Sep. 2011, pp. 383–390.

[4] M. H. Kheraluwala and R. W. De Doncker, “Single phase unity power factor control for dual active bridge converter,” Conf. Rec. of the IEEE ndustry Applications Society Annual Meeting (IAS 1993), Toronto, Canada, 2–8 Oct. 1993, pp. 909–916.

[5] K. Wang, C. Y. Lin, L. Zhu, D. Qu, F. C. Lee, and J. S. Lai, “Bidirectional DC to DC converters for fuel cell systems,” Proc. of the IEEE Workshop on Power Electronics in Transportation, Dearborn, MI, 22–23 Oct. 1998, pp. 47–51.

[6] Florian Krismer, “Modeling and Optimization of Bi-directional DC-DC Converter Topologies,” a doctoral dissertation, 2010.

[7] Denish Sekhar Segran, “Dynamic Modelling and Control of Dual-Active-Bridge Bi-directional DC-DC Converters for Smart Grid Applications,” a doctoral dissertation, 2013.

[8] R. L. Steigerwald, “A comparison of half-bridge resonant converter topologies,” IEEE Transactions on Power Electronics, vol. 3, no. 2, pp. 174–182, April 1988.

[9] R. L. Steigerwald, “High-frequency resonant transistor DC-DC converters,” IEEE Transactions on Industrial Electronics, vol. IE-31, no. 2, pp. 181–191, May 1984.

[10] Biao Zhao; Qiang Song; Wenhua Liu; Yandong Sun, "Overview of Dual-Active-Bridge Isolated Bidirectional DC–DC Converter for High-Frequency-Link Power-Conversion System," Power Electronics, IEEE Transactions on , vol.29, no.8, pp.4091,4106, Aug. 2014

[11] N. Mohan, T. Undeland, and W. Robbins, Power electronics: Converters, applications, and design. Hoboken, NJ: John Wiley, 2003.

[12] D. G. Holmes and T. A. Lipo, Pulse Width Modulation For Power Converters -Principles and Practice, ser. IEEE press series on power engineering. Hoboken, NJ: John Wiley, 2003.

[13] A. Pressman, K. Billings, and T. Morey, Switching Power Supply Design, 3rd ed. New York, NY: McGraw-Hill, 2009.

[14] J. Shepherd, A. Morton, and L. Spence, Higher Electrical Engineering, 2nd ed.Essex: Longman Scientific and Technical, 1977.

[15] T. Wildi, Electrical Machines, Drives, and Power Systems, 6th ed. New Jersey: Prentice Hall, 2006.

[16] J. W.H. Hayt and J. A. Buck, Engineering Electromagnetics, 6th ed., ser. Electrical Engineering Series. McGraw-Hill, 2001.

[17] D. Segaran, D. Holmes, and B. McGrath, “Comparative analysis of single- and three-phase dual active bridge bidirectional dc-dc converters,” Aust. J. Electr. Electron. Eng., vol. 6, no. 3, pp. 1--12, 2009.

[18] R. W. A. A. De Doncker, D. M. Divan, and M. H. Kheraluwala, “A three-phasesoft-switched high-power-density dc-dc converter for high-power applications,” IEEE Trans. Ind. Appl., vol. 27, no. 1, pp. 63--73, 1991, 0093-9994.

[19] X. Jing, F. Wang, D. Boroyevich, and S. Zhiyu, “Single-phase vs. three-phase high density power transformers," in Proc. IEEE Energy Conversion Congress and Exposition (ECCE), 2010, pp. 4368--4375.

[20] D. Segaran, D. G. Holmes, and B. P. McGrath, “Comparative analysis of single and three-phase dual active bridge bidirectional dc-dc converters," in Proc.Australasian Universities Power Engineering Conference (AUPEC), 2008, pp.1--6.

[21] R. P. Severns, “Topologies for three-element resonant converters,” IEEE Transactions on Power Electronics, vol. 7, no. 1, pp. 89–98, Jan. 1992.

[22] R. L. Steigerwald, R. W. De Doncker, and M. H. Kheraluwala, “A comparison of high-power DC-DC soft-switched converter topologies,” IEEE Transactions on Industry Applications, vol. 32, no. 5, pp. 1139–1145,Sept./Oct. 1996.

[23] Power converter circuits having a high frequency link, William McMurrayhttp://www.google.com/patents/US3517300U.S. Patent 3517300, June 23, 1970.

[24] Abedini, A.; Lipo, T., “A novel topology of solid state transformer," Power Electronic & Drive Systems & Technologies Conference (PEDSTC), 2010 1st , vol., no., pp.101,105, 17-18 Feb. 2010

[25] Falcones, S.; Xiaolin Mao; Ayyanar, R., “Topology comparison for Solid State Transformer implementation," Power and Energy Society General Meeting, 2010 IEEE , vol., no., pp.1,8, 25-29 July 2010

[26] Shojaei, A.; Joos, G., "A topology for three-stage Solid State Transformer," Power and Energy Society General Meeting (PES), 2013 IEEE , vol., no., pp.1,5, 21-25 July 2013

[27] J. W. Kolar, G. Ortiz “Solid-State-Transformers: Key Components of Future Traction and Smart Grid Systems,” Proceedings of the International Power Electronics Conference - ECCE Asia (IPEC 2014), Hiroshima, Japan, May 18-21, 2014.

[28] P. Steimer, “Enabled by High Power Electronics - Energy Efficiency, Renewables and Smart Grids,” in International Power Electronics Conference (IPEC), Sapporo, 2010, pp. 11–15.

[29] T. Dragicevic, J. C. Vasquez, J. M. Guerrero, and D. Skrlec, “Advanced LVDC Electrical Power Architectures and Microgrids: A Step Toward a New Generation of Power Distribution Networks.” IEEE Electrification Magazine, vol. 2, no. 1, pp. 54–65, Mar. 2014.

[30] Beldjajev Viktor, R. Indrek, and L. Tõnu, “Intelligent Transformer: Possibilities and Challenges," Scientific Journal of Riga Technical University, vol. 29, pp. 95-100, 2011.

[31] H. Akagi, “Classification, Terminology, and Application of the Modular Multilevel Cascade Converter (MMCC)," Power Electronics, IEEE Transactions on, vol. PP, pp. 1-1, 2011.

[32] Power conversion apparatus for DC/DC conversion using dual active bridges, Rik W. DeDoncker, Mustansir H. Kheraluwala, Deepakraj M. Divanhttp://www.google.com/patents/US5027264U.S. Patent 5027264, June 25, 1991.

[33] M. H. Kheraluwala, R. W. Gascoigne, D. M. Divan, and E. D. Baumann, “Performance characterization of a high-power dual active bridge dc-to-dc converter,” *IEEE Trans. Ind. Appl.*, vol. 28, no. 6, pp. 1294–1301,Nov./Dec. 1992.

[34] H. L. Chan, K. W. E. Cheng, and D. Sutanto, "A novel square-wave converter with bidirectional power flow," in *Proc. IEEE Int. Conf. Power Electron. Drive Syst.*, 1999, pp. 966–971.

[35] H. L. Chan, K. W. E. Cheng, and D. Sutanto, "Phase-shift controlled dc-dcconverter with bidirectional power flow," *IEE Proc. Electric PowerAppl.*, vol. 148, no. 2, pp. 193–201, Mar. 2001.

[36] H. L. Chan, K. W. E. Cheng, and D. Sutanto, "ZCS-ZVS bidirectional phase-shifted dc-dc converter with extended load range," *IEE Proc. ElectricPower Appl.*, vol. 150, no. 3, pp. 269–277, May 2003.

[37] J. Biela, M. Schweizer, S. Waffler, and J. W. Kolar, "SiC versus Si-Evaluation of potentials for performance improvement of inverter anddc-dc converter systems by SiC power semiconductors," IEEE Trans. Ind. Electron., vol. 58, no. 7, pp. 2872–2882, Jul. 2011.

[38] M. C. Lee, C. Y. Lin, S. H. Wang, and T. S. Chin, "Soft-magnetic Febasednano-crystalline thick ribbons," IEEE Trans.Magn., vol. 44, no. 11,pp. 3836–3838, Nov. 2008.

[39] M. Ehsani, A. Gao, S. E. Gay, and A. Emadi, Modern Electric, HybridElectric, and Fuel Cell Vehicles: Fundamentals, Theory, and Design.Boca Raton: CRC Press, 2005.

[40] G. J. Su and L. Tang, "A three-phase bidirectional dc-dc converter for automotive applications," in Proc. IEEE Ind. Appl. Soc. Annu. Meet.,2008, pp. 1–7.

[41] J. H. Jung, C. K. Kwon, J. P. Hong, E. C. Nho, H. G. Kim, and T. W.CHun, "Power control and transformer design method of bidirectional dc-dc converter for a hybrid generation system," in Proc. IEEE VehiclePower Propulsion Conf., 2012, pp. 1512–1515.

[42] H. Krishnaswami and N. Mohan, "Three-port series-resonant dc-dc converter to interface renewable energy sources with bidirectional load and energy storage ports," IEEE Trans. Power Electron., vol. 24, no. 10,pp. 2289–2297, Oct. 2009.

[43] S. Inoue and H. Akagi, "A bidirectional isolated dc-dc converter as a core circuit of the next-generation medium-voltage power conversion system," IEEE Transactions on Power Electronics, vol. 22, pp. 535–542, Feb. 2007.

[44] S. Inoue and H. Akagi, "A bidirectional dc-dc converter for an energy storage system with galvanic isolation," IEEE Transactions on Power Electronics, vol. 22, pp. 2299–2306, Nov. 2007.

[45] S. Inoue and H. Akagi, "A bi-directional dc/dc converter for an energy storage system," in Twenty Second Annual IEEE Applied Power Electronics Conference (APEC), 2007, pp. 761–767, Mar. 2007.

[46] N. Tan, N. Tan, S. Inoue, S. Inoue, A. Kobayashi, and H. Akagi, "Voltage balancing of a 320-V, 12-F electric double-layer capacitor bank combined with a 10-kW bidirectional isolated dc-dc converter," IEEE Transactions on Power Electronics, vol. 23, pp. 2755–2765, Nov. 2008.

[47] N. M. L. Tan, T. Abe, and H. Akagi, "Design and performance of a bidirectional isolated dc-dc converter for a battery energy storage system," *IEEE Trans. Power Electron.*, vol. 27, no. 3, pp. 1237–1248, Mar. 2012.

[48] B. Reese, M. Schupbach, A. Lostetter, B. Rowden, R. Saunders, andJ. Balda, "High voltage, high power density bidirectional multi-level converters utilizing silicon and silicon carbide (SiC) switches," in *Proc.23th IEEE Annu. Appl. Power Electron. Conf. Expo.*, 2008, pp. 252–258.

[49] R. Morrison and M. Egan, “A new power-factor-corrected single-transformer UPS design,” IEEE Transactions on Industry Application, vol. 36, pp. 171–179,Jan./Feb. 2000.

[50] H. Tao, A. Kotsopoulos, J. L. Duarte, and M. A. M. Hendrix, “A soft switched three-port bidirectional converter for fuel cell and super capacitor applications,” in Proc. 36th IEEE Power Electron. Spec. Conf., 2005,pp. 2487–2493.

[51] H. Tao, A. Kotsopoulos, J. L. Duarte, and M. A. M. Hendrix, “Design of a soft-switched three-port converter with DSP control for power flow management in hybrid fuel cell systems,” in Proc. Eur. Conf. Power Electron. Appl., 2005, pp. 1–10.

[52] H. Tao, A. Kotsopoulos, J. L. Duarte, and M. A. M. Hendrix, “Family of multiport bidirectional dc-dc converters,” IEE Proc. Electric Power Appl., vol. 153, no. 3, pp. 451–458, May 2006.

[53] C. Zhao, S. D. Round, and J. W. Kolar, “An isolated three-port bidirectional dc-dc converter with decoupled power flow management,” IEEE Trans. Power Electron., vol. 23, no. 5, pp. 2443–2453, Sep. 2008.

[54] H. Tao, A. Kotsopoulos, J. L. Duarte, and M. A. M. Hendrix, “Triple half-bridge bidirectional converter controlled by phase shift and PWM,”in Proc. 21st IEEE Annu. Appl. Power Electron. Conf. Expo., 2006,pp. 1256–1262.

[55] M. Phattanasak, R. G. Ghoachani, J. P. Martin, S. Pierfederici, and B.Davat, “Flatness based control of an isolated three-port bidirectional dc dc converter for a fuel cell hybrid source,” in Proc. IEEE Energy Convers. Congr. Expo., 2011, pp. 977–984.

[56] Z. Wang and H. Li, “An integrated three-port bidirectional dc-dc converter for PV application on a dc distribution system,” IEEE Trans. Power Electron., vol. 28, no. 10, pp. 4612–4624, Oct. 2013.

[57] G. Waltrich, J. Duarte, and M. Hendrix, “Multiport converters for fast chargers of electrical vehicles - focus on high-frequency coaxial transformers," in Proc.2010 IEEE International Power Electronics Conference (IPEC), 2010, pp. 3151-- 3157.

[58] M. Cacciato, F. Caricchi, F. Giuhlii, and E. Santini, “A critical evaluation and design of bi-directional dc/dc converters for super-capacitors interfacing in fuel cell applications,” in Proc. 39th IEEE Industry Applications Society Annual Meeting (IAS), vol. 2, 2004, pp. 1127--1133.

[59] Z. Fanghua, X. Lan, and Y. Yangguang, “Bi-directional forward-flyback dc-dc converter,” in Proc. 35th IEEE Power Electronics Specialists Conference(PESC), vol. 5, 2004, pp. 4058--4061.

[60] J. W.H. Hayt and J. A. Buck, Engineering Electromagnetics, 6th ed., ser.Electrical Engineering Series. McGraw-Hill, 2001.

[61] M. Pavlovsky, S. W. H. de Haan, and J. A. Ferreira, “Concept of 50 kwdc/dc converter based on zvs, quasi-zcs topology and integrated thermal and electromagnetic design,” in Proc. IEEE European Conference on Power Electronics and Applications (EPE), 2005, p. 9 pp.

[62] J. Biela, U. Badstuebner, and J. Kolar, “Design of a 5-kw, 1-u, 10-kw/dm3resonant dc dc converter for telecom applications,” IEEE Trans. Power Electron., vol. 24, no. 7, pp. 1701--1710, 2009.

[63] D. Segaran, B. P. McGrath, and D. G. Holmes, “Adaptive dynamic control ofa bi-directional dc-dc converter,” in Proc. IEEE Energy Conversion Congress and Exposition (ECCE), 2010, pp. 1442--1449.

[64] J. Jacobs, A. Averberg, and R. De Doncker, “A novel three-phase dc/dc converter for high-power applications," in Proc. 35th IEEE Power Electronics Specialists Conference (PESC), vol. 3, 2004, pp. 1861--1867.

[65] D. M. Divan and G. Skibinski, “Zero-switching-loss inverters for high-power applications," IEEE Trans. Ind. Appl., vol. 25, no. 4, pp. 634--643, 1989.

[66] R. L. Steigerwald, “High-frequency resonant transistor dc–dc converters,” IEEE Trans. Ind. Electron., vol. IE-31, no. 2, pp. 181–191, May 1984.

[67] Krismer, F.; Round, S.; Kolar, J.W., "Performance Optimization of a High Current Dual Active Bridge with a Wide Operating Voltage Range," *Power Electronics Specialists Conference, 2006. PESC '06. 37th IEEE* , vol., no., pp.1,7, 18-22 June 2006

[68] Krismer, F.; Kolar, J.W., "Efficiency-Optimized High-Current Dual Active Bridge Converter for Automotive Applications," *Industrial Electronics, IEEE Transactions on* , vol.59, no.7, pp.2745,2760, July 2012

[69] G. Goodwin, S. Graebe, and M. Salgado, Control System Design. PrenticeHall, 2001.

[70] T. Haimin, J. L. Duarte, and M. A. M. Hendrix, “Three-port triple-half-bridgebidirectional converter with zero-voltage switching,” IEEE Trans. PowerElectron., vol. 23, no. 2, pp. 782--792, 2008.

[71] T. Haimin, A. Kotsopoulos, J. L. Duarte, and M. A. M. Hendrix, “Transformer-coupled multiport zvs bidirectional dc-dc converter with wide input range," IEEE Trans. Power Electron., vol. 23, no. 2, pp. 771--781, 2008, 0885-8993.

[72] H. Z., T. D., S. T.S., and A. Khambadkone, “Interleaved bi-directional dual active bridge dc-dc converter for interfacing ultracapacitor in micro-grid application," in Proc. 2010 IEEE International Symposium on Industrial Electronics (ISIE), 2010, pp. 2229--2234.

[73] W. Kunrong, Z. Lizhi, Q. Dayu, H. Odendaal, J. Lai, and F. C. Lee, “Design, implementation, and experimental results of bi-directional full-bridge dc/dc converter with unified soft-switching scheme and soft-starting capability,” in Proc. 31st IEEE Power Electronics Specialists Conference (PESC), vol. 2,2000, pp. 1058--1063.

[74] F. Krismer and J. W. Kolar, “Accurate small-signal model for the digital control of an automotive bidirectional dual active bridge,” IEEE Trans. PowerElectron., vol. 24, no. 12, pp. 2756--2768, 2009.

[75] T. Haimin, J. L. Duarte, and M. A. M. Hendrix, “High-power three-port three-phase bidirectional dc-dc converter," in Proc. 42nd IEEE Industry ApplicationsSociety Annual Meeting (IAS), 2007, pp. 2022--2029.

[76] M. Rosekeit and R. W. De Doncker, “Smoothing power ripple in single phase chargers at minimized dc-link capacitance," in Proc. IEEE Energy Conversion Congress and Exposition Asia (ECCE Asia), 2011, pp. 2699--2703.

[77] Jorge García García, “Magnetic Components Design,” a Seminar, Master Degree Course on Industrial Electronics in Renewable Energy Generation Systems, University of Oviedo, 2013.

[78] M. N. Kheraluwala, R. W. Gascoigne, D. M. Divan, and E. D. Baumann, “Performance characterization of a high-power dual active bridge,” IEEE Trans. Ind. Appl., vol. 28, no. 6, pp. 1294--1301, 1992, 0093-9994.

[79] H. Akagi and R. Kitada, “Control and design of a modular multilevel cascade btb system using bidirectional isolated dc-dc converters,” IEEE Trans. Power Electron., vol. 26, no. 9, pp. 2457 -- 2464, 2011.

[80] A. Rodr´ıguez, J. Sebastian, D. G. Lamar, M. M. Hernando, and A. Vazquez, "An overall study of a dual active bridge for bidirectional DC/DC conversion," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep.2010, pp. 1129–1135.

[81] Amit Kumar Jain, and Rajapandian Ayyanar "PWM Control of Dual Active Bridge: Comprehensive Analysis and Experimental Verification," IEEE Trans. Power Electron., vol. 26, no. 4, 2011.

[82] G. James, D. Burley, D. Clements, P. Dyke, and J. Searl, Modern Engineering Mathematics. Pearson Prentice Hall, 2007.

[83] B. Zhao, Q. Yu, and W. Sun, "Extended-phase-shift control of isolated bidirectional dc-dc converter for power distribution in microgrid," IEEE Trans. Power Electron., vol. 27, no. 11, pp. 4667–4680, Nov. 2012.

[84] G. G. Oggier, R. Ledhold, G. O. Garcia, A. R. Oliva, J. C. Balda, and F.Barlow, "Extending the ZVS operating range of dual active bridge high power dc-dc converters," in Proc. IEEE Power Electron. Spec. Conf.,2006, pp. 1–7.

[85] G. D. Demetriades and H. P. Nee, "Characterization of the dual-active bridge topology for high-power applications employing a duty-cycle modulation," in Proc. IEEE Power Electron. Spec. Conf., 2008, pp. 2791–2798.

[86] G. G. Oggier, G. O. Garcia, and A. R. Oliva, "Switching control strategy to minimize dual active bridge converter losses," IEEE Trans. Power Electron., vol. 24, no. 7, pp. 1826–1838, Jul. 2009.

[87] G. G. Oggier, G. O. Garcia, and A. R. Oliva, "Modulation strategy to operate the dual active bridge dc-dc converter under soft switching in the whole operating range," IEEE Trans. Power Electron., vol. 26, no. 4,pp. 1228–1236, Apr. 2011.

[88] B. Zhao, Q. Song, and W. Liu, "Power characterization of isolated bidirectional dual-active-bridge dc-dc converter with dual-phase-shift control," IEEE Trans. Power Electron., vol. 27, no. 9, pp. 4172–4176, Sep.2012.

[89] H. Bai and C. Mi, "Eliminate reactive power and increase system efficiency of isolated bidirectional dual-active-bridge DC-DC converters using novel dual-phase-shift control," IEEE Trans. Power Electron., vol. 23,no. 6, pp. 2905–2914, Nov. 2008.

[90] H. Bai, C. Mi, C.Wang, and S. Gargies, "The dynamic model and hybrid phase-shift control of a dual-active-bridge converter," in Proc. 34th Annu. Conf. IEEE Ind. Electron. Soc. (IECON), 2008, pp. 2840–2845.

[91] H. Bai, Z. Nie, and C. Mi, "Experimental comparison of traditional phase-shift, dual-phase-shift, and model-based control of isolated bidirectional dc-dc converters," IEEE Trans. Power Electron., vol. 25, no. 6,pp. 1444–1449, Jun. 2010.

[92] M. Kim, M. Rosekeit, S. K. Sul, and R. W. A. D. Doncker, "A dual-phase-shift control strategy for dual-active-bridge dc-dc converter in wide voltage range," in Proc. 8th IEEE Int. Conf. Power Electron. ECCE Asia, 2011, pp. 364–371.

[93] B. Zhao,Q. Song, W. Liu, and W. Sun, "Current-stress-optimized switching strategy of isolated bidirectional dc-dc converter with dual- phase shift control," IEEE Trans. Ind. Electron., vol. 60, no. 10, pp. 4458–4467,Oct. 2013.

[94] B. Zhao, Q. Song, and W. Liu, "Efficiency characterization and optimization of isolated bidirectional dc-dc converter based on dual- phase-shift control for dc distribution application," IEEE Trans. Power Electron., vol. 28, no. 4, pp. 1711–1727, Apr. 2013.

[95] F. Krismer and J. W. Kolar, "Closed form solution for minimum conduction loss modulation of DAB converters," *IEEE Trans. Power Electron.*,vol. 27, no. 1, pp. 174–188, Jan. 2012.

[96] H. Zhou and A. M. Khambadkone, "Hybrid modulation for dual-active-bridge bidirectional converter with extended power range for ultra capacitor application," *IEEE Trans. Ind. Appl.*, vol. 45, no. 4, pp. 1434–1442, Jul./Aug. 2009.

[97] Y. Du, S. M. Lukic, B. S. Jacobson, and A. Q. Huang, "Modulation technique to reverse power flow for the isolated series resonant dc-dcconverter with clamped capacitor voltage," IEEE Trans. Ind. Electron.,vol. 59, no. 12, pp. 4617–4628, Dec. 2012.

[98] K. Wu, C. W. Silva, and W. G. Dunford, "Stability analysis of isolated bidirectional dual active full-bridge dc-dc converter with triple phase-shift-control," IEEE Trans. Power Electron., vol. 27, no. 4, pp. 2007–2017, Apr. 2012.

[99] Y. Xie, J. Sun, and J. S. Freudenberg, "Power flow characterization ofa bidirectional galvanically isolated high-power dc-dc converter over awide operating range," IEEE Trans. Power Electron., vol. 25, no. 1,pp. 54–66, Jan. 2010.

[100] B. Zhao, Q. Song, W. Liu, and Y. Sun, "Dead-time effect of the high frequency isolated bidirectional full-bridge dc-dc converter: Comprehensive theoretical analysis and experimental verification," IEEE Trans. Power Electron., vol. 29, no. 4, pp. 1667–1680, Apr. 2014.

[101] J. Li, Z. Chen, Z. Shen et al., "An adaptive dead-time control scheme forhigh-switching-frequency dual-active-bridge converter," in Proc. 27thAnnu. IEEE Appl. Power Electron. Conf. Expo., 2012, pp. 1355–1361.

[102] D. Costinett, R. Zane, and D. Maksimovic, "Automatic voltage and deadtime control for efficiency optimization in a dual active bridge converter, "in Proc. 27th Annu. IEEE Appl. Power Electron. Conf. Expo.), 2012,pp. 1104–1111.

[103] Gabriel Ortiz, Lukas Fassler, Johann Walter Kolar, and Oscar Apeldoorn, "Flux Balancing of Isolation Transformers and Application of "The Magnetic Ear" for Closed-Loop Volt–Second Compensation," IEEE Trans. Power Electron., vol. 29, no. 8, Aug. 2014.

[104] R. Patel, "Detecting impending core saturation in switched-mode power converters," in *Proc. 7th Nat. Solid-State Power Convers. Conf.*, Mar.1980, vol. B3, pp. 1–11.

[105] S. Klopper and J. A. Ferreira, "A sensor for balancing flux in converterswith a high-frequency transformer link," *IEEE Trans. Ind. Appl.*, vol. 33,no. 3, pp. 774–779, May/Jun. 1997.

[106] D. Wilson, "A new pulse width modulation method inherently maintain output transformer flux balance," in *Proc. 8th Nat. Solid-State Power Convers. Conf.*, Apr. 1981, vol. D1, pp. 1–14.

[107] F. P. Dawson, "DC-DC converter inter phase transformer design considerations: Volt-seconds balancing," IEEE Trans. Magn., vol. 26, no. 5,pp. 2250–2252, Sep. 1990.

[108] P. Ripka, "Review of fluxgate sensors," Sens. Actuat. A: Phys., vol. 33, no. 3, pp. 129–141, 1992.

[109] R. Kuttner, "Circuit techniques for eliminating primary current unbalance in push-pull power converters," in Proc. 7th Nat. Solid-State Power Convers. Conf., Mar. 1980, vol. F2, pp. 1–9.

[110] O. Garcia, P. Zumel, A. De Castro, P. Alou, and J. Cobos, “Current self-balance mechanism in multiphase buck converter,” IEEE Trans. Power Electron., vol. 24, no. 6, pp. 1600–1606, Jun. 2009.

[111] D. Costinett, D. Seltzer, D. Maksimovic, and R. Zane, “Inherent volt second balancing of magnetic devices in zero-voltage switched power converters,” in Proc. Appl. Power Electron. Conf. Expo., 2013, pp. 9–15.

[112] F. Stogerer, J. W.Kolar and U.Drofenik, “A novel concept for transformer volt second balancing of VIENNA rectifier III based on direct magnetizing current measurement,” in *Proc. Nordic Workshop Power Ind. Electron. Workshop*, Jun. 2000, pp. 134–139.

[113] W. M. Polivka, A. Cocconi, and S. Cuk, “Detection of magnetic saturation in switching converters,” in *Proc. Power Convers. Int. Conf.*, Mar. 1982, pp. 584–597.

[114] S. Han, I. Munuswamy, and D. Divan, “Preventing transformer saturation in bi-directional dual active bridge buck-boost DC-DC converters,” in Proc. Energy Convers. Congr. Expo., Sep. 2010, pp. 1450–1451.