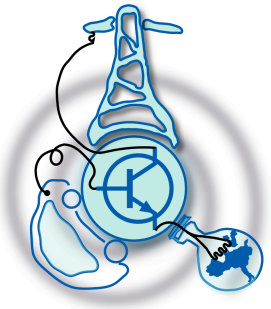
Design and Control of Single-phase Modular Multilevel Converter

by

Mario López Medina



Submitted to the Department of Electrical Engineering, Electronics, Computers and Systems
in partial fulfillment of the requirements for the degree of
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Abstract

The Modular Multilevel Converter (MMC) is a subject of current research in power electronics. Though a number of control and modulation strategies have been proposed, still there is no general agreement on the methodology used for their classification, analysis and evaluation.

This master thesis will analyze the operating principles of the MMC, with special focus on the different modulation strategies that can be applied. A new modulation approach will be developed , with the goal of reducing the size and cost of the passive components, such as the arm inductances and the cell capacitors. Control objectives as well as the evaluation and classification of the control strategies already proposed in the literature will also be covered. Finally, a new control strategy will be proposed. Simulation results will be provided in order to demonstrate the correct operation of the converter control as well as a brief comparison between different modulation strategies.

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Glossary

AC	Alternating current
DC	Direct current
FACTS	Flexible AC transmission system
HVDC	High voltage direct current
NPC	Neutral point clamped
FC	Flying capacitor
CHB	Cascaded H-bridge
MMC	Modular multilevel converter
M2C	Modular multilevel converter
MMCC	Modular multilevel cascade converter
SSBC	Single star bridge cells
SDBC	Single delta bridge cells
DSCC	Double star chopper cells
DSBC	Double star bridge cells
PLL	Phase-locked loop
FFT	Fast Fourier transform
N	Number of submodules per arm
n	Number of levels in output voltage

V_{DC}	DC bus voltage
i_D	DC-side current
V_j	Voltage inserted by submodule j
i_P	Upper arm current
i_N	Lower arm current
i_{Circ}	Circulating current
V_{limb}	Voltage in the limb inductors
V_{UN}	Output phase voltage
R_{arm}	Arm resistance
L_{arm}	Arm inductance
V_{capj}	Capacitor voltage of cell j
i_{out}	Output current
V_{up}	Voltage inserted by upper cells
V_{low}	Voltage inserted by lower cells
S_{jT}	Switching state for the top device in cell j
i_{grid}	Grid current
V_{grid}	Grid voltage
ω_e	Fundamental frequency
R_f	Output filter resistance
L_f	Output filter inductance
T_{ratio}	Transformer turns ratio
G_{RCR}	Transfer function of resonant output current regulator
G_F	Output filter transfer function
P_{ACrms}	AC-side rms power

G_{limb}	Transfer function of limb inductors
G_{CCR}	Transfer function of circulating current regulator
G_{RCCR}	Transfer function of resonant circulating current regulator
G_{VR}	Transfer function of voltage regulator in the overall stored energy control loop
${i_{volt}}^*$	Circulating current reference generated by the overall stored energy control loop

Subscripts

u,v,w	phases u, v and w

Superscripts

$\overline{x}$	DC component
$\widetilde{x}$	AC component
$\hat{x}$	Amplitude
x^*	Reference

Chapter 1

Introduction

1.1 Introduction

The increasing penetration of renewable energies, as well as more demanding requirements in terms of efficiency and reliability in the electrical network leads to a big challenge, as a significant part of the installed capacity will be connected to the distribution levels in the near future.

It is in this scenario where power power electronics makes its appearance. Innovative operational equipment based on power electronics and capable to be connected to the medium voltage grids, able to provide several functions to the power operator, such as controlling power flow, reduction in transmission losses and power quality improvement among others will be needed, example of this being HVDC and FACTS technologies.

Among the different multilevel topologies, the Modular Multilevel Converter (MMC) has currently become a subject of intense research. While it shares the appealing properties of other multilevel configurations, it offers some interesting and useful features. As a result of this, the MMC has been an active research topic in recent years.

Despite of its advantages, control of MMC is still a challenging task. Due to the fact that it is not still a mature technology, there is no general agreement about the different control strategies, modulation approaches, classification. Systematizing the analysis and evaluation of control and modulation strategies for MMCs will be the

major goal of this master thesis.

1.2 Objectives

The main objectives of this master thesis are:

- Study of the basic operating principle of the MMC topology.
- Evaluation and discussion of the different modulation strategies, based on the intrinsic features of the MMC configuration.
- Development of a modulation strategy, aiming to reduce the current ripple in the circulating current and consequently, enabling the reduction in size and cost of passive components, such as the arm inductances and cell capacitors.
- Analysis of the different control objectives for the MMC topology.
- Classification of the control strategies attending to various criteria.
- Choosing the passive components for the further development of a 3kW experimental rig.
- Design and simulation of a control strategy based on real parameters, for further experimental construction and verification. Special attention will be paid to the control of the circulating current.
- Analysis of the start-up stage of the converter.

1.3 Master Thesis Outline

This master thesis is divided into six chapters, with the following structure:

In chapter 1, an introduction concerning the main objectives of the thesis is presented.

Chapter 2 presents the state of the art of the MMC. Firstly, the modern electric network is described to explain the need for power electronics-based equipment and

particularly, the need for multilevel converters. Secondly, the main motivation and features of multilevel converters are discussed and the main topologies are briefly explained. To conclude, the MMC topology is introduced and its most relevant features and advantages are discussed.

In chapter 3, the basic structure and the operating principles are deeply described. After that, the different modulation approaches are analyzed based on the previous discussion. A modulation strategy is further proposed aiming to reduce the current ripple in the circulating current and as a consequence, enabling the use of downsized arm inductors.

Chapter 4 focuses on the control of the MMC, starting with the analysis of the different control objectives and a classification of the control strategies that have already been proposed. The design of a control strategy is latter addressed, which is verified by means of simulation. Finally, a comparison among modulation strategies is presented, with special attention to the arm inductance and cell capacitors required by each concept.

Chapter 5 summarizes the work developed along this thesis. Conclusions and future developments are finally presented.

Chapter 6 summarizes the activities developed in the host institution in case of an external master thesis.

Chapter 2

State of the Art

2.1 The new power-electronics-based energy network scenario

The current energy scenario is unavoidably changing. The strong dependence on fossil fuels and the progressive increase of its cost is leading to the investment of huge amounts of resources, economical and human, to develop new cheaper and cleaner energy resources, not directly related to fossil fuels [7] as well as to seek for the maximum efficiency in every energy conversion process. In this context, the electric power industry is undergoing profound technical, economical and organizational changes. Traditionally, the electric power industry was characterized by a vertical structure, consisting of power generation, transmission/distribution and trading [2]. The liberalization process has resulted in the unbundling of this organizational structure, where the different stages might be organized in separate business entities, subject to competition. As a consequence, the operation of the networks has been pushed near their technical limits, the stress on the system being considerably bigger than in the past. The efficient use of all network elements is of prime interest to the network operator, as the economical constraints have also become much tighter than in the past [2].

The traditional planning approaches for power networks are going through a rein-

vention process. The long lasting experience with the power unidirectionally flowing from the power plants to the customers is no longer valid. Growing volatility and an increasing unpredictability of the system behavior, requires innovative equipment to successfully handle such situations [2]. The introduction of distributed generation units close to the customers is changing the functionality and the requirements of the distribution networks. The grid operator is requested to provide network access to any interested stakeholder in a transparent and non-discriminatory manner.

The necessity to design electric power networks, maximizing their power transfer capability, while minimizing the costs, leads to a great engineering challenge [2]. It is in this scenario where power electronics makes its appearance. Innovative operational equipment based on power electronics can be present in all modern energy network stages:

- In the generation area, power electronics plays a key role in renewable generation systems. Photovoltaic generation and fuel cells require basically power conversion from DC to AC. Wind energy requires the use of variable speed drives to achieve the maximum efficiency in the wind energy capture process. Small hydrogenerators also obtain benefits from the use of variable speed drives. In the coming decades, electrical energy storage is expected to be widely used in power systems as capacitor, battery, flywheels and superconducting magnet technologies [1]. All these concepts require the use of electronic power converters.

- In the transmission stage, application of power electronics basically consists of High Voltage Direct Current transmission systems (HVDC) and Flexible AC Transmission Systems (FACTS). FACTS devices can be utilized to increase the transmission capacity, improve the stability and dynamic behavior of the electric grid, ensure better power quality and adequate interconnection of renewable and distributed generation and storage resources [2]. On the other hand, the main role of HVDC concerns the interconnection of electric grids in those cases in which the use of AC transmission reveals inadequate. This technology is mainly

applied to submarine cables, long distance overhead transmission, underground transmission and connecting AC systems of different frequencies [1].

- In the distribution area, an exciting opportunity called "Custom Power" enables solutions to deliver reliable electric service to the industrial and commercial customers. This term comprises the whole area of power conditioning technology used by customers under the term of Power Quality. Uninterruptible power supplies (UPS) and voltage regulators represent a major growth area in power electronics [1]. On the other hand, the promising and incoming generation of battery electric vehicles offering the possibility of grid support at every home or car park should be also bear in mind.

  Additionally, the development of the smart grid concept should not be forgotten. The smart power grid distributed energy system would provide the platform for the use of renewable sources and adequate emergency power for major metropolitan load centers and would safeguard in preventing the complete blackout of the interconnected power systems due to man-made events and environmental calamity and would provide the ability to break up the interconnected power systems into the cluster smaller regions [4].

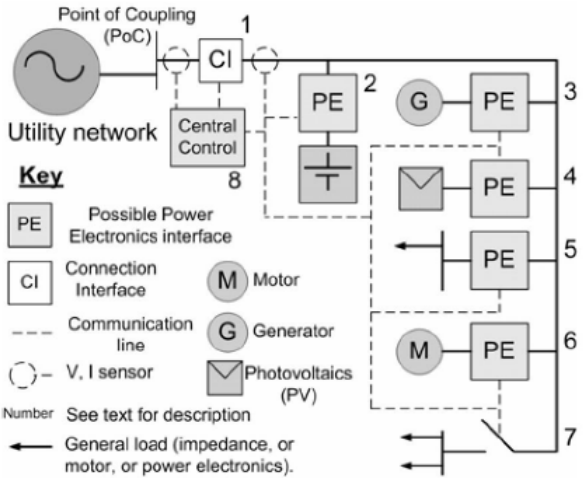

Figure 2-1: Potential Microgrid System Technologies [6]

- On the end-use side, power electronics conversion and switching technology has

been a fast-growing area for over two decades. Efficient lighting, computers, communications, lasers, visuals, sound, robots, medical tools, and of course, variable speed drives and the expanding need for dc power supplies are among the many other examples.

In the aforementioned search for efficiency in power systems, the big industrial consumers must be taken into account. In fact, there is a remarkable place for efficiency improvement in the field of electric motor driven applications. The medium voltage (MV) drives cover power ratings from 0.4 MW to 40 MW at the medium voltage level of 2.3 to 13.8 kV. In this way, the majority of the installed MV drives are in the 1 to 4 MW range with voltage ratings from 3.3 kV to 6.6 kV [5]. One of the major markets for the MV drive is precisely to retrofit applications intended to improve the efficiency and in the end, to achieve energy saving. It is reported that 97% of the currently installed MV motors operate at a fixed speed and only 3% of them are controlled by variable speed drives [5]. When fans or pumps are driven by a fixed speed motor, the control of air or liquid flow is normally achieved by conventional mechanical methods, such as throttling control, inlet dampers, and flow control valves, resulting in a substantial amount of energy loss [5]. As a consequence, the installation of the MV drive can lead to significant savings of energy demand.

2.2 Multilevel Converters

The previously described scenario has contributed to the appearance of new power converter topologies and new semiconductor technologies, capable to operate connected to the medium voltage grids. Desing of such medium-high voltage power converters can approached using classic power converter topologies and high-voltage semiconductors, or new modular converter topologies with low-medium voltage power devices [7], as shown in Fig. 2-2. In this context, multilevel converters are a good solution for power applications due to the fact that they can achieve high power using mature medium-power semiconductor technology [7].

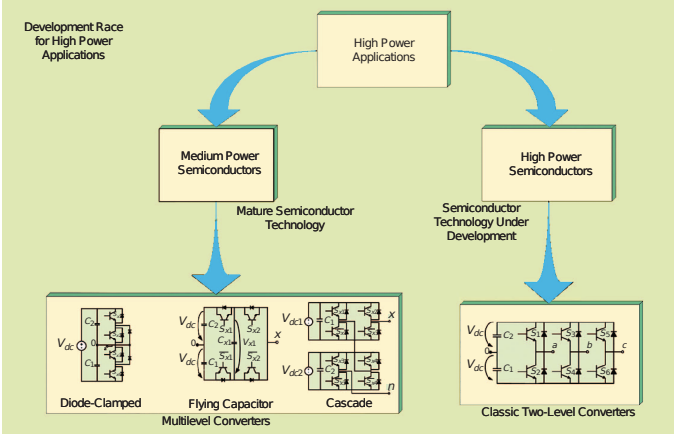

Figure 2-2: Two-level power converters versus most common multilevel power converters [7].

2.2.1 Motivation and Main Features

The motivation for multilevel converters mainly comes from the necessity of two different kind of converters: high voltage (and high power) converters and high output frequency converters with low switching frequency power devices.

If a high power converter is needed, a design based on using conventional circuits, serializing/parallelizing power switches could considered. However, this option presents some important drawbacks: serializing/parallelizing switching devices is difficult to implement practically, since voltage/current sharing between the devices represents a challenging task.

The main application field for high power converters is mainly centered on high power machine drives and power converters for grid applications such as HVDC, FACTS.

On the other hand, if a high power, high output frequency converter is needed, a conventional 2-level solution have limited possibilities due to the device switching frequency imposes restrictions. On the contrary, for a multilevel converter, the effective switching frequency can be higher than the individual device switching frequency. Thus, it can produce low THD waveshapes with relatively low switching frequencies.

The main application field for high output frequency converters is focused on very high speed motor drives, compressors, etc.

The motivation and features of multilevel power converters can be summarized as follows:

- Voltage sharing among devices will be handled automatically by the topology
- Multi-level waveform will lead to reduced harmonic distortion for a given switching frequency
- Increasing converter operating voltage (power rating) without the need of connecting devices in series
- Reduction of Electromagnetic Interference (EMI) due to lower voltage steps and thus, reduce filtering requirements and impact on insulation
- Drawing input current with very low distortion [11]
- Generating smaller common-mode voltage, thus reducing the stress e.g. in the motor bearings for the case of electric drives[11]

2.2.2 Review of Multilevel Topologies

A patent search carried out in [11] showed that multilevel power converters have been around for more than 40 years. An early traceable patent appeared in 1975 [13], in which the cascade inverter was first defined with a format that connects DC-sourced full-bridge cells in series to synthesize a staircase AC output voltage [11]. Through manipulation of the cascade inverter, with diodes blocking the sources, the diode-clamped multilevel inverter was then derived.

The most common multilevel converter topologies are the neutral point clamped converter (NPC), flying capacitor converter (FC) and cascaded H-bridge converter (CHB) [7].

2.2.2.1 Neutral Point Clamped (NPC) Converter

The diode-clamped converter, also called the neutral-point clamped converter, was first used in a three-level converter in which the mid-voltage level was defined as the

neutral point [11]. In 1981, A. Nabae, I. Takahashi, and H. Akagi presented the first NPC pulse width modulation (PWM) converter [14].

This kind of converter is based on a modification of the classic two-level converter topology adding two new power semiconductors per phase, as it can be seen in Fig. 2-3.

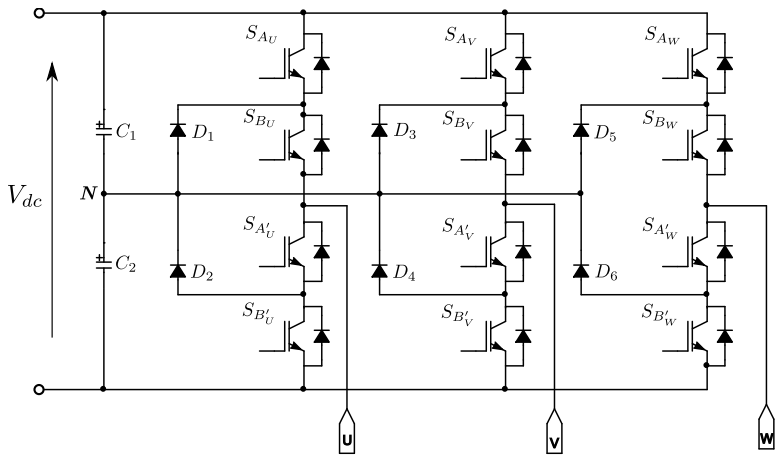

Figure 2-3: Three-level Neutral Point Clamped (NPC) converter

In this circuit, the DC bus voltage is split into three levels by two series-connected bulk capacitors, C_1 and C_2. The middle point of the two capacitors (N) can be defined as the neutral point. In this way, the three-level NPC in Fig. 2-3 is able to generate an output voltage V_{xN} with three states: $V_{dc}/2$, 0 and $-V_{dc}/2$.

The main difference of this topology with respect to the conventional 2-level converter are the diodes ($D_1 ... D_6$). Diodes of the same leg clamp the switch voltage to half the level of the DC bus voltage. E.g., when S_{AU} and S_{BU} are closed, D_2 balances the voltage sharing between S'_{AU} and S'_{BU} with S'_{AU} blocking the voltage across C_1 and S'_{BU} blocking the voltage across C_2. Without the presence of these diodes, the output voltage levels would not be defined.

Table 2.1 shows the different switching states for the three level output phase-to-neutral voltage.

The main advantage of this topology is that just one isolated DC supply is required. In other words, it is similar to a conventional converter in the sense of having a DC side and AC side. The main concerns for this power converter topology can be

V_{xN}	A	B	A'	B'
$V_{dc}/2$	1	1	0	0
0	0	1	1	0
$-V_{dc}/2$	0	0	1	1

Table 2.1: Switching states 3-level NPC converter

summarized as follows:

- Except in the three-level circuit, the capacitor voltages cannot be balanced by appropriate selection of switching patterns. For topologies with more than 3 levels, extra balancing circuit is needed or multiple DC supplies are required.

- As the number of levels increases, some diodes have to block large voltages. This situation makes the topology unattractive for more than 5 levels. Consequently, and assuming that each blocking diode voltage rating is the same as the active device voltage rating, the number of diodes required for each phase will be (m-1)x(m-2), being "m" the number of levels in the phase-to-neutral output voltage. This number represents a quadratic increase in m. When the number of levels increases, the number of diodes required will make the system impractical [11].

- This topology is not well suited for redundancy

2.2.2.2 Capacitor-Clamped (Flying Capacitor) Converter

In this topology, the voltage sharing between the switches is not made by the diodes, but by means of capacitors (C_3, C_4 and C_5), i.e., independent capacitors clamp the device voltage to one capacitor voltage level. Fig. 2-4 shows a three-level flying capacitor topology. Similarly to the NPC converter, this topology is able to generate an output phase voltage consisting of three levels: $V_{dc}/2$, 0 and $-V_{dc}/2$.

Table 3.1 shows the different switching states for the three level case.

The main operational issue concerns the capacitors voltage balancing. As an example, capacitor C_3 is charged when S_{AU} and $S_{B'U}$ are turned on, and it is discharged

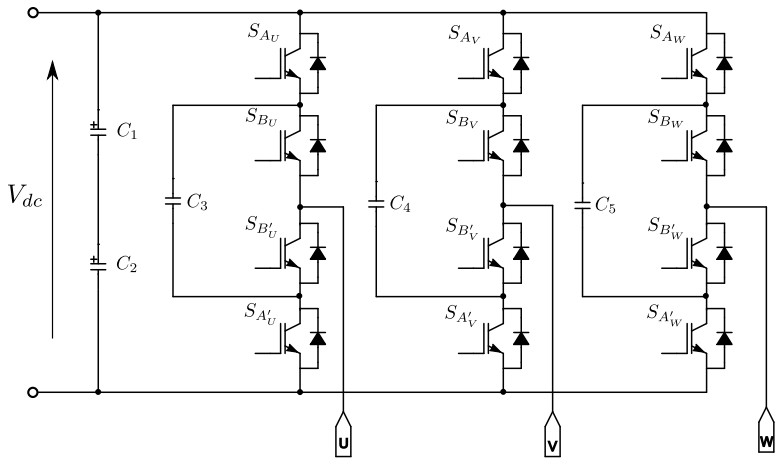

Figure 2-4: Three-level Flying Capacitor converter

V_{xN}	A	B	B'	A
$V_{dc}/2$	1	1	0	0
0	1	0	1	0
0	0	1	0	1
$-V_{dc}/2$	0	0	1	1

Table 2.2: Switching states 3-level flying capacitor converter

when S_{BU} and S'_{AU}. By proper selection of the 0-level switch combination, the charge of the capacitors can be controlled.

An advantage of this topology is that, similar to the NPC case, a single DC power supply is required. The voltage sharing between the devices is guaranteed as long as the clamping capacitors are kept charged at the right value. Unlike the NPC topology, where high voltage diodes are eventually required, no high voltage silicon devices are needed. On the other hand, the following disadvantages can be mentioned:

- Clamping capacitors need to be pre-charged at a certain voltage
- The switching strategy has to consider the need of balancing the clamping capacitors voltage, meaning that some kind of feedback mechanism has to be implemented.
- As the number of level increases, the number of capacitors required increases quickly. Similar to diode clamping, the capacitor clamping requires a large

number of bulk capacitors to clamp the voltage. Provided that the voltage rating of each capacitor is the same as that of the main power switch, a m-level converter will require a total of (m-1)x(m-2)/2 clamping capacitors per phase leg [11].

- Redundancy is difficult to implement using this topology

2.2.2.3 Cascaded H-Bridge (CHB) Converter

The CHB converter is a particular case of a cascaded converter, based on series connection of H-bridge cells. Each cell must have an isolated DC supply, which is usually obtained from an isolated AC supply and a diode bridge. Fig. 2-5 shows an individual H-bridge cell and the 5-level CHB converter.

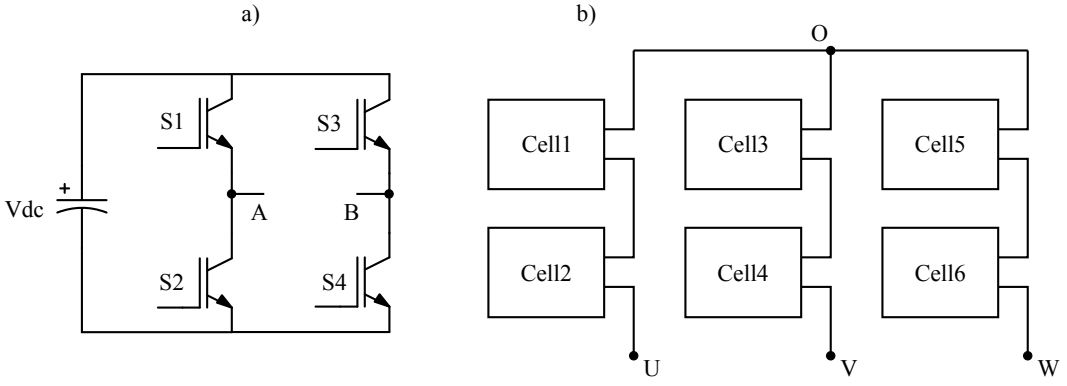

Figure 2-5: a) Individual H-Bridge cell. b) 5-level Cascaded H-Bridge converter

Each cell can produce three levels: V_{dc}, 0 and $-V_{dc}$. By series connection of N cells per phase, the output phase voltage (V_{U0}) presents 2N+1 levels and the phase-to-phase voltage (V_{UV}) is made from 4N+1 levels. In the case of Fig. 2-5, the output phase voltage can present the following voltage levels: $2V_{dc}$, V_{dc}, 0, $-V_{dc}$ and $-2V_{dc}$.

This topology provides some very attractive advantages:

- Voltage sharing between devices is automatic since there are isolated DC supplies.
- Allows redundancy by simply using more cells per phase than it is actually required

- High voltage is achieved by just connecting more cells
- The circuit is completely modular which represents an important advantage in terms of maintenance and manufacturing

Drawbacks of this technology are:

- Unlike the other topologies, each H-bridge cell needs an isolated DC supply. This leads often to some complex transformer arrangements
- The capacitors placed in each cell can be large due to the fact that each individual bridge is single-phase, and therefore with higher power ripple

It is finally noted that many other circuits respond to the name of cascaded converters, examples of these can be found in [8] [10] [11].

2.2.3 Multilevel Converter-based Applications

As it was previously mentioned, multilevel converters are considered today as a very attractive and promising solution for medium-voltage high-power applications and high output frequency converters. Several major manufacturers commercialize NPC, FC or CHB topologies with a wide variety of control methods, each one strongly depending on the application [7].

Multilevel converters can be found in controlled rectifiers, with the main purpose of avoiding the phase shift transformers in traditional multipulse rectifiers [11]. Another interesting application can be found in the field of DC-DC converters. In this way, the phase voltage of a diode-clamped or capacitor-clamped converter resembles that of a full-bridge phase-shift-modulated dc-dc converter [11]. Another important market for multilevel converters can be located in large motor drives. Particularly, the NPC converter is frequently found in high power AC motor drive applications like conveyors, pumps, fans and mills, among others [7]. In addition, the back-to-back configuration for regenerative applications has also been a major plus of this topology, used for example in regenerative conveyors for the mining industry or even

grid interfacing of renewable energy resources like wind power [7]. This configuration is mainly based on the use of a three-level active front end at the input side of a three-level NPC converter.

In the field of power systems, both NPC and cascaded multilevel converters are especially suitable for harmonic and reactive power compensation [11]. In fact, the first unified power flow controller (UPFC) in the world was based on a diode-clamped three-level inverter [15]. On the contrary, the capacitor-clamped converter cannot have balanced voltage for power conversion involving only reactive power, thus, it is not suited for reactive power compensation [11]. As it was mentioned, the cascaded multilevel converter is specially suitable for harmonic/reactive power compensation, since each H-bridge converter cell can balance its DC voltage without requiring active power and thus, without requiring additional isolated power sources.

To conclude, Fig.2-6 offers an overview summarizing different applications of multilevel converters.

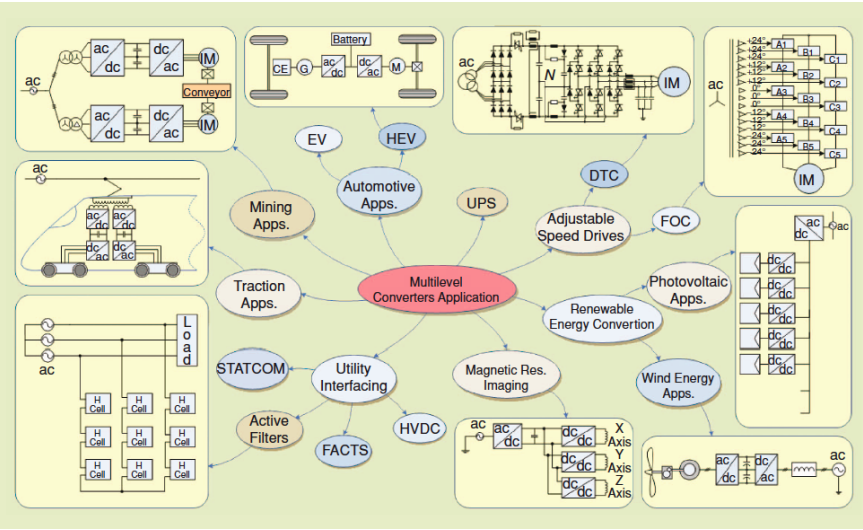

Figure 2-6: Multilevel Converter-based applications overview [7]

2.3 Modular Multilevel Converter (MMC / M2C)

The Modular Multilevel converter (MMC) was first proposed in 2003 by Marquardt and Lesnicar [16][17][18][19] and it is currently a subject of intense research. Fig.

2-7 shows the basic configuration of a three-phase MMC, based on N cells. The same circuit using voltage sources instead of capacitors had been already proposed by Alesina et al. in 1981 [20]. Each leg consists of two stacks of cells (or submodules) and two inductors (L_{arm}). The classic arrangement of the MMC uses submodules consisting of a half-bridge configuration, as shown in Fig. 2-8 (a).

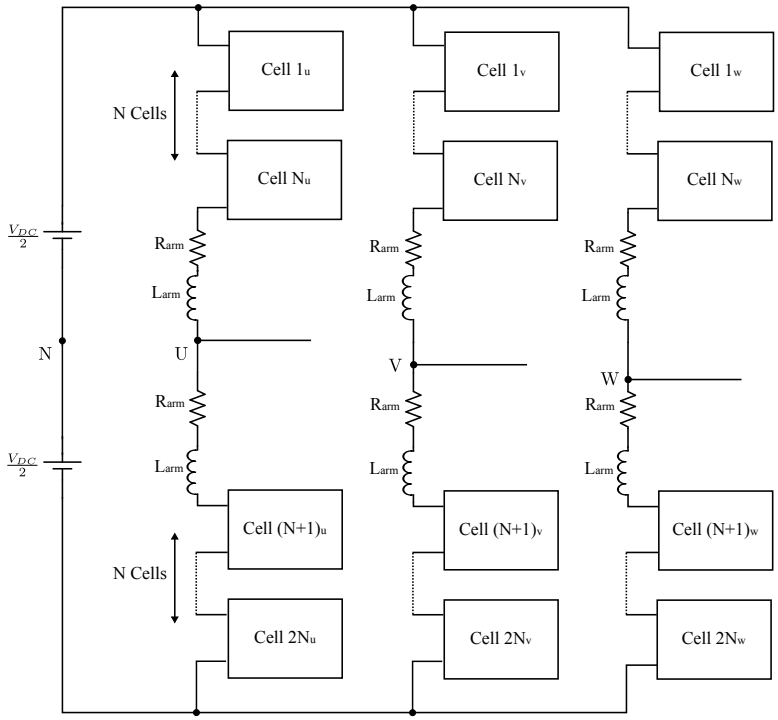

Figure 2-7: Circuit configuration of a three-phase MMC

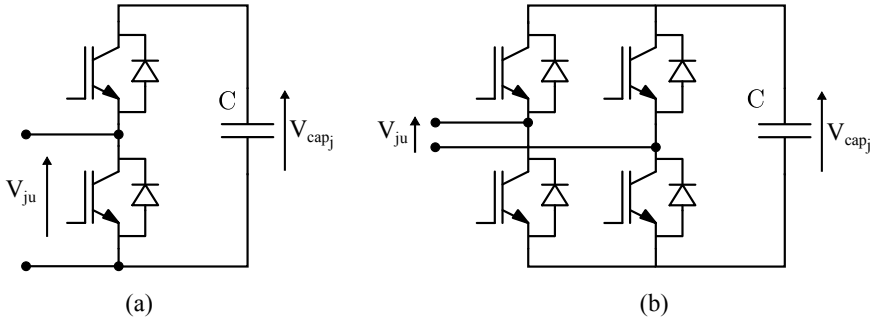

Figure 2-8: Basic circuit configuration of the submodules: (a) Half bridge (Chopper-cell). (b) Full bridge (Bridge-cell).

This converter offers several features, some of them are shared with the conventional multilevel topologies and others are quite different at first glance and may seem

strange when comparing to conventional voltage source converters [21]:

- Just one isolated DC supply is required. In other words, it is similar to a conventional converter in the sense of having a DC side and an AC side.
- Benefits of multilevel converter are automatically obtained, including low switching frequency, high quality in the output waveform, reduced voltage steps in the switches.
- Modular realization, easily scalable to different power and voltage levels [17]. This is similar to the CHB topology.
- Redundancy can be easily achieved just by using more cells than strictly needed. Faulty cells can be easily bypassed.
- The internal arm currents are not chopped, they flow continuously instead [21].
- Protection chokes (L_{arm}) are inserted into the arms. They do not disturb operation or generate overvoltage for the semiconductors since the arm currents are not chopped. Moreover, the arm inductors limit the AC-current whenever the DC-bus is short-circuited (fault condition) [21].
- The submodules are two terminal devices. There is no need to supply the DC side capacitor with energy. This is true for real power or reactive power transmission of the converter in any direction or combination [21].
- Voltage balancing of the submodules is not critical with respect to the timing of the pulses or the semiconductor switching times [21].
- Switching of cells is able to control both the DC side and the AC side unlike other converter topologies.
- Low switching losses [22].
- No bulk DC capacitor is needed. The energy is distributed along the different capacitors at each cell. This is an advantage to avoid catastrophic consequences in case of a fault condition.

On the other hand, this circuit topology presents some drawbacks:

- The number of devices required is usually higher compared to other approaches.
- As many capacitors as the number of required submodules are needed, which normally have a significant size. This is similar to the CHB topology.
- Control over the individual capacitor voltages at each cell must be carried out, which leads to important computational requirements.

It is finally mentioned that, although the term "Modular Multilevel Converter" is normally used in order to describe the topology shown in Fig. 2-7 with the cells shown in Fig. 2-8 (a), it can be considered as a member of a wider Modular Multilevel Cascade Converter (MMCC) family [23].

According to this classification, the MMCC family would consist of four main circuit configurations:

1. Single-Star Bridge-Cells (SSBC):

   It is based on single-phase full bridge cells with star connection of three clusters. This configuration has already been described as Cascade H-Bridge Converter (CHB) in Fig. 2-5.

2. Single-Delta Bridge-Cells (SDBC):

   This circuit configuration is based on single-phase full bridge cells with delta connection of three clusters. The mentioned topology is shown in Fig. 2-9.

3. Double-Star Chopper-Cells (DSCC)

   The Double-Star configuration is based either on the conventional topology presented in Fig. 2-7 with non coupled arm inductors or on the configuration shown in Fig. 2-10 with coupled arm inductors, but both using half-bridge cells as those shown in Fig. 2-8 (a).

   The reason for the name is that DSCC is based on a couple of star-connected MMCCs in which the low voltage DC sides of multiple reversible choppers are

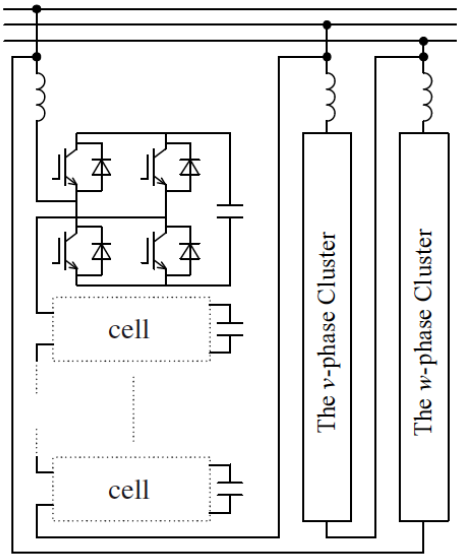

Figure 2-9: Circuit configuration of MMCC-SDBC [23].

cascaded to form each arm. It must be noticed that the use of the coupled inductors leads to a smaller size and lighter weight than the total of the two non-coupled inductors [23].

4. Double-Star Bridge-Cells (DSBC)

   This topology is based on a couple of star-connected MMCCs in which the low voltage AC sides of multiple single-phase full-bridge voltage-source converters are cascaded to constitute each arm. In addition, the DSBC configuration includes both Fig. 2-7 and Fig. 2-10 with the cells shown in Fig. 2-8 (b).

The term "Modular Multilevel Converter (MMC)" has been and will be used along this report to refer to the MMCC based on Double-Star Chopper-Cells (DSCC) with non-coupled arm inductors, according to the mentioned classification.

MMC topology has found its main application in the field of high or medium voltage power converters [24]. This is mainly due to its attractive features such as modularity and scalability, as well as the lack of a high voltage DC-link, as the stored energy is distributed among the cell capacitors. All these reasons have made the MMC a very suitable topology for HVDC applications. In fact, this topology can be

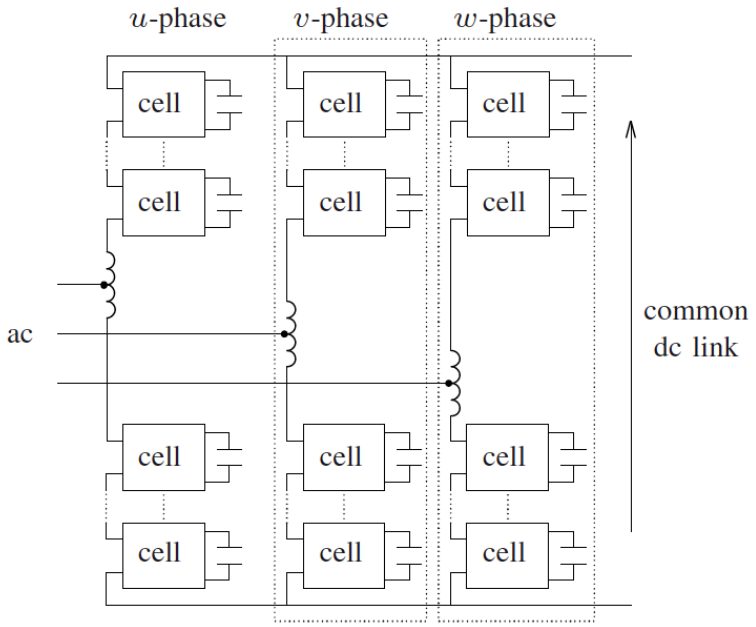

Figure 2-10: Circuit configuration of MMCC using coupled arm inductors [23].

found in practical applications under the trade name of "HVDC-PLUS", for power ratings of 400 MVA, 200 kV DC link voltage and 200 power cells [8][9].

The use of MMC for medium-voltage drives is currently receiving increased attention. The multilevel nature contributes to reduce the motor current ripple and consequently the resulting torque ripple, as well as to mitigating effects due to common-mode voltages, like ground leakage current and bearing current [25]. It must be noticed however that, as the MMC converter produces AC-voltage fluctuations in the capacitors of each cell at the output frequency [25], this topology would not be suitable for constant torque loads that require the rated torque in a low speed region, this issue being currently the focus of intensive research [26][27].

Chapter 3

Modular Multilevel Converter Fundamentals

3.1 Basic Structure and Operating Principle

The basic circuit configuration of a three-phase Modular Multilevel Converter can be seen in Fig. 3-1. Each leg (or limb) of the converter consists of two stacks of cells (or submodules), with N being the number of submodules per arm. The classic arrangement of the MMC uses two non-coupled inductors per leg (L_{arm}), with the different submodules having a half-bridge configuration, with a floating capacitor (see Fig. 2-8 (a)).

The goal of the arm inductors is twofold:

- They are necessary in order to handle the voltage difference between the top and bottom side of the converter. This feature allows them to be used for current control purposes as will be explained further on.
- They limit the current in case of a fault (short-circuit).

The basic operating principle of this kind of converter uses the differential voltage between the DC side (V_{DC}) and the overall DC component of the output voltage at the cells ($\sum V_{ju}$). This produces a circulating current (i_{Circu}), which is responsible for the

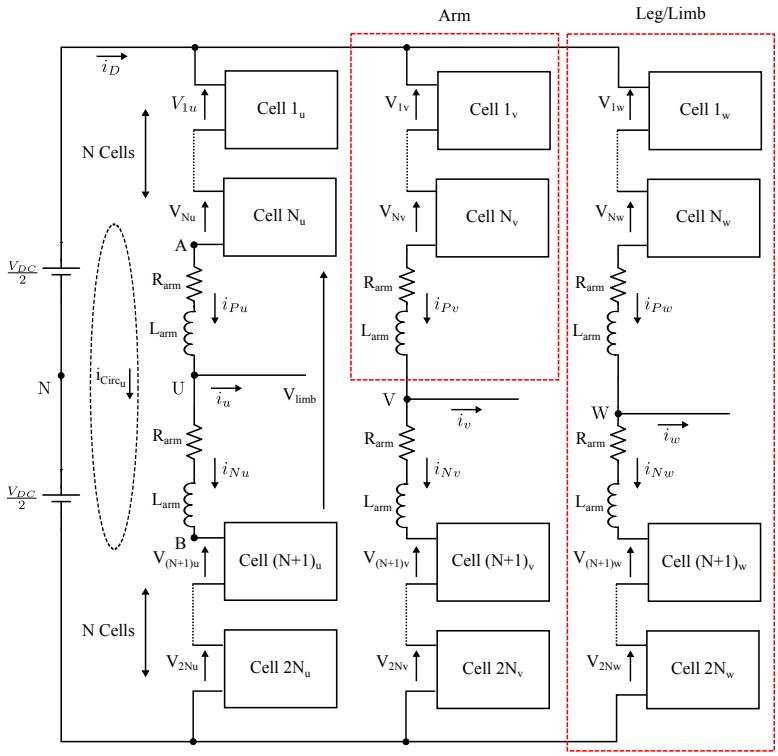

Figure 3-1: Circuit configuration of a three-phase MMC

power transfer between both sides of the converter. The differential voltage is achieved by proper control of the power devices at each cell, different control strategies could be used for this purpose. Independent of the control strategy being used, the average power transfer through each cell has to be equal to zero, which is the basic condition to maintain the average cell capacitor voltage constant. However, it is important to remark that the instantaneous power at each cell will have oscillations at frequencies typically multiple of the fundamental frequency (ω_e). Hence, these oscillations will lead to variations in the cells capacitors voltage, what is a characteristic feature of this topology.

3.1.1 Currents in the MMC

A relevant difference of the MMC with respect to conventional converter topologies, is that the arm currents (iP_u, iN_u) are not chopped, this being a relevant difference with respect to conventional converter topologies. The AC output current is split

between the upper and lower arms, each carrying half of it (3.1) (3.2). The current distribution must be guaranteed by the control strategy.

$$iP_u = i_{Circu} + \frac{i_u}{2} \tag{3.1}$$

$$iN_u = i_{Circu} - \frac{i_u}{2} \tag{3.2}$$

By adding the two previous expressions, the output AC currents are cancelled out, the circulating current is then obtained (3.3):

$$i_{Circu} = \frac{1}{2}(iP_u + iN_u) \tag{3.3}$$

This circulating current is an unique feature of this converter topology. It consists of a DC component and an AC component (3.4). The circulating current flows through the three phase legs of the converter and does not affect the AC voltages or currents.

$$i_{Circu} = \overline{i_{Circu}} + \widetilde{i_{Circu}} \tag{3.4}$$

For the case of a three-phase power converter, the DC component for each leg would be exactly one third of the current flowing from or into the DC side (i_D) (3.5). The sum of the three arm currents for phases u, v and w will cancel out the alternating components, the resulting current being therefore the continuous DC current flowing in the DC side. It should be pointed that power transfer in a balanced three-phase operation is constant.

$$\overline{i_{Circu}} = \frac{i_D}{3} \tag{3.5}$$

The alternating component of the circulating current is generated by the voltage differences naturally produced between the upper and lower cells due to the voltage oscillations in the cell capacitors. It has been reported that this component is basically at twice fundamental frequency ($2\omega_e$), being a negative sequence component [28][29].

On the contrary, in the particular case of a single-phase MMC converter, the DC side current (i_D) is not constant anymore, since it is equal to the arm current i_{Pu}, containing both the circulating current and the output AC current.

3.1.2 General Circuit Analysis

The MMC is primarily a voltage source converter, aimed to produce a certain output voltage V_{UN}. The limits for the output voltage need to be within a range of ($V_{DC}/2$ and $-V_{DC}/2$). In order to achieve this functionality, the capacitors of each submodule must be charged to $\frac{V_{DC}}{N}$. Therefore, both upper and lower arms must handle the whole DC bus voltage.

The output voltage equation (3.8) can be obtained just applying Kirchoff's voltage law to the upper and lower side of each phase leg of the converter. This equation can also be used to study the dynamic performance of the converter. It is noted that (3.6)(3.7) have been particularized for phase u, analogous equations can be used for the other two phases.

$$V_{UN} = \frac{V_{DC}}{2} - \sum_{j=1}^{N} V_{ju} - L_{arm} \cdot \frac{diP_u}{dt} - R_{arm} \cdot iP_u \tag{3.6}$$

$$V_{UN} = -\frac{V_{DC}}{2} + \sum_{j=N+1}^{2N} V_{ju} + L_{arm} \cdot \frac{diN_u}{dt} + R_{arm} \cdot iN_u \tag{3.7}$$

By adding up the above equations, substituting the arm currents by (3.1)(3.2), and considering the circulating current consisting of a DC component, the following expression can be obtained:

$$V_{UN} = \frac{1}{2}\left(\sum_{j=N+1}^{2N} V_{ju} - \sum_{j=1}^{N} V_{ju}\right) - \frac{L_{arm}}{2}\frac{di_u}{dt} - \frac{R_{arm}}{2} i_u \tag{3.8}$$

Some conclusions can be derived from (3.8):

- The output AC voltage V_{UN} depends only on the output current i_u and the difference between the arm voltages injected by the cells.

- Due to the presence of the term proportional to the arm inductance, the output voltage will not present levels with a constant value. As long as there is an AC output current, the voltage drop along the arm inductances will cause a variation in the output voltage levels.
- The term proportional to the arm inductance can be removed by using the coupled arm inductors configuration (Fig. 2-10). Discussion of this concept can be found in [24][30][31].
- For output current control tuning purposes, half the arm inductance must be added to the output filter or load inductance.

For the analysis of the circulating current, (3.9) can be used.

$$L_{arm}\frac{di_{Circu}}{dt} + R_{arm}i_{Circu} = \frac{V_{DC}}{2} - \frac{\sum_{j=N+1}^{2N} V_{ju} + \sum_{j=1}^{N} V_{ju}}{2} = \frac{V_{limb}}{2} \tag{3.9}$$

Several conclusions can be reached from the analysis of (3.9):

- It defines the voltage drop along one arm inductor due to the circulating current. This voltage drop is equal to the voltage difference between the DC bus and the sum of both upper and lower cell voltages.
- The circulating current i_{Circu} depends on the DC bus voltage and the sum of the cell voltages. Consequently, adding or subtracting the same voltage amount to/from both arms will not affect to the AC side output voltage, but it will affect to the circulating current.

Due to these reasons, it is logical to define the voltage provided by the upper (V_{up_u} (3.10)) and lower (V_{low_u} (3.11)) cells as a combination of the required DC bus voltage, the output AC voltage (V_{UN}) and the requirements for the control of the circulating current ($V_{limb}/2$).

$$V_{up_u} = \sum_{j=1}^{N} V_{ju} = \frac{V_{DC}}{2} - V_{UN} + \frac{V_{limb}}{2} \tag{3.10}$$

$$V_{low_u} = \sum_{j=N+1}^{2N} V_{ju} = \frac{V_{DC}}{2} + V_{UN} + \frac{V_{limb}}{2} \tag{3.11}$$

3.2 Modulation Strategies

After a thorough review of the existing literature, it was concluded that there is no clear, widely accepted, classification of the different modulation strategies for the Modular Multilevel Converter. Hence, a classification will be proposed in this master thesis.

Two main modulation strategies can be used to generate the output voltage V_{UN}, depending on the voltage applied to the limb inductors:

- Zero Voltage Applied to the Limb Inductors
- Voltage Applied to the Limb Inductors

They are discussed following.

3.2.1 Zero Voltage Applied to the Limb Inductors

In this strategy, the upper and lower cells generate the same voltage (V_{AN} and V_{BN}), the voltage applied to the limb inductors being therefore equal to zero. It must bear in mind that the half-bridge cells can provide two different states: V_{DC}/N or 0. Hence, the number of levels which can be obtained in the output voltage V_{UN} having N cells per arm, is $(N + 1)$.

To provide a better comprehension on how the output voltage levels are generated, Table 3.1 shows the combinations for the case of 2 submodules per arm (N=2). S_{jT} stands for the state (ON=1, OFF=0) of the top device in Fig. 2-8 (a), the bottom switch being in the complementary state.

It can be noticed that this approach leads to a constant number of cells inserted at any instant of time, which is equal to N. In order to provide the levels $V_{DC}/2$ and $-V_{DC}/2$, only one switching state is possible. On the other hand, to generate the 0V level, 4 different switching states can be used. These redundant states can

Submodules	Output Voltage (V_{UN})					
	$V_{DC}/2$	$-V_{DC}/2$	0V			
S_{1T}	0	1	0	1	0	1
S_{2T}	0	1	1	0	1	0
S_{3T}	1	0	1	0	0	1
S_{4T}	1	0	0	1	1	0
Inserted cells (N)	2	2	2	2	2	2

Table 3.1: Switching combinations for a 3-level MMC (N=2) based on zero limb inductor voltage approach.

be used in order to balance the capacitor voltages, depending on the direction of the arm currents. This issue will be discussed later.

With this modulation approach, it is not possible to control the circulating current, since the voltage applied along the limb inductors is unavoidable equal to zero. This restricts the control strategies that can be used.

Two main approaches can be defined to generate the switching states:

1. The first approach is similar to that used in traditional multilevel converters. The reference voltage, which is equal to the desired output voltage (V_{UN}), is compared to level shifted (in-phase disposition) triangular carriers, to obtain the gate commands. There are N carriers distributed along the output voltage limits ($V_{DC}/2$, $-V_{DC}/2$). Each carrier will be responsible for the gating signal of two complementary cells. An illustration of this approach can be seen in Fig. 3-2 for the case of 4 submodules per arm (5 levels) and 800V DC bus voltage.

   This method do not allow to control the DC bus voltage using a feedforward term (see (3.10)(3.11)), since the only reference which is being used is the output voltage. Examples of this method can be found in [33][34].

2. The second approach uses 2N triangular carriers, level shifted in-phase disposition. Unlike the first option, the reference voltage is either the upper cells voltage or the lower cells voltage (3.12)(3.13).

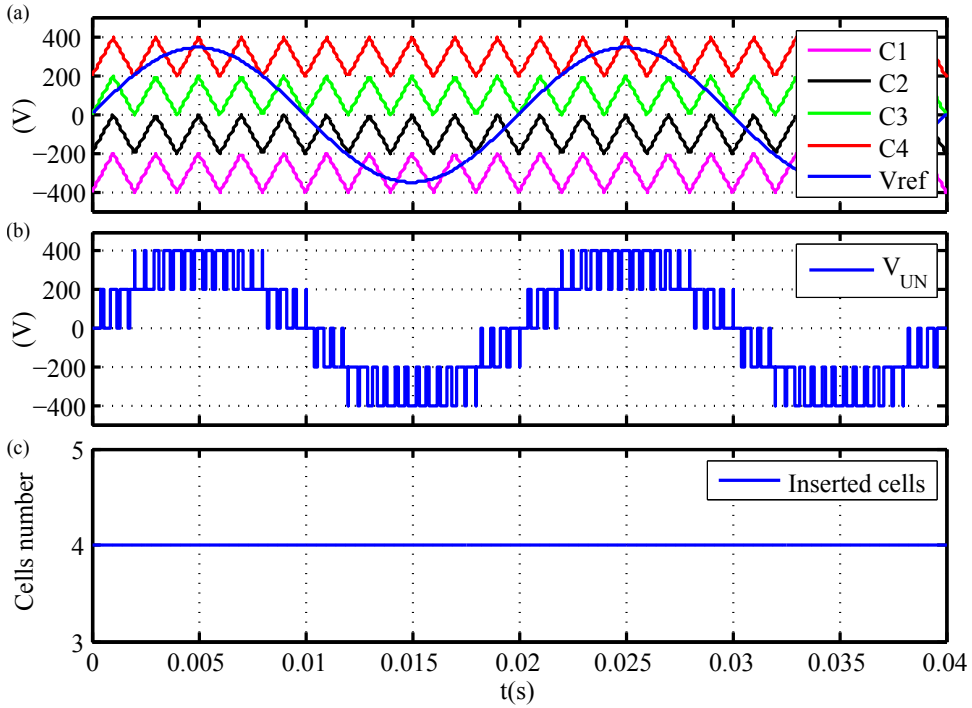

Figure 3-2: (a) Output voltage reference and level-shifted triangular carriers. (b) 5-level output voltage. (c) Inserted cells.

$$V_{up_u} = \sum_{j=1}^{N} V_{ju} = \frac{V_{DC}}{2} - V_{UN} \tag{3.12}$$

$$V_{low_u} = \sum_{j=N+1}^{2N} V_{ju} = \frac{V_{DC}}{2} + V_{UN} \tag{3.13}$$

One of the two voltage references is compared with the N triangular carriers in order to obtain the gate signals for the cells in one half of the converter, and the same reference is compared to N triangular carriers 180 degrees phase-shifted just to obtain the complementary states for the other half cells. This is necessary to generate the same voltages in both sides and, eventually, to apply zero voltage to the limb inductors. Note that in this case, there is a feedforward term to generate the DC bus voltage and the term for the output voltage reference. Fig. 3-3 illustrates this concept, the output voltage and the number of cells inserted being the same as for the previous case.

Tables 3.2 and 3.3 show the available switching states for the case of 4 submodules

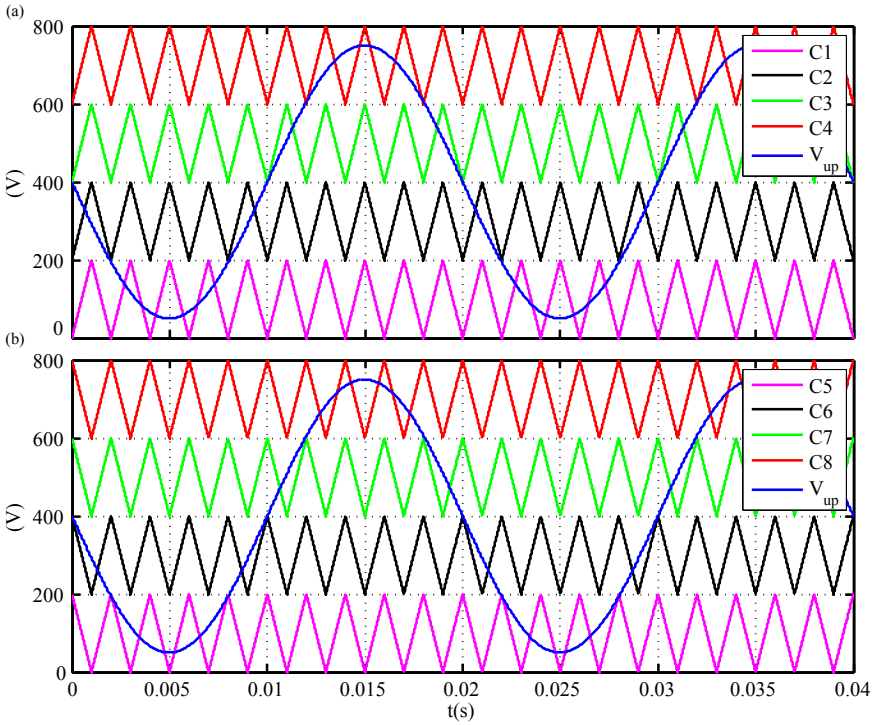

Figure 3-3: (a) Upper voltage cells reference and level-shifted triangular carriers. (b) Upper voltage cells reference and complementary level-shifted triangular carriers.

per arm (5-level MMC). It is observed that only one state provides the limit voltage levels $V_{DC}/2$ and $-V_{DC}/2$. On the other hand, there are 16 combinations to obtain the levels $V_{DC}/4$ and $-V_{DC}/4$ and 36 combinations to get the 0V level. Similar to the previous case, these redundant states can be used for capacitor voltage balancing purposes.

3.2.2 Voltage Applied to the Limb Inductors

With this strategy, and unlike the previous one, upper and lower cells can now have different voltage levels, V_{AN} and V_{BN}, in order to generate a differential voltage across the limb inductors. This leads to a higher number of levels in the output voltage, which now is equal to $2N+1$. On the other hand, the number of inserted cells is not constant anymore, and can be equal to $N+1$, N or $N-1$.

With this approach, the voltage references (3.10)(3.11) can be used, and the circulating current can be consequently controlled. However, due to the presence of a

Submodules	Output Voltage (V_{UN})																																					
	$V_{DC}/2$	$-V_{DC}/2$	$V_{DC}/4$																$-V_{DC}/4$																			
S_{1T}	0	1	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	1	1	1	1				
S_{2T}	0	1	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	1	1	1	1	1	1	1	1	0	0	0	0	1	1	1	1				
S_{3T}	0	1	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0				
S_{4T}	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1				
S_{5T}	1	0	1	1	1	1	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0				
S_{6T}	1	0	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0				
S_{7T}	1	0	1	1	1	1	1	1	1	0	0	0	0	1	1	1	1	1	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0				
S_{8T}	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1				
Inserted cells (N)	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4				

Table 3.2: Switching combinations for a 5-level MMC (N=4) based on zero limb inductor voltage approach. Part 1/2

Submodules	Output Voltage (V_{UN})																																		
	0 V																																		
S_{1T}	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
S_{2T}	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
S_{3T}	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
S_{4T}	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
S_{5T}	1	0	0	1	1	0	1	0	0	1	1	0	1	0	0	1	1	0	1	0	0	1	1	0	1	0	0	1	1	0	1	0	0	1	1	0
S_{6T}	1	1	0	0	0	1	1	1	0	0	0	1	1	1	0	0	0	1	1	1	0	0	0	1	1	1	0	0	0	1	1	1	0	0	0	1
S_{7T}	0	1	1	0	1	0	0	1	1	0	1	0	0	1	1	0	1	0	0	1	1	0	1	0	0	1	1	0	1	0	0	1	1	0	1	0
S_{8T}	0	0	1	1	0	1	0	0	1	1	0	1	0	0	1	1	0	1	0	0	1	1	0	1	0	0	1	1	0	1	0	0	1	1	0	1
Inserted cells (N)	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4

Table 3.3: Switching combinations for a 5-level MMC (N=4) based on zero limb inductor voltage approach. Part 2/2

differential voltage in the arm inductors, a significant ripple exists in the circulating current, which might require higher values for the arm inductance.

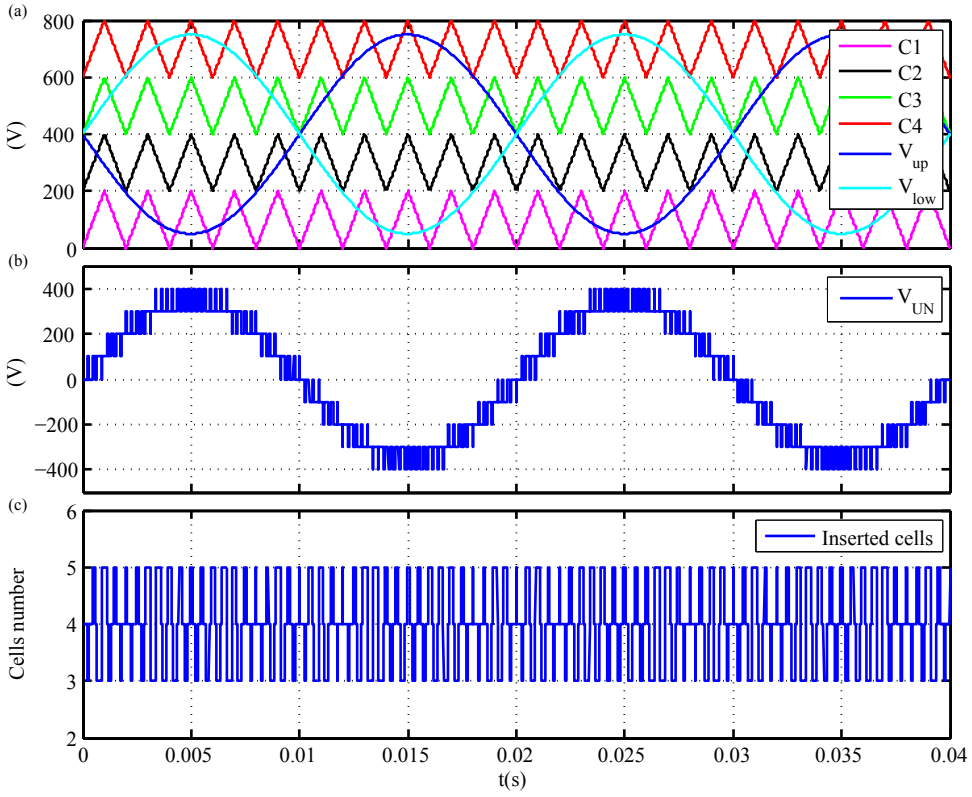

Figure 3-4: (a) Output voltage reference for upper and lower cells, and level-shifted triangular carriers. (b) 9-level output voltage. (c) Inserted cells.

Table 3.4 shows the different voltage combinations for the case of 2 submodules per arm (N=2). It can be easily noticed how the extra levels are obtained by combining different voltage levels in V_{AN} and V_{BN}. The first three rows correspond to the previous approach where no voltage was applied across the limb inductors. The same concept can be extended to the 4 submodules case.

In order to generate the different switching states, N triangular carriers level shifted in-phase disposition are needed. In this case, the references for the upper and lower cells are (3.10)(3.11). Both voltage references share the same carriers. Due to this, the number of inserted cells is not constant anymore, as previously discussed.

Fig. 3-4 shows the voltage references and the carriers, the output voltage and the number of inserted cells at each time. It can be easily noticed how the number of

V_{AN}	V_{BN}	V_{UN}
$V_{DC}/2$	$V_{DC}/2$	$V_{DC}/2$
0	0	0
$-V_{DC}/2$	$-V_{DC}/2$	$-V_{DC}/2$
$V_{DC}/2$	0	$V_{DC}/4$
$V_{DC}/2$	$-V_{DC}/2$	0
0	$V_{DC}/2$	$V_{DC}/4$
0	$-V_{DC}/2$	$-V_{DC}/4$
$-V_{DC}/2$	$V_{DC}/2$	0
$-V_{DC}/2$	0	$-V_{DC}/4$

Table 3.4: Output voltage levels (V_{UN}) generation in a 5-level MMC (N=2) based on voltage difference across the limb inductors.

levels in the output voltage is now equal to $2N + 1 = 9$ levels.

Another way of obtaining the switching states for the case of voltage applied to the limb inductors, can be found in [24][30]. This method is based on individual voltage references for each cell and phase-shifted carriers.

3.2.3 Proposed Hybrid Modulation Approach

In this subsection, a new modulation strategy is proposed, which is somehow based on the combination of the two methods described previously.

The strategy described in 3.2.2 inherently applies voltage to the limb inductors, as the number of cells inserted is not constant. Even if the term $V_{limb}/2$ in (3.10)(3.11) is set to zero, an alternating voltage is still applied to the arm inductors. The basic concept for this new method deals with a strategy that just applies voltage to the limb inductors when needed and in a smoother manner. As it can be observed in Fig. 3-4 (c), the voltage applied to the limb inductors is always oscillating between three values, resulting in considerable current ripple in the arm currents. If the way of applying that voltage was different, the current ripple could be reduced and smaller arm inductors would be needed.

The scheme showing the basic operation of this modulation strategy can be seen

in Fig. 3-5.

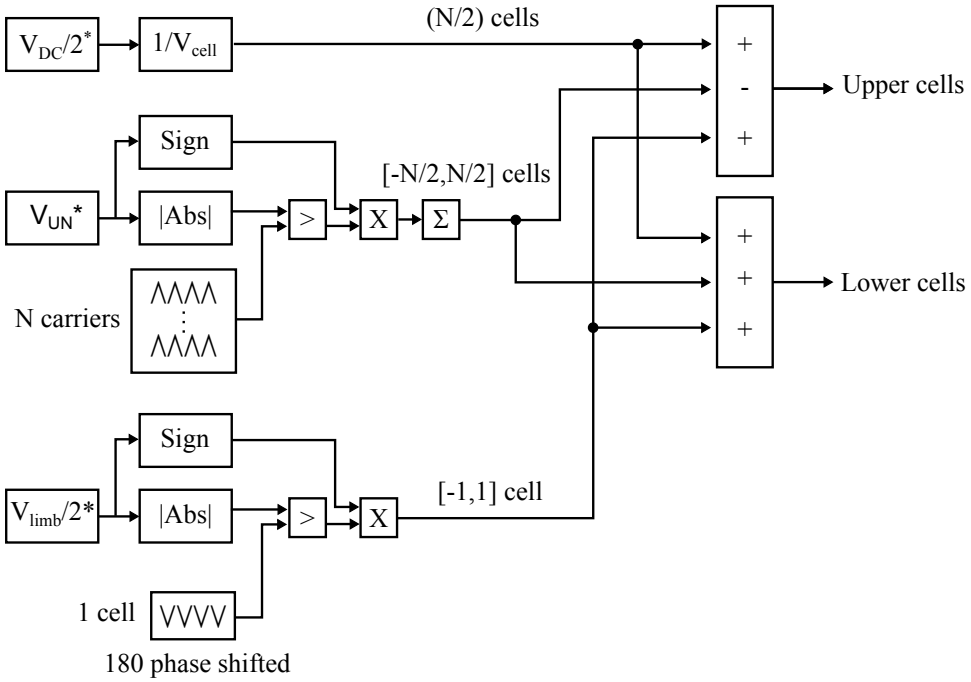

Figure 3-5: Hybrid modulation block diagram.

The proposed method is based on obtaining the required cells for each voltage term in (3.10)(3.11), individually. The different stages are explained as follows:

- First of all, the term corresponding to the DC bus voltage is divided between the cell voltage in order to obtain the fixed number of cells that generate that voltage.

- The term dealing with the output voltage reference ($V_{UN}{}^*$) can vary between $V_{DC}/2$ and $-V_{DC}/2$. As a consequence, it can not be compared to the carriers, which cover the range between 0 and V_{DC}. To solve this, the absolute value of the reference voltage [0, $V_{DC}/2$] is now compared to the carriers, being just half of them used. After this, the gate signals are multiplied by the sign of the reference voltage in order to obtain the real number of cells needed. The final number of cells will oscillate between $-N/2$ and $N/2$. It must be remarked that this number of cells is going to be added to the fixed number of cells obtained in the previous stage. Consequently, the final number of required cells will vary

between 0 and N, being always a positive value.

- The key point of this method is the generation of the limb voltage reference ($V_{limb}/2^*$). This reference can be positive or negative and it is then compared to one carrier (one cell) by using the same procedure as above. The mentioned carrier is 180 degrees phase shifted so that the generated pulses are added to the ones of the previous stage, just at the instants of time when they are not at high level value. This means that not extra cells are needed, being the number of required cells always inside the range [0, N]. Fig. 3-6 illustrates this explanation. It can be easily noticed how the pulses related to the limb voltage reference are added at the instants of time when the other pulses are at a low level condition.

  The main limitation of this method deals with values of the output voltage reference close to saturation, which will lead to very short instants of time when adding pulses is possible. This fact must be bear in mind when using this approach.

- Finally, the number of cells required for the upper and lower side of the converter is performed based on (3.10)(3.11).

When the limb voltage reference is set to zero (no circulating current control capability), the inserted number of cells is a constant number like in method 3.2.1. In this way, it is possible to generate the output voltage without inherently applying voltage to the limb inductors, unlike approach 3.2.2. As long as there is limb voltage reference, the number of inserted cells will vary between [N and N+2] or [N-2 and N] depending on positive or negative references. The reason of this variation is due to the fact that the required cells for the limb voltage are simultaneously added to both upper and lower side of the converter.

The main difference between this method and the one explained in 3.2.2 can be found in the variation on the number of inserted cells, which in the end is the voltage applied to the limb inductors. Fig. 3-7 illustrates this.

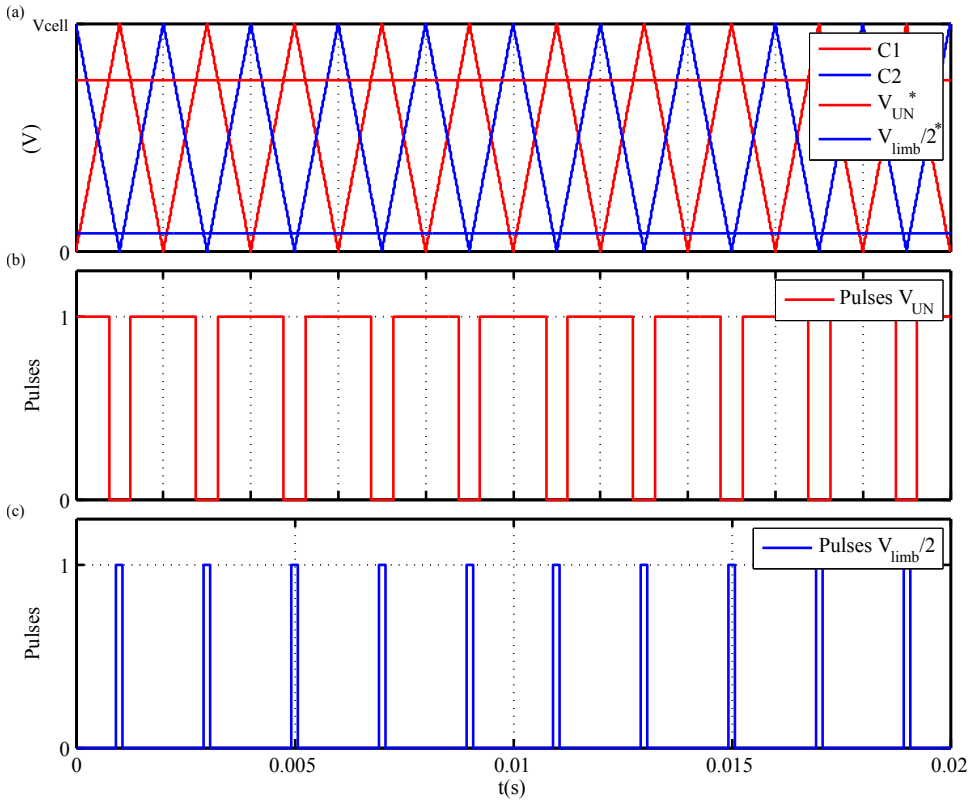

Figure 3-6: (a) Comparison between output voltage and limb voltage references and their related carriers. (b) Pulses related to the output voltage reference. (c) Pulses related to the limb voltage reference.

As it can be observed, the previous approach (Fig. 3-7(a)) applies three different voltage levels to get a certain limb voltage. This is inherent to that modulation strategy. On the other hand, the proposed method applies two levels to get a certain limb voltage but remaining more time at zero voltage ($N = 4$). This difference finally leads to a reduction in the current ripple present in the circulating current, which can be translated into the use of smaller arm inductors. However, the output voltage for this new method is based on N+1 levels, being lower than method 3.2.2.

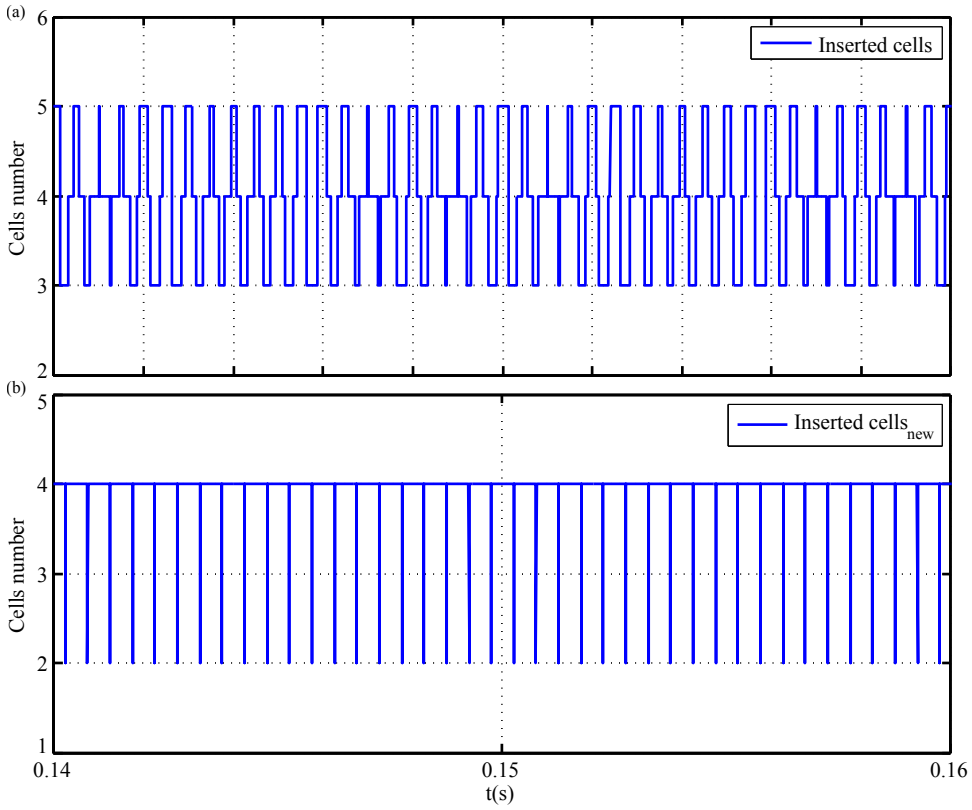

Figure 3-7: 4 submodules per arm (N=4). (a) Inserted cells by method 3.2.2. (b) Inserted cells by method 3.2.3.

Chapter 4

Control of Modular Multilevel Converter

4.1 Control Objectives

The basic operating principle of the Modular Multilevel Converter requires a differential voltage between the DC side (V_{DC}) and the overall DC component of the output voltage at the cells ($\sum V_{ju}$). This produces a circulating current (i_{Circu}), which is responsible for the power transfer between both sides of the converter. This differential voltage is achieved by proper control of the power devices at each cell, different control strategies could be used for this purpose. Independent of the control strategy being used, the average power transfer through each cell has to be equal to zero, which is the basic condition to maintain the average cell capacitor voltage constant.

The control of this kind of converter has to accomplish multiple objectives, they are as listed below. Since not all of them must be fulfilled simultaneously, different control strategies can be used.

- *Output Active and Reactive Power Control*

  The output power control for the MMC is similar to a conventional voltage-source converter. The output voltage reference is trimmed to guarantee the actual output active and reactive powers track the corresponding references.

- *DC Bus Voltage Control*

  In a conventional voltage source converter the DC bus voltage is controlled by means of the active power. In the MMC, the DC bus voltage can be ideally set in a direct manner by means of the feedforward term ($V_{DC}/2$) in (3.10)(3.11).

- *Circulating Current Control*

  The average power transfer throughout each submodule must be equal to zero, which means that the average power in the DC side must be equal to the average power in the AC side (output power). The control of the power on the DC side is carried out by means of the DC term in the circulating current (see (3.4)), which is actually responsible for the power transfer between both sides of the converter. This current can be controlled by means of the differential voltage applied to the limb inductors (V_{limb}).

- *Overall Submodules Capacitor Voltage Control*

  The average submodules capacitor voltage is controlled by regulating the overall energy stored in all capacitors. This is related to the AC component of the circulating current.

- *Submodules Capacitor Voltage Balancing*

  The submodules capacitor voltages must be adequately balanced, i.e. their oscillations must remain within acceptable limits. This is done by proper selection of the cells that have to be inserted at each time.

4.2 Control Strategies Overview

Similar as for the modulation strategies and though some work has been done in this field [35], there is not a widely accepted classification of the control strategies for the MMC. A general classification of the existing control strategies has been developed as a part of this master thesis, as presented following.

4.2.1 Open-loop Approaches

The term "open-loop" refers to the fact that there is not closed-loop control of inner converter variables. Two different approaches have been proposed.

- *Output Power Control + Capacitor Voltage Balancing*

  In this strategy, the desired output voltage as well as the balancing of the submodules capacitor voltages are generated by means of a certain algorithm. There is no control of the circulating current, so its behavior is completely free in principle. This fact allows the use of modulation strategies based on zero voltage application along the limb inductors.

  Under these conditions, the AC term of the circulating current is high and uncontrolled. This leads to a higher value of the RMS arm current and consequently, more losses on the limb inductors. Additionally, the oscillation in the capacitor voltages is also high as the circulating current is left uncontrolled. The use of this method implies the use of advanced algorithms for the capacitor voltage balancing, due to the fact that there is no control over the total stored energy. Examples of this methodology can be found in [28][32][33][34].

- *Estimation of Stored Energy [35][36]*

  This approach was proposed in [36] . In this case, the total energy stored in the capacitors is fully controlled through the control of the circulating current. This method has been included in the "open-loop classification" because the capacitor voltages are not measured but they are estimated from other quantities. The circulating current is not controlled by a closed-loop control, but there is a direct action over the differential voltage applied to the limb inductors.

4.2.2 Closed-loop Approaches

This concept includes some closed-loop control of inner variables of the converter, such as the circulating current, the total average capacitor voltage, etc. Multiple combinations of the control objectives previously listed can be done.

- *Stored Energy Control [28]*

  In this strategy, the total energy stored in the converter is controlled by measuring the capacitor voltages. The balance among the different arms is done by adding a sinusoidal component to the circulating current, which is controlled by the voltage applied to the limb inductors.

- *Phase-Shifted-Carrier-based Control [24][30]*

  This method is focused on closed-loop control of the total average voltage, the circulating current and the individual capacitor voltages. It applies individual voltage references for each submodule and it is based on phase-shifted carriers modulation strategy.

- *General Closed-Loop Approach*

  This term refers to a generic method, based on the fulfillment of all the control objectives listed in the previous section. Some comments can be made about it.

  The overall capacitor voltage control can be mainly carried out by two alternatives:

  - It can be controlled by means of an extra DC component and an AC component added to the circulating current reference.
  - It can be regulated by varying the output active power reference. If the total average voltage is bigger than the reference, more power is demanded from the output, and vice versa. As a consequence, an oscillation is driven to the output power reference and hence, a third harmonic component ($3 \cdot \omega_e$) occurs in the output current.

  The AC component of the circulating current can be controlled or it can be minimized or even suppressed. Some authors have published methods where it is suppressed [32][37] or minimized [28], but there is not a clear reason for doing that when the converter is being operated under a closed-loop control strategy.

On the other hand, there is the possibility of suppressing the AC component of the circulating current when applying the first approach mentioned in the open-loop strategies. This would eventually result in the minimization of the oscillations in the capacitor voltages. A deeper analysis on the individual control loops for this approach, will be performed in the following section.

4.3 Converter Design and Control Strategy

4.3.1 System Overview

One of the objectives of this master thesis is the design of a 3kW, single-phase, Modular Multilevel Converter, to operate connected to the grid. A further requirement is to define and implement a control strategy aimed to reduce the values of limb inductors and cell capacitors as much as possible. To achieve this, the control approach will be based on the proposed modulation method (3.2.3).

Fig. 4-1 schematically shows the converter and the auxiliary elements needed. The details of the converter are provided in Appendix A.

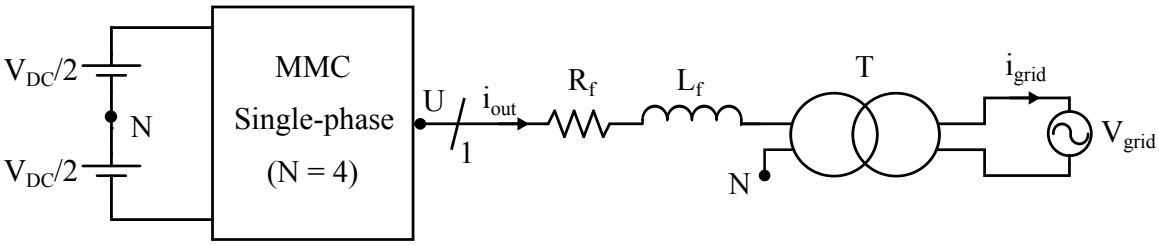

Figure 4-1: MMC Overall System scheme.

The control strategy has been designed to fulfill the control objectives listed previously and it is intended to be used with modulation approaches related to applying voltage across the limb inductors (3.2.2 and 3.2.3). Therefore, the references for the upper and lower cells are given by (4.1)(4.2).

$$V_{up}{}^{*} = \sum_{j=1}^{N} V_{ju} = \frac{V_{DC}{}^{*}}{2} - V_{UN}{}^{*} + \frac{V_{limb}{}^{*}}{2} \tag{4.1}$$

$$V_{low}{}^{*} = \sum_{j=N+1}^{2N} V_{ju} = \frac{V_{DC}{}^{*}}{2} + V_{UN}{}^{*} + \frac{V_{limb}{}^{*}}{2} \tag{4.2}$$

4.3.2 AC side: Active Power Control Loop

The control of the output active and reactive power is achieved by controlling the output AC current (i_{out}). Fig. 4-2 shows the corresponding block diagram, including the current control loop.

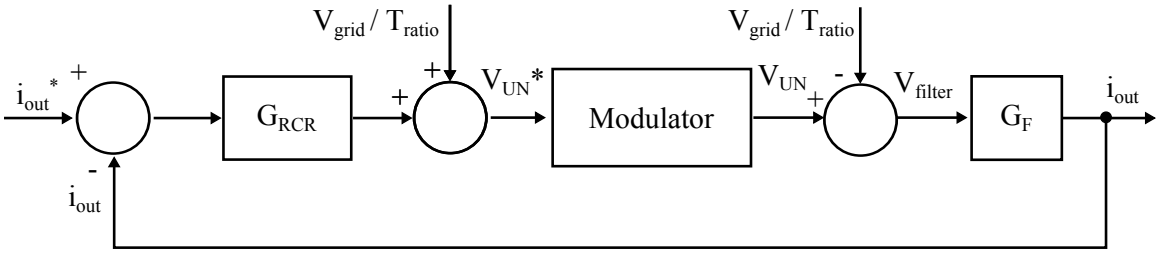

Figure 4-2: Output Current Control Loop Block Diagram.

Due to the fact that the system is single-phase, the conventional Park transformation cannot be performed and the reference ($i_{out}{}^{*}$) is not a DC quantity. A typical synchronous PI regulator would provide zero state error for the case of DC quantities, but in this case the reference must be an AC waveform. To handle this, a resonant PI current regulator (G_{RCR}) will be used, as it has the capability of perfectly tracking AC commands pulsating at ω_e. Its transfer function is given by (4.3).

$$G_{RCR} = 2K_{p_{out}} \cdot \left(\frac{s^2 + (1/T_{i_{out}})s + \omega_e^2}{s^2 + \omega_e^2}\right) \tag{4.3}$$

The feedforward term of the grid voltage (V_{grid}/T_{ratio}) has been added at the output of the regulator, to improve the dynamic response, with T_{ratio} being the turns ratio of the transformer. The resulting AC output voltage reference ($V_{UN}{}^{*}$) is then replaced in (4.1)(4.2), the resulting references being the input to the modulator.

To tune the current regulator, the output filter parameters (R_f and L_f), the leakage inductance of the transformer primary winding (L_{T1}) and half the arm inductance ($L_{arm}/2$) (see (3.8)) are considered as the plant of the system (G_F), as shown in

Fig. 4-2. Pole-zero cancellation was used for a bandwidth of 300 Hz. The regulator parameters are listed in Table 4.1.

Parameter	Value
$K_{p_{out}}$	$2\pi \cdot 300 \cdot (L_f + L_{T1} + L_{arm}/2)$
$T_{i_{out}}$	$(L_f + L_{T1} + L_{arm}/2)/(2R_f)$
ω_e	$2\pi 50$

Table 4.1: Output Current Regulator Parameters.

The magnitude of the output current reference ($i_{out}{}^*$), is obtained from the desired output active power ($P_{ACrms}{}^*$) using (4.4). The grid angle (θ_e) obtention is schematically shown in Fig. 4-3.

$$\hat{i_{out}}{}^* = \frac{2P_{ACrms}{}^*}{\hat{V_{grid}}} T_{ratio} \tag{4.4}$$

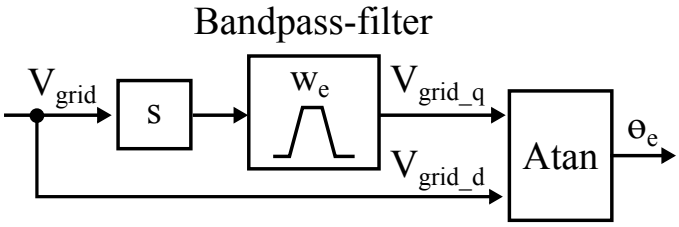

Figure 4-3: Grid angle obtention.

The derivative of the grid voltage is used to obtain a 90 degrees phase-shifted waveform, which can be considered as the q-axis component. The grid angle (θ_e) is performed as the arctangent of the q and d (which is directly the grid voltage) components. By controlling the phase-shift of the injected current with respect to the grid voltage, the reactive power can be also controlled. In a practical implementation, it must be considered that the derivative calculation can be problematic due to noise in the signal, requiring some kind of filtering.

Finally, Fig.4-4 shows the simulated waveforms of the command and actual current as well as the output voltage, with the converter operating at rated active power, the reactive power being equal to zero.

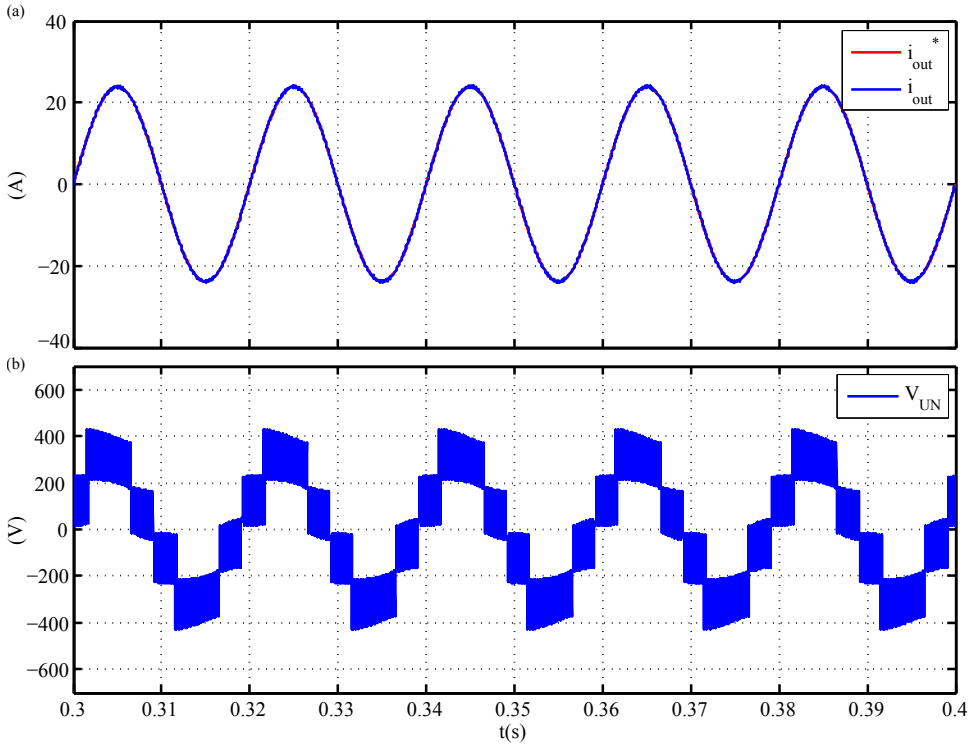

Figure 4-4: (a) Output current reference and output current measurement. (b) Output voltage.

4.3.3 DC Bus Voltage Control

In the MMC, the DC bus voltage can be ideally set adding a feedforward term ($V_{DC}/2^*$) to the upper and lower cells references (4.1)(4.2), no feedback loop being required in this case.

It is noted however that in the converter designed in this thesis, the DC bus is fixed by a DC power supply, as shown in Fig. 4-1.

4.3.4 Circulating Current Control Loop

As the circulating current is a fictitious variable, it cannot be directly measured, but estimated from the measurements of the upper and lower arm currents (3.3).

The control of the circulating current is performed through the voltage applied along the arm inductance (V_{limb}). If the same voltage is applied to both arms in (4.1)(4.2), the AC quantities will not be affected, ($V_{limb}{}^*$) being consequently the voltage applied along the limb inductances. Fig. 4-5 illustrates this concept.

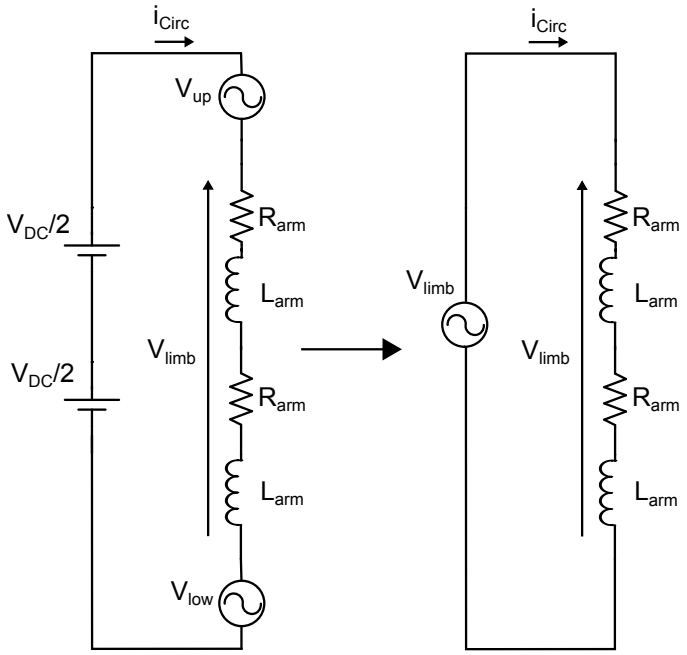

Figure 4-5: MMC one phase circuit simplification for control purposes.

According to Fig.4-5, the system to be controlled can be simplified to be the limb inductance transfer function (4.5). Fig. 4-6 shows the corresponding block diagram, including the whole circulating current control loop.

$$G_{limb} = \frac{1}{(2L_{arm})s + 2R_{arm}} \tag{4.5}$$

The reference for the DC term of the circulating current is obtained from the output active power reference, as indicated in (4.6).

$$\overline{i_{Circ}{}^{*}} = \frac{P_{ACrms}{}^{*}}{V_{DC}} \tag{4.6}$$

By doing this, the power from the DC side is forced to be equal to the power demanded from the AC side. An additional term ($i_{volt}{}^{*}$) is needed to account for the losses in the output filter and limb inductors, as well as to keep a constant average voltage in all capacitors. This term consists of both DC and AC components, and is obtained from another control loop. The AC component ($2\omega_e$)represents the AC term of the circulating current, which is related to the oscillation in the capacitor voltages. On the other hand, the DC term represents the additional active power needed to

compensate for the losses, and to keep a constant average voltage in the capacitors. Simulation in Fig. 4-7 shows both additional commands for the circulating current.

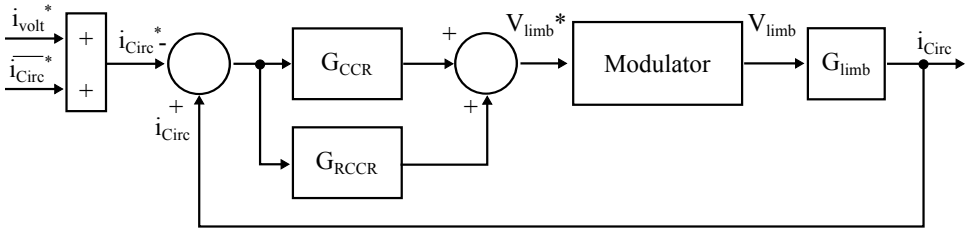

Figure 4-6: Circulating Current Control Loop Block Diagram.

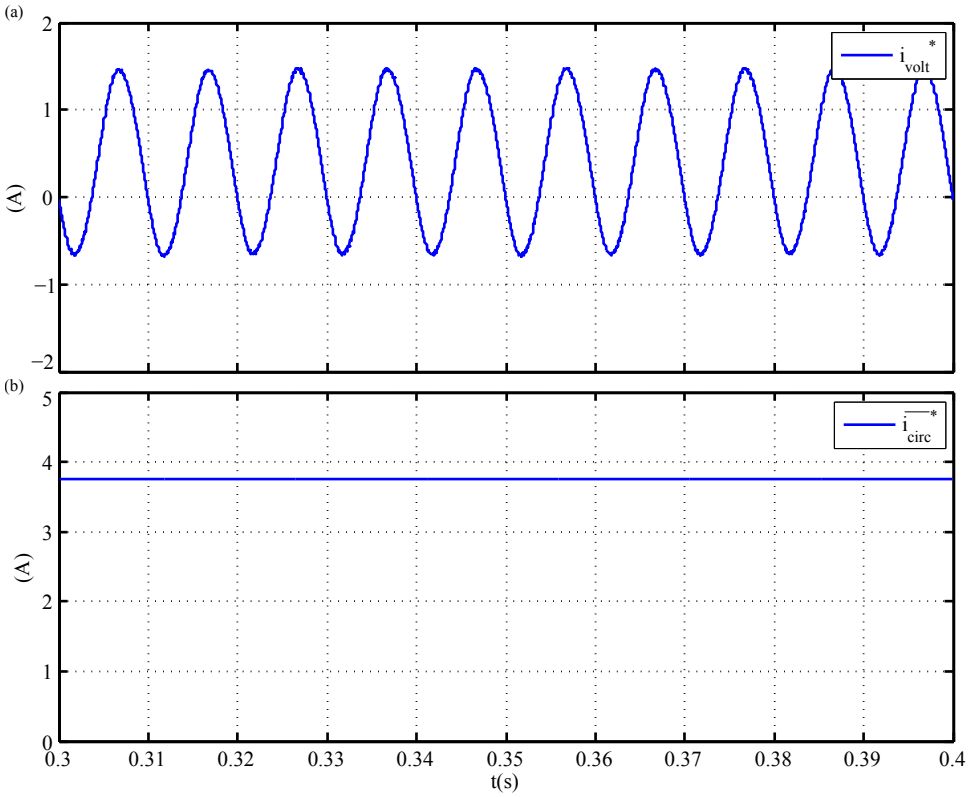

Figure 4-7: (a) Additional term of the circulating current coming from Overall Stored Energy control loop. (b) Feedforward term (DC term) of the circulating current reference.

Both references ($i_{volt}{}^*$ and $\overline{i_{Circ}{}^*}$) are added up to obtain the overall circulating current reference ($i_{Circ}{}^*$). In order to regulate both the AC and DC components present in the circulating current reference, the proposed control loop is based on two current regulators operating in parallel: a conventional PI regulator (G_{CCR}), responsible of controlling the DC component, and a resonant PI regulator (G_{RCCR})

responsible of controlling the AC component pulsating at $2\omega_e$. The mathematical expressions for both regulators are shown in (4.7)(4.8).

$$G_{CCR} = K_{pCCR}\frac{s + 1/T_{iCCR}}{s} \tag{4.7}$$

$$G_{RCCR} = 2K_{pRCCR} \cdot (\frac{s^2 + (1/T_{iRCCR})s + \omega_{e}^{2}_{RCCR}}{s^2 + \omega_{e}^{2}_{RCCR}}) \tag{4.8}$$

The controllers have been tuned using pole-zero cancellation, for a bandwidth of 300 Hz. The resonant PI current regulator is tuned to provide zero steady state error at 100 Hz ($2\omega_e$). Parameters for both regulators are listed in Table 4.2:

Parameter	Value
K_{pCCR}	$2\pi\cdot\ 300\cdot\ (2L_{arm})$
T_{iCCR}	$(2L_{arm})/(2R_{arm})$
K_{pRCCR}	$2\pi\cdot\ 300\cdot\ (2L_{arm})$
T_{iRCCR}	$(2L_{arm})/(2\cdot 2R_{arm})$
ω_{eRCCR}	$2\pi 100$

Table 4.2: Circulating Current Regulators Parameters.

Combining these two regulators in parallel, the overall transfer function (4.9) is obtained, the closed-loop frequency response function being shown in Fig.4-8. It is observed from this figure that 0 dB magnitude and 0 deg angle (i.e. zero error) is obtained at 0Hz and 100Hz.

$$\frac{i_{Circ}}{{i_{Circ}}^*} = \frac{(G_{CCR} + G_{RCCR})G_{limb}}{1 + (G_{CCR} + G_{RCCR})G_{limb}} \tag{4.9}$$

Fig. 4-9 shows the simulated waveforms of the total commanded and measured circulating current. It can be noticed that the measured current contains a significant current ripple, due to the low value of the arm inductance. Increasing the value of the arm inductances, that ripple would be reduced significantly. However, it must be bear in mind that one of the objectives of this thesis deals with the minimization of

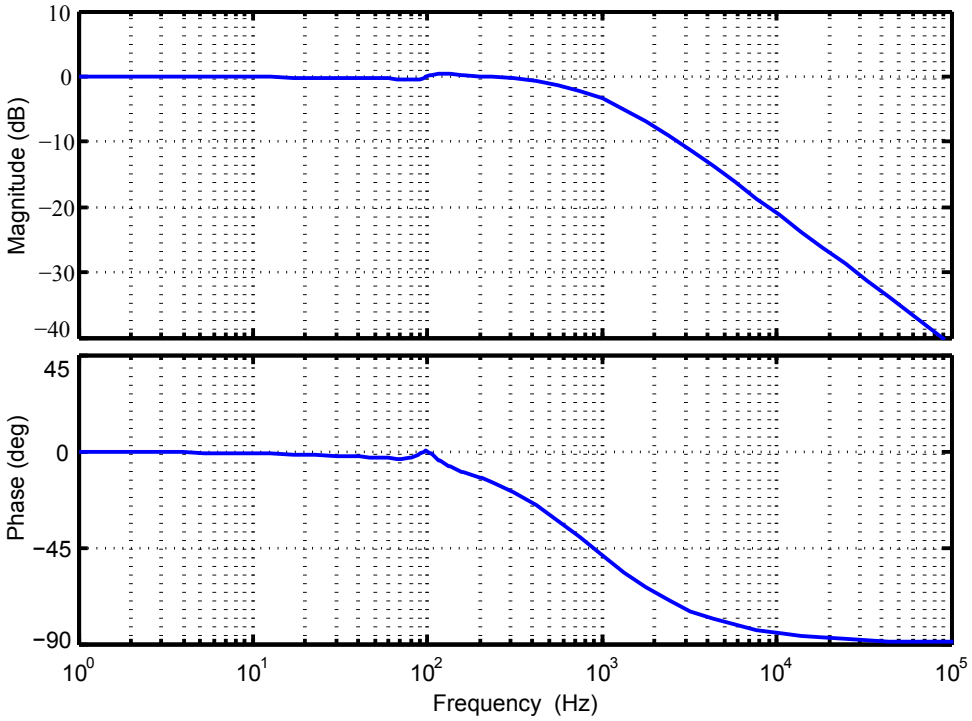

Figure 4-8: Frequency response function of the system with two PI current regulators in parallel.

the arm inductors. In order to provide further insight on the behavior of the control strategy, the low frequency region of the FFT of both the reference and the measured current, have been also included. It can be observed that both coincide at 0 and 100 Hz, meaning that the two regulators operating in parallel are able to perfectly track the DC and the 100 Hz components of the circulating current reference.

A different control strategy would be suppressing the AC component of the circulating current [32]. By taking advantage of the proposed control scheme, there is no much problem in suppressing the AC component as indicated in Fig. 4-10.

Simulation results about the AC circulating current suppression can be observed in Fig. 4-11. A quick look at the FFTs demonstrates how the 100 Hz component is completely removed from the circulating current.

To conclude, Fig. 4-12 has been included in order to show the arm currents and their composition. It can be observed how both arm currents are composed by the DC term and the 100 Hz components of the circulating current, and half the amplitude of the output current (50Hz component). This situation perfectly verifies expressions

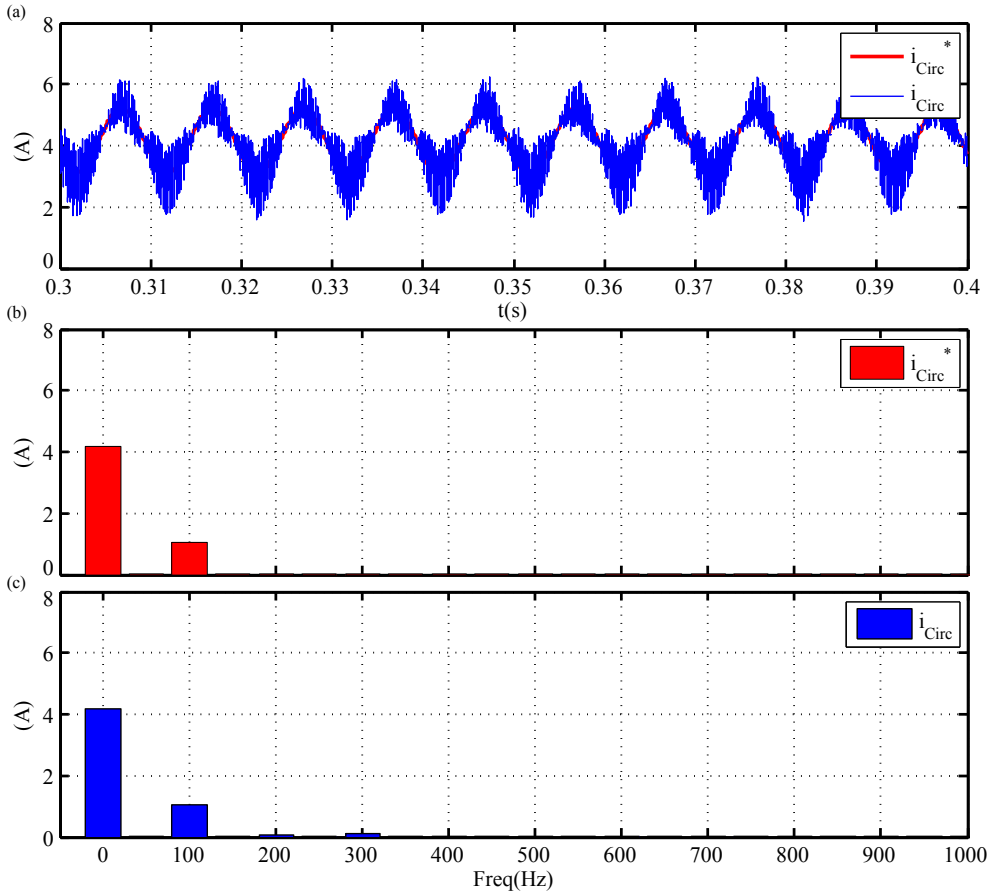

Figure 4-9: (a) Commanded and measured circulating current. (b) FFT of the commanded circulating current. (c) FFT of the measured circulating current.

(3.1)(3.2).

4.3.5 Overall Stored Energy Control Loop

In the control loop described in the previous section, the term $i_{volt}{}^{*}$ was obtained to control the total voltage of the submodule capacitors in a leg. This is necessary to keep a constant average voltage in each capacitor and compensate for the losses. Fig. 4-13 schematically shows the block diagram for this control loop, the reference being the target voltage for the sum of all capacitors in a leg (4.10).

$$Sum_{Vcap} = \sum_{j=1}^{2N} V_{capj} \tag{4.10}$$

To tune the PI regulator (G_{VR}), some simplifications have been introduced. The

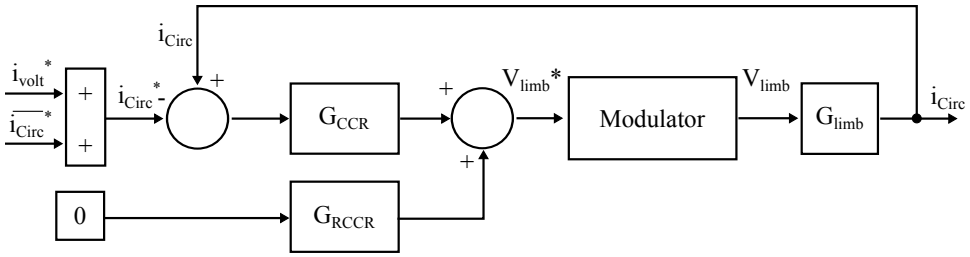

Figure 4-10: Circulating Current Control Loop Block Diagram.Suppression of the AC component.

plant to be controlled includes N capacitors connected at each time. However, for the modulation strategy being used, the number of cells connected at each time varies. The regulator has been tuned to achieve a bandwidth of 25 Hz and a maximum overshoot of 4%. The parameters are listed in Table 4.3.

$$G_{VR} = K_{pVR}\frac{s + 1/T_{iVR}}{s} \tag{4.11}$$

Parameter	Value
K_{pVR}	$2\pi \cdot 25 \cdot (C_{cell}/N)$
T_{iVR}	1/81

Table 4.3: Overall Stored Energy Regulator Parameters.

Finally, Fig.4-14 shows the simulated waveforms of the total voltage reference and the sum of all the capacitor voltages, the correctness of the control strategy being readily observed from the figure.

4.3.6 Submodules Capacitor Voltage Balancing

To complete the control strategy, in addition to the overall average voltage of the submodule capacitors, the individual capacitor voltages must be also balanced. This is schematically shown in Fig. 4-15.

Once the references for the upper and lower cell voltages (4.1)(4.2) are obtained, the modulation strategy calculates the number of required cells for each side of the

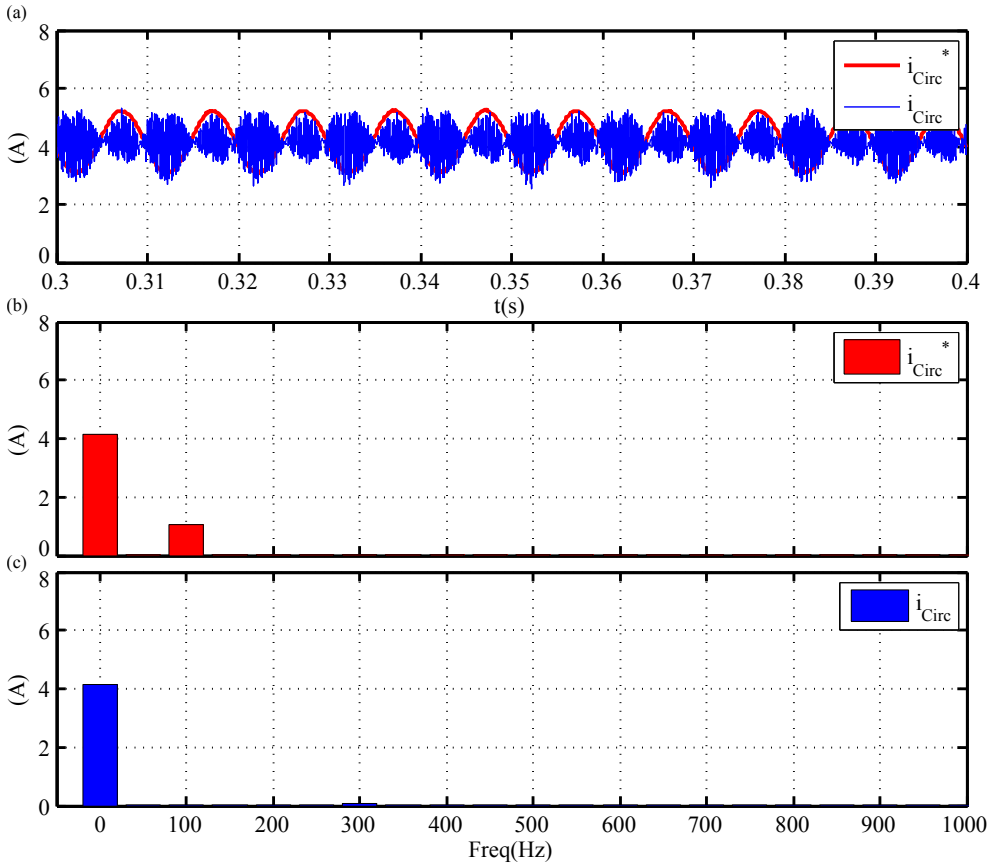

Figure 4-11: 100 Hz Suppression method. (a) Commanded and measured circulating current. (b) FFT of the commanded circulating current. (c) FFT of the measured circulating current.

converter (n_{up} and n_{low}), but not actual cells that must be inserted or removed. To do this, the balancing algorithm sorts the capacitor voltages. Then, depending on the direction of the arm currents (i_P in the upper side, and i_N in the lower side), the cells to be inserted are selected as follows:

- If the arm current is positive, the cells with the lowest capacitor voltages are inserted. By doing this, the incoming arm current charges the cell capacitor.

- If the arm current is negative, the cells with the highest capacitor voltages are inserted. By doing this, the outgoing arm current discharges the cell capacitor.

Finally, the output of the algorithms described, are translated into the respective gate signals for each submodule. Fig. 4-16 shows the simulated waveforms of all the

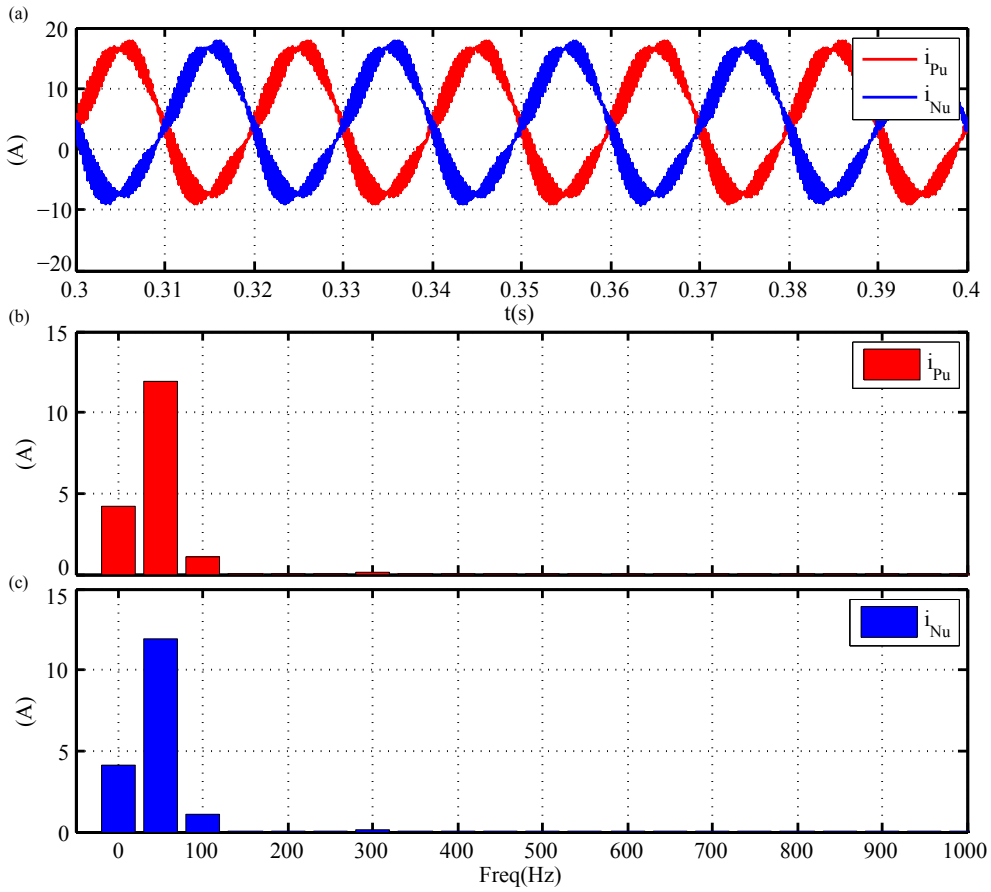

Figure 4-12: (a) Upper and lower arm currents. (b) Upper arm current FFT. (c) Lower arm current FFT.

submodules capacitor voltages. It can be observed how the average value is kept at the desired voltage. The amplitude of the oscillation can be reduced by increasing the cell capacitor. It is noted however that for this work, keeping the capacitor as small as possible was a design objective.

4.3.7 Converter Start-up

The start-up of the MMC is not a trivial issue. First, the cell capacitors must be initially charged at V_{DC}/N. When the converter is initially connected to the DC-side, a charging resistor must be inserted in order to limit the inrush current; consequently, the capacitors are charged at $V_{DC}/(2N)$. To boost the voltage to the desired value, the method first proposed in [17] can be used. In this method, the DC side is connected to a power supply with a voltage of V_{DC}/N. The different cells are individually

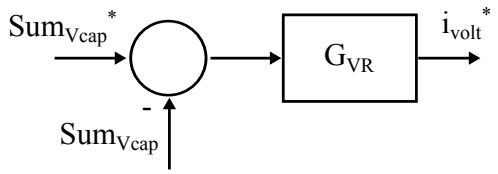

Figure 4-13: Overall Stored Energy Control Loop Block Diagram.

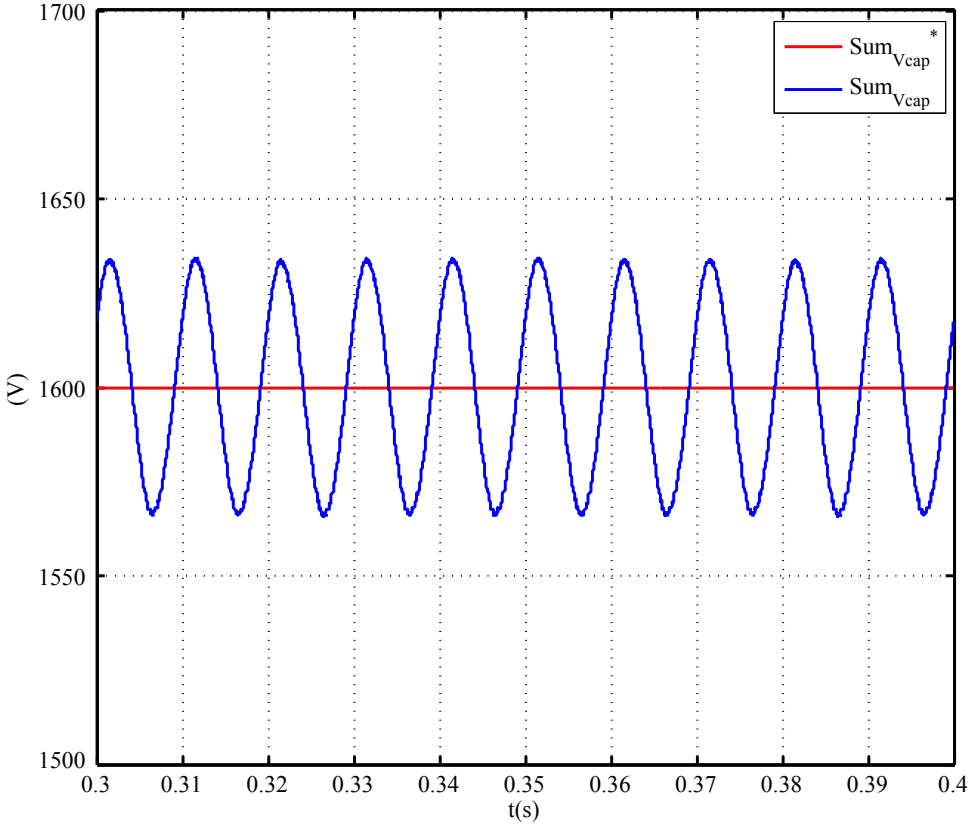

Figure 4-14: Reference and measured capacitor voltage for all the submodules.

inserted (keeping the remaining cells out) so that their capacitors are charged to the mentioned value. Though conceptually simple, this method is not very practical from the user point of view. In fact, authors do not offer much information about its implementation. A different approach is proposed in this thesis.

The proposed modulation strategy is based on inserting N cells at each time, when the circulating current control is disabled, what happens in the initial stage. By doing this, the inserted cells will be charged to V_{DC}/N, but with the balancing algorithm working in order to balance all the capacitor voltages. In this initial stage, all the control loops are disabled, with the exception of the output power control

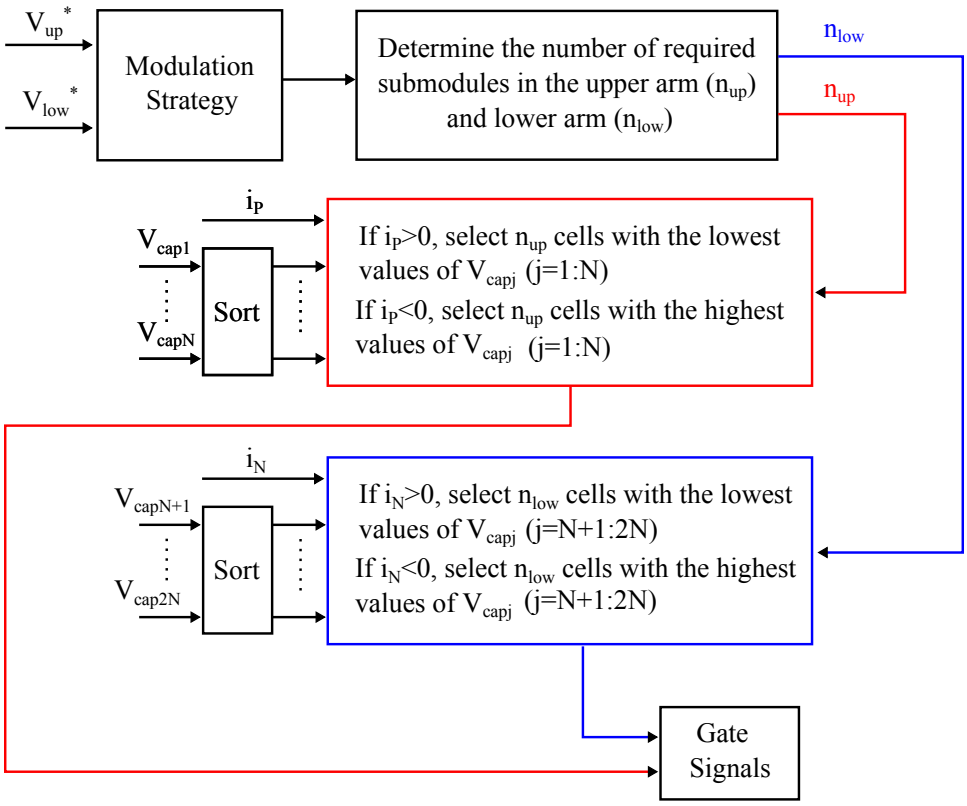

Figure 4-15: Block Diagram including submodule capacitor voltage balancing approach.

loop, whose reference is set to zero. The feedforward term makes possible that the converter generates an output voltage and as a consequence, the balancing algorithm can work properly. It must be bear in mind that the balancing algorithm does not change the state of the submodules if there is no change in the number of inserted cells, so providing a certain output voltage is therefore necessary.

4.4 Modulation Strategies Comparison Results

This section offers a comparison between the proposed modulation strategy (3.2.3) used so far in this chapter, and the "conventional" approach described in (3.2.2). Fig. 4-17 shows the circulating current in both cases, for the same parameters and operating conditions.

It can be noticed that the use of a low value for the arm inductance with the

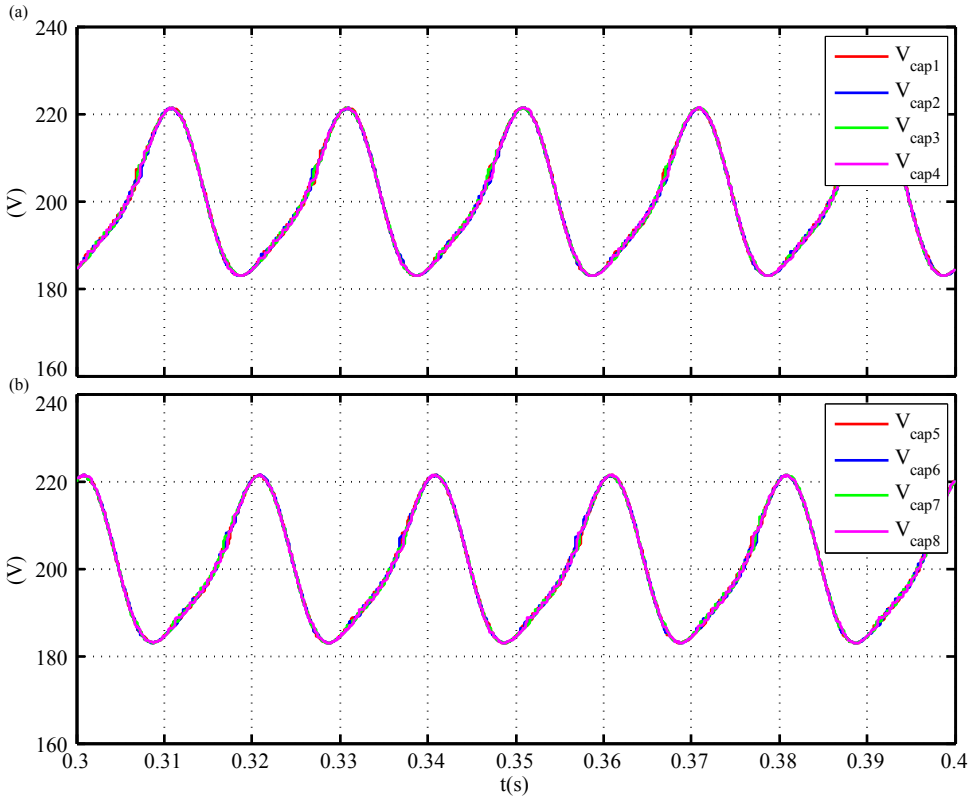

Figure 4-16: (a) Upper side capacitor voltages. (b) Lower side capacitor voltages.

"conventional" modulation approach results in a large ripple in the circulating current. On the contrary, the ripple is substantially reduced using the proposed method, eventually allowing a significant reduction of the size and cost of the arm inductances.

Fig. 4-18 shows the output voltage for both modulation approaches.

It can be observed that the proposed method produced $(N + 1 = 5)$ levels in the output voltage waveform. On the contrary, the "conventional" approach produces $(2N + 1 = 9)$. It is noted in this regard that the output voltage shown in the figure only consists of 7 levels, due to the fact the output voltage reference is not high enough to need all the possible levels with the arrangement used.

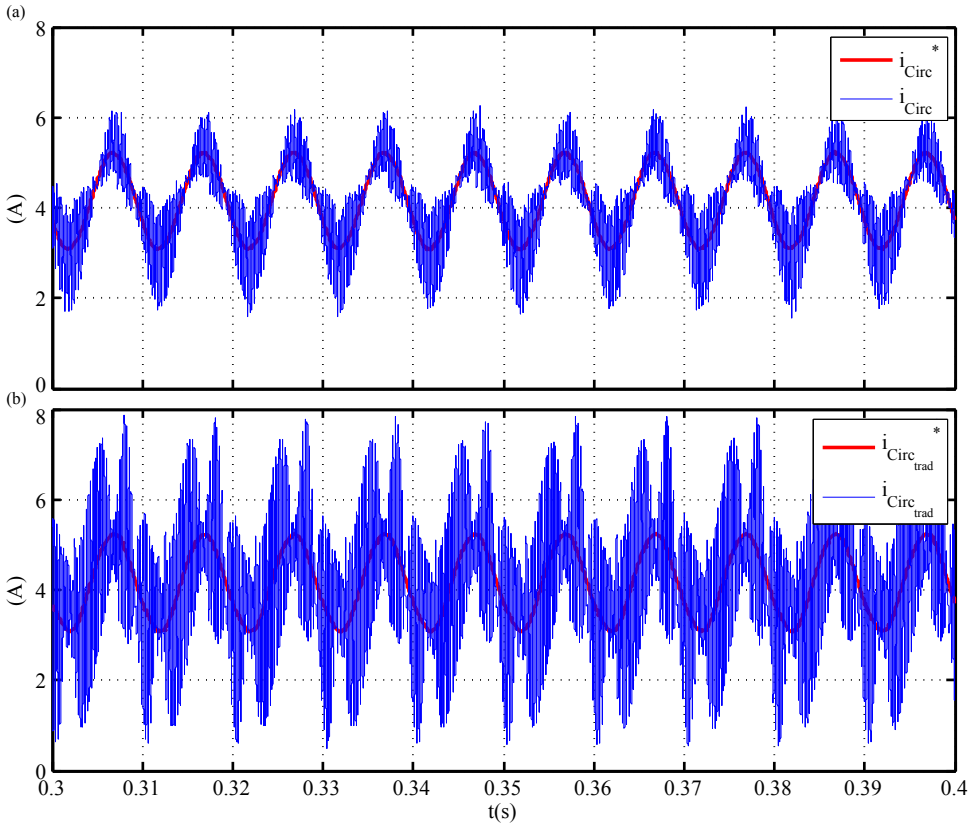

Figure 4-17: (a) Circulating current reference and circulating current indirect measurement. Proposed modulation strategy (3.2.3). (b) Circulating current reference and circulating current indirect measurement. Modulation strategy explained in 3.2.2.

4.5 Arm Inductance and Submodule Capacitance Results

The use of the modulation strategy proposed in this work, has allowed the use of lower values for the arm inductance. The cell capacitance has also been decreased in comparison to the values used in most of publications on this topic. To illustrate this, Table 4.4 shows typical values for the arm inductance and cell capacitance provided in the existing literature. The value within brackets represents the per unit value, which is the adequate metric to compare the different cases.

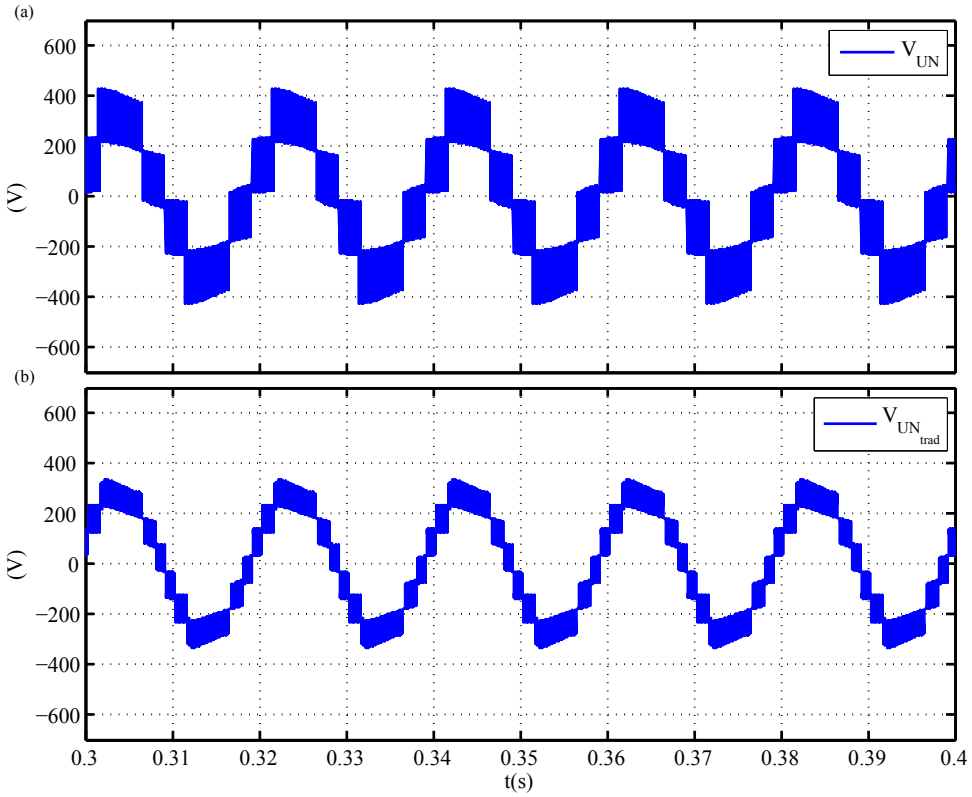

Figure 4-18: (a) Output voltage under proposed modulation strategy. (b) Output voltage using the modulation strategy described in 3.2.2.

Arm inductance (H)	Cell Capacitance (F)	Reference
$1e^{-3}$ (1.78%)	$800e^{-6}$	This thesis
$34e^{-3}$ (12.3%)	$5e^{-3}$	[38]
$3e^{-3}$ (8.57%)	$5e^{-3}$	[28]
$1e^{-3}$ (3.2%)	$3e^{-3}$	[24]
$3.1e^{-3}$ (3.5%)	$3.3e^{-3}$	[35]
$4e^{-3}$ (9.5%)	$13e^{-3}$	[32]
$1e^{-3}$ (8%)	$3.3e^{-3}$	[30]

Table 4.4: Arm inductances and cell capacitances survey.

Chapter 5

Conclusions and Future Developments

5.1 Conclusions

The needs in the current and future electrical grid has been presented in this work. Derived from these needs, the multilevel converters, and particularly the MMC topology, have been introduced. Its main features, structure and operating principles have been deeply discussed.

Analyzing the operation of the MMC, different modulation strategies have been described and assessed, primarily based on the voltage applied across the limb inductors. Furthermore, a new modulation strategy has been proposed aiming to reduce the current ripple in the circulating current, by changing the manner in which the available voltage is applied to the arm inductances. Thanks to this, the arm inductance can be reduced, leading to a decrease in its cost and size.

The different control objectives for the MMC have been presented and analyzed. A classification of the control strategies has been also presented, including closed-loop and open-loop approaches. A control strategy has been designed, paying special attention to the circulating current control; alternatives for the control and/or the suppression of the AC component of the circulating current have been discussed.

The design for a 3 kW single-phase MMC grid-connected has been performed,

using actual values for the different elements. The designed control strategy has been verified by means of simulation results. The proposed modulation strategy has been compared with other methods in order to demonstrate a reduction in the circulating current ripple. As a conclusion of this study, the value of the arm inductance can significantly be reduced, compared to the methods proposed in the literature. Furthermore, the cell capacitance has also been designed to be as lower as possible. To conclude, a strategy for the start-up of the converter has been proposed.

5.2 Future Developments

The future work derived from this master thesis concerns the construction of a real 3 kW MMC prototype, based on the designed parameters and aiming to perform a real implementation of the designed modulation and control strategies. Other future developments that can be derived from the work developed along this master thesis, are listed below:

- Deep study and analysis about the operating limits of the proposed modulation strategy.
- Deeper and precise study of the impact of the proposed modulation strategy on the individual devices switching frequency.
- Improve the submodules capacitor voltage balancing algorithm. Imbalance between the upper and lower arm voltages have not been taken into account.
- Real implementation of the control and modulation strategies based either on FPGA+DSP or on a real-time platform.

5.3 Quality Report

My only improvement suggestion deals with the master thesis timeframe. The master regulations recommend a six months timeframe for external master thesis, which is

totally impossible. Second semester subjects take place in February. So the actual timeframe available to stay in an external institution is from March to July, i.e. four months, as the master thesis must be submitted by the 15th of July.

In my opinion, it would be very interesting to explore the possibility of having the month of February available in case of an internship in an external institution.

Chapter 6

External Master Thesis

All the work developed along this master thesis was carried out within the PEMC group in the University of Nottingham.

Appendix A

Single-Phase MMC Parameters

Parameter	Value
Rated Power (P_{ACrms})	3kW
Grid voltage (V_{grid})	230 V
DC Bus (V_{DC})	800 V
Submodules per arm (N)	4
Cell voltage	200V
Switching frequency	4kHz
Arm inductance (L_{arm})	1 mH (1.78%)
Arm resistance (R_{arm})	0.1Ω
Cell capacitance (C_{cell})	$800\mu F$
Output filter inductance (L_f)	8.4 mH (15%)
Output filter resistance (R_f)	1Ω
Transformer turns ratio (T_{ratio})	1.3
Transformer primary winding leakage inductance (L_{T1})	10.71 mH

Table A.1: Single-Phase MMC Parameters.

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