# Grid Synchronization of Three-Phase Converters Using Cascaded Complex Vector Filter PLL

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***Abstract*—Synchronization is a key issue in distributed power generation and storage (*DPGS*), fast and accurate estimation of the grid voltage phase angle being requested. Synchronization methods can be roughly divided among a) zero-crossing-methods, b) Phase-Locked-Loop (*PLL*) and c) Frequency-Locked-Loop (*FLL*) methods, with PLL implemented in a synchronous reference frame (*SRF-PLL*) likely being the most popular choice. A drawback of these methods is that, in general, they do not implement harmonic rejection strategies, their performance in polluted networks being therefore compromised; also their implementation and tuning is not straight forward, often being made by trial and error.**

**This paper proposes a pre-filtering based synchronization method using cascaded complex-coefficient-filters (*CCCF*) and a complex *PLL*. The *CCCF* allows selection of the harmonic isolated/rejected, while the *CPLL* obtains the phase of the positive sequence component of the fundamental voltage needed for synchronization. The proposed method provides high rejection/adaptation capabilities against unbalances, frequency drift and harmonic distortion of the line voltages.**

***Index Terms* — Grid synchronization, complex *PLL*, complex coefficients filters, harmonic rejection.**[1]

## I. Introduction

Due to the growing interest in renewable energy resources, the traditional generation paradigms have changed [1]. New generation systems include large centralized power plants that coexist with small distributed and decentralized generation spots, located as close as possible to the consumers [1], thus reducing the transmission losses as well as the size and number of power lines needed, the resulting distributed system being referred as distributed power generation (*DPG*) [2]. To deal with *DPG* and distributed power storage (*DPS*) issues, the concept of microgrid was introduced in [3]. While this new concept can potentially increase the efficiency, bring economic improvements and emissions reduction [4, 5], new concerns arise related to power quality communication, dynamic behavior, stability, control, protection and secure operation, [6].

Operation of a microgrid requires knowledge of the magnitude and phase of the positive sequence component of the fundamental voltage, which is needed for grid synchronization as well as for operation –power factor correction, power flow calculation, islanding detection…. . Development of a fast, precise and robust synchronization method is therefore a critical issue.

Synchronization methods can be roughly divided into a) zero-crossings based methods [12], b) frequency-locked-loop based methods (FLL) [14, 15] and c) Phase-Locked-Loop (PLL) based methods [16-21], they are briefly discussed following.

*a) The zero-crossing based method.* Likely the simplest option to track the fundamental frequency of the grid voltage [12], they detect the zero crossings of this signal. However, the estimated frequency can only be updated each half period of fundamental voltage, also the reliability of the method being compromised under distorted conditions of the line voltage or when the measured signals are contaminated with noise [13].

*b) FLL based methods.* These methods track the frequency of the fundamental voltage, option for doing this are:

- *Dual Second Order Generalized Integrator using frequency-locked-loop (DSOGI-FLL)* [14] - This method separates the negative and positive sequence components using two quadrature-signal-generators (*QSG*) that act as a band-pass filter. The frequency of the input voltage is obtained from the relationship between the quadrature signal of the fundamental-*QSG* and the signal error between fundamental-*QSG* input and output.
- *Multiple SOGI-FLL (MSOGI-FLL) [15]* - The idea behind the *MSOGI-FLL* is to combine a set of *SOGI-QSG*s tuned at different frequencies, to remove specific harmonics present in a distorted network.

*c) PLL based methods.* These methods track the phase angle of the fundamental voltage, a variety of implementations can be found in the literature [16-25]. The *PLL*, or a combination of *PLL*s, can be implemented using phase (*abc*) quantities [16] or *dq* components in stationary [21] or synchronous reference frame [17-20]. Methods that implement a *PLL* in synchronous reference frame can be further divided into three different categories:

- *Synchronous reference frame PLL (SRF-PLL)* [17] - They transform the *abc* voltages to stationary *dq* voltages and use a simple PLL in the *q*-axis to obtain the grid frequency. The bandwidth of the PI controller looks for a compromise between dynamic response and disturbance rejection (see Fig. 1b). *PLL (SRF-PLL)* are the base for other methods described below.
- *Pre-filter stage SRF methods* [18, 22] - In order to isolate the positive sequence voltage, these methods insert a pre-filter stage, either in the stationary or synchronous reference frame, before the *SRF-PLL*. Options of these type of methods include:

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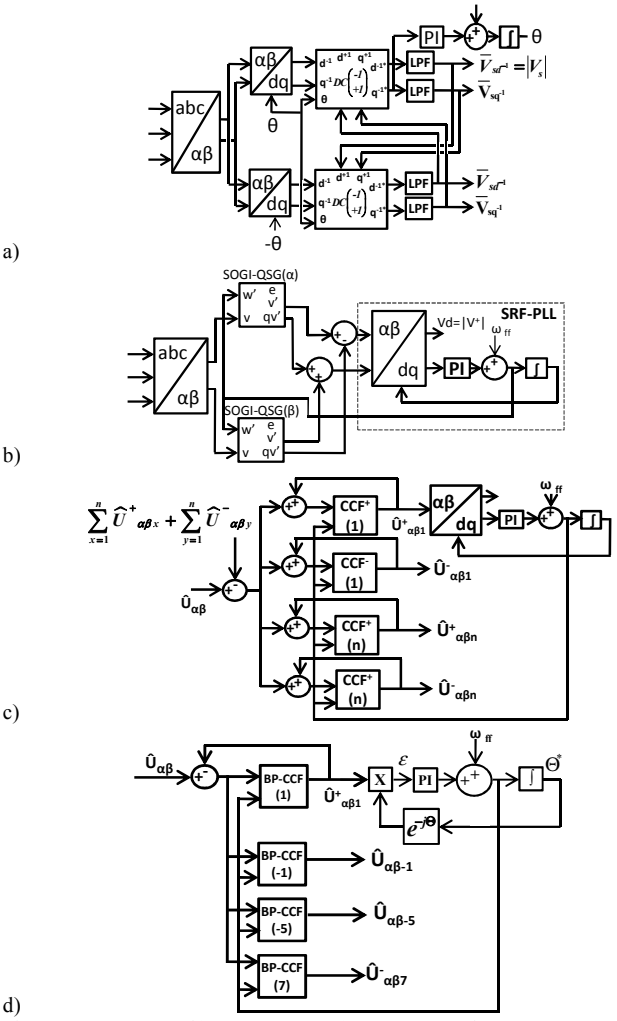


Fig. 1 a) *DSRF-PLL*, b) *DSOGI-PLL*, c) *MCCF-PLL* d) *BP-CCF-CPLL* block diagrams

a. Double synchronous reference frame *PLL* (*DSRF-PLL)* [18]. This method rotates the stationary reference components into the positive and negative sequence reference frames. Using a decoupling network, the negative sequence is filtered, the output signal feeding a *SRF-PLL* (see Fig. 1a).

b. Double Second Order Generalized Integrator *PLL* (*DSOGI-PLL*) [19]. This method is similar to a *DSOGI-FLL* with the difference that the output of the decoupling network that extracts the positive sequence feeds a *SRF-PLL* (see Fig. 1b).

c. Multiple Complex Coefficient Filter PLL (*MCCF-PLL*) [20]. Uses complex-coefficient-filters (in stationary reference frame) to isolate/remove specific components. A combination of *CCF*s isolate the positive sequence voltage, its output feeding a *SRF-PLL* (see Fig. 1c).

d. Band-pass Complex-coefficient-filter complex-PLL (*BP-CCF-CPLL)*. The method described in [21] isolates the positive sequence using a band-pass *CCF* and feds it to an Angle Tracking Observer (*ATO*). The method also extracts the fundamental frequency dependent harmonics using *BP-CCF*s which filter the error signal from the fundamental *BP-CCF* (see Fig. 1d).

- *Filter in the Loop methods* [22, 23] – These methods insert one or more filters before the *SRF-PLL* PI regulator to cancel specific harmonics, normally integer multiples of the fundamental frequency (e. g. -5$^{th}$ , 7$^{th}$ , -11$^{th}$,…). Two types of filters have been proposed; Adaptive Notch Filter (*ANF*) [22] and Second-Order Lead-Compensators (*SOLC*) [23]. A hybrid method that combines a pre-filter stage and filter in the loop is proposed in [24].

Potential limitations of the synchronization methods outlined above include showing resonances at frequencies near to the fundamental frequency, what can result in overshoots in those frequencies are excited, reduced harmonic rejection capability; and increased sensitivity to unbalances in the grid voltages, what compromises their performance in polluted networks. Also some of these methods are not configurable to reject more than one harmonic component, or do not exhibit good response under the overall disturbances alluded, making their performance suboptimal in a generic scenario.

This paper proposes a synchronization technique using a cascaded, complex-coefficient-filters (*CCCF*) topology and a complex *PLL*. The resulting design is simple and intuitive, with good dynamic response, and robust against unbalances and/or distorted line voltages. Also a methodology for the tuning of the controller is provided.

The paper is organized as follows: section II shows the principles of the proposed synchronization method. A simulation based analysis among the different pre-filter stage methods for different kinds of distortions is given in Section III. Experimental results demonstrating the viability of the proposed method are presented in Section IV. Section V contains the conclusions.

## II. Cascaded Complex Coefficient Filter PLL for Grid Synchronization

Fig. 2 shows the structure of the proposed method, cascade complex coefficient filter with complex *PLL* (*CCCF-CPLL*). It consists of two major blocks: a pre-filter stage and an Angle Tracking Observer (*ATO*). The pre-filter stage isolates the positive sequence component of the line voltage vector, while the *ATO* stage obtains its frequency, which is later used to feedback the pre-filter stage, making, thus making this filter adaptive. The design and operation of both stages is discussed following.

### *A. Pre-Filter Stage*

In addition to the positive-sequence fundamental component, the voltage vector in actual distribution lines often includes a negative-sequence at the fundamental frequency (if unbalanced) as well higher order harmonics of the fundamental frequency. The goal of the pre-filter stage is to isolate the positive-sequence fundamental component from the overall line voltage vector. This can be done either through filtering techniques [14, 20, 21] or decoupling networks [16, 18].

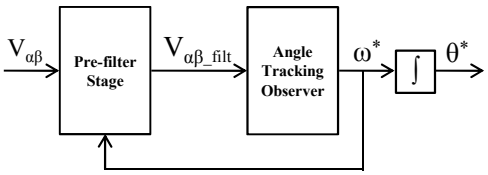


Fig. 2 – Schematic representation of the proposed filtering

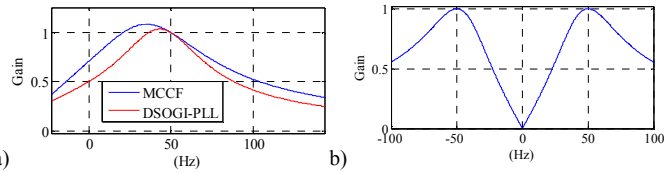


Fig. 3 - Frequency response function magnitude of a) *MCCF* and *DSOGI-PLL* and b) real coefficient filter. It is noted from a) that the unitary gain occurs at the rated frequency, but values larger than one (i.e. overshoot) occur at frequencies nearby.

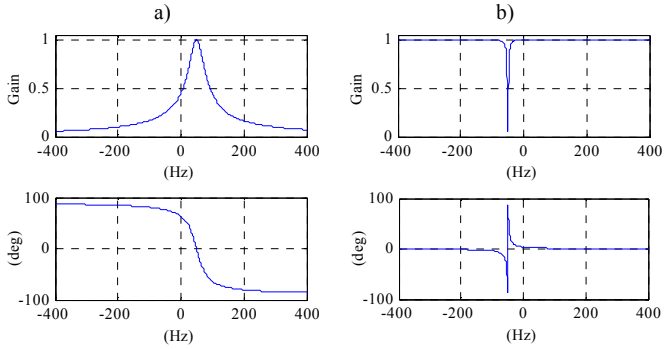


Fig. 4 – Frequency response function magnitude (top) and phase (bottom) of a) Band Pass and b) Band Stop complex coefficients filters

One disadvantage of the pre-filter stages proposed in [19, 20] is that although they provide unitary gain at the fundamental frequency, they can have a gain bigger than one at frequencies nearby (Fig. 3a). This type of behavior can produce overshoots in those frequencies are excited, what can occur e.g. during transients [26]. Also, conventional filtering techniques apply identical, real coefficients filters, to both the *d* and *q*-axis, which do not distinguish between positive and negative sequence components (see Fig 3b) [14, 17]. To overcome both problems, the use of cascaded complex-coefficient filters (*CCF*) is proposed in this paper. It is noted that conceptually, a *CCF* can also be represented as a real coefficient filter with cross-coupling between the *d* and *q*-axes [20]. Examples of first-order band-pass (*BP-CCF*) and band-stop (*BS-CCF*) complex-coefficient filters are shown in (1) and (2), their corresponding frequency response function and block diagram being shown in Fig. 4 and 5 respectively [20].

$$BP-CCF(s)=\frac{\omega_{bw\_bp}}{s-j\,n\,\omega_0+\omega_{bw\_bp}} \quad (1)$$

$$BS-CCF(s)=\frac{s-j\,n\,\omega_0}{s-j\,n\,\omega_0+\omega_{bw\_bs}} \quad (2)$$

*CCF*s intrinsically distinguish between positive and negative sequence components. Furthermore, band-pass *CCF* provides unitary gain at the fundamental frequency, the gain monotonically decreasing as the frequency moves apart from this value.

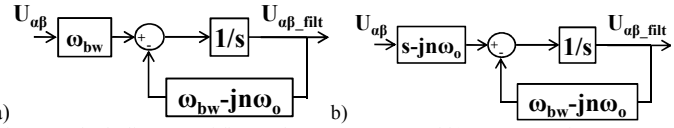


Fig. 5 – Block diagram of first order a) *BP-CCF* and b) *BS-CCF* using complex vector notation.

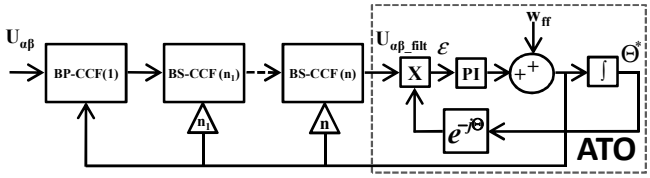


Fig. 6 – Block diagram of *CCCF-CPLL*. $\omega_{ff}$ stands for the nominal value of the grid frequency.

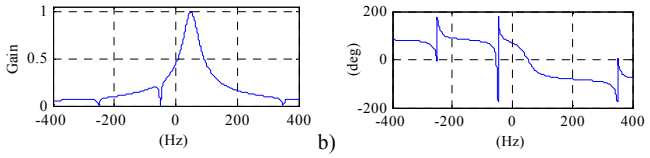


Fig. 7 – a) Magnitude and b) phase of the frequency response function of *CCCF-CPLL*

In the proposed method, a pre-filter stage consisting of a band-pass *CCF* (1) series connected with a set of *n* band-stop *CCF*s is used to separate the positive-sequence fundamental component of the grid voltage. Fig. 6 shows the overall pre-filter stage structure in the stationary reference frame (*αβ* coordinates). The *BP-CCF* is tuned for a center frequency $\omega_0$=50 Hz (European grid) and a bandwidth $\omega_{bw\_bp}$. The output of the *BP-CCF* block drives a set of cascaded *n* band-stop complex-coefficient filters (*BS-CCF*), tuned to rejected fundamental frequency dependent harmonics (-1st, -5th, 7th, -11th, 13th …) that typically exist in distorted grids, the bandwidth of the *BS-CCF* being $\omega_{bw\_bsn}$. Fig. 7a and b show the frequency response function magnitude and phase for the proposed pre-filter scheme.

### *B. Complex PLL in Stationary Reference Frame*

Once the fundamental frequency dependent harmonics have been removed from the measured line voltage, the frequency is estimated by means of an angle tracking observer (*ATO*) (see Fig. 6) [27]. The estimated frequency is used to make the filtering adaptive, the phase of the fundamental voltage being obtained by integration of the frequency. The *ATO* consists of a PI based closed-loop system whose input is the cross-product between filtered input signal ($U_{\alpha\beta\_filt}$) and a unitary vector rotating at the estimated frequency $e^{-i\theta^*}$ (3), being ($|U_{\alpha\beta\_filt}|$) the current vector module. The *ATO* error $\varepsilon(t)$ is proportional to the *sine* of the difference between the estimated ($\theta^*$) and the real angle ($\theta$) (3), $\sin(\theta-\theta^*)\approx\theta-\theta^*$ can be safely assumed if the angle error is small. The *ATO* closed-loop transfer function and the overall output transfer function are given by (4) and (5) respectively, with $G_{PI}(s)$ being the transfer function of the PI controller.

$$\varepsilon(t)=U_{\alpha\beta\_filt}\otimes e^{-i\theta^*}=\left|U_{\alpha\beta\_filt}\right|\sin(\theta-\theta^*) \quad (3)$$

$$\frac{\theta^*(s)}{\theta(s)}=\frac{G_{PI}(s)}{s+G_{PI}(s)},\ G_{PI}(s)=K_p\left(1+\frac{K_i}{s}\right) \quad (4)$$

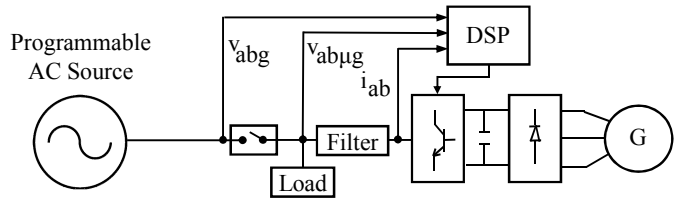


Fig 8. – Simulation scheme

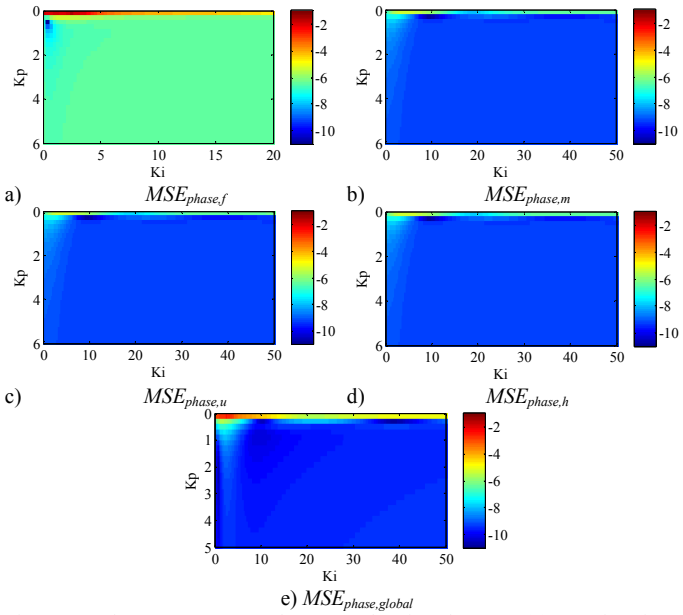


Fig. 9 – a)-d): *CCCF-CPLL* color maps showing the *MSE* (6) as a function of the controller gains for different types of disturbances and varying conditions in the line voltage. It is noted that a logarithmic scale has been used in order to improve the visualization, i.e. the color corresponds to $\log_{10}(MSE)$, e) Combined *MSE (9)* as a function of the controller gains with $w_h = w_u = w_m = 0.33$ and $w_f = 0.01$

$$\frac{w^*(s)}{\theta(s)} = \frac{s \cdot G_{PI}(s)}{s + G_{PI}(s)} \tag{5}$$

## III. Simulation Results

The proposed synchronization technique has been tested using the simulation scheme shown in Fig 8. Four different scenarios have been considered: 1) change of the grid frequency, 2) change of the grid voltage magnitude, 3) grid unbalance and 4) polluted grid conditions (harmonics). The simulation was performed using Matlab. Tustin was used for the discretization of the continuous transfer functions. For each case, the performance of the proposed method is compared with the results provided by the synchronization methods described in section I: *DSRF-PLL* (Fig. 1a), *DSOGI-PLL* (Fig. 1b), *MCCF-PLL* (Fig. 1c), *BP-CCF-CPLL* (Fig. 1d), and *CCCF-CPLL* (Fig. 6).

### *a) Gains selection*

Several gains need to be chosen for each method; a tuning methodology has been established, with the goal optimizing the tuning for each method, thus making the comparative analysis fair. The mean squared error (*MSE*) (6), between the real phase $(\theta)$ and the estimated phase $(\theta^*)$, was chosen as a reliable figure of merit, its minimization using numerical optimization has been used for the gain selection for each method. The *MSE* will be function of the proportional and integral gains of the controller, $k_p$ and $k_i$, color maps were found to be adequate to show this dependence. Similarly to (6), the *MSE* can also be calculated using the error in the estimation of the fundamental voltage magnitude (7) and of the fundamental voltage frequency (8), where subscripts *dist* refers to type the disturbance applied, *f* standing for a frequency step, *m* standing for an amplitude step, *u* for an unbalance in the grid voltage and *h* for the grid voltage containing harmonics.

$$MSE_{phase,dist}(t) = \frac{1}{T}\int\left(\theta - \theta^*\right)^2(t)\,dt \tag{6}$$

$$MSE_{amp,dist}(t) = \frac{1}{T}\int\left(V - V^*\right)^2(t)\,dt \tag{7}$$

$$MSE_{freq,dist}(t) = \frac{1}{T}\int\left(\omega - \omega^*\right)^2(t)\,dt \tag{8}$$

Fig. 9 shows the *CCCF-CPLL* error color maps obtained for the different types of distortions and transient conditions of the line voltage already described in this section. It is observed from the figure that the cases in b), c) and d) have similar color maps, meaning that the same set of gains provides near optimal results (i.e. minimum *MSE*) for those type of disturbances. It is noted however that the regions with lowest error in Fig. 9a occurs at different gains values. Choosing a set of $k_p$ and $k_p$ gains able to provide adequate response under any kind of distortion or varying condition in the line voltage can be done by combining the *MSE*s in Fig. 9a to 9d into a global $MSE_{phase,global}$ (9), the purpose of the weights $w_x$ being to select the type of disturbance that should be better rejected.

$$MSE_{phase,global} = w_f MSE_{phase,f} + w_m MSE_{phase,m} + \\ + w_u MSE_{phase,u} + w_h MSE_{phase,h} \tag{9}$$

While the same value could be used for all the four weights in (6), they can also be chosen to be different. For example, sudden step-like changes of the frequency are less likely to occur than other kind of distortions, due to the large inertia of the generators [10, 11]. Then, a smaller value for $w_f$, compared to the rest of weights in (6), could be used. Fig. 9e shows the $MSE_{phase,global}$ when $w_h = w_u = w_m = 0.33$ and $w_f = 0.01$. According to Fig. 9e, values of the gains $k_p$=0.3 and $k_i \approx 38$ would be adeuate choices, as $MSE_{phase,global}$ is small and has low sensitivity to changes of $k_p$ and $k_i$. It is also observd from Fig. 9e that other regions with low values of $MSE_{phase,global}$ exist, but have larger sensitivity to variations of $k_p$ and $k_i$.

Fig.10 shows the $MSE_{phase,global}$ color maps obtained using the tuning methodology described for all synchronization methods considered. The same weights as for the *CCCF-CPLL* were used. The $MSE_{phase,global}$ color maps are shown as a function of the *PLL* PI regulator gains, $k_p$ and $k_i$ respectively, for the scenarios described in Table I. It is observed from Fig. 10a and c that for the case of the *DSOGI-PLL* and *BP-CCF-CPLL*, there is a region of low values of $MSE_{phase,global}$, and with a relatively smooth transition *MSE* to

the regions with larger values. This means that these methods have a good disturbance rejection capability, and the *MSE* selection of the gains is not critical, i.e. slight changes in the gains do not have a critical impact on the performance of the method. Opposite to this, significantly larger variations of the $MSE_{phase,global}$ are observed in Fig. 10b for the case of the *DSRF-PLL,* meaning that this method is more sensitive to the tuning process. The results of optimization stage for each method are summarized in Table II.

While *DSRF-PLL* and *DSOGI-PLL* methods do not need to configure any extra block (see Fig. 1a and 1b), *BP-CCF-CPLL, MCCF-PLL* and *CCCF-CPLL* methods use a first-order *CCF* (see Fig. 5) for each component being removed/isolated (Figs 1d, 1c and 6). *BP-CCF-CPLL* method uses three band-pass complex-coefficient-filters: one for fundamental component, one for $-1^{st}$ harmonic (to isolate the negative sequence component due to unbalance) and another to isolate the $-5^{th}$ fundamental dependence harmonic. For the *MCCF-PLL* method, three band-pass complex-coefficient-filters tuned at the frequencies to be rejected need to be set while for the *CCCF-CPLL,* one band-pass complex-coefficient-filter is used for the fundamental component and two band-stop complex-coefficient-filters to reject $-1^{st}$ and $-5^{th}$ harmonics. The bandwidth $\omega_{bw}$ for all methods is defined in Table II.

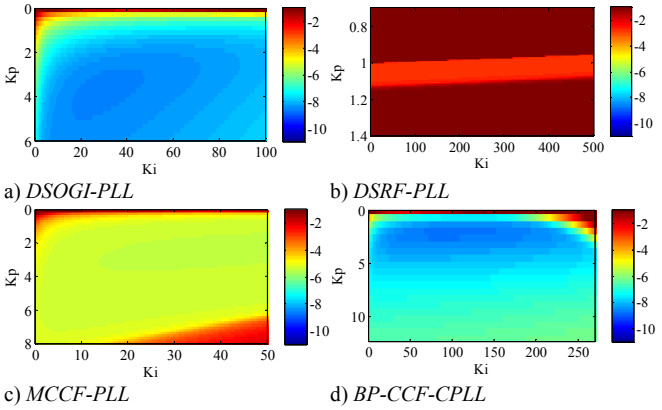


Fig. 10 – Color maps showing the $MSE_{phase,global}$ as a function of the controller gains for the different methods. Same logarithmic scale as in Fig. 9 was used.

| **Table I** - *Simulation Scenario* | | | | | |
|---|---|---|---|---|---|
| *Sim. Step* | Grid parameters | Harmonics | Frequency jump | Unbalance | Amplitude Jump |
| $10^{-4}$ s | 380V, 50Hz | 10% *pu* ($-5^{th}$) | 50Hz to 48Hz | 0.7 *pu* in phase *C* | 50% |

| **Table II** - *Optimization stage results* | | | |
|---|---|---|---|
| *DSOGI-PLL* | $k_p$ =3.72 | | $k_i$ =28.72 |
| *DSRF-PLL* | $k_p$ =1.06 | | $k_i$ =0.71 |
| *MCCF-PLL* | $k_p$ =2.21 | $k_i$ =44.13 | $W_{bw\_mccf}$ = 300 rad/s |
| *CCCF-CPLL* | $k_p$ =0.3 | $k_i$ =38.48 | $W_{bw\_bp\text{-}ccf}$ = 300 rad/s<br>$W_{bw\_bs\text{-}ccf(-1)}$ = 100 rad/s<br>$W_{bw\_bp\text{-}ccf(-5)}$ = 300 rad/s |
| *BP-CCF-PLL* | $k_p$ =1.98 | $k_i$ =104.2 | $W_{bw\_bp\text{-}ccf}$ = 300 rad/s |

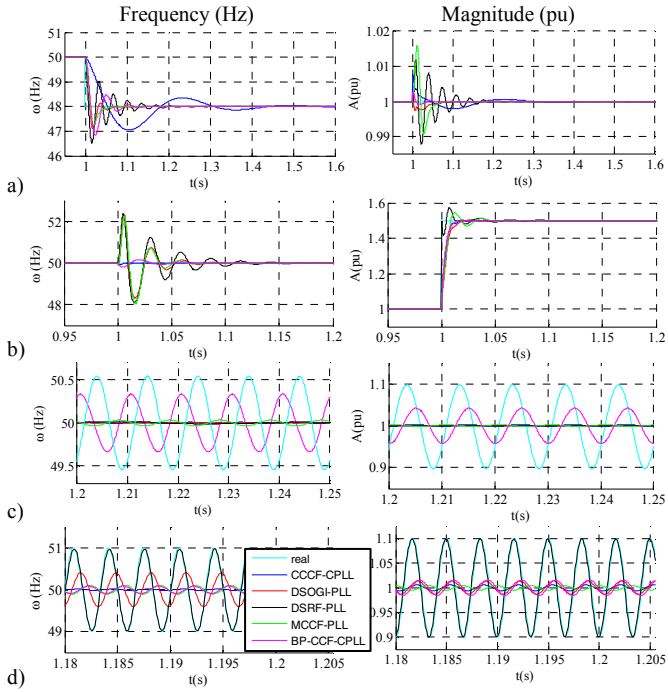


Fig. 11– Simulation Results. Estimated frequency (left) and magnitude (right) of the fundamental voltage by different methods for the case of a) step-like change of line voltage frequency, b) step-like change of the line voltage magnitude, c) phase voltage unbalance and d) frequency line voltage with harmonics.

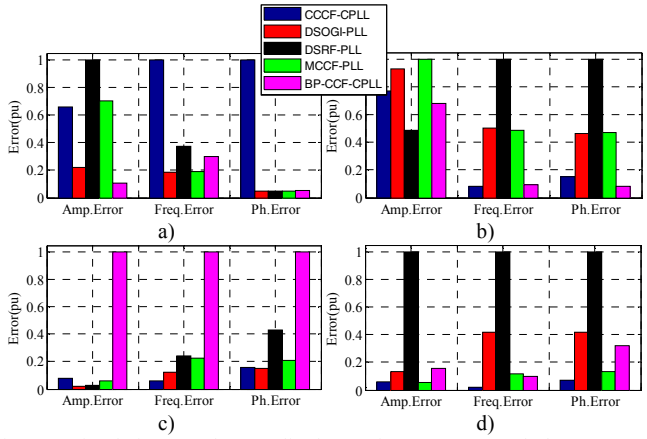


Fig. 12 –Simulation Results: amplitude (7), frequency (8) and phase (6) *MSE* for all the methods and for different types of disturbances: a) step-like change of line voltage frequency, b) step-like change of the line voltage magnitude, c) phase voltage unbalance and d) line voltage with harmonics

*b) Simulation results*

Fig. 11 shows the estimated frequencies (Hz) and amplitudes (p.u) for different types of disturbances in the line voltage, including changes in the fundamental voltage frequency and magnitude, unbalances and harmonics; the results for each event disturbance are discussed following.

- *Fundamental voltage frequency step-like change*: Fig. 11a shows the simulation results when the frequency changes from 50 to 48 Hz occurs (t=1s). It is observed that *CCCF-CPLL* shows the slowest response, while *MCCF-PLL*, *DSOGI-PLL*, and *BP-CCF-CPLL* and *DSRF-PLL* show similar, faster response, being the *DSOGI-PLL* the method with shortest settling time. Fig. 12 shows the mean squared error (*MSE*) for the estimated fundamental voltage phase,

(6), magnitude (7) and frequency (8). The bars for each case were normalized by dividing by the worst case, the maximum value for each case being therefore one. Fig. 12a summarizes the *MSE* for the case of a step-like change in the frequency, confirming the results observed in Fig. 11a.

- *Fundamental voltage amplitude step-like change* A 50% amplitude jump has been introduced in Fig. 11b in t=1s. It is observed from Fig. 11b and 12b that the *BP-CCF-CPLL* shows an overall better behavior, followed by the *CCCF-CPLL*. On the other hand, an amplitude change produces oscillations in the estimated frequency, *DSRF-PLL* showing the worst behavior in this regard. Regarding the error in the estimation of the frequency and phase terms, the behavior of *DSRF-PLL*, *DSOGI-PLL* and *MCCF-PLL* are the worst, showing a fast but oscillating response. It is finally noted that either for amplitude, frequency or phase *MSE*, the best methods to deal with changes in the amplitude are the *BP-CCF-CPLL* and the *CCCF-CPLL*. Conversely, *DSRF-PLL* shows the worst frequency and phase *MSE*, while *MCCF-PLL* exhibits the biggest amplitude *MSE*.
- *Phase voltage unbalance*: Fig 11c shows the simulation results of a 30% unbalance in phase *C*. It can be observed that the *DSOGI-PLL* shows the most appealing behavior, followed by the *CCCF-CPLL*, being the *BP-CCF-CPLL* the method with the lowest unbalance rejection capability. It is also noted that although the *DSOGI-PLL* shows good unbalance rejection, it has poor harmonic rejection capability (Fig. 11d). This is explained because the *DSOGI-PLL* has two *SOGI-QSG* (see Fig. 1a) that extract the positive sequence component, removing the negative sequence, however it does not have any extra block to remove high order fundamental dependence harmonics. The different *MSEs* during the unbalance for each method are summarized in Fig 12c. The *CCCF-CPLL* and the *DSOGI-PLL* are the methods with lowest *MSE* in all cases (amplitude, frequency and phase), while the *BP-CCF-CPLL* is the method with the poorest performance, as it does not reject the negative sequence component as it only uses a band-pass-filter for the positive sequence.
- *Harmonic voltage injection*. The impact of the harmonics on the estimated fundamental frequency and the fundamental voltage component are shown in Fig. 11d. It is observed that *MCCF-PLL* and *CCCF-CPLL* almost totally reject all the harmonics. On the other hand *BP-CCF-CPLL*, *DSOGI-PLL* and *DSRF-PLL* show lower harmonic rejection capability; significant oscillations in the estimated frequency being observed for both methods. Fig. 12d summarizes the simulation results when harmonics in the grid voltage are present.

## IV. Experimental Results

Experimental verification of the behavior of the synchronization methods discussed in this paper is presented in this section. The experimental setup is shown in Fig. 13. A diesel generator "G" rated 100kVa, 380V and 152A, was used as the primary power source for the master and slave inverters. LCL filters, with a resonance frequency of 575Hz are used to connect the inverters to the grid. The master inverter was programmed to produce the same type of disturbances discussed in the previous sections. A *TMS320F28335 DSP* has been used for the implementation of the algorithms. A sampling frequency of 10 kHz was used, which is equal to the switching frequency. Tustin transformation was used for the discretization of the continuous transfer functions. The gains for the different methods have been tuned to the values obtained through the optimization methods described in the previous section (see Table II).

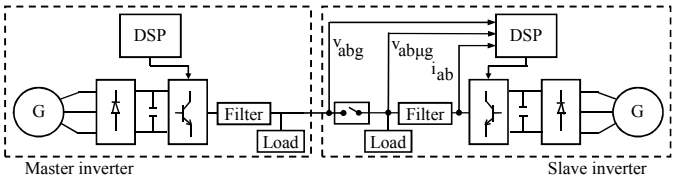

Fig. 13 –Experimental Setup

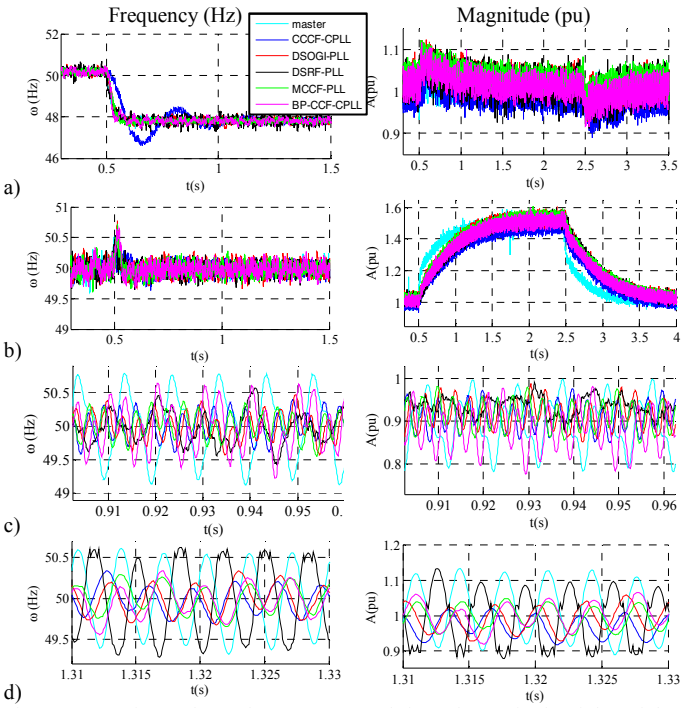

Fig. 14– Experimental Results. Frequency (left) and magnitude (right) of the fundamental voltage estimated by different methods for the case of a) step-like change of line voltage frequency, b) step-like change of the line voltage magnitude, c) phase voltage unbalance and d) frequency line voltage with harmonics.

Fig. 14 shows the frequency and amplitude experimentally measured for the same disturbances and transient conditions discussed in section III, Fig. 15 shows the different *MSEs*, these results are discussed following.

- *Fundamental voltage frequency step-like change:* Fig. 14a shows the results when a step-like frequency variation from 50 to 48Hz (t=0.5) occurs. It is observed that all methods show a similar response, except the proposed method that is slower updating the grid frequency, so it causes an

additional phase shift. The experimental results mostly agree with the simulation results. It is noted that this is not considered a critical issues as such kind of transient is not expected to occur in practice.

- *Fundamental voltage amplitude step-like change* Fig. 14b shows the response of the different methods when a step-like variation of 50% is applied to the fundamental voltage magnitude. The dynamic response of all methods is very similar, which is also confirmed by Fig. 15b. Some disagreement is observed among the experimental results in Fig. 15 and the simulation results in Fig. 12. This discrepancy would be explained by the fact that, contrary to the simulation (see Fig. 8 and 11b), the output voltage amplitude of the master inverter cannot be changed instantaneously (see Fig. 14b),
- *Phase voltage unbalance*: An unbalance of 30% in phase C was and Fig. 14c shows the frequency and amplitude obtained by each synchronization method. As for the simulation results, the *BP-CCF-CPLL* method exhibits a slightly worse unbalance rejection capability, with a negative sequence component showing up both in amplitude and frequency. The other methods perform very similar.
- *Harmonic voltage injection*: Fig. 14d shows the output amplitude and frequency of all synchronization methods when a -5th harmonic of magnitude 0.1p.u. is present in the grid voltage. The *DSRF-PLL* exhibits the poorest performance, with the rest of synchronization methods showing a similar behavior. Still, according to Fig. 15d, the *CCCF-CPLL* shows the lowest overall error (amplitude, frequency and phase), which is in accordance with the simulation results presented in section III. The differences in terms of harmonic rejection are related, as in the case of the unbalance experiment, to the low-pass behavior of the synchronization control strategy of the slave inverter, whose current PI regulators are set to $k_p$ = 8.4 and $k_i$ = 60.

Table III summarizes the results obtained for each method according to several criteria:

- Simplicity: conceptual complexity of the methods.
- Flexibility: possibility of adapting the system, e.g. rejected/isolated harmonics, depending on the grid characteristics.
- Application on APF: possibility to measure high order harmonics to be further compensated by an APF.
- Tune complexity: properties of optimization stage process (e.g. smoothness of the *MSE* color map, …).
- Dynamic response: refers to the settling time when frequency changes occur.

Conceptually, the proposed method is relatively simple, as it consists of a *BP-CCF*, several *BS-CCF*s (depending on the harmonics that want to be rejected) and a *CPLL* series connected, not being necessary decoupling networks (e.g. *DSOGI-PLL* or *MCCF-PLL*), which would increase the complexity of the method. *CCCF-CPLL* method also has good

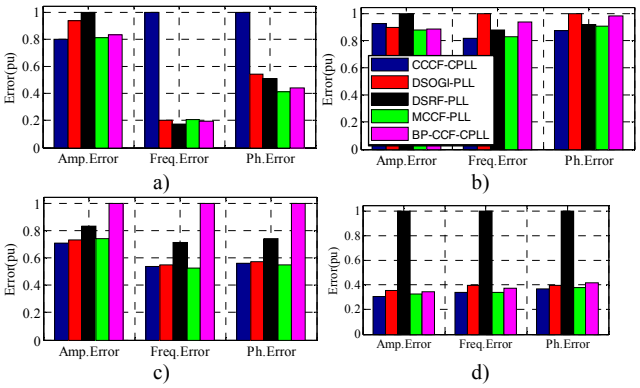


Fig. 15 –Experimental Results: amplitude (7), frequency (8) and phase (6) *MSE* for all the methods and for different types of disturbances: a) step-like change of line voltage frequency, b) step-like change of the line voltage magnitude, c) phase voltage unbalance and d) line voltage with harmonics

**Table III.** *Comparison of synchronization methods*

| | *CCCF-CPLL* | *DSOGI-PLL* | *DSRF-PLL* | *MCCF-PLL* | *BP-CCF-CPLL* |
|---|---|---|---|---|---|
| **Simplicity** | LOW | HIGH | HIGH | MEDIUM | LOW |
| **Flexibility** | EXCELLENT | LOW | LOW | EXCELLENT | MEDIUM |
| **Freq. adapt** | YES | YES | YES | YES | YES |
| **Application to APF** | NO | NO | NO | YES | YES |
| **Tune Complexity** | MEDIUM | LOW | HIGH | LOW | LOW |
| **Execution Time (us)** | 7.22 | 4.98 | 8.32 | 6.94 | 7.42 |
| **Response time** | MEDIUM | MEDIUM | MEDIUM | EXCELLENT | EXCELLENT |
| **Unbalance response** | EXCELLENT | EXCELLENT | GOOD | EXCELLENT | LOW |
| **Harmonic Rejection** | EXCELLENT | MEDIUM | LOW | EXCELLENT | MEDIUM |

flexibility, as only one *BS-CCF* is needed for each component be rejected. Methods like *DSOGI-PLL* and *DSRF-PLL* do not provide a mechanism to decouple harmonics.

All methods are frequency-adaptive so they can move the central frequency of their filters in case of changes in the fundamental frequency. The frequency estimation of the proposed method has slower dynamics compared to the others methods, although it is noted that the rate of frequency variation of a grid is small [10, 11] (e.g. the UNE-EN 5016 limits the maximum frequency shifts: for interconnected systems the mean frequency value, calculated each 10s, should not exceed ±1% during the 99.5% of a week, though exceptionally deviations between +4% and −6% are permitted).

If the synchronization method is to be used in an APF, the *MCCF-PLL* and the *BP-CCF-CPLL* would be in principle better options, as they provide the amplitude and phase of the harmonics to be compensated.

Regarding their tuning, the *CCCF-CPLL* shows a smooth and wide tuning area so it is easy to tune. Contrary to this, *DSRF-PLL* method is rather sensitive to variations of the parameters.

As for the computational requirements, *DSOGI-PLL* has the lower burden, though it is at the price of lower performance.

Finally, regarding unbalanced line voltages and harmonic rejection, both *CCCF-CPLL* and *MCCF-PLL* have excellent performance, with *DSRF-PLL* and *BP-CCF-CPLL* being the worst in this aspect.

## V. CONCLUSIONS

A synchronization method for grid connected power converters is presented in this paper. The method is based on a pre-filter-complex-coefficient stage to eliminate disturbances and a complex PLL to extract the phase and magnitude of the fundamental voltage vector component. The use of complex-coefficient filters allows selection of the positive/negative sequence harmonics to be removed/isolated.

A *MSE* based tuning methodology of the controller gains has been developed. Simulation and experimental results comparing the proposed methods with existing synchronization methods in different scenarios has been presented. From the tests performed, it is concluded that the proposed method shows an excellent overall performance, especially in terms of harmonic and unbalance rejection capability, as well as acceptable transient response when changes in the fundamental voltage occurs, accomplishing with international connection standards [10, 11].

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