Improving the Third Quadrant Operation of Superjunction MOSFETs by Using the Cascode Configuration

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***Abstract*— In this paper, the third quadrant behavior of a High-Voltage (HV) Superjunction MOSFET (SJ-FET) in Cascode Configuration (CC) with a Low-Voltage silicon MOSFET (LV-FET) is deeply studied by means of an analytical model and experimental data. The third quadrant dynamic behavior of the SJ-CCs is compared to the standalone counterparts by evaluating their reverse recovery time (t_{RR}), reverse recovery peak current (I_{RRM}) and reverse recovery charge (Q_{RR}). An analytical model and experimental results show that the SJ-CC avoids or mitigates the activation of the SJ-FET body-diode during the third quadrant operation. As a consequence, the SJ-CC strongly improves the widely used Figure-of-Merit (FoM) $R_{ON}{\cdot}Q_{RR}$, which considers the on-state resistance of the transistors (R_{ON}). In addition, the results obtained using a SJ-CC are similar or better than the achieved by SJ-FETs with enhanced reverse recovery (i.e., irradiated SJ-FETs). This paper also includes a comparison with commercial wide bandgap switches, concluding that the $R_{ON}{\cdot}Q_{RR}$ value provided by the SJ-CC is around eight times higher than the provided by a commercial GaN cascode.**

***Index Terms*—Cascode configuration, Superjunction MOSFET, third quadrant, reverse conduction, reverse recovery charge (Q_{RR}), synchronous rectification, silicon.**

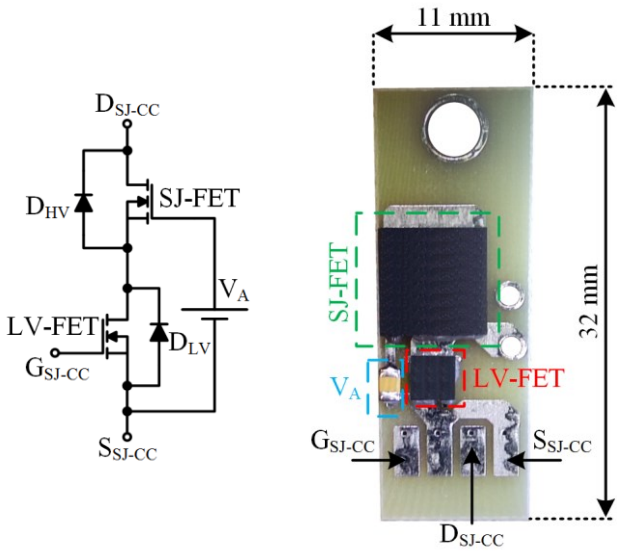
I. Introduction

THE Superjunction MOSFET (SJ-FET) is one of the greatest contributions of the last 30 years in the power electronics field. This silicon-based technology, which was introduced in 1998 [1]-[3], offers lower on-state resistance ($R_{ON\text{-}HV}$), gate charge ($Q_{G\text{-}HV}$) and output charge ($Q_{OSS\text{-}HV}$) than traditional vertical MOSFETs. As a result, the SJ-FET has become the main High-Voltage (HV) power switching device for a voltage that ranges between 600 V and 900 V.

Taking into account the SJ-FET qualities, its benefits mainly arises when it operates in first quadrant (i.e., the current flows from the drain to the source), and under hard-switching conditions. However, there are applications, such as synchronous DC-DC converters and inverters, where the power transistor operates in the third quadrant, also called reverse conduction (i.e., the current flows from the source to the drain). The technique in which these applications are based on is referred to as Synchronous Rectification (SR) and it consists in replacing diodes by transistors. Among other things, SR reduces conduction losses due to the low voltage drop in $R_{ON\text{-}HV}$ in comparison to the forward voltage drop of a diode, and enables bidirectional power conversion.

The main problem is the poor performance of the SJ-FET body-diode, which jeopardizes the third quadrant operation [4]-[5]. The Reverse Recovery (RR) effect damages the performance of the power converter in terms of both power efficiency and Electromagnetic Interference (EMI). As a result, several techniques have been proposed to minimize the RR effect in order to enable the use of SJ-FETs in SR, taking advantage of their good switching behavior and low $R_{ON\text{-}HV}$. Differently from the prior literature, a Cascode Configuration (CC) combining a SJ-FET and a Low-Voltage silicon MOSFET (LV-FET) to improve the RR (see Fig. 1) is proposed in this paper.

Nowadays, the CC is the preferred approach of some semiconductor companies to achieve normally-off GaN and SiC power transistors [6]-[10]. However, the CC has not been evaluated for silicon power switching devices until few years ago. The use of a SJ-FET in CC with a LV-FET (SJ-CC) was firstly proposed to reduce switching losses in [11]-[12]. A theoretical model of the switching mechanism during forward conduction of SJ-CCs paying especial attention to critical



(a) (b)

Fig. 1. SJ-FET in CC with a LV-FET (SJ-CC): (a) Basic schematic. (b) Plug-in board with a SJ-CC prototype.

parasitic elements can be found in [13]. Moreover, it was demonstrated that the SJ-CC can outperform the SJ-FET in standalone configuration when the switching frequency is in the order of hundreds of kHz and operating under hard-switching and high-forward current conditions [14]-[15]. Differently from the aforementioned papers, this work aims to model the third quadrant operation of the SJ-CC and to propose this configuration as a method to minimize the RR effect of the SJ-FET body-diode, enabling the use of these devices for SR [16].

This paper is organized as follows. The impact of the SJ-FET body-diode in SR is described in Section II together with a review of the techniques that have been proposed to alleviate this problem. The third quadrant operation of the SJ-CC is detailed in section III, including both the static and the dynamic analysis. Section IV is focused on the experimental results, including the third quadrant curves that validate the analytical model presented in Section II, and the RR evaluation that shows the improvement achieved by the SJ-CC. Finally, the conclusions are gathered in Section V.

II. Third Quadrant Operation of a SJ-FET in Standalone Configuration

A. Operating States of a SJ-FET in Reverse Conduction (Static Operation)

Three different states can be identified when a SJ-FET in standalone configuration operates in the third quadrant. Fig. 2 shows the basic schematic for each state and the equivalent circuits are depicted in Fig. 3.

State A [see Fig. 2(a) and Fig. 3(a)]. The SJ-FET is in off-state because the gate-to-source voltage of the device (V_{GS-HV}) is lower than its threshold voltage (V_{Th-HV}). Then, the source-to-drain current (I_{SD}) flows entirely through the SJ-FET body-diode (D_{HV}) and the source-to-drain voltage (V_{SD-HV}) can be modeled as:

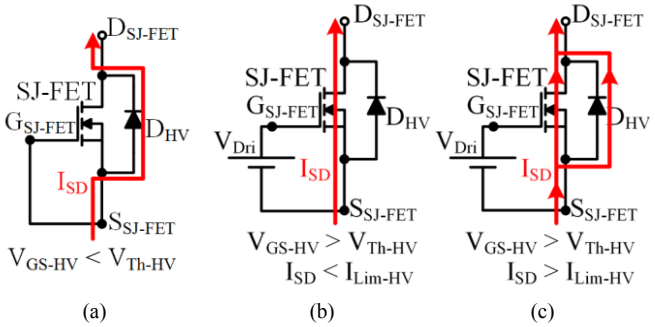


Fig. 2. Basic schematics of the SJ-FET in standalone configuration operating in third quadrant: (a) State A. (b) State B. (c) State C.

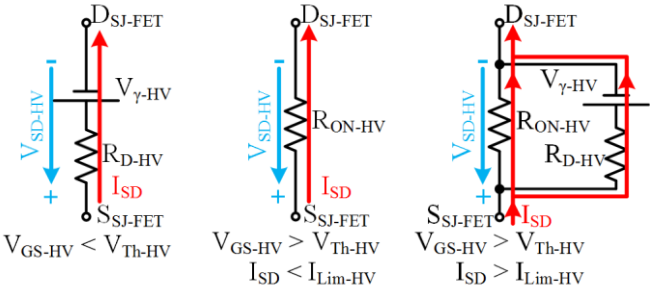


Fig. 3. Equivalent circuits of the SJ-FET in standalone configuration operating in third quadrant: (a) State A. (b) State B. (c) State C.

$$V_{SD-HV} = I_{SD} \cdot R_{D-HV} + V_{\gamma-HV}, \quad (1)$$

where $V_{\gamma-HV}$ and R_{D-HV} are the knee voltage and the dynamic resistance of D_{HV}, respectively. It is important to note that $V_{\gamma-HV}$ typically ranges between 0.6 V and 0.7 V.

State B [see Fig. 2(b) and Fig. 3(b)]: The SJ-FET is in on-state because V_{GS-HV} is higher than V_{Th-HV}. Therefore, I_{SD} flows completely through the channel of the SJ-FET. However, this is only true for a certain current range because for a high I_{SD} value, the voltage drop in R_{ON-HV} will overcome $V_{\gamma-HV}$ and, consequently, a current drift through D_{HV} will appear. Hence, the next condition must be satisfied to operate in state B:

$$I_{SD} \cdot R_{ON-HV} < V_{\gamma-HV}. \quad (2)$$

Therefore, the maximum current that the channel can conduct without activating D_{HV} can be defined as:

$$I_{Lim-HV} = \frac{V_{\gamma-HV}}{R_{ON-HV}}. \quad (3)$$

In this state, V_{SD-HV} can be modeled as:

$$V_{SD-HV} = I_{SD} \cdot R_{ON-HV}. \quad (4)$$

State C [see Fig. 2(c) and Fig. 3(c)]: The SJ-FET is in on-state because V_{GS-HV} is higher than V_{Th-HV}. Differently from state B, D_{HV} is activated since I_{SD} is higher than I_{Lim-HV}. Hence, a part of the current flows through the SJ-FET channel while the other part flows through D_{HV}. In this state, V_{SD-HV} can be modeled as:

$$V_{SD-HV} = \frac{R_{ON-HV} \cdot R_{D-HV}}{R_{ON-HV} + R_{D-HV}} \left(I_{SD} + \frac{V_{\gamma-HV}}{R_{D-HV}} \right). \quad (5)$$

B. *Reverse Recovery of a SJ-FET (Dynamic Analysis)*

The RR of D_{HV} appears when it is forced to stop conducting current and to block voltage [17]. Then, it will arise when the SJ-FET changes from states either A or C to off-state. Since it is important to understand when these transitions appear and their consequences, an example based on a synchronous boost converter will be given in this section. For the sake of simplicity, it is assumed that the inductor current (I_L) is always positive. Hence, four stages can be identified.

In stage 1 [see Fig. 4(a)], the low-side SJ-FET (Q_1) is in on-state and the high-side SJ-FET (Q_2) is in off-state. Then, I_L flows through the channel of Q_1. Note that since I_L flows from the drain to the source, Q_1 is operating in the first quadrant during this stage. On the other hand, during stage 3 [see Fig. 4(b)], Q_1 is in off-state and Q_2 is in on-state. Therefore, I_L flows through the channel of Q_2, which operates in the third quadrant (i.e., I_L flows from the source to the drain). According to Section II.A, part of the current would flow through D_{HV} if I_L is higher than I_{Lim-HV} in stage 3. However, as will be explained below, the D_{HV} activation during this stage has minor impact on the RR effect.

In order to avoid shoot-through, dead-times between the turn-off of a transistor and the turn-on of the other transistor are mandatory. During dead-times, I_L flows through the body-diode of Q_2 [see Fig. 4(c)], which operates in state A. Stage 2 denotes the dead-time between the turn-off of Q_1 and the turn-on of Q_2 while Stage 4 considers the dead-time between the turn-off of Q_2 and the turn-on of Q_1. Stage 4 is particularly critical because when the dead-time ends (i.e., transition between stage 4 and stage 1), the body-diode of Q_2 must stop conducting current and must start blocking voltage. Then, the RR caused by the accumulation of charge carriers arises because the body-diode needs to eliminate this charge before blocking any voltage. The charge elimination is done by generating an inverse current that flows through the channel of Q_1 during its turn-on and, consequently, the RR of Q_2 causes extra power losses in Q_1 [17]. It is important to highlight that during dead-times, I_L completely flows through the body-diode of Q_2 whereas in the stage 3, none or only a part of I_L flows through it. Therefore, since the RR of D_{HV} worsens with the current level, the possible activation of D_{HV} during stage 3 has minor impact on the RR effect.

The RR of a MOSFET is typically evaluated in terms of RR time (t_{RR}), RR peak current (I_{RRM}) and RR charge (Q_{RR}). The lower the parameters, the lower the RR impact. At this point, it is important to note that Q_{RR} not only considers the actual RR charge of the SJ-FET body-diode ($Q_{RR-D-HV}$), but also the charge (Q_{OSS-HV}) stored in the output capacitance of the MOSFET (C_{OSS-HV}). Then, during its turn-on, Q_1 conducts the inductor current (i.e., I_L), the current needed to charge the output capacitance of Q_2, and the current needed to eliminate charge carriers that are accumulated in the body-diode of Q_2. The

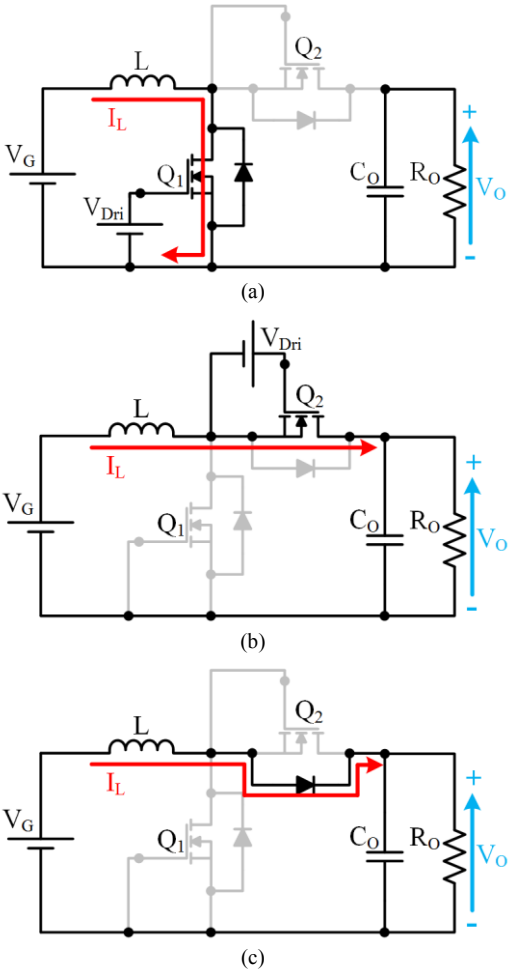


Fig. 4. Four stages of the synchronous boost converter assuming that I_L is always positive: (a) Stage 1. (b) Stage 3. (c) Stages 2 and 4.

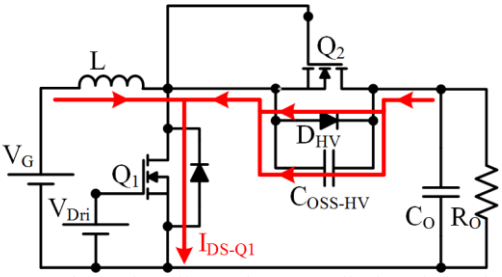


Fig. 5. Current paths for the different charge contributions during the RR of a SJ-FET in standalone configuration.

current paths for the different charge contributions when the RR takes place (i.e., during the transition between stage 4 and stage 1) are shown in Fig. 5. In the particular case of SJ-FETs, Q_{RR} is dominated by $Q_{RR-D-HV}$, which rises with the temperature, the current level through D_{HV} and the derivate of the drain current of Q_1 during its turn-on (di_{DS-Q1}/dt). Fig. 6 exemplifies the main idealized waveforms involved in the RR process, highlighting t_{RR}, I_{RRM}, Q_{RR}, the drain-to-source voltage of Q_1 (V_{DS-Q1}) and the drain-to-source current of Q_1 (I_{DS-Q1}) during the transition between stage 4 and stage 1 (i.e., turn-on transition of Q_1) [17].

In order to minimize the SJ-FET body-diode impact on SR, some techniques have been proposed by several authors in the past:

Dead-time minimization. Selecting the optimum dead-time

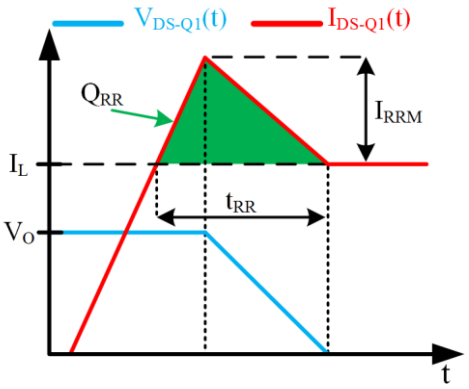
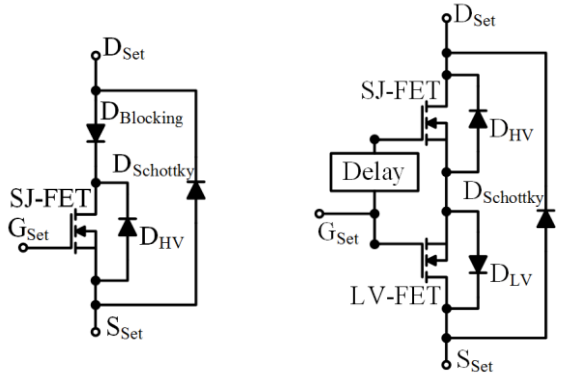


Fig. 6. Idealized voltage and current waveforms during the RR.



(a) (b)

Fig. 7. Two approaches based on using a set of semiconductor devices acting as a single transistor: (a) SJ-FET with antiparallel Schottky diode. (b) SJ-FET in combination with a LV-FET, a Schottky diode and a delay.

that completely avoids the activation of the SJ-FET body-diode is a direct method for minimizing Q_{RR} [18]-[20]. The difficulty is that the optimum dead-time depends on several factors, such as the operating conditions of the converter, and, consequently, auxiliary circuits are mandatory to ensure the minimum dead-times for each situation, increasing the complexity. It is important to note than if the dead-time is shorter that the optimum one, a shoot-through that strongly deteriorates the efficiency takes place. On the other hand, if the dead-time is longer than the optimum one, the SJ-FET body-diode is activated and, as a consequence, $Q_{RR\text{-}D\text{-}HV}$ is not eliminated.

$di_{DS\text{-}Q1}/dt$ minimization. This is another direct method to reduce the SJ-FET body-diode impact [18]. In this case, the approach is based on reducing the RR by minimizing $di_{DS\text{-}Q1}/dt$ during the turn-on of Q_1. Note that as was previously mentioned, the RR rises with di_{DS}/dt. A straightforward method for reducing di_{DS}/dt is to increase the gate resistance of Q_1. The drawback is that the switching losses caused by the coexistence of voltage and current at the channel of Q_1 will rise because the device spends more time performing the switching transitions.

Sets of semiconductor devices acting as a single transistor. This technique includes all the approaches where several semiconductor devices are added in order to avoid the activation of the SJ-FET body-diode [18], [21]-[24]. Fig. 7(a) shows the easiest approach, where a Schottky diode ($D_{Schottky}$) is placed in antiparallel with the SJ-FET while the diode connected in series with the SJ-FET ($D_{Blocking}$) blocks the reverse current through the SJ-FET. The problem is that since the SJ-FET never operates in the third quadrant, this technique implies that SR is not performed. In addition, the conduction losses rise when the device operates in the first quadrant due to the $D_{Blocking}$ conduction. Several modifications have been proposed to solve the previous problems. For instance, Fig. 7(b) shows a configuration that adds a LV-FET to block the third quadrant operation of the SJ-FET only when it is desired [21], [23]. However, the approach increases the complexity not only because of the higher number of elements, but also because a delay must be added in the turn-off gate signal of the SJ-FET with respect to the LV-FET one.

SJ-FET with fast body-diode. SJ-FETs focused on improving the third quadrant operation can be found in the market. Although Schottky diodes co-integration was initially proposed [25], current SJ-FETs with enhanced RR are mainly based on irradiation process [26]-[28]. Device irradiation normally requires special facilities, thus adding cost and jeopardizing other electrical parameters such as $V_{Th\text{-}HV}$, $R_{ON\text{-}HV}$ or leakage current.

Snubbers. This technique includes the approaches based on the use of an auxiliary circuit to suppress the impact of the SJ-FET body-diode on Q_1 [29]-[31]. In general, this kind of approaches increases the number of elements, which is translated into higher cost and more parasites.

Soft-switching. The use of resonant converters mitigates the impact of the SJ-FET body-diode [32]-[34]. However, they add the problems related to the resonant conversion itself, such as the losses caused by the higher RMS currents.

III. Third Quadrant Operation of a SJ-CC

A. Operating States of a SJ-CC in Reverse Conduction (Static Analysis)

Five different states can be identified during the third quadrant operation of a SJ-CC. The operating state depends on the gate-to-source voltage of the LV-FET ($V_{GS\text{-}LV}$), the on-state resistance of the LV-FET ($R_{ON\text{-}LV}$), the threshold voltage of the LV-FET ($V_{Th\text{-}LV}$), the knee-voltage ($V_{\gamma\text{-}LV}$) and the dynamic resistance ($R_{D\text{-}LV}$) of the LV-FET body-diode (D_{LV}), the on-state resistance of the SJ-FET (i.e., $R_{ON\text{-}HV}$), the knee-voltage (i.e., $V_{\gamma\text{-}HV}$) and the dynamic resistance ($R_{D\text{-}HV}$) of the SJ-FET body-diode (i.e., D_{HV}), and the source-to-drain current (i.e., I_{SD}). Fig. 8 shows the basic schematics for each state and the equivalent circuits are depicted in Fig. 9.

State 1 [see Fig. 8(a) and Fig. 9(a)]. The LV-FET is in off-state because $V_{GS\text{-}LV}$ is lower than $V_{Th\text{-}LV}$. Then, I_{SD} flows completely through D_{LV} and, therefore, the source-to-drain voltage of the LV-FET ($V_{SD\text{-}LV}$) can be modeled as:

$$V_{SD-LV} = V_{\gamma-LV} + I_{SD} \cdot R_{D-LV}. \quad (6)$$

Therefore, $V_{GS\text{-}HV}$ is equal to:

$$V_{GS-HV} = V_A + v_{SD-LV}. \quad (7)$$

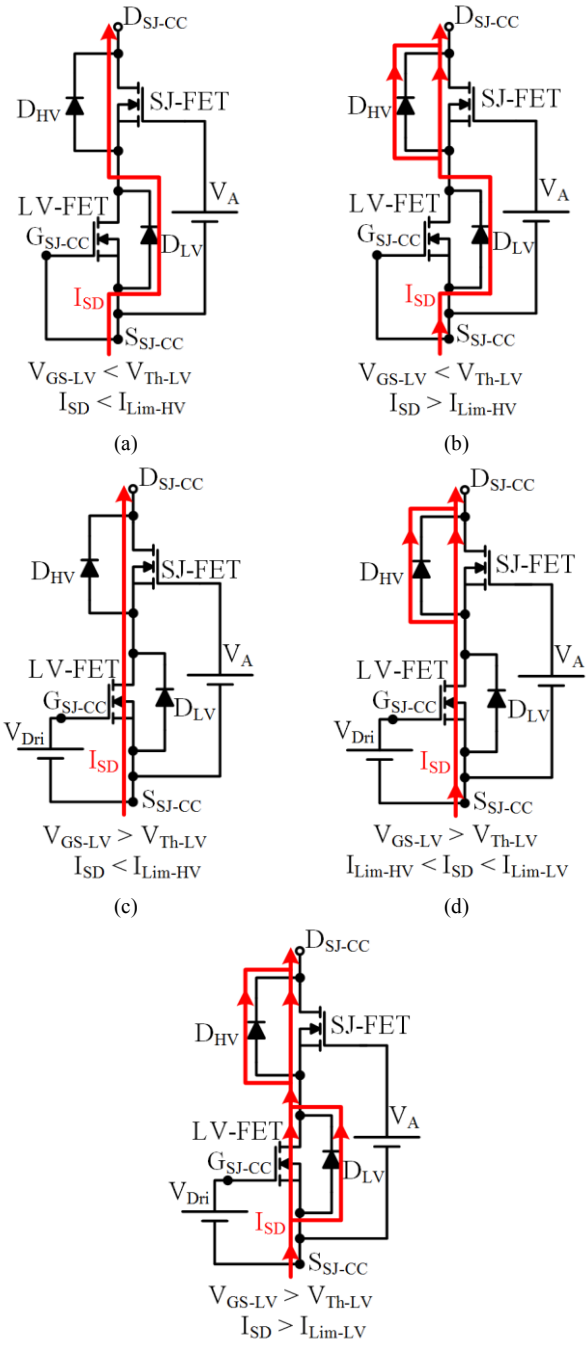


Fig. 8. Basic schematics of the SJ-CC operating in third quadrant: (a) State 1. (b) State 2. (c) State 3. (d) State 4. (e) State 5.

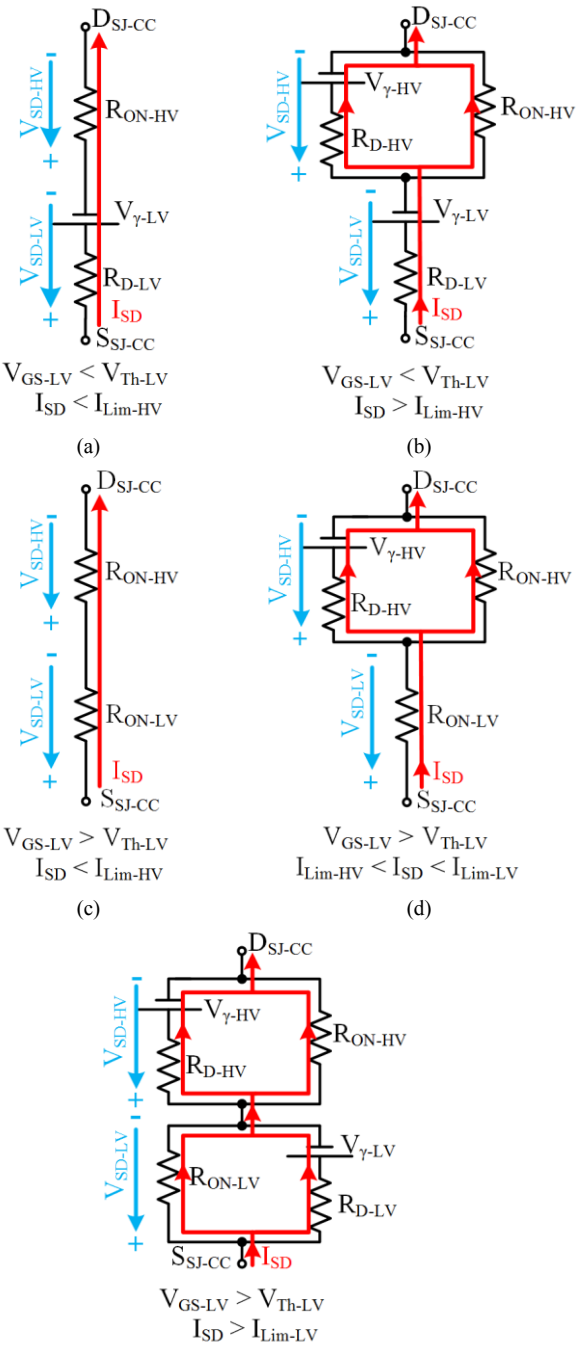


Fig. 9. Equivalent circuits of the SJ-CC operating in third quadrant: (a) State 1. (b) State 2. (c) State 3. (d) State 4. (e) State 5.

V_A should be selected high enough to ensure that $V_{GS\text{-}HV}$ is higher than $V_{Th\text{-}HV}$ under these conditions. In this sense, V_A higher than 10 V is enough to guarantee the desired operation. A suitable approach consists in obtaining V_A from the voltage supply of the LV-FET gate driver (i.e., $V_A = V_{Dri}$). In any case, since $V_{GS\text{-}HV}$ is higher than $V_{Th\text{-}HV}$, the SJ-FET is in on-state and, therefore, the current flows through the channel of the SJ-FET. As in the case of the standalone configuration, D_{HV} can be activated for high I_{SD} values (i.e., $I_{SD} > I_{Lim\text{-}HV}$). However, this state considers that I_{SD} is lower than $I_{Lim\text{-}HV}$ and, consequently, D_{HV} is not activated. Then, equation (4) can be used to model $V_{SD\text{-}HV}$.

State 2 [see Fig. 8(b) and Fig. 9(b)]. As in the previous state, the LV-FET is in off-state because $V_{GS\text{-}LV}$ is lower than $V_{Th\text{-}LV}$ and, consequently, the SJ-FET is in on-state since $V_{GS\text{-}HV}$ is almost equal to V_A. Then, the current flows through D_{LV} and equation (6) is valid to model the voltage drop at the LV-FET. The difference with respect to state 1 is that I_{SD} is higher than $I_{Lim\text{-}HV}$, which causes a current drift through D_{HV}. Under these conditions, the voltage drop at the SJ-FET can be modeled using equation (5).

State 3 [see Fig. 8(c) and Fig. 9(c)]. The LV-FET is in on-state because $V_{GS\text{-}LV}$ is higher than $V_{Th\text{-}LV}$. Then, I_{SD} completely flows through the channel of the LV-FET and $V_{SD\text{-}LV}$ can be

modeled as:

$$V_{SD-LV} = I_{SD} \cdot R_{ON-LV}. \quad (8)$$

As in the previous states, V_{GS-HV} is almost equal to V_A and, therefore, the SJ-FET is in on-sate. State 3 considers that I_{SD} is lower than I_{Lim-HV}. Then, I_{SD} entirely flows through the channel of the SJ-FET and D_{HV} is not activated. Equation (4) is valid to model V_{SD-HV} during this state.

State 4 [see Fig. 8(d) and Fig. 9(d)]. As in the previous state, the LV-FET is in on-state because V_{GS-LV} is higher than V_{Th-LV} and, therefore, the SJ-FET is in on-state since V_{GS-HV} is almost equal to V_A. Then, the current flows through the channel of the LV-FET and equation (8) is valid to model V_{SD-LV}. The difference with respect to state 3 is that I_{SD} is higher than I_{Lim-HV}, which causes a current drift through D_{HV}. Under these conditions, V_{SD-HV} can be modeled according to equation (5).

State 5 [see Fig. 8(e) and Fig. 9(e)]. From a theoretical point of view, an I_{SD} value high enough could impose a current drift through D_{LV} and a fifth state would have to be taken into account when V_{GS-LV} is higher than V_{Th-LV}. However, considering the low R_{ON-LV} value (tens of mΩ), the I_{SD} value required for reaching this state (above 60 A considering current LV-FET technology) makes no sense for the current rating of the SJ-FETs. In any case, this state will be studied next in order to provide a consistent model. Since D_{LV} is activated during this state, the following condition must be satisfied:

$$I_{SD} \cdot R_{ON-LV} > V_{\gamma-LV}. \quad (9)$$

Then, D_{LV} is activated once the following current limit is overcome:

$$I_{Lim-LV} = \frac{V_{\gamma-LV}}{R_{ON-LV}}. \quad (10)$$

Taking into account all the previous statements, equation (5) is valid to model V_{SD-HV} and V_{SD-LV} can be modeled as:

$$V_{SD-LV} = \frac{R_{ON-LV} \cdot R_{D-LV}}{R_{ON-LV} + R_{D-LV}} \left(I_{SD} + \frac{V_{\gamma-LV}}{R_{D-LV}} \right). \quad (11)$$

B. Reverse Recovery of a SJ-CC (Dynamic Analysis)

The RR effect of a SJ-CC takes place when the whole transistor is forced to block voltage after operating in the third quadrant. Continuing with the example of the synchronous boost converter detailed in Section II.B, the RR effect appears after the dead-time between the turn-off of the SJ-CC and the turn-on of the low-side transistor (i.e., transition between the stage 4 and the stage 1 of the synchronous boost converter). Taking into account that V_{GS-LV} is 0 V during dead-times, the RR effect implies that SJ-CC moves from states 1 or 2 to off-state.

As in the standalone configuration, t_{RR}, I_{RRM} and Q_{RR} can be used to evaluate the RR. As Fig. 10 shows, there are four sources of Q_{RR} in the case of the SJ-CC. It can be seen that Q_{RR} considers not only $Q_{RR-D-HV}$ and Q_{OSS-HV}, but also the RR charge of the LV-FET body-diode ($Q_{RR-D-LV}$) and the charge (Q_{OSS-LV}) stored in the output capacitance of the LV-FET (C_{OSS-LV}). It is important to note that the major contribution theoretically would come from $Q_{RR-D-HV}$. However, this contribution can be eliminated or mitigated if the SJ-CC is properly designed according to the current level that is going to drive (i.e., using a SJ-FET with R_{ON-HV} low enough to ensure that v_{SD-HV} never reaches $V_{\gamma-HV}$ for the considered I_{SD}). If the previous condition is satisfied, Q_{OSS-HV} would become the most relevant source of Q_{RR}. Regarding the LV-FET contributions, both $Q_{RR-D-LV}$ and Q_{OSS-LV} have minor impact in comparison to the two first sources of Q_{RR}.

Differently from the standalone configuration, the SJ-CC avoids or mitigates the impact of D_{HV} on the RR (i.e., $Q_{RR-D-HV}$). Basically, if the SJ-CC operates in state 1 during the dead-times, $Q_{RR-D-HV}$ is completely removed by avoiding the activation of D_{HV}. Moreover, if the SJ-CC operates in state 2, $Q_{RR-D-HV}$ will be lower than in the case of the standalone configuration because only a part of the current flows through D_{HV}. Remember that in the case of the standalone configuration, D_{HV} conducts all the current during the dead-times (check state A in Section II.A). This is the key point that explains why the SJ-CC achieves a better third quadrant behavior than the standalone counterpart. It is important to note that although the aforementioned reasoning seems obvious, it has not been previously reported in the literature.

Fig. 11 shows the theoretical current [following equations (1) to (11)] that flows during the dead-times through the channel of a SJ-FET in standalone configuration ($I_{Ch-HV-St}$), through the channel of the same SJ-FET in CC ($I_{Ch-HV-CC}$), through D_{HV} in standalone configuration ($I_{D-HV-St}$) and through D_{HV} in CC ($I_{D-HV-CC}$) versus I_{SD}. As previously explained, all the current flows through D_{HV} regardless the current level in the standalone configuration. In the case of the SJ-CC, the current completely flows through the channel of the SJ-FET when I_{SD} is lower than I_{Lim-HV}. For higher current levels, D_{HV} is activated and the current shared depends on $V_{\gamma-HV}$, R_{D-HV} and R_{ON-HV}, and can be determined by using (4) and (5). Typically, R_{D-HV} is lower than R_{ON-HV} and, consequently, the slope of $I_{D-HV-CC}$ is higher than that of $I_{Ch-HV-CC}$ once I_{Lim-HV} is overcome.

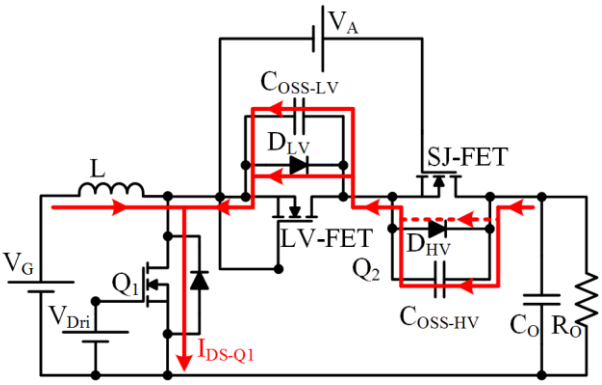


Fig. 10. Current paths for the different charge contributions during the RR of a SJ-CC. The dashed line highlights the possibility of eliminating $Q_{RR-D-HV}$ when the SJ-CC is properly designed.

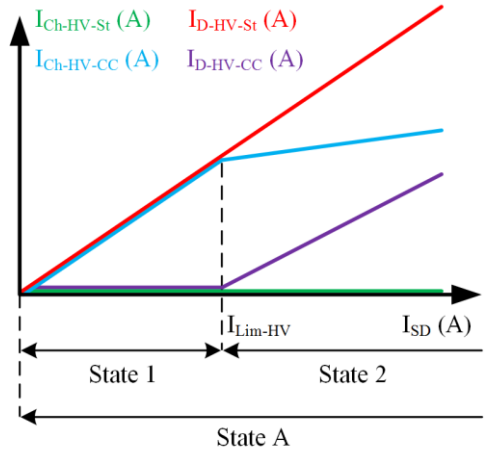


Fig. 11. Theoretical current that flows during the dead-times through the channel of a SJ-FET in standalone configuration ($I_{Ch\text{-}HV\text{-}St}$), through the channel of the same SJ-FET in CC ($I_{Ch\text{-}HV\text{-}CC}$), through D_{HV} in standalone configuration ($I_{D\text{-}HV\text{-}St}$) and through D_{HV} in the CC ($I_{D\text{-}HV\text{-}CC}$) versus I_{SD}.

IV. Experimental Results

Although more than 40 SJ-CCs were implemented combining different SJ-FETs and LV-FETs, the most representative cases will be considered in this paper. As Fig. 1(b) shows, the implementations were made with discrete devices in a plug-in board. It is important to note that SJ-FETs optimized for hard-switching from the major manufactures were used for these implementations. The main electrical parameters of the SJ-FETs and the LV-FETs that will be mentioned along the rest of the paper are summarized in Table I and Table II, respectively. It is important to note that each particular SJ-CC design is identified with two numbers along the rest of the paper. The first number identifies the SJ-FET whereas the second number identifies the LV-FET. For instance, SJ-CC 3-1 implies that the SJ-CC is made up of the SJ-FET 3 and the LV-FET 1.

A. Reverse Conduction Curves of the SJ-CC (Static Analysis)

The SJ-CC reverse conduction model presented in Section III is validated by measuring experimentally the static third quadrant curves of the SJ-CC prototypes. Fig. 12 shows the analytical [following equations (1) to (11)] and the experimental static third quadrant curves of different SJ-CC designs, identifying the operating states with a circle. It is important to note that state 5 cannot be shown because, as previously mentioned, $I_{Lim\text{-}LV}$ cannot be reached due to the current ratings of the SJ-FETs. The designs used in Fig. 12(a) have the same SJ-FET and different LV-FETs. It can be seen that changing the LV-FET has minor impact on the static reverse conduction behavior of the SJ-CC. Note that this does not imply that both designs provide the same dynamic behavior. This point will be studied in Section IV.B. The designs used in Fig. 12(b) have the same LV-FET and different SJ-FETs. In this case, it can be concluded that changing the SJ-FET has major impact on the static reverse conduction behavior of the SJ-CC. It is important to note that static reverse conduction refers to the third quadrant operation of transistors without performing any switching. As Fig. 12(b) shows, $V_{\gamma\text{-}HV}$ is similar in both SJ-

TABLE I. Main Electrical Parameters of the SJ-FETs Used in the Different SJ-CC Prototypes

	BV_{DSS} (V)	$R_{ON\text{-}HV}$ (mΩ)	Q_{GD} (nC)	Q_G (nC)	Q_{OSS}[*1] (nC)
SJ-FET 1	600	178	27	51	124
SJ-FET 2	600	136	22	48	153
SJ-FET 3	650	123	11	35	239

[*1] at V_{DS} = 400 V

TABLE II. Main Electrical Parameters of the LV-FETs Used in the Different SJ-CC Prototypes

	BV_{DSS} (V)	$R_{ON\text{-}LV}$ (mΩ)	Q_{GD} (nC)	Q_G (nC)	Q_{OSS}[*1] (nC)
LV-FET 1	30	8.1	1.7[*1]	5.5[*1]	11[*1]
LV-FET 2	12	7.5	0.76[*2]	3.1[*2]	5.7[*2]
LV-FET 3	30	4.4	1.4[*1]	5.2[*1]	7.2[*1]

[*1] at V_{DS} = 15 V [*2] at V_{DS} = 6 V

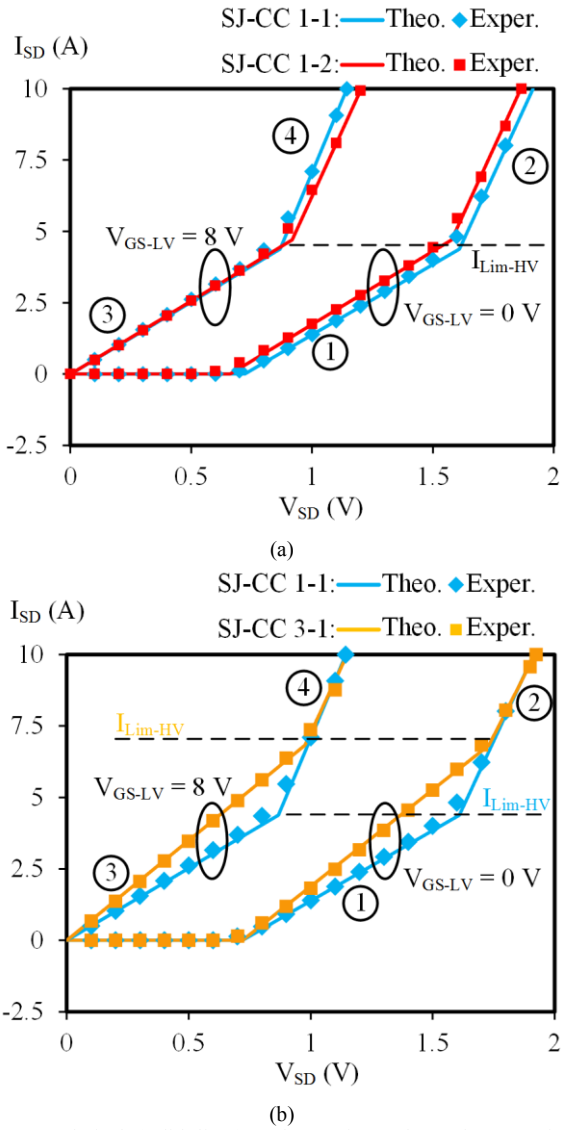


Fig. 12. Analytical (solid lines) and experimental (markers) static third quadrant curves of different SJ-CC designs highlighting the operating states: (a) Two SJ-CC designs with the same SJ-FET and different LV-FETs. (b) Two SJ-CC designs with the same LV-FET and different SJ-FETs.

FETs and, therefore, the SJ-FET voltage drop needed to activate D_{HV} is also similar. For the same I_{SD} level, $V_{SD\text{-}HV}$ is higher in the case of the SJ-CC 1-1 because $R_{ON\text{-}HV}$ is higher, which is translated into a lower $I_{Lim\text{-}HV}$ value. As a result, the SJ-CC 3-1 can address higher current levels without activating D_{HV}.

Finally, Fig. 13 shows the static reverse conduction curves of the same SJ-FET in standalone configuration and in CC with the LV-FET 1. Note that $I_{Lim\text{-}HV}$ is the same in both configurations.

B. Reverse Recovery of a SJ-CC (Dynamic Analysis)

In order to characterize the RR of the SJ-FETs, both in cascode and in standalone configuration, a boost converter is used replacing the power rectifier by a transistor with a short circuit between its gate and its source (see Fig. 14). Except for the Device Under Test (DUT), which can be a SJ-FET in standalone configuration or a SJ-CC, all the components of the boost converter are fixed, including the SJ-FET in standalone configuration that is used as low-side transistor. The switching frequency is 100 kHz and the inductor was designed to ensure a negligible current ripple.

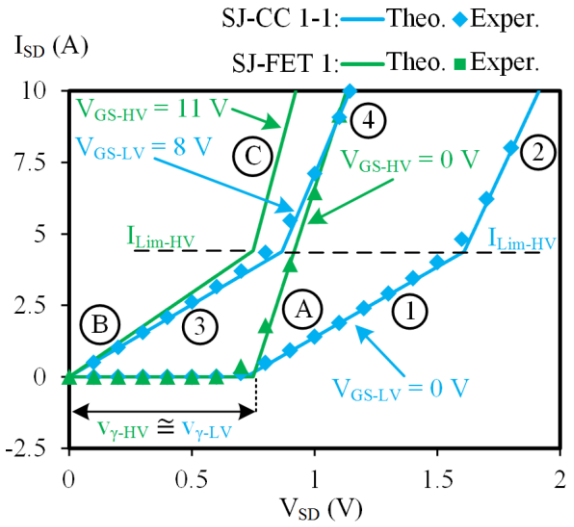


Fig. 13. Analytical (solid lines) and experimental (markers) static third quadrant curves of the SJ-FET 1 in standalone configuration and in CC with the LV-FET 1 highlighting the different operating states.

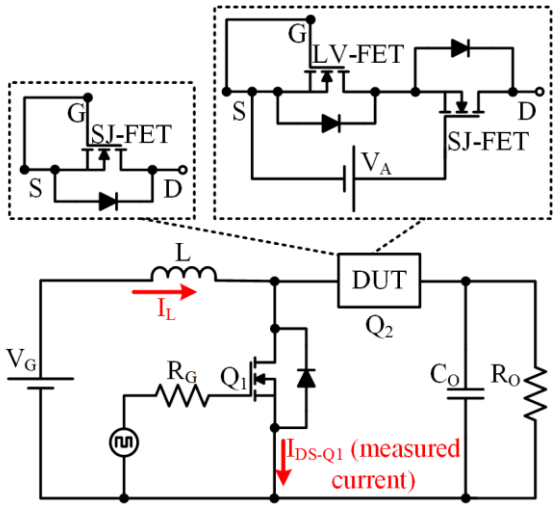


Fig. 14. Schematic of the boost converter used to characterize the RR of the DUT (either SJ-FETs in standalone configuration or SJ-CCs).

The current that flows through the low-side transistor (i.e., $i_{DS\text{-}Q1}$) is measured during the turn-on in order to evaluate t_{RR}, I_{RRM} and Q_{RR}. $di_{DS\text{-}Q1}/dt$ is controlled by the gate resistance of the low-side transistor and it is fixed to 130 A/µs for the RR tests. Note that the input and output voltages are 12.5 V and 50 V, respectively. Therefore, the DUT blocks 50 V during the off-state. Below, it is explained why this value is high enough to characterize the RR of the DUTs even when the used SJ-FETs are able to block voltages up to 600 V. In order to analyze the RR of the DUTs under different conditions, the tests are carried out at three I_L values: 1.2 A, 2.4 A and 6 A. The current waveform are captured in less than one second in order to mitigate the temperature impact. An example is given in Fig. 15, which shows the measured current when a SJ-FET is used either in CC or in standalone configuration. Note that the figure changes the vertical axis subtracting I_L in order to identify the RR in an easily way. This first experimental result shows that the SJ-CC clearly improves the third quadrant dynamic behavior with respect to the standalone counterpart. It can be seen that t_{RR}, I_{RRM} and Q_{RR} are lower in the case of the SJ-CC.

In Section IV.C the comparison between the RR of SJ-CCs and SJ-FETs in standalone configuration is analyzed in detail at different operating conditions. In this section, only the RR of the SJ-CC is characterized, omitting any comparison with other power transistors.

Fig. 16 shows the current waveforms for three SJ-CC designs that have the same LV-FET and different SJ-FETs. According to (3) and as Fig. 12 shows, $I_{Lim\text{-}HV}$ is around 4 A and 6 A for the SJ-CC 1-1 and the SJ-CC 3-1, respectively. Note that $I_{Lim\text{-}HV}$ is around 5.1 A in the case of the SJ-CC 2-1. Therefore, the three SJ-CCs operate in state 1 and the activation of D_{HV} is avoided when the current level is 1.2 A or 2.4 A. As a result, there is no appreciable deterioration of the RR when I_L rises from 1.2 A to 2.4 A. When the current is 6 A, the SJ-CC 1-1 and the SJ-CC 2-1 operate in state 2, whereas the SJ-CC 3-1 operates close to the limit between states 1 and 2. Therefore, the deterioration of the RR in the case of SJ-CC 1-1 and SJ-CC 2-1 at this current level is caused by the activation of D_{HV}.

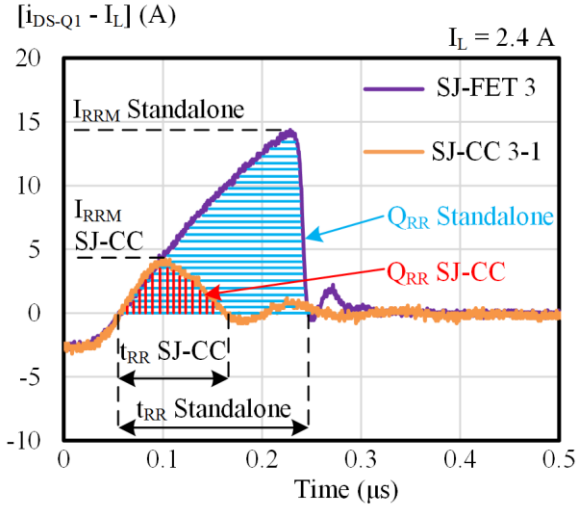
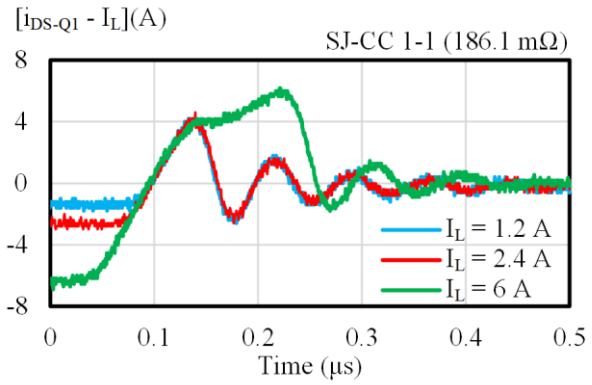
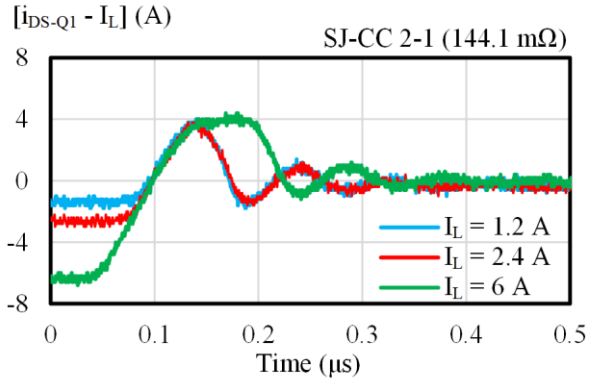


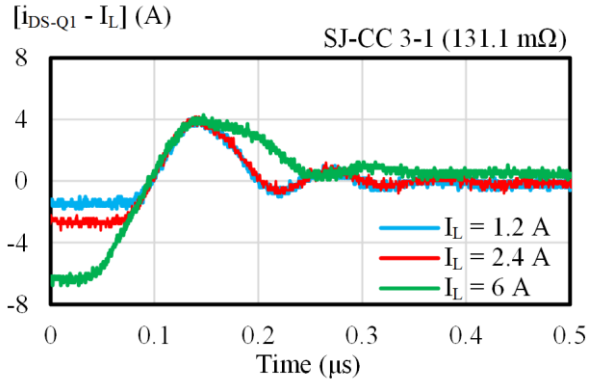
Fig. 15. Experimental comparison between the RR of the SJ-FET 3 in CC with the LV-FET 1 and in standalone configuration when I_L is equal to 2.4 A.



(a)



(b)



(c)

Fig. 16. Measured current waveforms for three SJ-CC designs with the same LV-FET but different SJ-FET: (a) SJ-CC 1-1. (b) SJ-CC 2-1. (c) SJ-CC 3-1.

As previously explained, the SJ-CC eliminates or mitigates $Q_{RR\text{-}D\text{-}HV}$ and, consequently, $Q_{OSS\text{-}HV}$ constitutes the major source of Q_{RR}. In order to demonstrate this statement, the measured Q_{RR} will be compared to $Q_{OSS\text{-}HV}$. It is important to note that $Q_{OSS\text{-}HV}$ is evaluated by measuring experimentally $C_{OSS\text{-}HV}$ of each SJ-FET. Fig. 17 shows and example of the $C_{OSS\text{-}HV}$ and $Q_{OSS\text{-}HV}$ measurement of SJ-FET 3 versus $V_{DS\text{-}HV}$, which will help us to justify both the importance of $Q_{OSS\text{-}HV}$ and the voltage range of the experimental boost converter.

As Fig. 17 shows, $Q_{OSS\text{-}HV}$ rises with $V_{DS\text{-}HV}$ and achieves the 90% of the final value when the voltage is around 20 V. Since the voltage across the LV-FET is close to its breakdown voltage during the off-state [15], fixing 50 V as the output voltage of the boost converter is enough to measure most of the $Q_{OSS\text{-}HV}$ contribution and to characterize the RR of the DUT. Note that

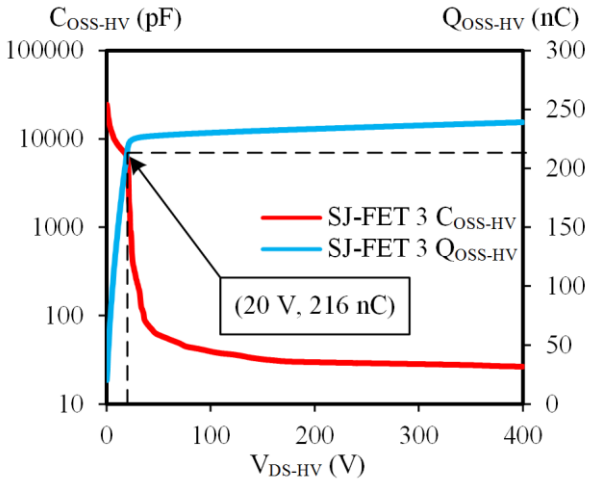


Fig. 17. Measured $C_{OSS\text{-}HV}$ and $Q_{OSS\text{-}HV}$ of the SJ-FET 3 versus $V_{DS\text{-}HV}$. Note that $Q_{OSS\text{-}HV}$ achieves the 90% of its final value at 20 V.

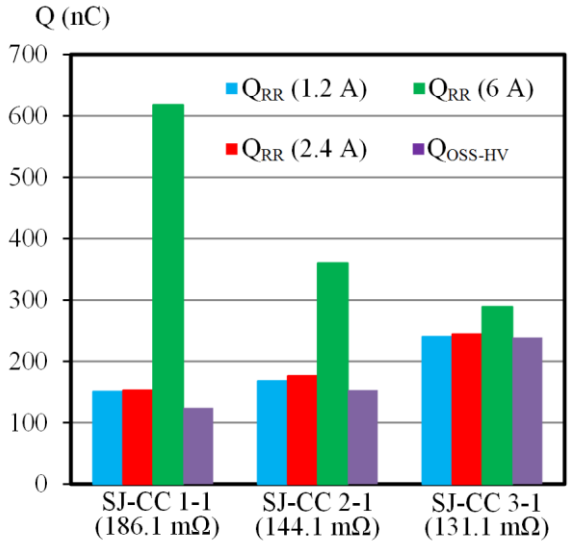


Fig. 18. Q_{RR} measurements for three SJ-CC designs with the same LV-FET and different SJ-FETs.

since the highest breakdown voltage of the LV-FETs considered for the tests is 30 V (see Table II), using 50 V as output voltage ensures that the SJ-FET blocks a voltage equal or higher than 20 V.

Fig. 18 shows the measured Q_{RR} for three SJ-CCs with the same LV-FET (i.e., the SJ-CCs tested in Fig. 16) including the measured $Q_{OSS\text{-}HV}$. It can be seen that the results match with the previous reasoning: the activation of D_{HV} is avoided when the SJ-CC operates in state 1 (i.e., $I_L < I_{Lim\text{-}HV}$) and, consequently, the measured Q_{RR} is slightly higher than $Q_{OSS\text{-}HV}$. On the other hand, Q_{RR} rises when the SJ-CC operates in state 2 (i.e., $I_L > I_{Lim\text{-}HV}$) because D_{HV} conducts a part of I_L. The higher Q_{RR} increase of SJ-CC 1-1 with respect to the Q_{RR} increase of SJ-CC 2-1 in state 2 (i.e., I_L = 6 A) is because D_{HV} of the SJ-FET 1 conducts more current than D_{HV} of SJ-FET 2. Note that $R_{ON\text{-}HV}$ is higher in the case of the SJ-FET 1, which is translated into a higher $V_{SD\text{-}HV}$ value for the same I_L level and, therefore, higher current flowing through D_{HV} (i.e., the D_{HV} of SJ-FET 1 accumulates more charge carriers than that of SJ-FET 2). This reasoning is valid when $V_{\gamma\text{-}HV}$ is equal for both SJ-FET, which

is a good approximation in practice.

As in the case of the static reverse conduction, the dynamic third quadrant operation barely depends on the LV-FET selected for the SJ-CC implementation. Fig. 19 shows the measured current waveforms of three SJ-CC implemented with the same SJ-FET and different LV-FETs when I_L is 2.4 A. This statement is also valid for other current levels.

C. Comparing the RR of SJ-CCs and SJ-FETs in Standalone Configuration

In order to evaluate the RR improvement that could be achieved by the SJ-CC, the RR behavior was also studied for SJ-FETs in standalone configuration. Four groups of transistors are considered for the experimental comparison. The first group contains the previously mentioned SJ-FETs optimized for hard-switching in standalone configuration (i.e., the ones detailed in Table I). The second group is made up of SJ-FETs with enhanced RR (i.e., irradiated SJ-FETs) in standalone configuration. The third group implements a SJ-CC using one of the irradiated SJ-FETs (IRR SJ-FET 1) in CC with the LV-FET 1. Finally, the fourth group contains the SJ-FETs optimized for hard-switching from the first group in CC with the LV-FET 1.

Fig. 20, Fig. 21 and Fig. 22 show the measured Figures-of-Merit (FoM) $R_{ON}{\cdot}t_{RR}$, $R_{ON}{\cdot}I_{RRM}$ and $R_{ON}{\cdot}Q_{RR}$, respectively. The results at 6 A are omitted for the first group due to their too high self-heating in the experimental tests and possible malfunction. As expected, SJ-FETs with enhanced RR provide better results than the SJ-FETs optimized for hard-switching operation. Moreover, it can be seen that all the SJ-CCs overcome the

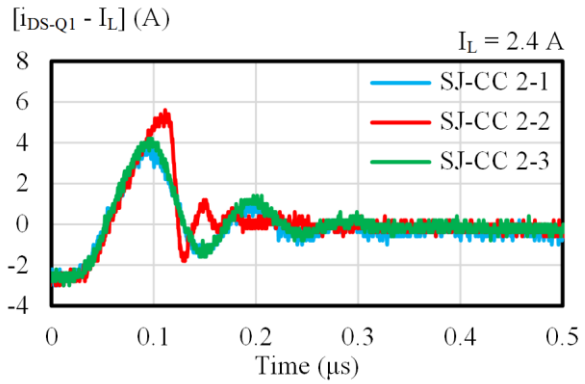


Fig. 19. Measured current waveforms for three SJ-CC designs with the same SJ-FET but different LV-FET when I_L is 2.4 A.

standalone counterparts. In addition, the SJ-CCs achieve similar or better results than the SJ-FETs with enhanced RR.

Although $R_{ON}{\cdot}Q_{RR}$ is the most important FoM since Q_{RR} determines the RR losses, it is important to consider both $R_{ON}{\cdot}t_{RR}$ and $R_{ON}{\cdot}I_{RRM}$ in order to check if the Q_{RR} changes are caused by a t_{RR} change, by a I_{RRM} change or by a change of both parameters. It can be seen that in the cases of the SJ-FETs optimized for hard-switching in standalone configuration and in CC, the rise of Q_{RR} with I_L is caused by the increase of both t_{RR} and I_{RRM}. This reasoning is not valid for the SJ-FETs with enhanced RR in standalone configuration and in CC. In these cases, the increase of Q_{RR} that appears when I_L rises from 1.2 A to 2.4 A is also caused by the increase of both t_{RR} and I_{RRM}. However, since I_{RRM} remains almost constant when I_L rises from 2.4 A to 6 A, the increase of Q_{RR} that appears under this condition is mainly caused by the increase of t_{RR}.

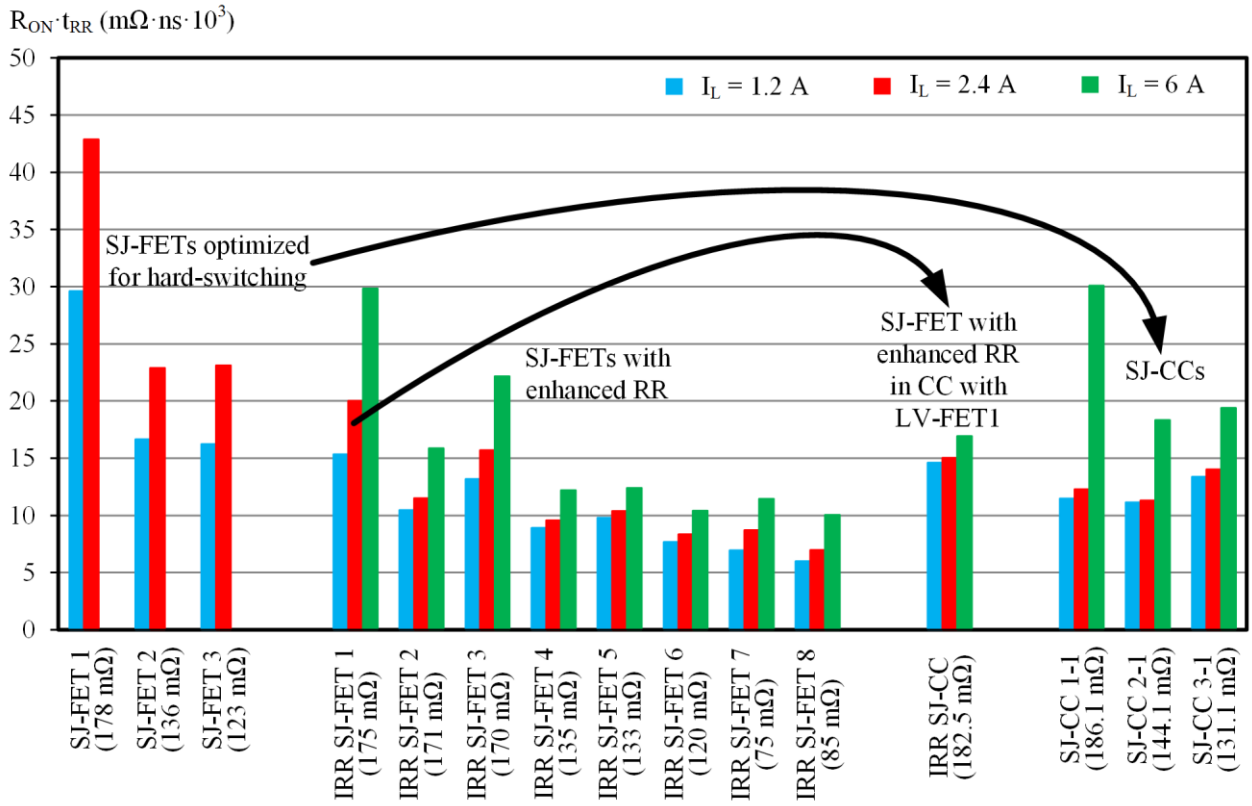


Fig. 20. $R_{ON}{\cdot}t_{RR}$ FoM for different SJ-FET commercial technologies (three major SJ-FET manufacturers included).

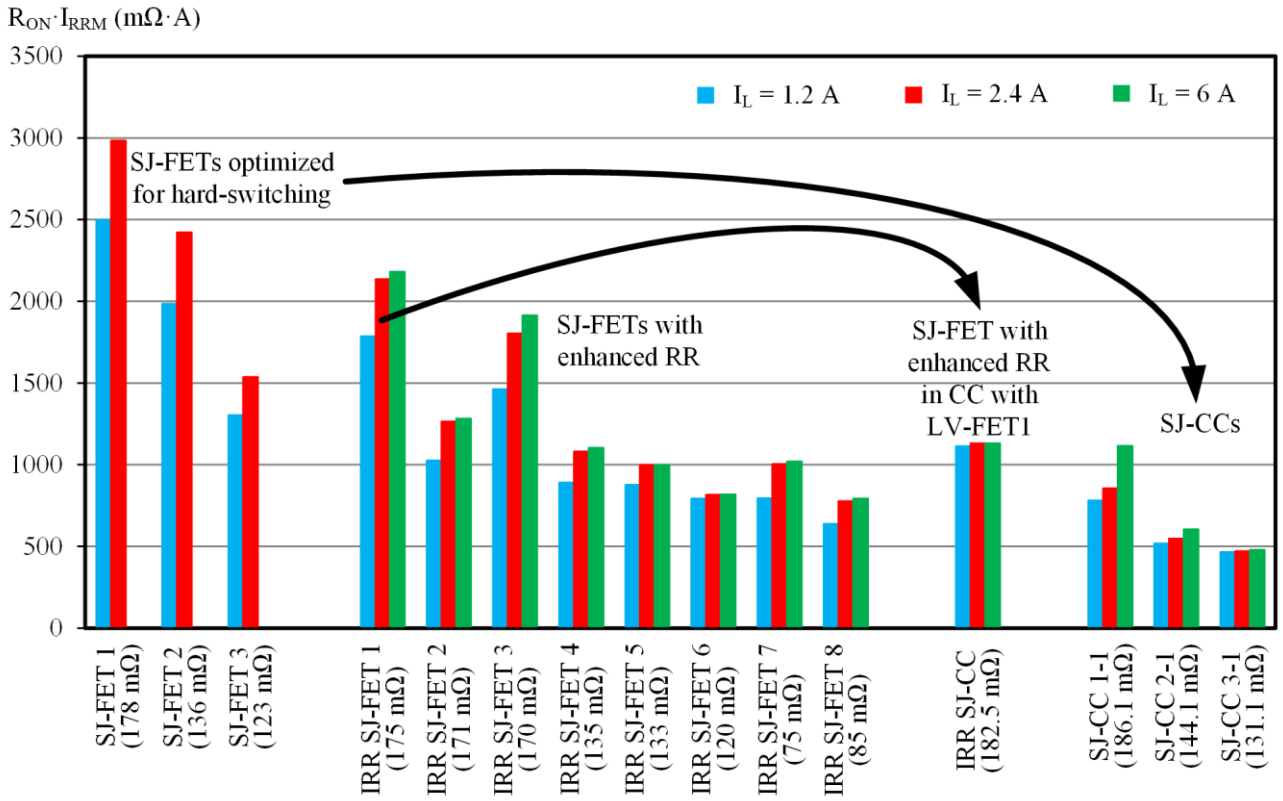


Fig. 21. $R_{ON}{\cdot}I_{RRM}$ FoM for different SJ-FET commercial technologies (three major SJ-FET manufacturers included).

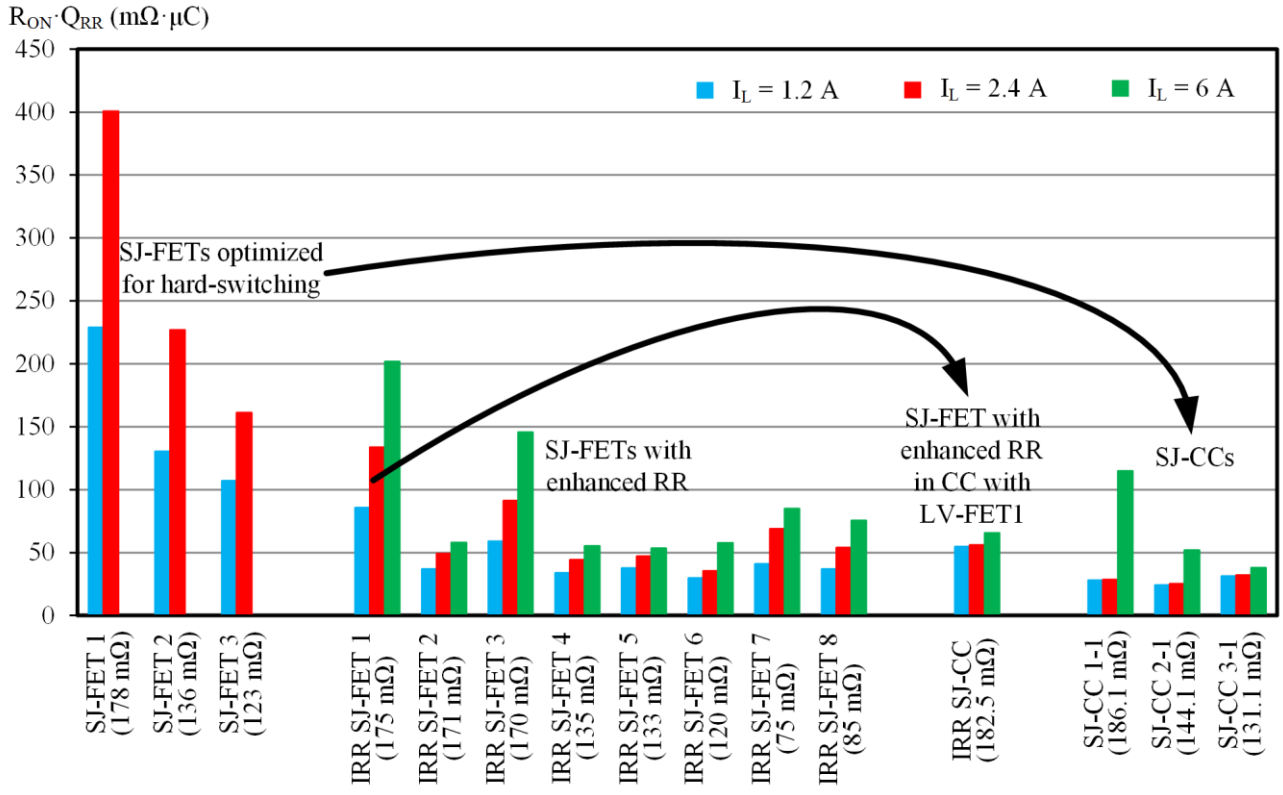


Fig. 22. $R_{ON}{\cdot}Q_{RR}$ FoM for different SJ-FET commercial technologies (three major SJ-FET manufacturers included).

As Fig. 22 shows, the $R_{ON}{\cdot}Q_{RR}$ values provided by the CCs of the fourth group are between four and eight times lower than those of the SJ-FETs from the first group (i.e., the standalone counterparts). Effectively, SJ-CC 1-1 and SJ-CC 2-1 show lower $R_{ON}{\cdot}Q_{RR}$ than any other SJ-FET for 1.2 A and 2.4 A, whereas SJ-CC 3-1 has the best compromise of $R_{ON}{\cdot}Q_{RR}$ in a wider range of current. As previously explained, SJ-CC 3-1 has higher $I_{Lim\text{-}HV}$ than SJ-CC 1-1 and SJ-CC 2-1 due to the lower

$R_{ON\text{-}HV}$ value of SJ-FET 3 with respect to SJ-FET 1 and SJ-FET 2. As a result, SJ-CC 3-1 avoids the D_{HV} activation for almost all the current range of the tests (D_{HV} is slightly activated when $I_L = 6$ A), which explains why it provides the best average result for the considered current range. However, there is a trade-off between parasitic capacitances and $R_{ON\text{-}HV}$ in Superjunction technology: the lower the $R_{ON\text{-}HV}$ value, the higher the parasitic capacitances. As a result, SJ-FET 3 has higher $Q_{OSS\text{-}HV}$ than SJ-FET 1 and SJ-FET 2. Since $Q_{OSS\text{-}HV}$ is the main source of Q_{RR} of the SJ-CCs when I_L = 1.2 A or 2.4 A, SJ-CC 3-1 provides higher $R_{ON}\cdot Q_{RR}$ than SJ-CC 1-1 and SJ-CC 2-1 in this current range.

D. Comparing the RR of SJ-CCs and Other Switch Technologies

The target of this section is to achieve a general vision of the improvement achieved by the SJ-CC comparing it to commercial 600 V switches that are not based on the Superjunction technology. The switches selected for the comparison are wide bandgap devices, which offer great dynamic reverse conduction behavior. In this way, the results achieved by the SJ-CC 3-1 are compared to those of a GaN HEMT in CC (290 mΩ), a normally-off GaN transistor (100 mΩ) and a SiC Schottky diode (dynamic resistance of 110 mΩ).

Fig. 23 shows the measured $R_{ON}\cdot t_{RR}$, $R_{ON}\cdot I_{RRM}$ and $R_{ON}\cdot Q_{RR}$ of the considered power switches. It can be seen that the SiC Schottky diode provides the best results, while the SJ-CC 3-1 provides the worst ones. It is important to highlight that although the normally-off GaN transistor provides lower $R_{ON}\cdot Q_{RR}$ than the GaN-CC, the last one achieves lower $R_{ON}\cdot t_{RR}$. Focusing the attention on the $R_{ON}\cdot Q_{RR}$ results, it can be seen that the SJ-CC 3-1 achieves a results around eight times higher than the GaN-CC.

It can be concluded that although the SJ-CC reduces Q_{RR} with respect to the standalone counterpart by avoiding or mitigating $Q_{RR\text{-}D\text{-}HV}$, the RR caused by the charge stored in the SJ-FET output capacitance (i.e., $Q_{OSS\text{-}HV}$) is so high that achieving the low RR levels of wide bandgap switches is not possible.

V. Conclusions

Although SJ-FETs provide great performance when they operate in the first quadrant and under hard-switching conditions, using them in SR does not offer good results. The reason is that their body-diode provides low performance, and since it is activated during the dead-times, it causes a RR effect that jeopardizes the third quadrant operation. Differently from the standalone configuration, the SJ-CC avoids or mitigates the activation of this body-diode by keeping the SJ-FET in on-state when the transistor operates in the third quadrant. Evaluating the RR in terms of t_{RR}, I_{RRM} and Q_{RR}, enables the comparison of the SJ-CC with SJ-FETs in standalone configuration, GaN-CCs, normally-off GaN transistors and SiC Schottky diodes. The results show that a SJ-CC always improve the third quadrant performance with respect to the same SJ-FET in standalone configuration. Moreover, the results provided by SJ-CCs are similar or better that those of irradiated SJ-FETs in standalone configuration. Focusing the attention on the comparison with the previously mentioned wide bandgap devices, it can be concluded that the SJ-CC provides a $R_{ON}\cdot Q_{RR}$ value around eight times higher than the GaN-CC. Taking into account the good switching behavior that the SJ-CC showed in previous works, this configuration constitutes a power transistor suitable for high switching frequency, high current

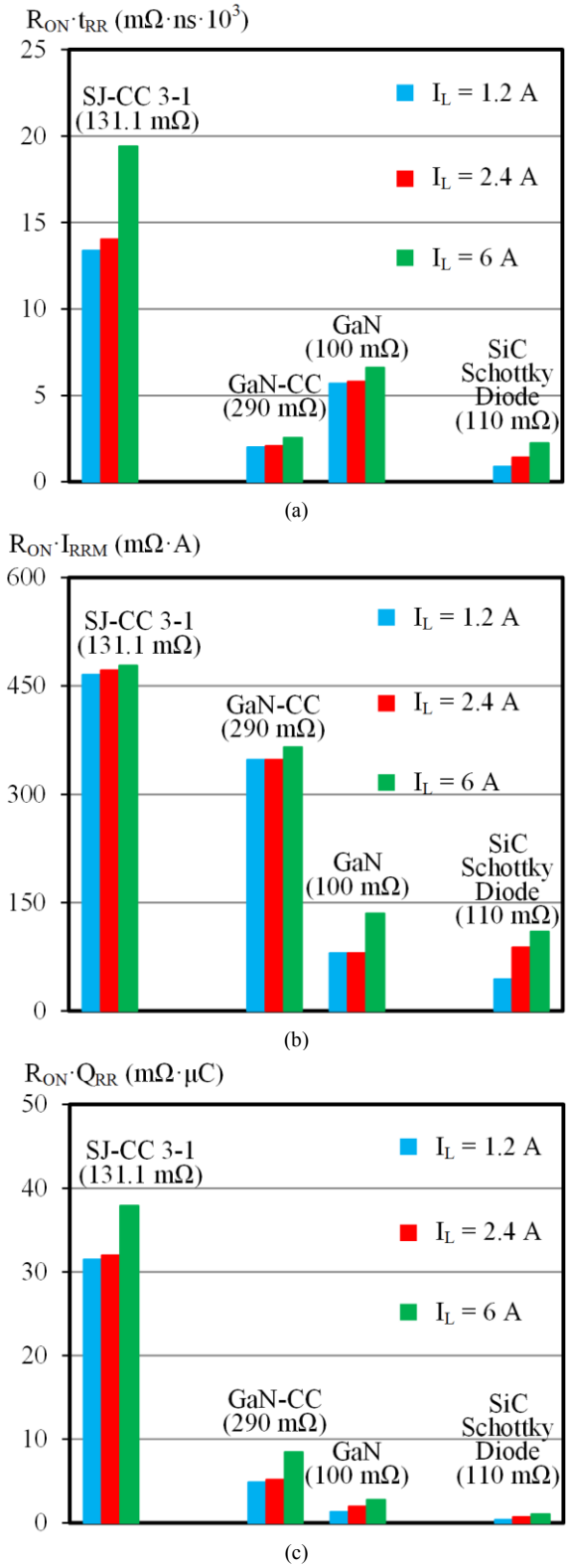


Fig. 23. Comparison between the RR of the SJ-CC 3-1 and switches that are not based on Superjunction technology: (a) $R_{ON}\cdot t_{RR}$. (b) $R_{ON}\cdot I_{RRM}$. (c) $R_{ON}\cdot Q_{RR}$.

and SR that keeps the reliability, the maturity and the good relationship between performance and cost of the SJ-FET technology.

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