A very simple analog control for QSW-ZVS source/sink buck converter with seamless mode transition

Kevin Martin, Aitor Vázquez, Manuel Arias, Javier Sebastián
Electronic Power Supply Systems Group, *University of Oviedo*
Gijón, Spain
martinkevin@uniovi.es

***Abstract*—A simple, analog, control circuit is proposed for seamless transition between source and sink modes in a Quasi-Square-Wave Zero Voltage Switching (QSW-ZVS) source/sink buck converter. The inductor current is controlled by a variable-width hysteretic current mode control. The upper and lower bounds of the hysteretic band are clamped to ensure QSW-ZVS operation with a single current command from the control loop and independently from the power flow direction. This enables the control of any PWM converter able to operate in QSW-ZVS with a single control loop. If the proposed circuit is used, using a complex multi-mode or look-up-table based digital control is no longer required, simplifying the implementation and lowering the cost of the converter. A 50 W buck converter is built to demonstrate the proposed control circuit and experimental measurements are shown to verify its correct operation.**

***Index Terms*—bidirectional control, dc-dc converters, soft switching.**

I. Introduction

The synchronous buck converter is a topology commonly used in point-of-load applications. These kind of applications usually require compact, inexpensive, but efficient solutions. A well-known approach to achieve these objectives is the use of Quasi-Square-Wave (QSW) mode of operation [1], also known as Triangular Current Mode (TCM) [2]. By switching the converter transistors at a variable frequency adapted to the load, Zero Voltage Switching (ZVS) can be achieved [1]–[3]. When a synchronous buck converter is used, it is even possible to obtain ZVS operation for bidirectional power flows [4].

Operating the buck converter in QSW-ZVS has several beneficial effects, making this option more attractive than the traditional fixed frequency implementation for some applications. First of all, the soft switching of both MOSFETs can greatly enhance efficiency by essentially eliminating their turn-on losses. This loss reduction, in turn, allows the designer to increase the switching frequency of the converter. Due to the high inductor current ripple required for the operation in this mode, the inductive value will be smaller than that of a fixed frequency buck converter. Thus, the use of QSW-ZVS could also help reducing the size of the buck output filter, as the magnetic element is usually the largest and heaviest one [5], [6].

Although the principle of operation of QSW-ZVS converters is relatively simple, the implementation of its control requires several sensors and digital control platforms are almost always used, significantly increasing the cost of the converter [2], [7], [8]. The use of digital control also allows the addition of additional safety features, communication and monitoring systems or online reconfiguration of the power converters for applications such as DC-microgrids [9], [10]. However, some of these sensors and complex controls are only required when features such as a fine control of the dead-time [5], [8] or phase-shedding [5] are required, allowing the use of significantly simpler circuitry in cost sensitive applications.

As the use of power converters and electronic loads increase, some applications such as interconnection of automotive DC buses with energy storage systems [7] or DDR (Double Data Rate) Memory terminators [11], require the management of active loads. These active loads can both demand power from the bus or inject current into it, as shown in Fig. 1. The buck converter will be responsible for regulating its output voltage in order to provide a stable bus for any connected load. This kind of converters are usually known as source/sink converters [11], as they can source current to the bus or sink it

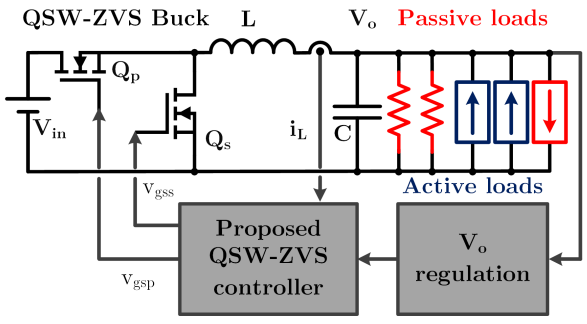

Fig. 1. Output voltage regulated source/sink converter supplying power to active and passive loads.

This work has been supported by the Spanish Government under the project MINECO-13-DPI2013-47176-C2-2-R, the Principality of Asturias under the grant "Severo Ochoa" BP14-085 and the project SV-PA-17-RIS3-4 and by European Regional Development Fund (ERDF) grants.

978-1-5386-5541-2/18/$31.00 ©2018 IEEE

back into the primary power source if the passive load power demand is lower than the power injected by the active loads.

In this work, a simple bidirectional control circuit for the QSW-ZVS synchronous source/sink buck converter is presented. The principle of operation and the controller design are shown in Section II. In Section III, details about the prototype design and experimental results of the proposed solution are presented and the correct operation of the control circuit is verified. Finally, in Section IV, some conclusions are drawn.

II. Description of the Proposed Control Circuit

A. Issues with voltage mode control for bidirectional QSW-ZVS converters

To ensure correct QSW-ZVS operation of a synchronous buck converter, two essential conditions must be met. First, the inductor has to be magnetized during a long enough on time (t_{on}) to ensure its current i_L reaches a peak current (I_{ctrl}) of about twice the desired average output current. Then, the inductor has to be demagnetized until i_L reaches a slightly negative value ($-I_{zvs}$) which is large enough to discharge the MOSFET parasitic capacitor during a small resonant period [3]. This two-event process is then repeated every switching period with the required value of t_{on}.

Due to these conditions, QSW-ZVS operation requires a variable switching frequency. As $-I_{zvs}$ is fixed and has to be reached every switching period, the average output current depends solely on the value of I_{ctrl} given by the control loop. As the inductance is also fixed, I_{ctrl} can only be increased by lowering the switching frequency.

Output voltage control for unidirectional QSW-ZVS converters typically uses a Digital Pulse-Width Modulator (DPWM) and a control loop which defines the t_{on} independently from the inductor current i_L [5]. For a source mode converter, t_{on} can be calculated by the control loop to accurately determine the value of I_{ctrl}. However, as QSW-ZVS operation has inherently variable frequency, it is not possible to calculate the exact switching period. The ZVS Current Detection (ZCD) which ends the switching period can only be estimated by the voltage control and its implementation depends on the measurement of actual switch or inductor currents, as seen in Fig. 2(a). However, when the power flow is reversed and the converter enters sink mode, the control will fail. In this situation, the magnetizing interval of the inductor has to finish when i_L reaches I_{zvs} and not I_{ctrl}. The t_{on} command now conflicts with the ZCD event, while the switching period and the value of I_{ctrl} cannot be controlled, as seen in Fig. 2(b). The traditional control method should be modified when a power flow reversal is detected in order to estimate the switching period. However, this would not guarantee a tight control of the converter output voltage.

B. Control method proposal

It is important to note that correct operation of the QSW-ZVS converter requires keeping the inductor current i_L within an upper and a lower bound. Depending on whether it is in source or sink mode, one of those bounds is fixed and the other one should be provided by the control loop. As the current measurement was already required for traditional QSW-ZVS voltage digital control, it seems appropriate to use a hysteretic current mode control (HCMC) for the analog implementation [12], [13]. HCMC ensures that i_L is always kept within the bounds of the hysteretic band, switching the MOSFETs when it reaches those limits.

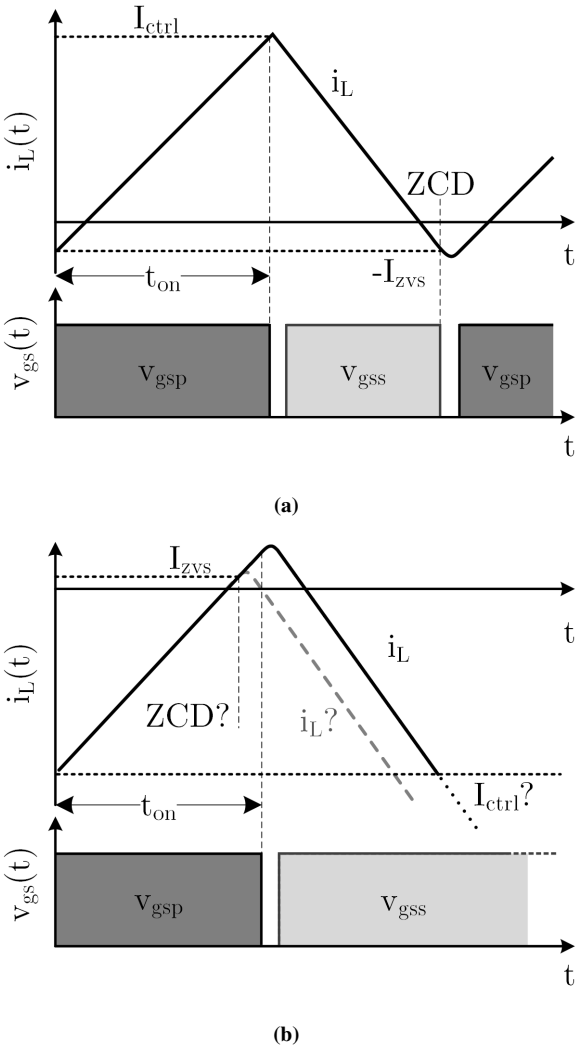

Fig. 2. Inductor current and gate signals for the main switch and the synchronous rectifier of a QSW-ZVS buck converter with traditional voltage mode control: (a) forward power flow (source mode) (b) inverted power flow (sink mode).

However, traditional HCMC has a fixed-width hysteretic band, which is unsuitable for this application. Using fixed bounds does not ensure that the current i_L reaches $\pm I_{zvs}$ and the transistors achieve ZVS. For proper QSW-ZVS operation, the hysteretic band width has to adjust to keep the current between I_{ctrl} and $-I_{zvs}$ for forward power flow (source mode) and between I_{zvs} and a negative I_{ctrl} for inverted power flow (sink mode).

Variable-width HCMC has been previously implemented on a digital control platform [7], [13]. The variable-width band is generated by adding and subtracting half the band width

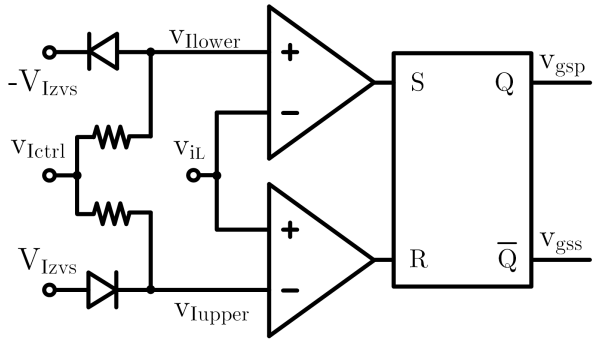

Fig. 3. Proposed implementation of the variable-width HCMC analog controller.

to the control value to generate the upper and lower bounds which are fed to the comparators. As this is not simple to implement with analog circuitry, a totally different approach is taken. For unidirectional power flow, operating in source mode, $-I_{zvs}$ could be used as the lower, fixed bound, while I_{ctrl} acts as the upper, controllable bound which allows a variable width of the hysteretic band. If I_{ctrl} is directly provided by the control loop, there is no need to implement analog adders, greatly simplifying the circuit. However, when I_{ctrl} becomes negative and the power flow has to be inverted, I_{zvs} has to be used as the upper, fixed bound while I_{ctrl} is the new lower, controllable bound.

In order to allow bidirectional power flow, the circuit shown in Fig. 3 is used. It is important to note that this circuit is implemented with the scaled voltages provided by the current sensor and the control loop and not the actual currents:

- v_{IL} is the measurement of the inductor current i_L provided by the current sensor.
- v_{Ictrl} is the desired peak or valley value of i_L, which is determined by the control loop.
- V_{Izvs} and $-V_{Izvs}$ fix the resonant current required for the operation in QSW-ZVS mode, scaled to match the current sensor gain.
- v_{Iupper} and v_{Ilower} determine the upper and lower bounds of the hysteretic band and depend on v_{Ictrl}, V_{Izvs} and $-V_{Izvs}$.

The latch generates the gate signals v_{gsp} and v_{gss} based on two events: Set and Reset. At the beginning of each switching cycle, the latch is set by the comparator, changing the value of v_{gsp} from a logic '0' to a logic '1'. The main switch of the buck converter is then on, magnetizing the inductor. When the measured v_{IL} reaches the upper bound (i.e. $v_{Iupper} = \max\{v_{Ictrl}, V_{Izvs}\}$), the latch is reset. The main switch is then turned off, the synchronous rectifier is turned on and the inductor is demagnetized. When v_{IL} reaches the lower bound (i.e. $v_{Ilower} = \min\{v_{Ictrl}, -V_{Izvs}\}$), the latch is set and a new switching cycle starts.

During the start up of the converter, v_{IL} is zero and cannot trigger any Set nor Reset events. In order to ensure the first switching cycle actually starts and the inductor is magnetized, the Q output of the latch should have a default value of '1'.

Using the proposed circuit, there are three possible scenarios. When v_{Ictrl} is greater than V_{Izvs}, the average inductor current is positive, power flows from input to output and the converter operates in source mode (see Fig. 4(a)). If I_{ctrl} becomes smaller than $-V_{Izvs}$, the average inductor current is then negative, the power flow is reversed and the converter sinks current (see Fig. 4(b)). If v_{Ictrl} takes a value between V_{Izvs} and $-V_{Izvs}$, the command provided by the control loop is ignored due to the clamping. In this situation, no net power is transferred in any direction and the converter operates at its maximum switching frequency, which depends on V_{Izvs}, $-V_{Izvs}$ and the inductor value.

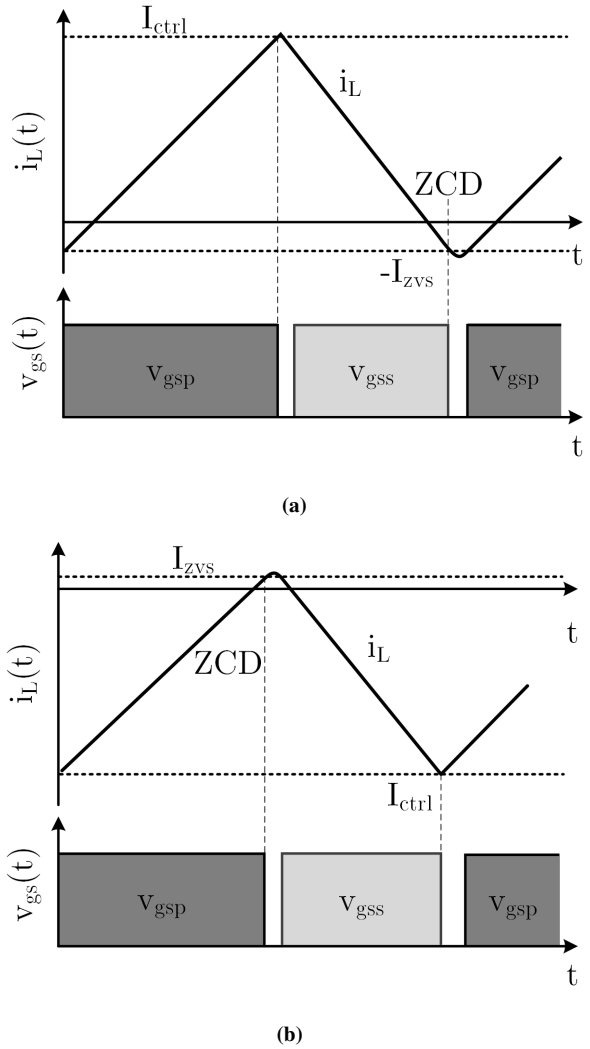

Fig. 4. Inductor current and gate signals of a QSW-ZVS buck converter with variable-width HCMC control: (a) source mode (b) sink mode.

The value of v_{Ictrl} will typically be determined by a control loop. Although this work is based on the control of the output voltage, the circuit shown in Fig. 3 can be applied to control any electrical variable of the power converter, such as the input voltage or the average output current.

Using just the simple circuit shown in Fig. 3 is not enough to properly control the MOSFETs of the converter. The signals v_{gsp} and v_{gss} provided by the latch outputs are complementary with extremely short rise and fall times. An appropriate MOSFET driver should be used to ensure that the dead-time between

these control signals is long enough to achieve ZVS as well as ensuring that the MOSFET are driven with a high enough current. The length of these dead-times can be either fixed [3] or adaptive [8], the later being more efficient but significantly more complex and costly to implement.

Finally, while this controller has been proposed for a buck converter, it is also suitable for different topologies capable of operating in QSW-ZVS. The circuit shown in Fig. 3 could be applied without any modification to, for example, a boost converter. However, it is important to identify which of the MOSFET is responsible for the magnetizing of the inductor to apply the signal v_{gsp} to its gate and to control the synchronous rectifier with v_{gss}. This controller can also be used for unidirectional converters if v_{Ictrl} is not allowed to become negative and its clamping to V_{Izvs} is removed.

III. Experimental results

A 48 V to 24 V, ±50 W synchronous buck converter is designed and built to demonstrate the correct operation of the proposed control circuit. The design of the power stage follows the traditional procedure described in the literature and the main parameters of the prototype shown in Fig. 5 are detailed on Table I. The control circuit presented in the previous section is used and a type II output voltage regulator is used to provide the control command v_{Ictrl}.

A. Synchronous buck converter design

A pair of Toshiba TPH7R006PL MOSFETs were chosen for this prototype for their relatively low price and size, their low on resistance and an equivalent output capacitor of just 302 pF [14]. With an inductor value of 69.6 µH, the converter can operate with ZVS with a I_{zvs} of roughly 150 mA.

In this kind of controls, it is critical to have an accurate, noise-free current measurement in order to ensure the tight control of the output voltage and the correct operation in QSW-ZVS of the converter. The implementation of the current sensor becomes a key design aspect, which will mostly impact

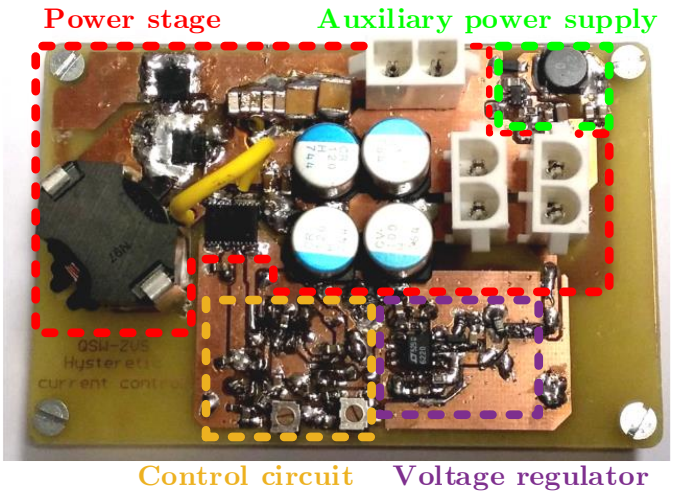

Fig. 5. Prototype of the QSW-ZVS source/sink buck converter with the variable-width HCMC analog controller.

TABLE I
Main design parameters of the QSW-ZVS source/sink buck converter.

Parameter	Value
Input voltage V_i (V)	48
Output voltage V_o (V)	24
Min. switching frequency f_{smin} (kHz)	40
Max. output power (W)	±50
Inductance L (µH)	69.6
Output capacitor C (µF)	445
Input capacitor C_i (µF)	42.0
MOSFETs	TPH7R006PL
Magnetic core	RM8
Magnetic material	N97
Number of turns	17
Full load losses (W)	1.2
Full load efficiency (%)	97.6

the cost and the size of the control system. For this work, a CQ-3200 Hall effect current sensor [15] is chosen due to three main reasons. First, it is simple to use and requires no additional circuitry, reducing the part count and volume of the converter. The chosen model also provides a measurement offset, which simplifies the sensing of bidirectional current and removes the need for symetrical supply voltages across the whole control circuit. Finally, this sensor has a bandwidth of 1 MHz, which is enough to reproduce the triangular inductor current i_L.

However, it is important to note that the limited bandwidth of the current sensor will slightly clip the peak and valley measurements. This clipping is more significant for larger values of i_L and should be accounted for when setting the clamping voltages for I_{zvs} and -I_{zvs}. In this prototype, potentiometers are used to compensate the clipping and ensure that the converter is always able to reach the peak or valley current to operate in QSW-ZVS regardless of the sensor effect. If the whole control circuit proposed in this paper was to be implemented in a single integrated circuit, it would be desirable to use an embedded current sensor with a very high bandwidth or to implement some mechanism which dynamically adapts the clamping values based on the processed power levels.

The control is implemented with a simple type II regulator. It is designed with a relatively small bandwidth and phase margin to clearly show its effect in the measurements.

B. Experimental measurements

The prototype shown in Fig. 5 is tested to verify the correct behavior of the proposed control circuit in both static and dynamic operation, as well as the ability to control the output voltage when the power flow through the converter is reversed.

For the results shown in Fig. 6 the converter operates in steady state while processing 50 W in source mode. The scope snapshots show the gate to source voltage v_{gsp} which controls the main MOSFET of the buck converter in yellow (CH1), the output voltage V_o in green (CH2), the drain to source voltage of the main MOSFET v_{dsp} in purple (CH3) and the actual i_L measured with a current probe in magenta (CH4).

In Fig. 6(a) it can be seen how i_L closely matches the expected waveform when operating at full load. With an

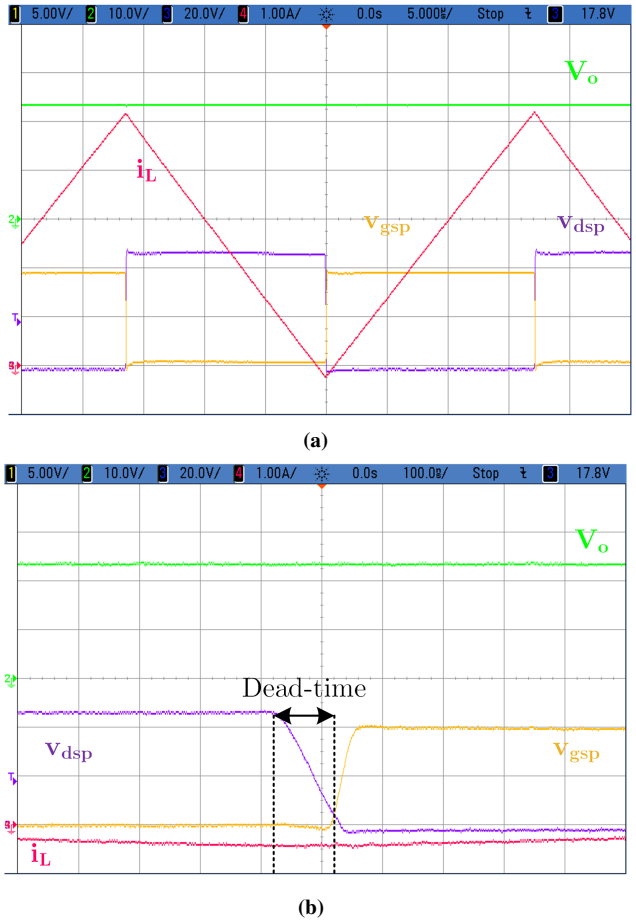

Fig. 6. Static operation of the QSW-ZVS source/sink buck converter: (a) source mode at full load (b) detail of the main switch turn on.

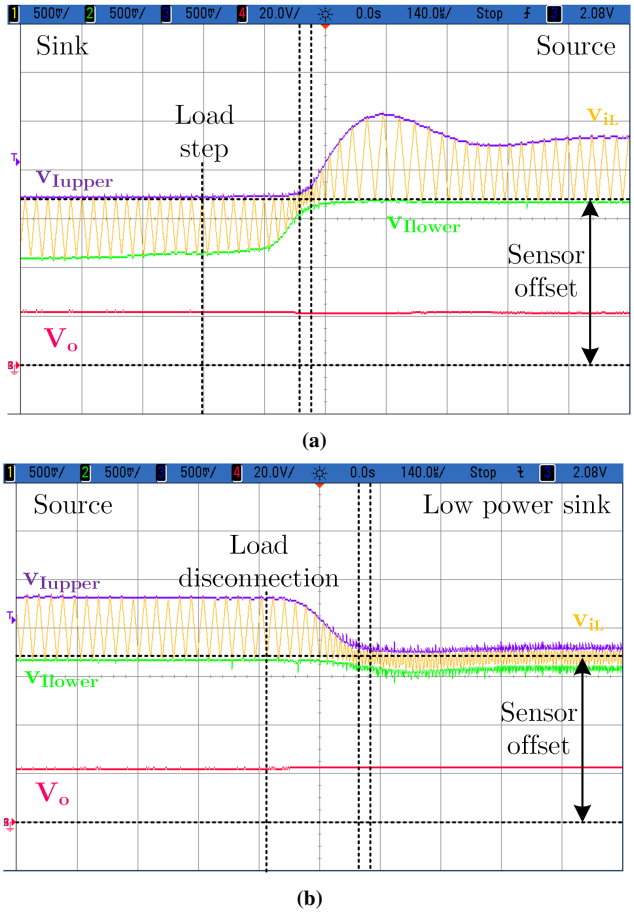

Fig. 7. Dynamic behavior of the QSW-ZVS source/sink buck converter: (a) load step from $-50\,\mathrm{W}$ (sink) to $50\,\mathrm{W}$ (source) (b) load step from $50\,\mathrm{W}$ (source) to $0\,\mathrm{W}$

output current of $2.08\,\mathrm{A}$, the maximum value of i_L is slightly above $4\,\mathrm{A}$ and its minimum is about $-200\,\mathrm{mA}$. Due to the manual adjustment required with this implementation, the exact desired value of $-I_{zvs}$ is not reached and the switching frequency is close to but slightly lower than the expected $40\,\mathrm{kHz}$. However, this does not significantly affect the correct operation in QSW-ZVS and the measured efficiency in this operating point is $97.5\,\%$.

Fig. 6 shows a close-up of the relevant waveforms during the main MOSFET turn-on. It can be clearly seen how, during the dead-time, i_L is negative, discharging the output capacitance of the MOSFET before its gate signal rises. Due to the fixed length of the dead-times and how difficult it is to precisely adjust the value of $-V_{Izvs}$ with the potentiometer, full ZVS is not achieved and the MOSFET is turned on with its output capacitor still charged to a little voltage under $5\,\mathrm{V}$. Although the converter operates in a partial half switching condition, the increase in losses can be neglected. In order to ensure the converter operates exactly in QSW-ZVS mode, a slightly larger dead-time or an additional circuit to ensure soft switching is always achieved should be used.

Fig. 7 shows two different scenarios of dynamic operation where the prototype was tested. The experimental results show the i_L measured by the Hall sensor in yellow (CH1), the lower bound of the hysteretic band I_{lower} in green (CH2), the upper bound of the hysteretic band I_{upper} in purple (CH3), and the output voltage V_o in magenta (CH4). The zero reference is the same for all four channels. It must be noted that channels 1 to 3 have an offset of $1.65\,\mathrm{V}$ due to the current sensor, which is indicated in Fig. 7. It should be noted that, for these figures, the value of I_{zvs} and $-I_{zvs}$ in these tests is slightly higher than required to clearly show the hysteresis band during zero power operation.

Fig. 7(a) shows a load step from $-50\,\mathrm{W}$ to $50\,\mathrm{W}$. The three different operation modes the converter goes through are highlighted. First, the converter operates in sink mode and the average inductor current is negative. Its upper bound is V_{Izvs} and its lower bound is v_{Ictrl}. Shortly after the load step, v_{Ictrl} increases, reducing the width of the hysteresis band and the inductor current valley. For a few switching cycles when v_{Ictrl} approaches zero, the hysteresis band is defined by V_{Izvs} and $-V_{Izvs}$. During this time, the switching frequency is maximum and there is no net power transfer in any direction. As v_{Ictrl} continues increasing, it goes over V_{Izvs} and keeps enlarging the width of the hysteresis band, increasing the inductor current peak to enter source mode and provide the required current to the loads. A small overshot can be seen in v_{Iupper} as the implemented control loop provides a relatively small phase

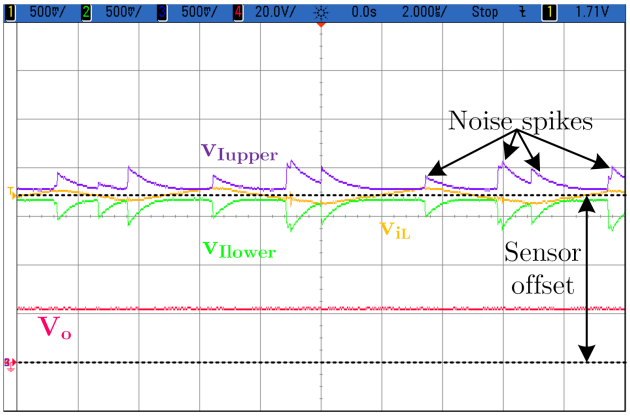

Fig. 8. Static operation of the QSW-ZVS source/sink buck converter at 0 W, showing the control commands.

margin, close to 55°. Although the control loop is relatively slow to clearly show the transition, it can be seen how V_o does not change significantly.

Fig. 7(b) shows a load step from 50 W to 0 W, as the passive load is disconnected. The converter goes through three operation modes again. First, the converter operates in source mode with positive average inductor current. Shortly after the load step, v_{Ictrl} decreases, and for a few switching cycles there is no net power transfer in any direction. However, the control loop has to correct the output voltage offset caused by the load step and the converter operates in sink mode transferring a very low current from its output capacitor to the power source.

Finally, Fig. 8 shows the steady state operation of the converter with an open circuit at its output, processing 0 W. Although the output voltage is correctly regulated and the inductor current is well within bounds, it can be seen how this implementation, as most current based controls, is noise sensitive. While the current measurement is rather clean, both v_{Ilower} and v_{Iupper} pick up switching frequency noise. Integration of the control on a single IC could mitigate this issue.

IV. Conclusion

In this work, a simple, analog, control circuit for a QSW-ZVS source/sink converter has been presented and its principle of operation has been demonstrated with experimental results. While the proposed control circuit offers basic functionality, it can be used as a core building block for enhanced implementations including features such as variable dead-times or additional control loops (e.g. voltage droop control or current limiting).

The quality of the current sensor chosen for this application plays a critical role in the implementation of the control circuit. Using a high-bandwidth, highly linear current sensor can significantly simplify the need for additional circuitry which compensates the distortion of the measured inductor current. Additionally, if the sensor adds a measurement offset, the control circuit can be implemented with asymmetrical supply voltages and the auxiliary power supplies are greatly simplified.

While this work is focused on the seamless source-sink and sink-source transitions in a QSW-ZVS buck converter, the proposed circuit could be easily adapted to apply variable-width HCMC to any PWM topology which can operate in QSW and can be used in unidirectional applications. Due to the control circuit focusing on the magnetizing and demagnetizing of the inductor current, it is possible to use the same conditions for the Set and Reset events and simply choose the appropriate MOSFETs to drive with the v_{gsp} and v_{gss} signals.

References

[1] V. Vorperian, "Quasi-square-wave converters: topologies and analysis," *IEEE Transactions on Power Electronics*, vol. 3, no. 2, pp. 183–191, Apr. 1988.

[2] C. Marxgut, J. Biela, and J. W. Kolar, "Interleaved triangular current mode (TCM) resonant transition, single phase PFC rectifier with high efficiency and high power density," in *Proc. Int. Power Electronics Conf. - ECCE ASIA -*, Jun. 2010, pp. 1725–1732.

[3] D. Maksimovic, "Design of the zero-voltage-switching quasi-square-wave resonant switch," in *Proc. 24th Annual IEEE Power Electronics Specialists Conf. PESC '93 Record*, Jun. 1993, pp. 323–329.

[4] B. Ray and A. Romney-Diaz, "Constant frequency resonant topologies for bidirectional DC/DC power conversion," in *Proc. 24th Annual IEEE Power Electronics Specialists Conf. PESC '93 Record*, Jun. 1993, pp. 1031–1037.

[5] A. Vazquez, A. Rodriguez, D. G. Lamar, and M. M. Hernando, "Master-slave technique for improving the efficiency of interleaved synchronous boost converters," in *Proc. IEEE 15th Workshop Control and Modeling for Power Electronics (COMPEL)*, Jun. 2014.

[6] S. Ćuk. (2017, Apr.) Step-down dc-dc converter eliminates ferrite cores at 50kHz enabling power supply on chip with one-cycle transient. Website. Power Electronics - Informa USA Inc. [Online]. Available: http://www.powerelectronics.com/power-management/step-down-dc-dc-converter-eliminates-ferrite-cores-50khz-enabling-power-supply-chip

[7] P. Scortaru, D. V. Nicolae, M. Cernat, and Z. Puklus, "Reversible DC-to-DC converter for a dual voltage automotive system using zero voltage switching technique," in *Proc. 11th Int. Conf. Optimization of Electrical and Electronic Equipment*, May 2008.

[8] S. Chen, O. Trescases, and W. T. Ng, "Fast dead-time locked loops for a high-efficiency microprocessor-load ZVS-QSW DC/DC converter," in *Proc. IEEE Conf. Electron Devices and Solid-State Circuits*, Dec. 2003, pp. 391–394.

[9] J. M. Guerrero, J. C. Vasquez, J. Matas, L. G. de Vicuna, and M. Castilla, "Hierarchical control of droop-controlled AC and DC microgrids — a general approach toward standardization," *IEEE Transactions on Industrial Electronics*, vol. 58, no. 1, Jan. 2011.

[10] M. Rodriguez, G. Stahl, L. Corradini, and D. Maksimovic, "Smart DC power management system based on software-configurable power modules," *IEEE Transactions on Power Electronics*, vol. 28, no. 4, pp. 1571–1586, Apr. 2013.

[11] R. Kollman, J. Betten, and B. S. Lee, "Power supply solution for DDR bus termination," *Analog Applications*, 2001.

[12] R. Redl and N. O. Sokal, "Current-mode control, five different types, used with the three basic classes of power converters: Small-signal AC and large-signal DC characterization, stability requirements, and implementation of practical circuits," in *Proc. IEEE Power Electronics Specialists Conf*, Jun. 1985, pp. 771–785.

[13] Y. Wen and O. Trescases, "Analysis and comparison of frequency stabilization loops in self-oscillating current mode DC –DC converters," *IEEE Transactions on Power Electronics*, vol. 28, no. 10, pp. 4753–4766, Oct. 2013.

[14] D. Costinett, D. Maksimovic, and R. Zane, "Circuit-oriented treatment of nonlinear capacitances in switched-mode power supplies," *IEEE Transactions on Power Electronics*, vol. 30, no. 2, pp. 985–995, Feb. 2015.

[15] Asahi Kasei, "CQ-3200 High-speed response coreless current sensor datasheet," Asahi Kasei, Datasheet, 2016.