

Advanced control techniques to improve the efficiency of IPOP modular QSW-ZVS converters

Aitor Vazquez, *Member, IEEE*, Alberto Rodriguez, *Member, IEEE*, Diego G. Lamar, *Member, IEEE*, and Marta M. Hernando, *Senior Member, IEEE*.

Abstract--Quasi-Square Wave mode with Zero Voltage Switching (QSW-ZVS) is an operation mode in which the switching losses can be minimized. However, a large inductance current ripple is needed in this mode, which limits the maximum attainable power of the topology. A possible way to increase the power managed by a QSW-ZVS mode converter is to use a modular converter. An Input Parallel Output Parallel (IPOP) arrangement, in which the current can be shared among the modules, can increase the total power proportionally to the number of modules. This paper addresses two main proposals. The first one is a master-slave technique to extend the QSW-ZVS mode to an IPOP modular converter, achieving an interleaved solution which minimizes the total input current ripple and assures the current balance among the modules. The second one is a comparison of four different control techniques applied to the IPOP modular converter to improve the overall efficiency at light to medium load: balanced master-slave technique, master-slave with phase-shedding, asymmetrical master-slave and burst mode (or hysteretic control). These four strategies are theoretically analyzed, experimentally validated and compared using a 150V to 400V 2kW modular IPOP prototype made up of four synchronous boost converter operating in QSW-ZVS mode.

Index Terms—Control techniques, DC-DC power conversion, IPOP, modular converters, QSW-ZVS.

I. INTRODUCTION

ENERGY management is one of the well-established topics in today's concerns related to power electronics. Energy recovery systems [1]-[4], energy storage systems [5]-[9], renewable energies and zero emissions buildings [10]-[12], DC distribution grids and smart grids [12]-[16] are good examples of this topic. In these applications, an energy storage device is present in the power architecture, so a bidirectional DC-DC power converter is needed to manage it. Furthermore, DC-DC power converters are traditionally designed to achieve the highest efficiency when they work at full power. However, in the previously stated applications converter efficiency at intermediate and low power levels is actually more important due to the charge and discharge process of the energy storage element. Therefore, a bidirectional DC-DC converter with a high efficiency at medium and light load is required in these applications.

This work was supported by the Spanish Government under projects MINECO-13-DPI2013-47176-C2-2-R and MINECO-15-DPI2014-56358-JIN, through funding from the Government of Asturias through the project FC-15-GRUPIN14-143 and FEDER funds.

The authors are with University of Oviedo, Electronic Power Supply Systems group, Edificio 3, Campus de Viesques s/n, 33204 Gijón, SPAIN (e-mail: vazquezaitor@uniovi.es).

The simplest bidirectional DC-DC power converter is the synchronous boost or buck converter [17], shown in Fig. 1. This topology is suitable for applications in which input and output voltages are close to each other and no galvanic isolation is needed for safety reasons. This converter can operate into different operation modes, as it is widely known. Continuous Conduction Mode (CCM) with a large inductance value allows to work with a small inductor current ripple, which is desirable for energy storage systems. However, the switching losses are dominant in this mode and might limit its performance in terms of the switching frequency (i.e. low power density) or total power. Quasi-Square Wave Mode with Zero Voltage Switching (QSW-ZVS), also known as Triangular Current Mode (TCM) is another operation mode which can be applied to this converter if the inductance value is reduced [18]. In this mode, during the dead time between the gate signals of the transistors, the inductance current becomes negative, forming a resonant circuit with the parasitic output capacitance of S_1 (C_{DS1}). Due to the resonance, the capacitor can be fully discharged and Zero Voltage Switching (ZVS) can then be achieved when S_1 is turned on. Moreover, in this case, S_2 is turned-off close to Zero Current Switching (ZCS), hence, the overall switching losses are reduced drastically. Nevertheless, the price to be paid in this operation mode is that a large current ripple is needed which is a disadvantage for energy storage applications.

Modular converters (also known as multiphase converters or composite converters) are formed by several converters (called here modules) connected in a particular arrangement (series, parallel or cascade) to take advantage of the reduction of current or voltage stress, in comparison with a stand-alone converter [19]-[21]. The Input Parallel Output Parallel (IPOP) connection has been widely used in DC-DC power converters in combination with an interleaved control [22]-[25]. This interleaved technique allows to reduce the total current ripple of the resulting IPOP modular converter, becoming an interesting approach for high power applications. Hence, an IPOP modular converter is suitable to minimize the

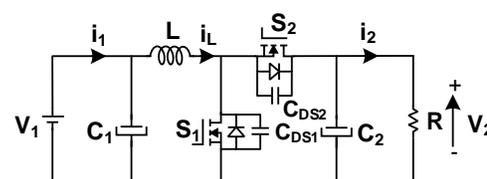


Fig. 1. Synchronous boost converter.

forementioned disadvantage of QSW-ZVS mode, which is the large current ripple. Furthermore, another advantage of an IPOP modular converter is the scale laws which are inherent in any modular converter [19]. These scale laws allow to use better devices in terms of losses, and then, to increase even more the overall efficiency in the modular IPOP converter in comparison with a stand-alone converter.

This work faces two challenges. The first one is to develop a very simple control strategy for an IPOP modular converter composed by several synchronous boost converters operating in QSW-ZVS mode. The main goal of this first task is to develop a control technique to extend easily a variable switching frequency control to properly operate in QSW-ZVS mode for a modular converter. Moreover, this control has to deal with the current sharing among the modules and with the interleaved phase-shift, in order to reduce the input current ripple. Therefore, the advantages of QSW-ZVS operation mode (very high efficiency at full load and also a high efficiency at light load) can be extended to higher power levels, minimizing, at the same time, one of the problems of this operation mode (the high current ripple). The second challenge addressed in this paper is to propose some control techniques for an IPOP modular converter based on QSW-ZVS synchronous boost modules, to take advantage of the modular approach to improve even further the overall efficiency at medium and light load.

This paper is organized as follows. In Section II, a master-slave technique is presented and analyzed to control an IPOP modular converter. The proposed technique is developed to adopt an interleaved control for QSW-ZVS mode for reducing the current ripple. In Section III, three different control strategies to improve an IPOP modular QSW-ZVS converter efficiency are summarized and compared in terms of the overall losses: phase-shedding, asymmetrical master-slave and burst mode. The experimental results are presented in Section IV. An IPOP modular converter formed by four, up to six synchronous boost converters working in QSW-ZVS mode is built to validate and to compare the theoretical and experimental results. Finally, in Section V the main conclusions of this paper are outlined.

II. CONNECTING QSW-ZVS CONVERTERS IN PARALLEL

A. Variable frequency QSW-ZVS mode and its problematic

In this section, some important parameters of QSW-ZVS operation mode are summarized, even though this operation mode is well known in the literature. However, these parameters will play an important role in the analyzed modular techniques, as the variable switching frequency control.

The ideal waveforms of a synchronous boost converter operating in QSW-ZVS mode can be seen in Fig. 2. Four regions are observed during each switching period (T): the magnetizing interval (i.e. on-time, t_{on}), the demagnetizing interval (i.e. off-time, t_{off}), and two dead times (t_{d1} and t_{d2}). The on-time and off-time regions are known as linear intervals, while both dead time regions are known as resonant intervals. The lower limit for the first dead time (t_{d1}) is constrained by the need to avoid a short-circuit when S_2 is turned on and S_1 is

turned off. On the other hand, excessive large values of t_{d1} will result in higher losses in the parasitic body diode of S_2 . During the second dead time (t_{d2}) the inductance current becomes negative, forming a resonant circuit with the parasitic output capacitance of S_1 (C_{DS1}). Due to the resonance, the capacitor can be fully discharged and ZVS can then be achieved when S_1 is turned on. Moreover, in this case, S_2 is turned-off close to Zero Current Switching (ZCS), hence, the overall switching losses are reduced drastically. Dead time t_{d1} has little importance and is neglected in most of the studies on QSW-ZVS, only the interval t_{d2} being considered for ZVS [18], [26] and [27].

A disadvantage of QSW-ZVS is the operation at light load. There are two possibilities to face this problem: operate at constant switching frequency [26], [28]-[30] or at variable switching frequency [31], [32]. With constant switching frequency, the level of reactive current of the converter increases when power decreases and, therefore the converter power losses increase, reducing the efficiency at light load. In the second approach, the dead time t_{d2} and the switching period are adjusted to keep exactly the necessary negative current to achieve ZVS; the lower the power, the higher the switching frequency. Following this variable switching frequency approach is possible to keep a high efficiency even at light load, which is desirable for the applications stated in this work. However, the price to be paid is the increase in the electromagnetic emissions and a more complex control, most of them based on peak current controls [31], software based calculations of t_{on} , t_{off} and t_{d2} (with the subsequently increase in the processing time) [32] or in Look-up-Tables (LUT) [33]. To minimize the control stage complexity, a direct variable frequency control is proposed in [34]. In this approach, the switching period and the switching time intervals are generated directly based on two events: a Zero Current Detection (ZCD) for the inductor current and a Zero Voltage Detection (ZVD) for the drain-to-source voltage of S_1 . Therefore, this approach is very simple and it does not have a high computational cost as the previous ones. In this paper, this particular control is extended to IPOP connection to maintain a high efficiency at light load operation.

An IPOP modular converter can extend the QSW-ZVS operation mode advantages to higher power levels. Nevertheless, the variable switching frequency performance

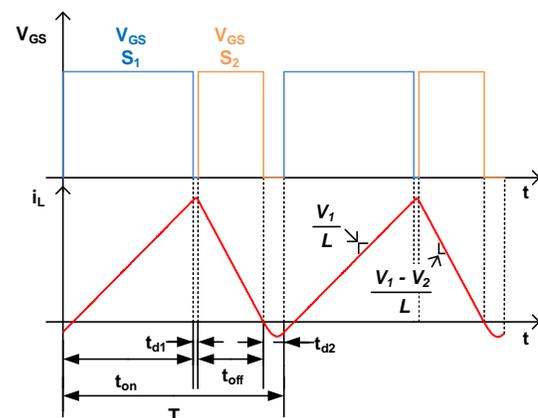


Fig. 2. Theoretical waveforms for a synchronous boost converter operating in QSW-ZVS mode.

adds more complexity to the modular converter control, which also has to interleave all the modules and to balance the current among them. Some current sharing techniques can be adopted to minimize this problem [31]-[39]. However, most of them are based on an additional current control loop, which increases the complexity of the control stage, especially when a large number of modules are planned to be used as an IPOP modular converter. In this section a control technique to extend the direct variable frequency control proposed in [34] is going to be studied in order to simplify traditional current sharing solutions and to obtain a very simple control for an IPOP QSW-ZVS converter.

B. Master-slave technique for IPOP QSW-ZVS modular converters

A possible way to address the aforementioned challenge is to use a master-slave approach. This approach has been widely used in interleaving control techniques for AC-DC Power Factor Corrector converters [38], [39]. This section summarizes a description of how to adopt this technique for a QSW-ZVS operation mode with a direct frequency control.

Under the master-slave approach, one module plays the role of master. The other $N-1$ modules play the role of slaves (being N the total number of modules in the IPOP modular QSW-ZVS converter). Only the master module is operating in closed loop (the slave modules are operating in open loop). The master control stage uses the direct variable frequency control to generate its control signals. These control signals are shared among the slaves to be used as their own control signals in the next switching period. To illustrate this control, in Fig. 3 an example of the control signals of a master and a slave module is shown. This T_{prev} time interval is phase-shifted φ degrees according to the interleaved strategy and the number of modules used (N) (i.e. $\varphi = 360/N$). As the same on-time is applied to all the slaves, the current balancing is naturally achieved without the addition of any other control or circuitry.

Nevertheless, there are some small differences among the modules, due to the tolerances and component derating. So, there is a degree of freedom under this master-slave control, which is the second dead time t_{d2} . This time is generated based on ZVD event for each module and it can be different for

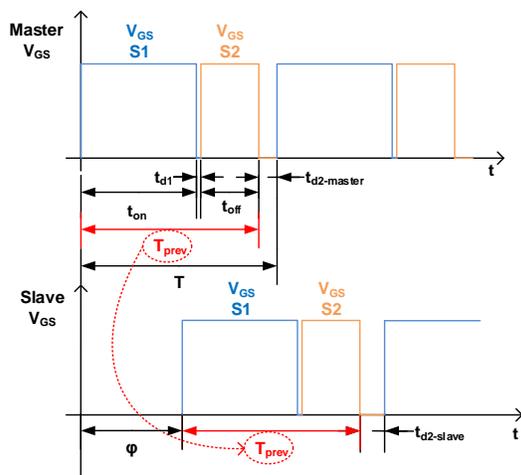


Fig. 3. Example of control waveforms for master-slave solution.

each converter, which is a difference in comparison with the traditional master-slave approach, and it can be adopted thanks to the use of the direct frequency control. This ZVD event is generated when the drain-to-source voltage of main transistor (S_1) reaches zero. By adopting this solution, ZVS is achieved in all the modules, despite of the difference of the output capacitor value of each MOSFET among them. The price to be paid is a little current unbalance due to the different switching period of each module. However, it should be noted that t_{d2} is always several orders of magnitude lower than t_{on} and t_{off} , so this unbalance is in general bearable. Therefore, a natural current sharing among modules is achieved by the application of the same switching time (T_{prev}) in all of them. The current sharing among the modules under this control technique strongly depends on the component values, especially in the inductance value. Even though a natural current balance is achieved, some differences may appear if this inductance is very different from one slave module to the other. However, in QSW-ZVS operation mode the inductor should be carefully design and build, because this inductance determines the maximum peak current and the nominal switching frequency. Hence, small variations of the inductance value are expected when this mode is used.

A basic diagram of the master-slave control technique is shown in Fig. 4. As can be seen, the master module needs 5 different input signals which are: the number of slaves (N), the discretized output voltage which is coming from an analog-to-digital converter (named here as ADC), the ZCD and ZVD events from the direct frequency control previously detailed, and the value of t_{d1} , which is constant.

The slave module only needs four input signals, which are: the number of slaves (N), the previous time from the master (T_{prev} , i.e. $t_{on}+t_{off}+t_{d1}$), the ZVD event from the direct frequency control and a synchronization signal (i.e. $sync$). This signal is needed to apply the phase-shift between the control signals of different slave modules, according to the interleaving approach. In this case, the main switch signal of the master (S_1) is used as synchronization.

A detailed control block diagram for this master-slave strategy is shown in Fig. 5. The master module (see Fig. 5(a)) generates two complementary Digital Pulse Width Modulated

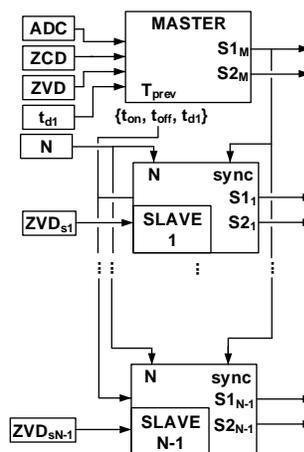


Fig. 4. Master-slave control diagram.

(DPWM) signals ($d[n]$ and $d_c[n]$) from the ADC after being processed by the regulator and ZCD event. A discrete regulator determines the on-time based on the output voltage sensed ($v_o[n]$) and the ZCD event determines the off-time. Then, a dead time generator applies both dead times (i.e. t_{d1} and t_{d2}), the former being constant, the latter based on the ZVD event. An enable signal (ENB) is also added for safety reasons.

The block diagram of a slave module is slightly different (see Fig. 5(b)). In this case, both complementary DPWM signals are obtained directly from the input information coming from the master (i.e. T_{prev}). A phase-shift generator is used here with signals N and $sync$ to phase-shift the digital ramp (and consequently the DPWM signal). Finally, ZVD event is also used to define the second dead time t_{d2} as in the master case.

III. PROPOSED CONTROL TECHNIQUES TO IMPROVE EFFICIENCY

The previously stated master-slave technique can extend the direct frequency control to an IPOP modular converter, assuring a good current balance among the modules. However, this totally balance approach could not provide the maximum efficiency. To illustrate this point, suppose a general IPOP arrangement as is depicted in Fig. 6. The total input voltage (V_I) and the total output voltage (V_O) are equal for all the modules.

Each module has an input and output currents named here as I_{In} and I_{On} for a given n-module. Furthermore, each module also has a certain amount of losses (for the n-module, P_{Ln}) and, therefore a certain efficiency (η_n).

Based on this general structure, the total efficiency of the modular converter can be calculated based on the individual efficiency of each module. Hence, the efficiency of a module is

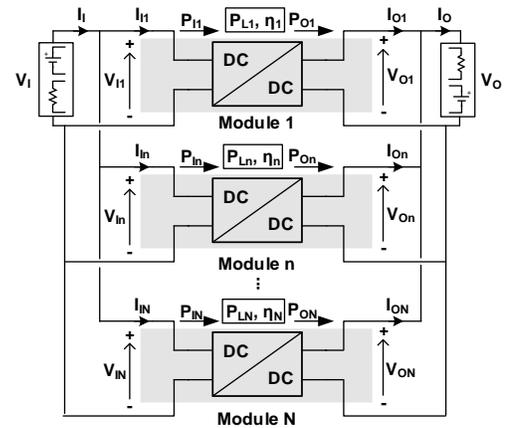


Fig. 6. General IPOP converter composed by N modules.

defined as

$$\eta_n = \frac{P_{On}}{P_{In}} = \frac{V_{On} \cdot I_{On}}{V_{In} \cdot I_{In}} = \frac{V_O \cdot I_{On}}{V_I \cdot I_{In}} \quad (1)$$

In an IPOP modular converter, the total input and output currents are the sum of the input and output currents of each module,

$$I_O = \sum_{n=1}^N I_{On} \quad (2)$$

$$I_I = \sum_{n=1}^N I_{In} \quad (3)$$

Then, the total efficiency of an IPOP modular converter can be expressed as

$$\eta_T = \frac{P_O}{P_I} = \frac{V_O \cdot I_O}{V_I \cdot I_I} = \frac{V_O \cdot \sum_{n=1}^N I_{On}}{V_I \cdot \sum_{n=1}^N I_{In}} = \frac{\sum_{n=1}^N P_{On}}{\sum_{n=1}^N P_{In}} \quad (4)$$

where P_{On} and P_{In} are the output and input power of a given n-module. This efficiency can also be calculated in terms of the losses of each module, as

$$\eta_T = \frac{P_O}{P_I} = \frac{P_I - P_{LT}}{P_I} = \frac{P_I - \sum_{n=1}^N P_{Ln}}{P_I} \quad (5)$$

where P_{LT} are the power losses of the IPOP modular converter. Equations (4) and (5) are always valid for an IPOP modular converter, independently of the control strategy applied.

In the master-slave control strategy, all the modules operate, theoretically, with the same power and current balanced. In order to simplify the explanation, a linear variation of total power (P_O) will be considered for all the cases (see Fig. 7). So, if P_O of the modular converter varies linearly from 0 to the maximum power (P_T), then the power of each module varies following the same pattern from 0 to P_T/N . This basic power profile example is shown in Fig. 7(a). Under this balanced current control the previously expressions can be simplified by imposing that all the modules work with the same current level,

$$I_{On} = \frac{I_O}{N} \rightarrow P_{On} = \frac{P_O}{N} \quad (6)$$

$$I_{In} = \frac{I_I}{N} \rightarrow P_{In} = \frac{P_I}{N} \quad (7)$$

Then, using (6) and (7) and replacing them into (4) and (5) yields

$$\eta_T = \frac{P_O}{P_I} = \frac{V_O \cdot \sum_{n=1}^N I_{On}}{V_I \cdot \sum_{n=1}^N I_{In}} = \frac{V_O \cdot N \cdot I_{On}}{V_I \cdot N \cdot I_{In}} = \eta_n \quad (8)$$

$$\eta_T = \frac{P_I - P_{LT}}{P_I} = \frac{P_I - N \cdot P_{Ln}}{P_I} \quad (9)$$

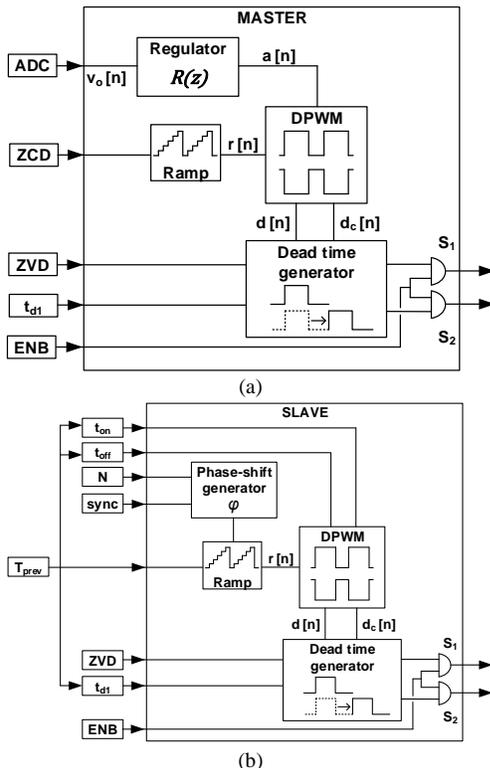


Fig. 5. Block diagram for the master-slave control technique. (a) Master module control. (b) Slave module control.

As it seems logical, equation (8) establishes that the efficiency of the IPOP modular converter when is controlled with a balanced current technique is the same as the efficiency of a module. Moreover, from another point of view, the total losses of an IPOP modular converter are N times the losses of a module (9). Therefore, this control strategy is not increasing the efficiency in comparison with a standalone converter. In this section, three different control techniques will be explored to take advantage of the modular design in order to improve this efficiency.

A. Phase-shedding (sequential turn-on)

The phase-shedding technique has been proposed in [40]-[43]. This control technique is based on sequentially turn-on the modules when the power increases and vice-versa. Hence, only the modules needed are active (i.e. providing energy to the load) depending on the total power demanded, reducing the total losses of the modular converter. The classic approach to implement this phase-shedding technique is based on an extra functionality of the controller which implies a module manager or similar control block. This new block determines the number of modules which must be active, and how much power they have to provide. Most precisely, the previous proposed approach is depicted in Fig. 7(b). As can be seen, for a linear variation on the total output power (P_o) demanded from 0 to P_T , each module increases its power till it reaches its maximum attainable value (P_T/N). The rest of the modules keep disconnected (i.e. without processing any power). Then, another module is turned-on and this scheme is repeated till the total demanded power is fulfilled. The inverse strategy is followed when total power decreases. The main problem of this technique is the increase in the control complexity due to the necessity of a manager. As can be seen in Fig. 7(b), every single module has to be able to vary its own power and the control has to deal with the turn-on and turn-off process of the whole modular converter.

A possible way to implement this technique in a very simple way is to take advantage of the master-slave control explained in the previous section. Instead of allowing all the modules to

vary its power, under this solution only the master module is performed to change its power. The other modules operate in open loop and at constant power (i.e. at its maximum attainable power, P_T/N). Therefore, the master module (manager) only has to deal with the turn-on and turn-off of slaves modules. The same power profile example using this method is shown in Fig. 7(c). This solution is simpler than the previous one and it is more flexible because the addition of a new slave module does not change the control strategy of the modular converter (as it will be shown later on).

This approach has a limitation regarding the component tolerances, which is related to the ZVS condition. Under this control technique, all the slave modules work with constant t_{d2} . This parameter (t_{d2}) depends on the MOSFET output parasitic capacitor. Hence, if this capacitance varies among the different slave modules due some component tolerance then ZVS cannot be guaranteed during the dead time in all of them. In this case, partial ZVS operation is achieved instead, but the efficiency is not degraded a lot, as it has been proved in [44]. Moreover, if this change were critical, then the ZVD event would be used as in the balanced control technique, to assure full ZVS operation, but this solution is more complex than the use of the same t_{d2} for all the slave modules. Nevertheless, the manufacturing tolerances are low enough to expect very small variations of this parasitic capacitance.

This master-slave with phase-shedding control can be implemented following the control diagram shown in Fig. 8. Here, the master module uses the same input signals as the master-slave explained in the previous section (Fig. 5). However, now it generates two output signals for all the slaves: n_{slave} and n_{en} . The index n_{slave} varies from 0 up to $N-1$ and is used to determine how many slaves modules must work together. The index n_{en} varies from n_{slave} down to 0, and is used for enabling the control signals of each slave module (i.e. to activate or deactivate a slave module). The phase-shift of the slave modules is also calculated based on n_{slave} and n_{en} , as it will be explained later. The slave module has these indexes as inputs, as well as a synchronization signal as in the previous

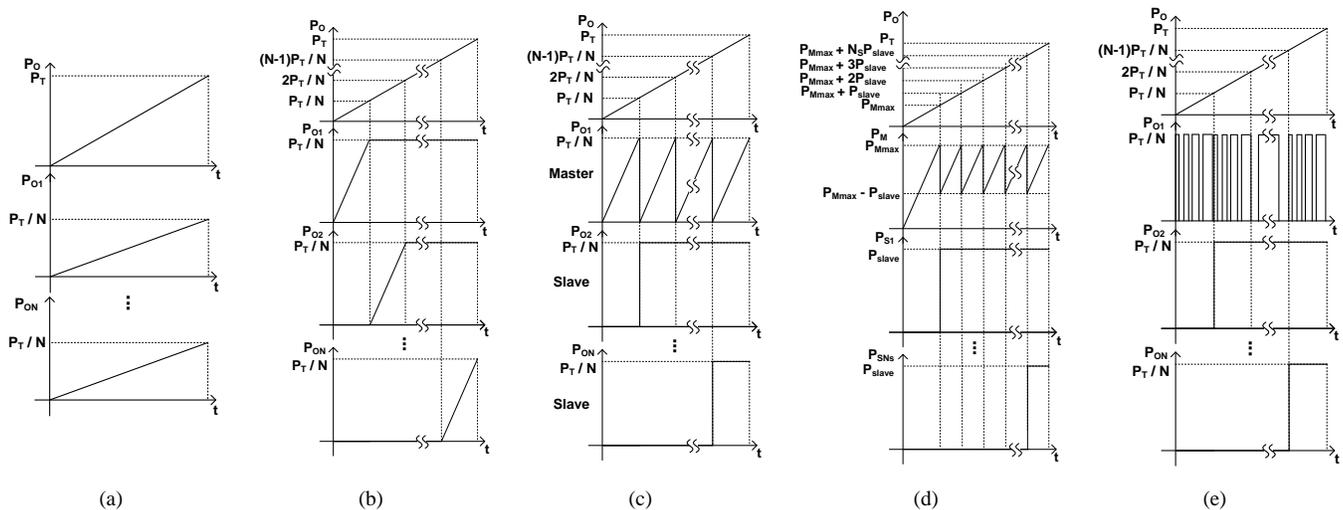


Fig. 7. Power profile example of an IPOP modular converter under different control techniques. (a) Balanced technique. (b) Phase-shedding technique (previous proposed approach). (c) Phase-shedding technique (master-slave approach). (d) Asymmetrical master-slave technique. (e) Burst mode technique.

case. It should be noted that all the slave modules work with the same switching period (i.e. same t_{on} , t_{off} , t_{d1} and t_{d2}). Hence, the current is naturally balanced among these modules without the addition of any other control circuitry due to the fact that all of them operate with the same amount of current (either at P_T/N watts or zero watts).

The internal block diagrams for both master and slave modules are pretty similar to the previous technique shown in Fig. 5. The only difference here is the module manager. This block calculates both indexes n_{slave} and n_{en} depending on the total number of modules (N) and the output power. Once again, it should be highlighted that the master module is the only one which is operating in closed loop operation. The main challenge is the generation of the phase-shift according to the variable number of active slave modules, in order to keep them interleaved. First, the interleaving cannot be applied to all the modules because the master operates in closed loop with the direct frequency control. Therefore, this module operates with variable switching frequency. On the other hand, all the slaves operate in open loop, so they operate at constant switching frequency. Hence, the synchronization of a variable frequency signal with a constant frequency one require high computational effort, which implies the loss of simplicity needed in this control stage. Due to this, under this master-slave with phase-shedding control technique, only the slaves modules are interleaved each other. It should be noted that the more slaves operate, the lower the total input current ripple. At heavy load operation, the total input current ripple is lower in comparison with light load, in which few slaves operate together.

The second important thing to be taken into account is that the interleaved phase-shift (φ) can be calculated with n_{slave} and the switching period of a slave module (T) as $\varphi = T/n_{slave}$. As synchronization signal, the slave module uses the control signal of the previous slave module for S_1 . The first slave module is not synchronized and this signal is '0' (see Fig. 8). Hence, this phase-shift is always the same for all the slave modules, independently of their position. Moreover, the phase-shift value changes almost immediately when the master recalculates n_{slave} , depending on the output power.

Finally, the index n_{en} is decreased in every slave module being n_{slave} for slave number 1, $n_{slave}-1$ for slave number 2 and so on till it reaches 0. Therefore, by using this method, the slaves are enabled without any other calculation or addition of any other control block.

For this phase-shedding control strategy, the total losses of the IPOP modular converter can be calculated as

$$P_{LT-ps} = P_{Ln-ps} + n_{ps} \cdot P_{Ln-ps@Pmax} \quad (10)$$

where P_{Ln-ps} are the losses of the active module (i.e. the module which is varying its power), $P_{Ln-ps@Pmax}$ are the losses of a module when it is working at its maximum power and n_{ps} is the number of active modules which are working at its maximum power. This n_{ps} might vary from 0 up to $N-1$. It should be highlighted that (10) is also valid for the master-slave with phase-shedding approach, in which P_{Ln-ps} will be the total losses of the master module and $P_{Ln-ps@Pmax}$ will be the total

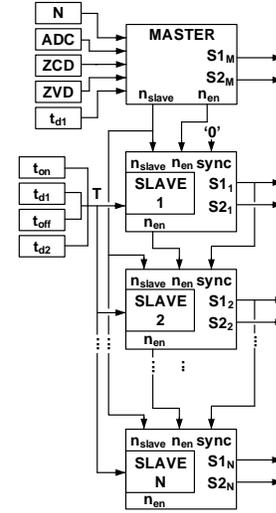


Fig. 8. Master-slave with phase-shedding control diagram.

losses of a slave and n_{ps} will be the number of slaves (n_{slave}).

These losses can be minimized due to the slave modules operate in open loop and only at maximum power (only in one point). So, these modules can be optimized for working at this load, choosing the best components in terms of losses to obtain a maximum efficiency, thanks to QSW-ZVS operation mode. Furthermore, this master-slave with phase-shedding control can be easily applied to a QSW-ZVS synchronous boost converter due to the current source behavior of this topology when it works in open loop operation.

B. Asymmetrical master-slave mode

In the two previous control strategies, all the modules are equal (i.e. they are designed following the same specifications and with the same components). Under balanced control, all the modules work together at the same time, and all of them have to face the light load condition. Under master-slave with phase-shedding this problem is minimized, because only one module (the master) has to work with a variable power (the slave modules only provide their maximum power or zero watts). Nevertheless, both techniques have a common disadvantage. In case of QSW-ZVS operation mode with variable switching frequency, the light load operation is achieved by increasing the switching frequency (as it was explained in Section II). Then, the lower the power, the higher the frequency. Therefore, the traditional procedure to design a converter operating in QSW-ZVS is to define the lowest switching frequency at maximum output power providing a good efficiency at full load operation. Then, when the load decreases, the switching frequency increases introducing more switching losses and, consequently, decreasing the efficiency. However, the switching frequency cannot increase indefinitely. Hence, the switching frequency is always limited to a maximum (this maximum can be chosen taking into account the switching losses, inductance losses, EMI emissions, or other criteria). This maximum switching frequency is given for a minimum power, which can be calculated from [18] as

$$P_{min} = \frac{V_1^2(V_2 - V_1)}{V_2} \cdot \frac{1}{2Lf_{smax}} \quad (11)$$

Moreover, if the load decreases below P_{min} the converter starts working at constant switching frequency, increasing the reactive current and, consequently, the losses, as was mentioned before.

This problem can be faced with different control strategies [31]-[33] and is quite common in other bidirectional converters which work under ZVS. The best example is the Dual Active Bridge (DAB), and the control strategies to maintain ZVS under light load condition such as adding a PWM control, implementing a different phase-shift pattern or adopting a burst mode [35]. These control techniques might be adopted, but most of them increase the control complexity, which goes against the philosophy followed in this paper.

The asymmetrical master-slave approach could avoid this increase of complexity in the control stage. This control technique actually is the same as the previous one, but changing the design procedure. Instead of using equal modules, under this asymmetrical solution, the master module and the slaves are different, and they work at different maximum powers. The idea is to keep the master module working above its minimum power (P_{min}), avoiding the zone in which the losses are increased due to the reactive current. To do that, the power of a slave module is the difference between the maximum and the minimum power of the master module ($P_{slave} = P_{Mmax} - P_{min}$). As the master and the slave modules are not the same, then the number of modules is different from the previous symmetrical techniques. The number of slaves needed (N_s) can be determined as

$$N_s = \frac{P_T - P_{Mmax}}{P_{slave}} \quad (12)$$

where P_{Mmax} is the maximum power of the master module and P_{slave} is the power of a slave. As in the previous control technique, it should be pointed out that only the master operates in closed loop and varying its power. The slave modules operate in open loop, and they only can be operating either at full power (P_{slave}) or at zero output power. All the control strategy, signals and block diagrams are the same as the previously stated for the master-slave phase-shedding technique. The only difference here is the maximum power of the slave module. A power profile example of this technique is shown in Fig. 7(d).

The only condition that must be fulfilled to achieve an efficiency higher than other control techniques is that the efficiency of the slave module (when it is working at P_{slave} power) must be higher than the efficiency of the master module when it is working as the same power ratio (i.e. when the master works at P_{slave}). Mathematically, this condition can be expressed as

$$\eta_{slave} > \eta_{master}(P_{slave}) \quad (13)$$

As in the case of phase-shedding technique, the design of the slave module can be optimized because it only operates at a specific output power. In this work, it is going to take advantage of QSW-ZVS operation mode to reach (13) condition, because now the design must be carried out for a specific output power level (P_{slave} , different to the master one) and for a given constant switching frequency. Obviously, the efficiency results obtained for a specific operation point design could be higher than the results obtained for a design which must fulfill an

operation range. Moreover, it can take advantage of the degree of freedom of the selection of P_{slave} from the efficiency point of view. An example of this optimization to reach (13) condition is provided in in Section III-D.

Finally, the overall modular converter losses under this asymmetrical control technique can be calculated as

$$P_{LT-asim} = P_{Lmaster} + n_{s-act} \cdot P_{Lslave} \quad (14)$$

where $P_{Lmaster}$ are the losses of the master module, P_{Lslave} are the losses of a slave module and n_{s-act} is the number of active slaves. The n_{s-act} parameter ranges from 0 up to N_s . The condition shown in (13) can be used for relating (14) and (10) to obtain a maximum for the slave module losses:

$$P_{Lslave} < k_{eff} \cdot \frac{n_{ps}}{n_{s-act}} \cdot P_{Lmaster@Pslave} \quad (15)$$

where $P_{Lmaster@Pslave}$ are the losses of master module operating at a power of P_{Lslave} , and k_{eff} is a figure-of-merit of the efficiency. This parameter ranges from 0 to 1. The lower this parameter, the higher the efficiency improvement obtained in the asymmetrical master-slave in comparison with the master-slave with phase-shedding, if the same master module is used in both control techniques. If k_{eff} is 1, then both techniques (asymmetrical and phase-shedding) obtain the same efficiency.

C. Burst mode (hysteretic turn-on)

With the previous asymmetrical control technique, the master module works in a certain power range (higher than P_{min}) in which its efficiency is high enough. However, when no slaves are needed (i.e. when the total power demanded by the load is lower than $P_{Mmax} + P_{slave}$) then the master module could work out of this power range. Hence, the efficiency of the overall modular power converter decreases. Once again, the use of a modular approach may be able to overcome this problem by the adoption of a properly control strategy. In this case, the main goal is not to design the master to work in a certain power range, but in a certain operational point (for a given power) in which its efficiency is maximized, turning-on or off all the modules for regulating the output voltage an improvement of the efficiency at light load can be achieved. This control strategy is called burst mode or hysteretic turn-on and is not new. It has been widely applied in analog control ICs since several decades ago, to prevent or implement a light load operation [45]-[48]. Nevertheless, in this case this technique is applied not only at light load, but with any power demanded by the load. This burst control can be seen as a limit case of the previous control strategy, assuming that the minimum power of the master module equals to the maximum power. A power profile example for this burst control is shown in Fig. 7(e). For simplicity, in this case all modules are considered identical once again but this is not mandatory, and they could manage a power of P_T/N , being P_T the maximum power demanded by the load.

As can be seen in Fig. 7(e), the slave modules are turned-on when power increases in the same way of the master-slave with phase-shedding control technique. The master module can now work only in two states: turned-on providing its maximum power (P_T/N) or turned-off. To implement this control strategy, a hysteretic control could be implemented, as it was proposed

in [48] for resonant converters. Under this control technique, the master operates at constant switching frequency (constant t_{on}) and the hysteretic control is in charge of the output voltage regulation, depending on the total power demanded. The slave modules operate in open loop (as in the two previous control techniques). Under this control technique, when the total power demanded by the load is lower than P_T/N and no slaves are needed, then the master module operates always as its maximum output power (i.e. at its maximum efficiency), keeping the efficiency as high as possible, even at very light load. All the control signals and block diagrams are, once again, the same as the previously stated for the master-slave phase-shedding technique. The only difference here is the addition of the hysteretic control block in the master module. As in the previous control technique, the burst mode operation is quite simple to implement based on a master-slave approach.

The total IPOP modular converter power losses when operates under burst control can be estimated as

$$P_{LT-burst} = \frac{t_{onHist}}{T_{Hist}} \cdot P_{Ln@Pmax} + n_{s-burst} \cdot P_{Ln@Pmax} \quad (16)$$

where $P_{Ln@Pmax}$ are the losses of a module when it works at its maximum power, T_{Hist} is the hysteretic period of the master module, t_{onHist} is the on-time of the master module (i.e. the time in which this module is working at its maximum power) and $n_{s-burst}$ is the number of slaves working. The $n_{s-burst}$ index ranges from 0 up to $N-1$, being N the total number of modules. Equation (16) is only an approximation of the total power losses, because the turn-on and turn-off losses of a module are not considered here. It should be pointed out that this technique can also be applied to an asymmetrical IPOP modular converter (i.e. with different modules and different maximum powers). The control strategy does not vary and (16) can be generalized as

$$P_{LT-burst} = \frac{t_{onHist}}{T_{Hist}} \cdot P_{LnMaster} + K \cdot n_{s-Pslave} \cdot P_{LnSlaveP} \quad (17)$$

where $n_{s-Pslave}$ are the number of slave modules which can work at P_{slave} power, $P_{LnSlaveP}$ are the losses of a slave module when it works at P_{slave} power and K are the number of slave modules.

D. Theoretical efficiency estimation and comparison

As a summary of this section, a theoretical efficiency comparison of the four previous control techniques is shown. A basic power losses estimation is done for a synchronous boost converter working in QSW-ZVS mode. Once the efficiency of a specific module has been estimated, expressions (9), (10), (14), (16) and (17) are used to estimate the total power losses of the IPOP modular converter.

To illustrate the different behavior of each control technique the following scenario has been chosen. A conversion from 150V to 400V has been selected. The maximum power demanded to the modular converter is set to 2kW. Then, for balanced control (master-slave), master-slave with phase shedding technique and burst mode, master and slave modules are considered equal and each of them are able to manage a maximum output power of 500W. Hence, the number of modules in those techniques is $N = 4$. For the asymmetrical master-slave control technique, the same master module has

been considered here for a fair comparison. The nominal switching frequency is set to 100kHz (i.e. the switching frequency at maximum power). The maximum attainable switching frequency is set to 220kHz. The inductance value for QSW-ZVS for these specifications is 97 μ H. Then, the minimum power according to (11) is around 200W. The estimated efficiency for a 500W module is shown in Fig. 9. As can be seen, below 200W, the efficiency begins to decrease. Between 200W and full power, the efficiency keeps almost constant and higher than 97.3%. It should be highlighted that in this theoretical efficiency estimation, gate losses, conduction losses and switching losses (including reverse recovery) of both transistors, inductance losses (hysteresis, fringe, proximity and AC losses) and capacitor losses are considered. The driver losses are not included in this efficiency calculation.

As it was stated previously for the asymmetrical master-slave technique, the design of the slave module is slightly different. First, the power of the slave module has to be chosen. In this case, as the minimum power of the master module is 200W, then the power of the slave module is set to 300W. The number of slave modules needed is obtained from (12), in this case $N_s = 5$. Once the number of slave modules and its power are known, the minimum efficiency of these slave modules, needed to improve the efficiency at light load in comparison with the previous control techniques, can be found using (14) in order to fulfill condition (13). In this example, the efficiency of the master module at 300W is estimated in 97.38%, as it has been highlighted in Fig. 9. Then, the efficiency of the slave module must be higher than this value to improve the overall efficiency. For this given example, the efficiency of the slave module after its optimization is estimated to 97.98%. With this efficiency, parameter k_{eff} can be calculated from (15), being in this example 0.8, which means that the overall efficiency of the asymmetrical master-slave approach has an improvement of 0.2 in comparison with balanced master-slave following (15) and (16). This efficiency is a condition that must be fulfilled in the design of the slave modules. Moreover, for the overall efficiency estimation in the asymmetrical master-slave technique, the minimum efficiency of the master module is 97.25%.

Once the estimation of losses of all modules of all control techniques has been outlined, the overall efficiency of an IPOP modular converter is plotted in Fig. 10. This estimated

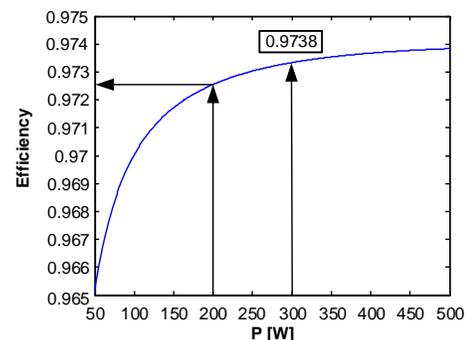


Fig. 9. Estimated efficiency of 500W module playing the role of master and values needed for the asymmetrical master-slave technique.

efficiency can be calculated using equations (9), (10), (14), (16) and (17) for every single control technique.

As can be seen, the balanced control technique obtains an estimated efficiency which is similar to the estimated efficiency of one module (i.e. the master module shown in Fig. 9). The maximum estimated efficiency is 97.4% and it is obtained at full load (2kW). Below 1kW, this estimated efficiency decreases, being 96.5% at 200W. With the master-slave with the proposed phase-shedding technique, this overall estimated efficiency is improved below 1kW (see the black curve in Fig. 10). As it was expected, under light load the use of an optimum number of slave modules allow to reduce the overall estimated losses of the modular converter. However, this technique has almost the same efficiency at full load in comparison with the balanced control. The asymmetrical master-slave approach obtains the estimated efficiency plotted in red in Fig. 10. Under this control technique, the number of modules has been increased from 4 to 6, and 5 modules work with 300W instead of 500W. As can be seen, this technique allows to improve even more the overall estimated efficiency from 500W to 2kW. In this range, the overall estimated efficiency is always above 98% due to the optimization of slave modules. The saw-tooth pattern in the shape of the estimated efficiency curve is due to the activation of the slave modules (i.e. the turn-on and off of each slave). Moreover, as can be seen, the overall efficiency under this control technique hits a peak exactly when a slave module is turned on and then decreases. This peak is due to the relationship between the master and the slave efficiencies. As it was stated before, the slave module has a very high efficiency at 300W (97.98%). Then, when another slave is turned on, the additional power losses due to the new slave module are very low. The master module has to provide 200W and its efficiency is still high at this power level. Consequently, the sum of the total power losses of all modules are also low. This effect does not happen under phase-shedding control, because the master module starts working at almost 0W and the efficiency of this module is very low at this power level.

Finally, the overall estimated efficiency for the burst mode control technique with four 500W modules is plotted in green in Fig. 10. Once again, this control technique improves the overall estimated efficiency for power ranges from 0 up to 1kW, where efficiency is always around 99%. This demonstrates that

this control technique is more suitable than the previous ones when the efficiency at medium and light load has to be very high. However, the overall estimated efficiency of the burst mode above 1kW is lower than the estimated efficiency obtained for the asymmetrical master-slave control technique (but higher than balanced and phase-shedding techniques). This effect is related to the scale laws in a modular converter. The higher the number of modules (N), the lower the theoretical losses obtained in the modular converter [19], even if no better devices are used. Following this reasoning, the asymmetrical master-slave approach deals with 6 modules, while the burst mode uses only 4 modules. This difference may explain the lower estimated efficiency obtained by the latter one in comparison with the former. In order to obtain a fair comparison, a burst mode approach but using 6 modules is also studied. In this case, a 500W master module is used in combination with 5 300W slave modules (i.e. following the same design for the asymmetrical master-slave technique). The overall estimated efficiency obtained in this case is plotted in purple in Fig. 10.

IV. EXPERIMENTAL RESULTS

Once the potential improvements in the overall efficiency of each control technique have been explored, an IPOP modular converter has been built in the laboratory to experimentally test these control techniques. Two different modules has been designed and built: module-type I and II. Specifications and main components of module-type I and module-type II are shown in Table I.

The control platform used is a Spartan 6 FPGA from Xilinx. To implement the direct frequency control, a simple resistor divider and a LM393 comparator from Texas Instruments is used for the ZVD event. A current sensor based on a custom made toroid, a series resistance and another LM393 comparator is used for obtaining the ZCD event. The output voltage is measured directly with a resistor divider and an aliasing filter, and then is discretized by a 12 bit Analog to Digital Converter (i.e. AD7476A from Analog Devices). The inductance has been designed taking into account the AC losses and fringe effect

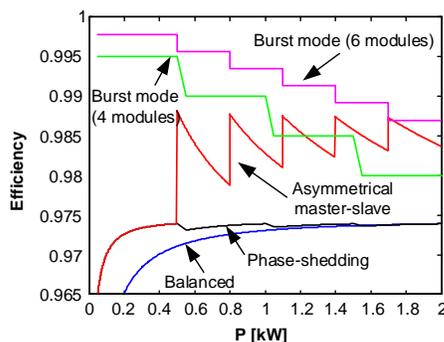


Fig. 10. Overall estimated efficiency comparison of the IPOP modular converter under balanced control, master-slave with phase-shedding, asymmetrical master-slave and burst mode (with 4 and 6 modules).

TABLE I. COMPONENTS AND MAIN SPECIFICATIONS FOR THE MODULE-TYPE I.

Parameter	Module-Type I	Module-Type II
V_1	150V	150V
V_2	400V	400V
f_s	100kHz (min. 80kHz-max. 240kHz)	100kHz (min. 80kHz-max. 240kHz)
Maximum power	500W	300W
C_{OSS}	2,2nF	2,2nF
L	97μH, ETD41, 3F3, Ferroxcube. Litz wire 0.1mm.	138μH, ETD39, 3F3, Ferroxcube. Litz wire 0.1mm.
C_1	2 x 3.3μF, 250V, MKT 1 x 22 μF, 250V, electr.	2 x 3.3μF, 250V, MKT 1 x 22 μF, 250V, electr.
C_2	2 x 1μF, 680V, MKP 1 x 4.7μF, 450V, electr.	2 x 1μF, 680V, MKP 1 x 4.7μF, 450V, electr.
Transistors	SPW47N60CFD, Infineon 600V, 46A, 83mΩ, 2200pF	SPW47N60CFD, Infineon 600V, 46A, 83mΩ, 2200pF
Switch driver	EL7104	EL7104

losses, placing the wires far from the air-gap. The prototypes built can be seen in Fig. 11. The power stage of a module-type I is depicted in Fig. 11(a). The heatsink and the inductance have been removed for clarity reasons. The IPOP modular converter is depicted in Fig. 11(b).

A power supply model 6813B and an electronic load N3300A (both from Keysight) are used for testing the modular converter. The overall input and output currents and voltages are measured with multimeters Fluke 187. The driver losses are not measured in these tests.

The most significant waveforms measured of both module-types can be seen in Fig. 12, both operating at maximum power. Both modules achieve ZVS being the current ripple larger in module-type I (Fig. 12(a)) in comparison to module-type II (Fig. 12(b)), as it was expected.

The measured efficiency of module-type I is shown in Fig. 13. The efficiency at full power is 98.01% which is slightly higher than the estimated one. However, in spite of this little error, the shape of the efficiency curve fits pretty well with the estimation shown in Fig. 9. Once again, for power higher than 200W efficiency is above 97.5%, being almost flat from 250W to 500W. Below 200W, the efficiency decreases due to the constant switching frequency behavior, as it was predicted by the theoretical and estimated model. According to this measured efficiency, for the design of the asymmetrical master-slave control, then the 300W module-type II, which will always play the role of a slave, must have an efficiency higher than the efficiency of the module-type I (which is going to act as master) at 300W, being 97.98%.

The measured efficiency for the module-type II was 98.69%. In this case, the efficiency curve is not provided, because this

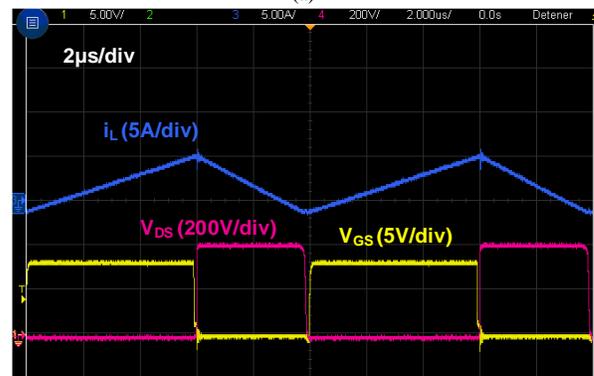
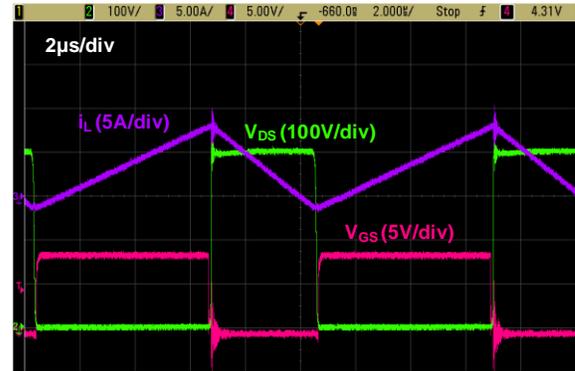


Fig. 12. Significant operational waveforms measured at full power. (a) Module-type I (500W). (b) Module-type II (300W).

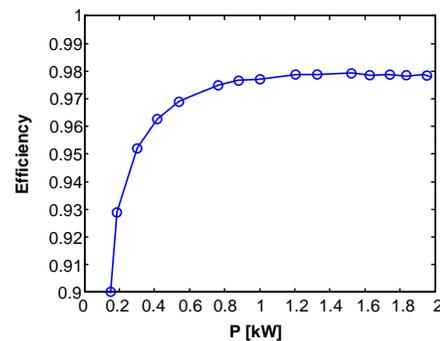
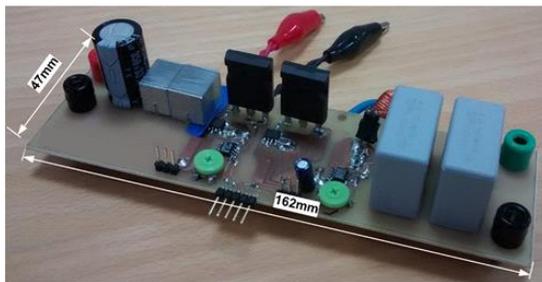


Fig. 13. Measured efficiency of module-type I



(a)



(b)

Fig. 11. Pictures of the prototypes built. (a) Module-type I power stage. (b) IPOP modular converter.

module only works either at its maximum output power, either at zero power. Hence, condition (13) is fulfilled for improving the overall IPOP modular converter efficiency with these modules, using the proposed control techniques.

Some experimental operational waveforms of the balanced master-slave control proposed here can be found in Fig. 14 for the IPOP modular converter working at full power (i.e. 2kW, 4 modules-type I of 500W each one, only one operating in closed loop as a master). As can be seen in Fig. 14(a), the slaves are naturally balanced following this approach, and they are pretty well interleaved with the master module, see Fig. 14(b). Moreover, all the modules work under ZVS and roughly at its optimum point of reactive inductance current.

asymmetrical master-slave, the master-slave with phase-shedding and last the balanced master-slave. It should be highlighted that the burst mode obtains the best results in terms of the medium and light operation (custom efficiency, red column in Fig. 17). However, the other techniques do not obtain a higher custom weighted efficiency for medium and light load operation, especially the balanced master-slave technique, which custom efficiency cannot be seen in Fig. 17.

V. CONCLUSIONS

A master-slave control technique has been proposed to extend the variable direct frequency control to an IPOPOP modular converter composed by several synchronous boost QSW-ZVS modules. This technique has the advantage of the simplicity and the current is naturally balanced among the modules without the addition of any complex circuitry or more calculations for the control stage. Thanks to the use of ZVD event, the slave modules work with different t_{d2} ; hence, the ZVS is warranted in all of them. However, the current balance depends on the tolerances of the components used by each module. This technique allows to extend the benefits of QSW-ZVS operation mode with variable switching frequency to higher power levels, especially the high efficiency at light load, and to reduce the input current ripple in a very simple way.

Moreover, four different control techniques have been deeply analyzed in this paper in terms of the efficiency at light to medium load. These techniques can be used to improve even further the efficiency at light load, taking advantage of the modular approach and the QSW-ZVS mode. The balanced control technique is based on the previous master-slave control and it does not bring any advantage from the point of view of the modular converter efficiency at light load. The phase-shedding control technique has already been modified in this paper to be adopted to an IPOPOP modular converter made up with QSW-ZVS boost converters. Then, an asymmetrical master-slave control technique has also been developed to improve the performance of the IPOPOP modular converter when it has to operate below medium output power. This technique is based on the use of modules of different power. Finally, a burst mode technique has also studied as a possible extreme approach for improving the efficiency at light load.

The four control techniques have been theoretically analyzed in terms of the losses of the overall IPOPOP modular converter. A

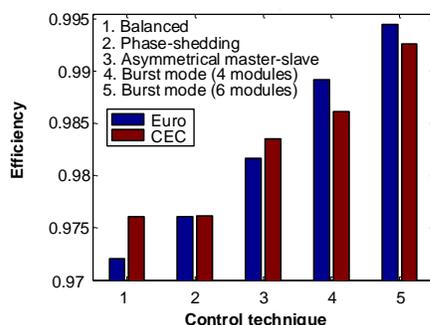


Fig. 17. Measured weighted efficiency according to Euro-Efficiency and CEC for each control technique.

comparison of the estimated efficiency is carried out and two different modules (type I and II) has been built in the lab in order to experimentally validate these results with a prototype of 2kW, up to six different modules. The obtained results are good enough to compare the four control techniques under study. Furthermore the estimated results and the experimental ones are pretty similar. Finally, a third comparison is established using weighted efficiencies (such as CEC and EuroEff).

The balanced control technique has the advantage of the simplicity and the reduction of the input current ripple. However, it does not have any advantage from the efficiency point of view. The master-slave with phase-shedding control technique has the advantage of the improvement in the efficiency in comparison with the previous one, but the price to be paid is that only the slave modules are interleaved, so, the total input current ripple is not minimized, especially at light load. The asymmetrical master-slave control technique is another possibility to improve even more the efficiency at light load, thanks to QSW-ZVS operation mode. Although the efficiency is improved, this control technique has the previously stated disadvantage for the phase-shedding control technique, and it is even more complex to design. The burst mode control technique can be seen as the application of the previous one pushed to the boundary. This control technique has been the best in terms of the efficiency at light load. Nevertheless, a hysteretic control (or similar) is needed under this control technique and, from the dynamic point of view, this could be an important drawback to take into account.

VI. REFERENCES

- [1] R. Naayagi, "A review of more electric aircraft technology," Energy Efficient Technologies for Sustainability (ICEETS), 2013 International Conference on, pp. 750-753, April 2013.
- [2] A. Boulanger, A. Chu, S. Maxx and D. Waltz, "Vehicle Electrification: Status and Issues," Proceedings of the IEEE, vol. 99, no. 6, pp. 1116-1138, June 2011.
- [3] C. Attaianese, V. Nardi and G. Tomasso, "A High Efficiency Conversion System for Elevators," Clean Electrical Power, 2007. ICCEP '07. International Conference on, pp. 236-242, May 2007.
- [4] C. Chan and Y. S. Wong, "The state of the art of electric vehicles technology," Power Electronics and Motion Control Conference, 2004. IPEMC 2004. The 4th International, vol. 1, pp. 46-57, Aug. 2004.
- [5] J. Cao and A. Emadi, "A New Battery/UltraCapacitor Hybrid Energy Storage System for Electric, Hybrid, and Plug-In Hybrid Electric Vehicles," Power Electronics, IEEE Transactions on, vol. 27, no. 1, pp. 122-132, Jan. 2012.
- [6] A. F. Burke, "Batteries and Ultracapacitors for Electric, Hybrid, and Fuel Cell Vehicles," Proceedings of the IEEE, vol. 95, no. 4, pp. 806-820, April 2007.
- [7] Sparacino, A.R.; Reed, G.F.; Kerestes, R.J.; Grainger, B.M.; Smith, Z.T., "Survey of battery energy storage systems and modeling techniques," Power and Energy Society General Meeting, 2012 IEEE, vol., no., pp.1,8, 22-26 July 2012.
- [8] Affanni, A.; Bellini, A.; Franceschini, G.; Guglielmi, P.; Tassoni, C., "Battery choice and management for new-generation electric vehicles," Industrial Electronics, IEEE Transactions on, vol.52, no.5, pp.1343,1349, Oct. 2005.
- [9] F. Blaabjerg, F. Iov, T. Kerekes and R. Teodorescu, "Trends in power electronics and control of renewable energy systems," Power Electronics and Motion Control Conference (EPE/PEMC), 2010 14th International, pp. K-1-K-19, Sept. 2010.
- [10] European Union, "Implementing the Energy Performance of Buildings Directive (EPBD)," Concert Action Energy Performance of Buildings, October 2013. [Online]: <http://www.epbd-ca.org/Medias/Pdf/CA3-BOOK-2012-ebook-201310.pdf>. [Last accessed: Jul. 2015].

- [11] Energy European Commission, Nearly zero-energy buildings. [Online]: <https://ec.europa.eu/energy/en/topics/energy-efficiency/buildings/nearly-zero-energy-buildings>. [Last accessed: Jul. 2015].
- [12] T. Dragičević, X. Lu, J. C. Vasquez and J. M. Guerrero, "DC Microgrids—Part I: A Review of Control Strategies and Stabilization Techniques," in *IEEE Transactions on Power Electronics*, vol. 31, no. 7, pp. 4876-4891, July 2016.
- [13] L. R. Lewis, B. H. Cho, F. C. Lee and B. A. Carpenter, "Modeling, analysis and design of distributed power systems," *Power Electronics Specialists Conference, 1989. PESC '89 Record., 20th Annual IEEE, Milwaukee, WI, 1989*, pp. 152-159 vol.1.
- [14] Y. Li and Y. Han, "A Module-Integrated Distributed Battery Energy Storage and Management System," in *IEEE Transactions on Power Electronics*, vol. 31, no. 12, pp. 8260-8270, Dec. 2016.
- [15] A. Kárpáti, G. Zsigmond, M. Vörös and M. Lendvai, "Uninterruptible Power Supplies (UPS) for data center," *2012 IEEE 10th Jubilee International Symposium on Intelligent Systems and Informatics, Subotica, 2012*, pp. 351-355.
- [16] H. Thai, O. Deleage, H. Chazal, Y. Lembeye, R. Rolland and J.-C. Crebier, "Design of Modular Converters; Survey and Introduction to Generic Approaches," *Applied Power Electronics Conference and Exposition, 2009. APEC 2009. Twenty-Fourth Annual IEEE*, pp. 1427-1433, Feb. 2009.
- [17] D. Sable, F. Lee and B. Cho, "A zero-voltage-switching bidirectional battery charger/discharger for the NASA EOS satellite," *Applied Power Electronics Conference and Exposition, 1992. APEC '92. Conference Proceedings 1992., Seventh Annual*.
- [18] Vorperian, V., "Quasi-square-wave converters: topologies and analysis," *Power Electronics, IEEE Transactions on*, vol.3, no.2, pp.183,191, Apr 1988.
- [19] Kasper, M.; Bortis, D.; Kolar, J.W., "Scaling and balancing of multi-cell converters," *Power Electronics Conference (IPEC-Hiroshima 2014 - ECCE-ASIA), 2014 International*, pp.2079-2086, May 2014.
- [20] W. Chen, X. Ruan, H. Yan and C. Tse, "DC/DC Conversion Systems Consisting of Multiple Converter Modules: Stability, Control, and Experimental Verifications," *Power Electronics, IEEE Transactions on*, vol. 24, no. 6, pp. 1463-1474, June 2009.
- [21] S. Thomas, M. Stieneker and R. De Doncker, "Development of a modular high-power converter system for battery energy storage systems," *Power Electronics and Applications (EPE 2011), Proceedings of the 2011-14th European Conference on*, pp. 1-10, Sept. 2011.
- [22] S. Luo, Z. Ye, R.-L. Lin and F. Lee, "A classification and evaluation of paralleling methods for power supply modules," *Power Electronics Specialists Conference, 1999. PESC 99. 30th Annual IEEE*, vol. 2, pp. 901-908, 1999.
- [23] M. Li, C. Tse, H.-C. Iu and X. Ma, "Unified Equivalent Modeling for Stability Analysis of Parallel-Connected DC/DC Converters," *Circuits and Systems II: Express Briefs, IEEE Transactions on*, vol. 57, no. 11, pp. 898-902, Nov. 2010.
- [24] H. Zhou, T. Duong, S. T. Sing and A. Khambadkone, "Interleaved bidirectional Dual Active Bridge DC-DC converter for interfacing ultracapacitor in micro-grid application," *Industrial Electronics (ISIE), 2010 IEEE International Symposium on*, pp. 229-2234, July 2010.
- [25] J.-S. Lai, B. York, A. Koran, Y. Cho, B. Whitaker and H. Miwa, "High-efficiency design of multiphase synchronous mode soft-switching converter for wide input and load range," *Power Electronics Conference (IPEC), 2010 International*, pp. 1849-1855, June 2010.
- [26] Maksimovic, D., "Design of the zero-voltage-switching quasi-square-wave resonant switch," *Power Electronics Specialists Conference, 1993. PESC '93 Record., 24th Annual IEEE*, vol., no., pp.323,329, 20-24 Jun 1993.
- [27] Costa, J.M.F.D.; Silva, M.M., "Small-signal models and dynamic performance of quasi-square-wave ZVS converters with voltage-mode and current-mode control," *Circuits and Systems, 1995., Proceedings., Proceedings of the 38th Midwest Symposium on*, vol.2, no., pp.1183-1188 vol.2, 13-16 Aug 1995.
- [28] Yang, L.; Zhang, Y.; Lee, C.Q., "A family of constant-switching-frequency quasi-square-wave converters," *Electrical and Computer Engineering, 1993. Canadian Conference on*, vol., no., pp.309,312 vol.1, 14-17 Sep 1993.
- [29] Yang, L.; Zhang, Y.F.; Lee, C.Q., "Analysis of the boost constant-frequency quasi-square-wave converters," *Circuits and Systems, 1994., Proceedings of the 37th Midwest Symposium on*, vol.2, no., pp.1172,1175 vol.2, 3-5 Aug 1994.
- [30] Knecht, O.; Bortis, D.; Kolar, J.W., "Comparative Evaluation of a Triangular Current Mode (TCM) and Clamp-Switch TCM DC-DC Boost Converters," *Energy Conversion Congress and Exposition (ECCE 2016, IEEE)*, vol., no., pp., 18-22 September 2016.
- [31] Andreassen, Pal; Undeland, T.M., "Digital Control Techniques for Current Mode Control of Interleaved Quasi Square Wave Converter," *Power Electronics Specialists Conference, 2005. PESC '05. IEEE 36th*, vol., no., pp.910,914, 16-16 June 2005.
- [32] Jong-Bok Baek; Woo-In Choi; Bo-Hyung Cho, "Digital Adaptive Frequency Modulation for Bidirectional DC-DC Converter," *Industrial Electronics, IEEE Transactions on*, vol.60, no.11, pp.5167,5176, Nov. 2013.
- [33] Yousefzadeh, V.; Babazadeh, A.; Ramachandran, B.; Alarcon, E.; Pao, L.; Maksimovic, D., "Proximate Time-Optimal Digital Control for Synchronous Buck DC-DC Converters," *Power Electronics, IEEE Transactions on*, vol.23, no.4, pp.2018,2026, July 2008.
- [34] A. Vazquez, A. Rodríguez, D. G. Lamar and M. M. Hernando, "Master-slave technique for improving the efficiency of interleaved synchronous boost converters," *2014 IEEE 15th Workshop on Control and Modeling for Power Electronics (COMPEL), Santander, 2014*, pp. 1-9.
- [35] A. Rodríguez, A. Vázquez, D. G. Lamar, M. M. Hernando and J. Sebastián, "Different Purpose Design Strategies and Techniques to Improve the Performance of a Dual Active Bridge With Phase-Shift Control," in *IEEE Transactions on Power Electronics*, vol. 30, no. 2, pp. 790-804, Feb. 2015.
- [36] R.W. Erickson, D. Maksimovic, "Fundamentals of Power Electronics," 2nd Edición, Springer Science+Business, 2001.
- [37] Canesin, C.A.; Gonçalves, F.A.S., "A Multi-Cell Variable Frequency Interleaved ZCS Boost Rectifier Digitally Controlled by FPGA," *Industrial Electronics, 2006 IEEE International Symposium on*, vol.2, no., pp.1382,1387, 9-13 July 2006.
- [38] Huber, L.; Irving, B.T.; Adragna, C.; Jovanovic, M.M., "Implementation of open-loop control for interleaved DCM/CCM boundary boost PFC converters," *Applied Power Electronics Conference and Exposition, 2008. APEC 2008. Twenty-Third Annual IEEE*, vol., no., pp.1010,1016, 24-28 Feb. 2008.
- [39] Hangseok Choi, "Interleaved Boundary Conduction Mode (BCM) Buck Power Factor Correction (PFC) Converter," *Power Electronics, IEEE Transactions on*, vol.28, no.6, pp.2629,2634, June 2013.
- [40] Sang Hee Kang; Maksimovic, D.; Cohen, I., "Efficiency Optimization in Digitally Controlled Flyback DC-DC Converters Over Wide Ranges of Operating Conditions," *Power Electronics, IEEE Transactions on*, vol.27, no.8, pp.3734,3748, Aug. 2012.
- [41] O. Garcia, P. Zumel, A. de Castro and A. Cobos, "Automotive DC-DC bidirectional converter made with many interleaved buck stages," *Power Electronics, IEEE Transactions on*, vol. 21, no. 3, pp. 578-586, May 2006.
- [42] Jen-Ta Su; Chih-Wen Liu, "A Novel Phase-Shedding Control Scheme for Improved Light Load Efficiency of Multiphase Interleaved DC-DC Converters," *Power Electronics, IEEE Transactions on*, vol.28, no.10, pp.4742-4752, Oct. 2013.
- [43] Ying-Chi Chen; Jihh-Da Hsu; Yong-Ann Ang; Ta-Yung Yang, "A new phase shedding scheme for improved transient behavior of interleaved Boost PFC converters," *Applied Power Electronics Conference and Exposition (APEC), 2014 Twenty-Ninth Annual IEEE*, vol., no., pp.1916,1919, 16-20 March 2014.
- [44] M. Kasper, R. M. Burkart, G. Deboy and J. W. Kolar, "ZVS of Power MOSFETs Revisited," in *IEEE Transactions on Power Electronics*, vol. 31, no. 12, pp. 8063-8067, Dec. 2016.
- [45] Saggini, S.; Orietti, E.; Mattavelli, P.; Pizzutelli, A.; Bianco, A., "Fully-digital hysteretic voltage-mode control for dc-dc converters based on asynchronous sampling," *Applied Power Electronics Conference and Exposition, 2008. APEC 2008. Twenty-Third Annual IEEE*, vol., no., pp.503,509, 24-28 Feb. 2008.
- [46] Abu-Qahouq, J.; Hong Mao; Batarseh, I., "Multiphase voltage-mode hysteretic controlled DC-DC converter with novel current sharing," *Power Electronics, IEEE Transactions on*, vol.19, no.6, pp.1397-1407, Nov. 2004.
- [47] Kohama, T.; Sogawa, Y.; Tsuji, S., "Design of optimized on-off control to improve efficiency of paralleled converter system," *Power Electronics Conference (IPEC-Hiroshima 2014 - ECCE-ASIA), 2014 International*, vol., no., pp.2781, 2786, 18-21 May 2014.
- [48] Hien Nguyen; Zane, R.; Maksimovic, D., "ON/OFF Control of a Modular DC-DC Converter Based on Active-Clamp LLC Modules," *Power Electronics, IEEE Transactions on*, vol.30, no.7, pp.3748,3760, July 2015.

- [49] C. W. C. E. C. B. Brooks, "Guideline for the use of the Performance Test Protocol for Evaluating Inverters Used in Grid-Connected Photovoltaic Systems," 2005. [Online]: http://www.gosolarcalifornia.ca.gov/equipment/documents/Sandia_Guideline_2005.pdf. [Last accessed: Jun. 2014].
- [50] EC 1275/2008 Regulation of 2005/32/EC, EcoDesign. European Parliament. December 2008. [Online]: <http://ec.europa.eu/enterprise/policies/sustainable-business/ecodesign/>. [Last accessed: Jul. 2015].
- [51] EC 278/2009 Regulation of 2005/32/EC, EcoDesign. European Parliament. April 2009. [Online]: <http://ec.europa.eu/enterprise/policies/sustainable-business/ecodesign/>. [Last accessed: Jul. 2015]



Aitor Vazquez (S'2010, M'2015) was born in Oviedo, Spain, in 1984. He received the M.Sc. degree in telecommunication engineering, in 2009, and the Ph.D. degree in electrical engineering in 2016, from the University of Oviedo, Gijon, Spain. Since 2010 he has been a researcher with the Power Supply System Group and an Assistant Professor with the Department of Electrical and Electronic Engineering at the University of Oviedo. His current research interests

include modularization techniques applied to bidirectional dc-dc converters for HEV, battery management power supplies, DC distribution grids, power factor corrector ac-dc converters and energy recovery systems.



Alberto Rodriguez (S'2007, M'2014) was born in Oviedo, Spain, in 1981. He received the M.S. degree in telecommunication engineering in 2006 from the University of Oviedo, Gijón, Spain, and the Ph.D. degree in electrical engineering in the same university in 2013. Since 2006, he has been a researcher with the Power Supply System Group and an Assistant Professor with the Department of Electrical and Electronic Engineering at the University of Oviedo. His research interests are focused on multiple ports

power supply systems, bidirectional DC-DC power converters and wide band gap semiconductors.



Diego G. Lamar (M'2008) was born in Zaragoza, Spain, in 1974. He received the M.Sc. degree, and the Ph.D. degree in Electrical Engineering from the University of Oviedo, Spain, in 2003 and 2008, respectively. In 2003 and 2005 he became a Research Engineer and an Assistant Professor respectively at the University of Oviedo. Since September 2011, he has been an Associate Professor. His research interests are focused in switching-mode power supplies, converter modelling, and power-factor-

correction converters.



Marta M. Hernando (M'1995-SM'2011) was born in Gijon, Spain, in 1964. She received the M.Sc. and Ph.D. degrees in Electrical Engineering from the University of Oviedo, Gijon, Spain, in 1988 and 1992, respectively. She is currently a Professor at the University of Oviedo. Her main interests include switching-mode power supplies and high-power factor rectifiers.