Switching frequency optimization for a Solid State Transformer with Energy Storage Capabilities

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Abstract—This paper is focused on establishing a procedure for measuring the efficiency dependency on the switching frequency for a solid state transformer (SST), being one of the ports connected to an energy storage device (Lithium-Ion battery). Multiple contributions for measuring the efficiency/losses for different power converter structures for energy storage applications can be found in the literature. However, there are few references which consider the effects of the high frequency model of the battery in the complete system performance. This research will obtain a parametric high frequency model of the battery cells, based on a vector fitting method in frequency domain. This model will be used for the estimation of the overall system losses. It will be demonstrated that the contribution of the battery losses, as well as its behavior as a function of the switching frequency, can significantly affect the selection of the converter's switching frequency.

I. INTRODUCTION

Lately, there is an increased interest in the use of isolated multiport converters for interfacing multiple energy sources, loads and/or Energy Storage Systems (ESS) [1]. One solution for this interfacing converter is based on the so-called Solid-State Transformer (SST), which allows for removing the low frequency transformer usually employed for achieving the required galvanic isolation. There are several key aspects to be improved in the SST design, being the efficiency one of the most important. For the efficiency estimation, there are some contributions in the literature [2]–[5] with values ranging from 88% to 97%.

When an ESS is integrated in one of the converter ports, it is critical to consider its contribution to the overall efficiency and, moreover, to determine the safe operation conditions for the ESS itself. The impact of the converter switching harmonics on Lithium-Ion batteries has been already discussed [5]. For the integration of the ESS there are two main options: 1) to

use a dedicated DC/DC converter for the interface or 2) to directly connect the battery to the DC side of one of the ports. When possible, the second option is preferred due to both cost reduction and increased reliability on the power electronics interface. However, the interface without any active element will impose on the battery higher stresses due to the current harmonics. In order to mitigate the current ripple effects, a film capacitor for the dc-link can be put in parallel with the battery and, if required, a series inductance on the converter DC terminals. Still, adding passive elements decreases the overall reliability of the system and thus its use should be optimized.

Considering the effects of the switching harmonics, it is clear that the switching frequency value will affect different system elements in opposite ways. For the case of the power converter, increasing the switching frequency will increase the switching losses. However, considering the impact on the battery, higher values will reduce the losses and the current ripple due to the inductive behavior. For these reasons, the losses at the different elements in the system must be considered. In this paper, the following losses are included: 1) losses at the input and output bridges, including voltage drop in the semiconductors and dead-time effects; 2) winding losses on the high-frequency transformer; 3) conduction losses at the series filter; 4) conduction losses at the dc-link and 5) high frequency losses at the battery cells.

In order to analyze and characterize these losses, this paper is organized as follows. Section II will include a description of the system where the ESS is used. Section III will show the proposed high frequency analytical model as well as the experimental characterization of the battery cells and the parameter estimation. Section IV will consider the high frequency model for the converter passive elements, i.e. transformer, series inductances and dc-link capacitor. Section V will include the simulation results as well as the experimental validation for the calculation of the power converter efficiency under different working conditions.

II. System description

Regarding the power converter options, Fig. 1 shows three alternative power converter topologies. All of them are classified as bidirectional multiport DC-DC converters with galvanic isolation for the integration of an ESS. For option 1a), an additional power conversion state between the ESS and the power converter port can be used (with the same topologies proposed in 1b) or 1c)).

For this paper, option 1a) is used. Even if the real setup consists on a Tripple-Active-Bridge (TAB) converter. As explained in Section II, only two of the ports are considered during the analysis. This simplification will allow to focus the study on the energy storage losses, removing the additional control complexity in the TAB converter. It is also worth noting that, even if some previous research has been conducted for the efficiency calculation in power converters with energy storage capabilities, [5], [6], there are not investigations considering active bridge converter based configurations without resonant network topologies. On these kind of converters, it is expected that the high pulsating nature of the DC currents (often filtered with a parallel connected dc-link capacitor) potentially affects the battery-aging.

The TAB with the ESS is used as the interface of a low-voltage distribution microgrid, as shown in Fig. 2. The TAB internal structure and the laboratory setup are shown in Fig. 3 and 4 respectively. The high-side DC link for the first port is connected to the AC main grid three-phase active rectifier, the second port is connected to the ESS and the third one to the low-side DC link. At the low-side DC link there are two independent 4-wire inverters, namely head nanogrid converters (HNGC), providing the AC distribution downstream to the so called nanogrid (nG). For the control of the TAB, the power-flow at the high-side (i_{hs}) and ESS (i_{ess}) ports are controlled by means of the corresponding currents at each port, whereas the dc-link voltage at the low side (v_{ls}) is controlled by the low-side port. A more detailed explanation can be found in [7].

For this paper, a simplified power and control structures are selected in order to keep the focus on the losses impact due to the ESS. The high-side port is disconnected, and the analysis is restricted to the ess and ls ports. The v_{ls} voltage is controlled by one of the nanorgrid head converters and the solid state transformer operates in power control mode, thus enabling the evaluation of the bidirectional power flow between the battery and the low-side port. This allows for investigating the effects on the losses due to the charge/discharge of the battery operated at different power levels. Under that considerations, the analyzed system is reduced to a double-active-bridge (DAB), as shown in Fig. 5.

III. Battery cells high frequency model

In order to derive the model for the ESS, the battery has to be modeled at cell level. For that purpose, firstly the cells' high frequency impedance has been recorded in the laboratory. Secondly, the parameters of the battery model have been estimated by a vector fitting method. The investigated cell is a 18650-sized high-energy round cell with a nominal capacity $C_{Nominal,Cell}$ of $3.2Ah$ and a nominal cell voltage $U_{Nominal,Cell}$ of $3.3V$. On obtaining the proposed high frequency model, it has to be mentioned that the impedance spectrum of a battery is dependent on the actual state of charge (SOC), the temperature and cycling [8]–[10]. The SOC effect will be later shown during the presentation of the experimental results.

For the impedance spectrum recording, an Agilent 4294A Precision Impedance Analyzer has been used. The device is capable of taking measurements in the impedance range of 1mOhm to 1MOhm with an accuracy of 0.08% and operates in the frequency range of $40Hz - 110MHz$. For a good accuracy the cell was connected via high frequency coaxial cables to the terminal connection, applying the four-point probes method [11]. The scheme of the setup, as well as the considered high frequency model, is shown in Fig. 6. The high frequency model topology has been already proposed in previous literature references [12].

All measurements have been recorded in the range of $40Hz - 200kHz$ in potentiostatic mode (constant voltage amplitude for the excitation signal) with a $100mV$ amplitude and an averaging factor of 16. Moreover, a DC-Bias voltage has been applied in order not to charge or discharge the battery. The ambient and the cell's temperature and were kept constantly at 27 degrees C during the measurement. The temperature was observed with an HIBOK75 infrared thermometer.

As presented in [12], the impedance based high frequency model shown in Fig. 6, consists of two resistors and two inductors. The parameters of this model were derived by approximating the frequency response of the cells for different SOC with the expression shown in (1), where s is the Laplace variable [13]–[15].

$$f(s) \approx \sum_{m=1}^{N} \frac{c}{s-a} + d + se \qquad (1)$$

The relationship between the coefficients shown on (1) and the high-frequency model parameters have been done as follows. Using the equivalent high-frequency model shown in Fig. 6, the cell high frequency impedance is given by (2)

$$Z_{cell}(s) = R_1 + sL_1 + \frac{L_2 s R_2}{L_2 s + R_2} \qquad (2)$$

By comparing the polynomial coefficients of (1) and (2), the equivalences in (3) and (4) can be obtained.

$$R_1 = \frac{d \cdot a - c}{a}; \quad R_2 = d - \frac{d \cdot a - c}{a} \qquad (3)$$

$$L_1 = e; \quad L_2 = \frac{1}{a}\left(d - \frac{d \cdot a - c}{a}\right) \qquad (4)$$

The estimated parameters for the two different SOCs of 50% and 100% are presented in Table I.

A comparison between the measured and the modeled impedance (magnitude and phase) is presented in Fig. 7 and Fig. 8 for 50% and 100% SOC respectively. As it is clearly
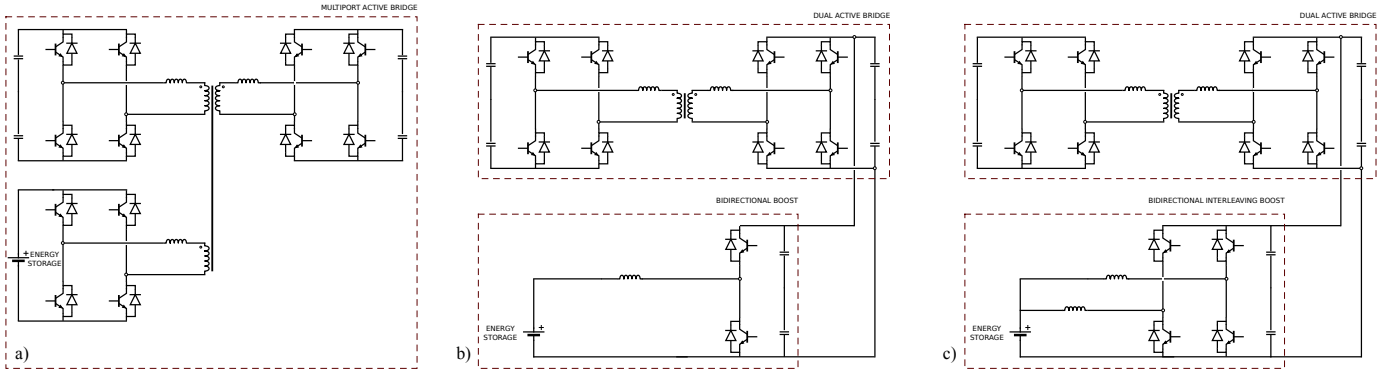
Fig. 1. Considered bidirectional multiport DC-DC converters with galvanic isolation. a) Triple-Active-Bridge with ESS integrated in one of the ports, b) Dual-Active-Bridge with ESS integrated by using a bidirectional boost converter, c) Dual-Active-Bridge with ESS integrated by using a bidirectional interleaving boost converter.
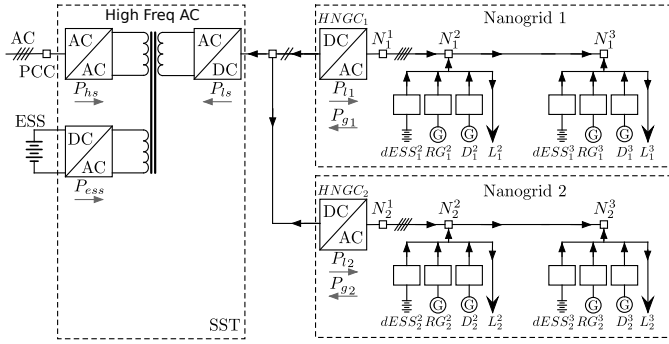

Fig. 2. Proposed MG structure. The 3P-SST allows for the exchange of power among the different grid points (AC mains, centralized ESS and AC nG). Each of the nG is powered by a 4-wire HNGC. The internal nodes (N_x^y) of the two nG represent buildings to which the different loads (L_x^y), DG (both renewable, RG_x^y, and dispatchable, D_x^y) and dESS are connected.

Fig. 4. Experimental setup. The figure shows the TAB and low-side converter as well as the ESS.
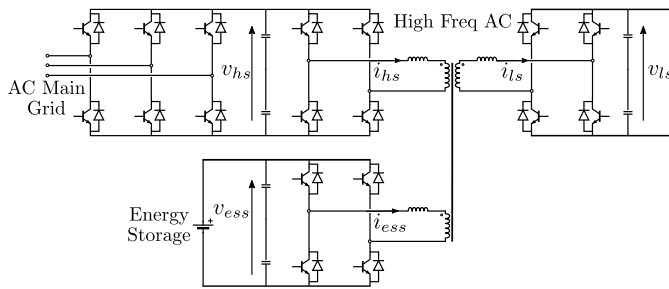
Fig. 3. TAB internal structure and variables used for the control implementation.
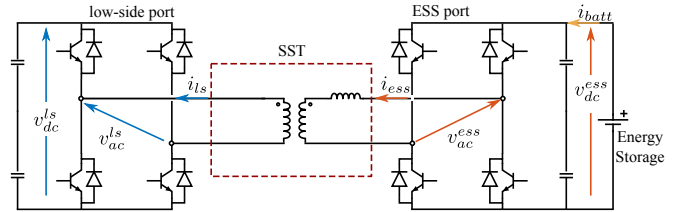
Fig. 5. Double-Active-Bridge topology used for the paper analysis.

shown, there is a good matching between the real data and the approximation. Also, both cells have a similar behavior, which validates the approach of modeling few cells in order to get the complete high frequency model of the storage system by the needed parallel/series connection.

The complete ESS is built by 8 modules connected in series. Each of the modules has an arrangement of 15 parallel strings, being each string made by 15 cells connected in series. This leads to the final electrical model for the overall impedance: 120 series cells and 15 parallel strings. The complete system

transfer function is then given by the equivalent impedance (5).

$$Z_{batt}(s) = \frac{c_{series}}{s_{parallel}} = \frac{120}{15} = 8 \cdot Z_{cell}(s) \qquad (5)$$

This assumption is also consistent with the low dispersion found in the parameters of the Lithium-Ion cells when dealing with the traditionally used low-frequency models [16], [17]. It is also easily perceived the expected inductive behavior of the cells on the high frequency region. As it also can be seen, there is a noticeable difference on the impedance values, depending on the SOC which could potentially affect the overall performance of the power converter, as later discussed in Section V.
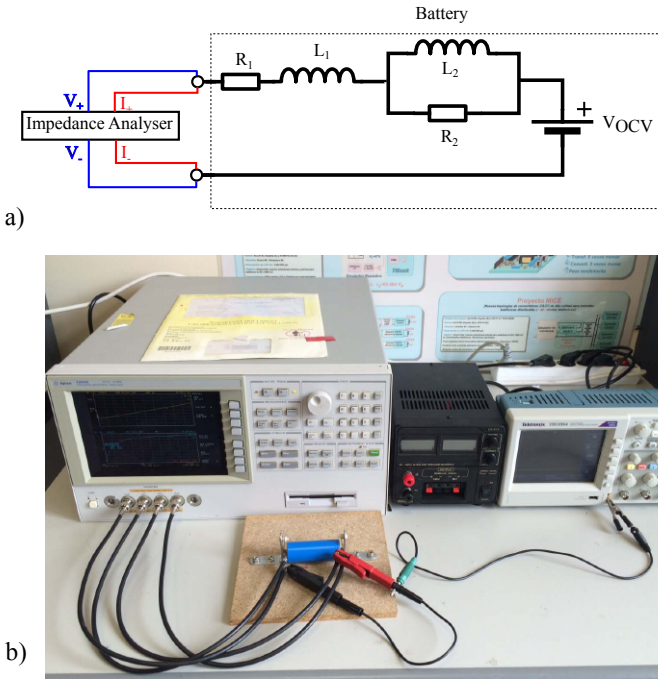
Fig. 6. Impedance measurement setup. a) Connection scheme and used high-frequency model. b) Measurement setup using the impedance analyzer.

Fig. 7. Measured and approximated impedance for SOC = 50%

TABLE I
ESTIMATED BATTERY PARAMETERS

Parameter	100% SOC	50% SOC
R_1	50.66 $m\Omega$	115.0 $m\Omega$
R_2	28.4 $m\Omega$	6.9 $m\Omega$
L_1	2.6847 μH	2.4307 μH
L_2	0.13364 μH	0.61274 μH

IV. POWER CONVERTER HIGH FREQUENCY MODEL

For the power converter characterization, different elements have been measured in the high frequency region by first using the same impedance analyzer than for the battery cells. The solid state transformer, series inductances and power stack have been considered. This will allow to build a precise high frequency model of the complete system.

The transformer impedance, series inductances and power stack impedances are shown in Fig. 9, 10 and 11. It is worth noting that for the case of the power stack measurements, the impedance between the positive and negative terminals of the stack has been recorded. That impedance accounts for the dc link, the snubbers and the discharge resistance. This overall impedance, dominated by the dc-link value, is connected in parallel with the ESS and thus affecting the share of the high frequency components.

From the data depicted at Fig. 9, the parameters for the transformer high frequency model have been obtained. The equivalent circuit as well as the corresponding values is shown in Fig. 12. It is recalled here that even if the transformer is a three port, just the two ports interfacing the ESS and the low-side dc link are represented. Still, for setting the values, the standard procedure for three-winding transformers have been used [18].
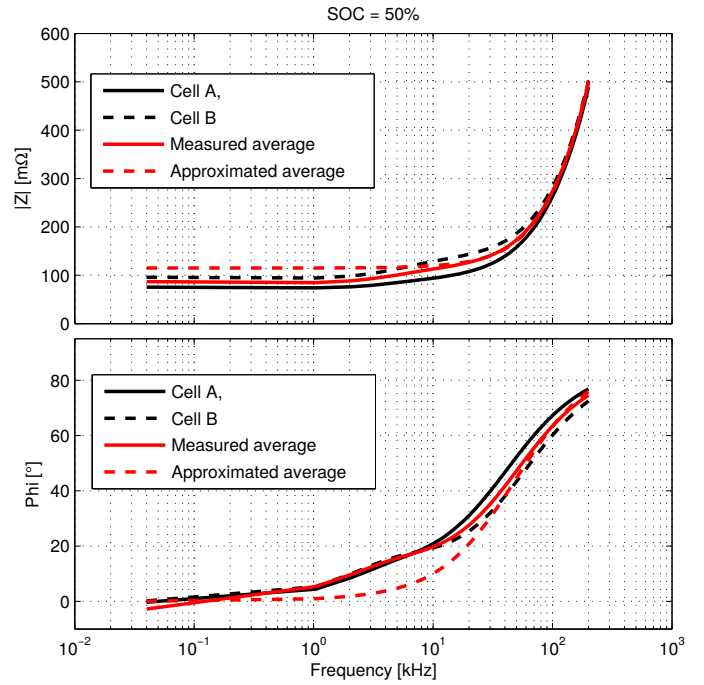

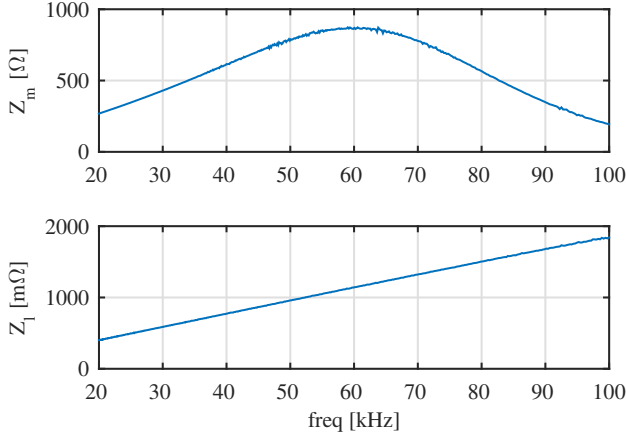Fig. 8. Measured and approximated impedance for SOC = 100%

Fig. 9. Transformer high frequency impedance. Top, magnetizing impedance. Bottom, leakage impedance $20 - 100$kHz.

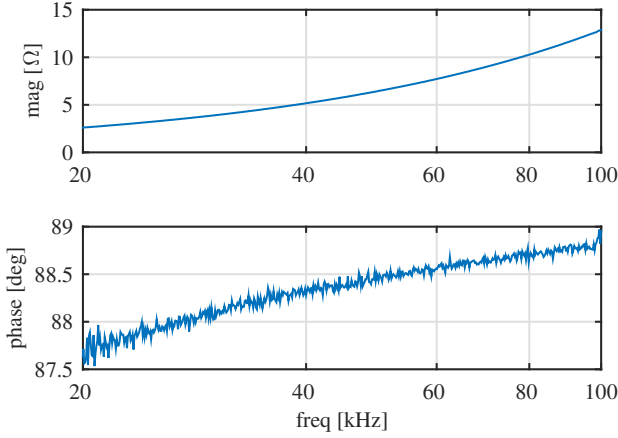Fig. 11. Stack high frequency impedance in the range $20 - 200$kHz.

Fig. 10. Stack high frequency impedance in the range $20 - 100$kHz.

$R_1 = 4m\Omega \quad L_1 = 90nH \qquad R'_2 = 4m\Omega \quad L'_2 = 110nH$

Primary

$C_m = 3.3nF$

Secondary

$R_m = 870\Omega$

$L_m = 2.1mH$
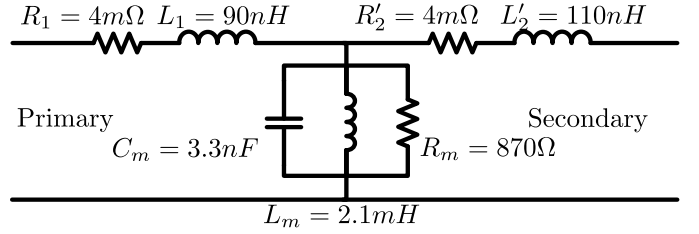
Fig. 12. SST model and experimentally measured parameters including parasitic elements.

V. POWER CONVERTER OPERATION AND EFFICIENCY MEASUREMENT

A. Simulation results

With the developed high-frequency model of the cell, several simulations have been carried out. The operation has been tested by integrating the ESS into a DAB power converter, as shown in Fig. 5. The power converter has been initially designed for a nominal switching frequency of $20kHz$. Different switching frequencies below and above the nominal one (range of $16kHz$ to $24kHz$) have been used and the efficiency has been calculated when the converter reached the steady state operation. DC-link total capacitance has been varied for each switching frequency in order to keep the current ripple at the battery terminals at 1% level. Using a single-phase shift [19], the transferred power through the inductor in the DAB can be described as (6).

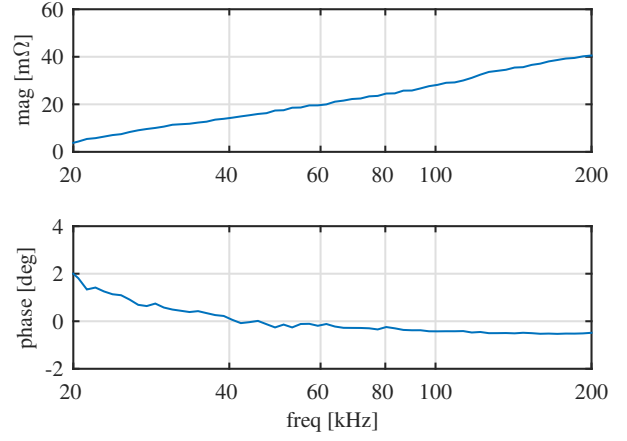$$P_{DAB} = \frac{V_{out}^2 \phi(\pi - \phi)}{(2\pi f_s)L\pi} \qquad (6)$$

For the following measurements the phase shift angle, ϕ, has been set to 90 degrees in order to achieve the maximum power transfer capability. The measurement of the efficiency at each element is described here:

- **Power converters**. Considering the power going from the sending port (s) to the receiving port (r), the efficiency at the sending power converter is calculated as $\eta_s = \frac{v_{ac}^s i_{ac}^s}{v_{dc}^s i_{dc}^s}$ and at the receiving as $\eta_r = \frac{v_{dc}^r i_{dc}^r}{v_{ac}^r i_{ac}^r}$.

- **High frequency transformer and series inductor**. The efficiency of both elements is measured as a single element, using the ratio of the AC power at the receiving port (output) to the power of the sending port (input). $\eta_{sst} = \frac{v_{ac}^r i_{ac}^r}{v_{ac}^s i_{ac}^s}$. The model used for the SST, including the parasitic elements, is shown in Fig. 12. The used transformer is a planar transformer, and its parameters have been experimentally measured as explained before.

- **Battery losses**. The losses account for the capacitor bank and the battery itself. For the capacitor bank, the losses have been calculated using the equivalent ESR (real part of the dc-link impedance). For the case of the battery, using the proposed high frequency model shown in Fig. 6. The efficiency is calculated as the ratio between the power delivered to the battery ideal voltage source (V_{ocv}) and the power at the converter DC terminals (v_{dc}^r).

The resulting efficiency measurements are depicted in Fig. 13. The aforementioned conditions, switching frequencies between $[16, 20]kHz$ and 90deg for the phase shift were used

in order to get the maximum power transfer.

Important conclusions can be obtained from the results analysis. Considering the efficiency of the individual system elements, Fig. 13a), the DAB has, independently of the frequency, the maximum efficiency of all the elements. The input and output bridges both have a mostly constant efficiency, showing a decrease in the efficiency trend with increased switching frequency, as expected from the increased switching losses. However, when adding the effect of the battery high frequency model to the output bridge, there are significant differences. First of all, there is a reduction in the efficiency due to the battery high frequency losses. Also, there is an important dependency on the SOC, being the efficiency higher with higher SOC. Since the efficiency is increased with increased frequencies (inductive behavior of battery high frequency model), it is expected that this changes the optimal switching frequency. It is also worth noting the reduction in the losses by adding a parallel capacitor to the battery ($C = 5\mu F$). Analyzing the overall system efficiency, as shown in 13b), the switching frequency at which the maximum efficiency is located varies noticeable with the battery SOC and the selected parallel capacitors. This opens the possibility of operating the power converter at variable switching frequency in order to minimize the system losses.
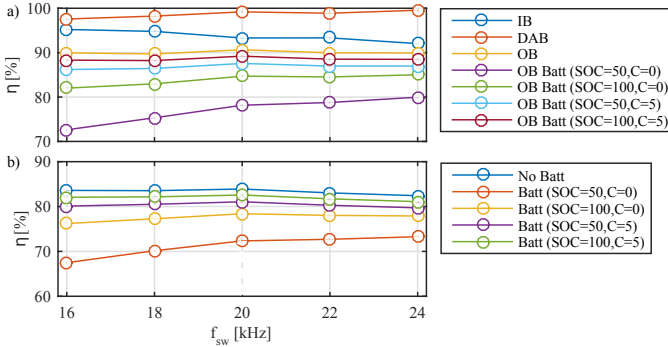

Fig. 13. Estimated efficiency calculations for the overall converter structure. a), the efficiency results for the individual elements is shown. b), the overall system efficiency is depicted. IB, input bridge; DAB, transformer; OB, output bridge; SOC state of charge; C connected parallel capacitor with the battery in μF.

B. Experimental results

For the experimental results validation, the setup previously shown in Fig. 4 has been used. The most important parameters both for the converter and the ESS are shown in Table II.

Several experiments were conducted in order to evaluate the impact of the selection of the switching frequency. By using a similar strategy to the one taken during the simulation results, the power converter was first measured working under different switching frequencies $[16 - 20kHz]$. The power was kept constant at the different frequencies by adjusting the phase shift. The converter is operated in open loop in order to keep the phase shift constant during the measurements. The results for the efficiency calculation are shown in Fig. 15. As

Parameter	Value
Power Converter	
Power	150kVA
Switching freq.	20kHz
Port 1	Header Converter 750Vdc
Port 2	ESS 375Vdc
Port 3	Inner Microgrid. Low DC link 750Vdc
DC-link capacity (each port)	$420\mu F$
Series inductors (Port 2 and 3)	$38\mu H$
Li-Ion Battery	
Rated voltage	384V
Max. voltage	438V
Max. discharge current (2C)	96A
Max. charge current (3C)	144A
Nom. capacity	18.4kWh

expected, due to the switching losses, the converter efficiency decreases with the frequency.

Following, a complete set of experiments considering the power flow between the battery and a load connected at the low-side port (36Ω resistive load), have been carried out. During all the experiments, the SOC of the battery was kept to the 80%. The waveforms shown in Fig. 14 were captured with an scope with a sample time of $0.5\mu s$. Isolated voltage probes (100MHz bandwidth, 1000:1) were used for the voltage measurements and current probes (DC-150MHz, 300APeak) for the currents. The data was stored and processed offline for getting the efficiency values. For calculating the battery losses, the derived high-frequency model has been used.

In Fig. 16, the different powers measured at the two involved transformer ports, considering also the dc side for the case of the battery port and the battery losses normalized with respect to the dc port power are shown. From the figure it is clear that the battery losses are reduced with increasing switching frequencies, as expected due to the inductive behavior of the high frequency model.

In Fig. 17, the efficiencies for the individual elements of the power converter are shown. As it can readily seen, the efficiency of the battery and the efficiency of the battery bridge and transformer follow opposite trends. As already explained, this is due to the inductive behavior of the battery and the switching losses at the switches and at the transformer. Because of that opposite trend, an optimal point for the switching frequency is expected. This is confirmed with the results depicted in Fig. 18, where the converter efficiency with and without the battery is represented. Obviously, adding the battery results in a lower overall efficiency for a percentage varying between almost 10% to 2%. However, it is more important the fact that the overall efficiency curve has a maximum in the vicinity of $22kHz$, which moves apart from the converter nominal frequency by a 10%. The boost in the efficiency with respect to the nominal frequency is around 1%, which is an important contribution to the complete system efficiency. It is also important to remark that the obtained experimental results are in agreement with the ones predicted by the simulation.
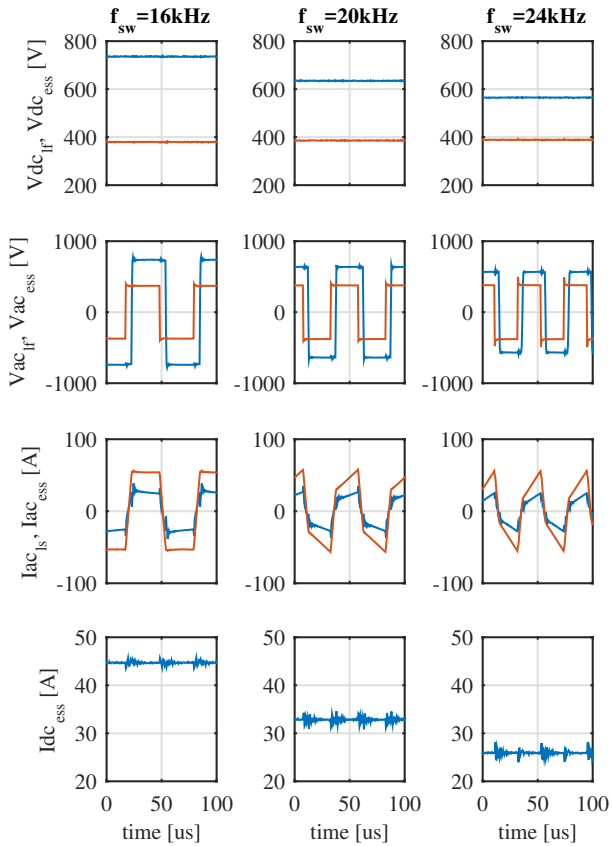
Fig. 14. Experimental results. Recorded waveforms for the dc voltages, ac voltages, ac currents and battery dc current for three different switching frequencies. When two traces appear, blue color is used for the low-side port and red for the ESS port.

VI. CONCLUSION

This paper has developed an analysis on the selection of the switching frequency effects for an isolated power converter with integrated ESS. As shown in the results, the battery losses are dependent on the switching frequency. Moreover, the contribution of the battery losses to the overall efficiency can have a noticeable effect. This makes the selection of the optimal switching frequency a non-trivial task. For determining the switching frequency effects on the complete system, the high frequency model of the solid state transformer, the power stack and the battery cells at two different SOC have been experimentally obtained. The efficiency of the power converter has been calculated using a full scale laboratory setup. By operating the converter at variable switching frequency, $[16 - 20kHz]$, the losses on the real battery, for a SOC of 80%, have been experimentally calculated and their impact have been extensively discussed. As shown, a boost of 1% in the overall system efficiency can be achieved by proper selection of the switching frequency. It is worth remarking that this result depends on the selection of the dc-link capacitance. Additional experiments considering different SOC as well as
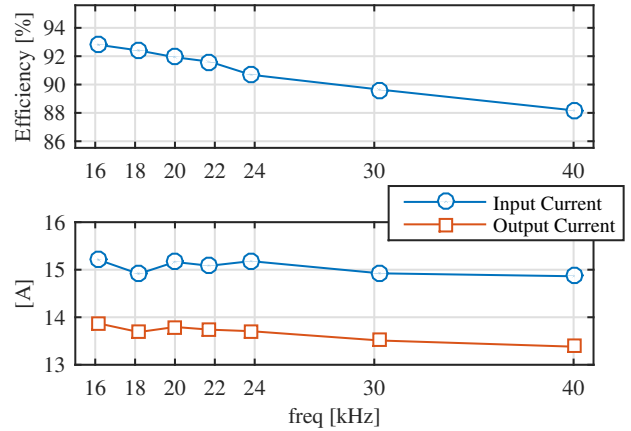

Fig. 15. Experimental results. Measured efficiency with the power converter operated in open loop under different switching frequencies. The power is kept constant by adjusting the phase shift.
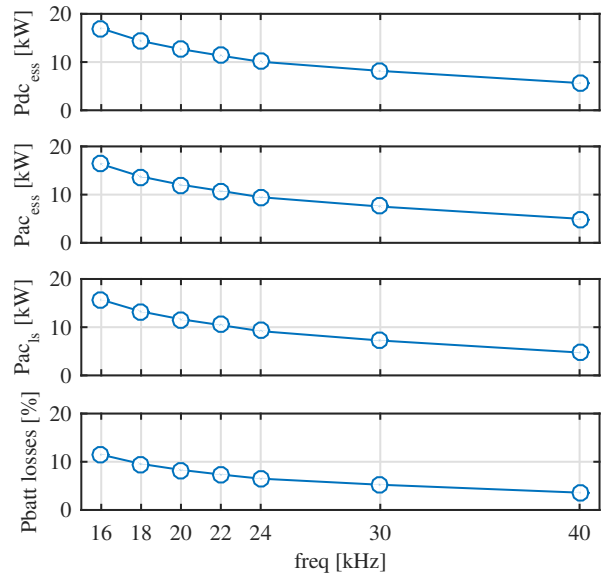

Fig. 16. Experimental results. Power and ESS losses in function of the switching frequency. From top to bottom: a) power at the dc side of the battery port, b) power at the ac side of the battery port, c) power at the ac side of the low port, d) battery losses normalized with respect to the dc power.

an online implementation of a varying switching frequency strategy and low-side dc-link voltage control are part of ongoing research.
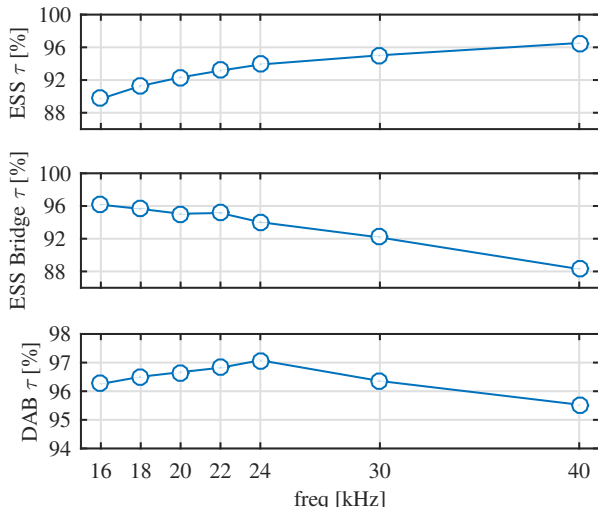
VII. ACKNOWLEDGMENTS

Fig. 17. Experimental results.Power converter efficiency in function of the switching frequency. From top to bottom: a) battery efficiency, b) battery port efficiency, c) transformer and series inductance efficiency
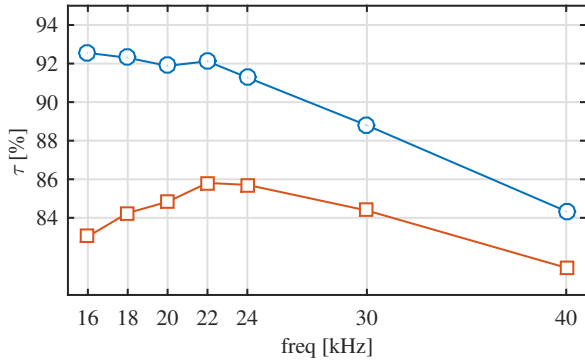

Fig. 18. Experimental results. Compared efficiency of the power converter (blue) and the power converter with the battery (red). As it can be seen the battery efficiency creates a maximum at $22kHz$ which boost the efficiency for a 1%.

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