A sustained increase of input current distortion in active input current shapers to eliminate electrolytic capacitor for designing ac to dc HB-LED drivers for retrofit lamps applications

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***Abstract*—Nowadays, the solid-sate lighting technology evolution has changed traditional solutions in lighting. High-Brightness Light–Emitting Diodes (HB-LEDs) have become very attractive light sources due to their excellent characteristics: high efficiency, high life-time and low maintenance. It is evident that HB-LED drivers must be durable and efficient to achieve these advantages. Moreover, for replacing incandescent bulbs, the ac-dc HB-LED driver must be low cost and comply with international regulations (i.e. injection of low frequency harmonics into the mains). Traditionally, authors have focused its efforts on increasing efficiency. All these solutions obviate the elimination of traditional electrolytic capacitor of ac to dc converters, highlighting that this is the price to pay for a very low-cost solution. This paper presents a new proposal to design a simple and low-cost ac to dc HB-LED driver for retrofit lamps without electrolytic capacitor. The proposed solution comes from a very well-known technique used in the past: Active Input Current Shapers (AICS), but in this case without electrolytic capacitor. If the electrolytic capacitor of an AICS is removed, then low frequency ripple arises in its intermediate dc bus, increasing the distortion of the line input which already has appreciable distortion. However, the increase of distortion is very slight. Also, the low frequency ripple is not transferred to the output due to the high output dynamic response of AICS, avoiding flickering. This paper presents a theoretical analysis that guarantees a trade of between compliance with international regulations and the use of other capacitor technologies different from the electrolytic one. Finally, a 24W experimental prototype has been built and tested in order to validate the theoretical results presented in this digest.**

Keywords—Ac to dc power conversion, harmonic distortion, LEDs, lighting, power factor, switched mode power supplies.

I. INTRODUCTION

It is known that High-Brightness Light–Emitting Diodes (HB-LEDs) are a fast emergent technology, considered as the true alternative to many mature technologies (i.e. incandescent bulbs, compact fluorescent lamps, etc.) due to its high efficiency, low maintenance and durability. To perform these advantages HB-LED drivers must be both durable and efficient.

Since HB-LEDs are diodes, the default method for driving them is controlling the dc forward current trough this semiconductor device. If the primary energy source is the ac line, then some type of ac to dc converter must be placed between the line and the HB-LEDs. Also, it is known that the low-frequency harmonic content of the line current must comply with specific regulations (IEC 61000-3-2 [3-5] and ENERGY STAR® program [6]). Traditionally, these regulations establish a very strict harmonic content for lighting (e.g. IEC 61000-3-2, Class C), so that only sinusoidal line waveforms is able to comply with the aforementioned regulations. Therefore, the only practical method to comply with these regulations is to use active high Power Factor (PF) converters. These converters are known as Power Factor Correctors (PFCs), which are expensive and complex solutions. However, for power levels lower than 25 W the compliance with IEC 61000-3-2 regulation becomes more relaxed due to the fact that luminaries must comply with this regulation in Class D [6]. Hence, new solutions can arise.

A possible application for substituting incandescent bulbs lamps is to use two strings of around 10 HB-LEDs of 1 W in parallel connected to the output of an ac to dc driver to produce the same luminance flux as the one produced by a 100 W incandescent bulb. These configurations supply output voltages around of 20 V and power levels lower than 24 W. The most extended solution adopted is to use a flyback converter operating in Discontinuous Conduction Mode (DCM) with switching frequencies below 100 kHz in order to obtain efficiencies around 82 %. Traditionally, authors have focused their efforts on increasing the efficiency of the ac-to-dc driver in spite of increasing its cost and complexity. Some examples are solutions based on an asymmetrical half bridge flyback converter [7], two

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stage resonant buck converter [8] or tapped-inductor buck converter [9-10]. However, all these proposals exhibit a main drawback: the use of an electrolytic capacitor to reduce the low frequency ripple of the output current.

This paper presents a low-cost ac to dc HB-LED driver conceived from a well-known concept: the Active Input Current Shapers (AICS). The proposal of this solution comes from the latest regulations modifications for low power lighting equipment (i.e. IEC 61000-3-2, Class D) which are now more relaxed than previous ones (i.e. IEC 61000-3-2, Class C), and therefore, a sinusoidal input current is not needed. In AISCs, if the electrolytic capacitor that stabilize intermediate bus is substituted by other technology, then some low frequency ripple arises in the intermediate bus, increasing the distortion of the line current. However, this added distortion is slight in comparison to traditional distortion of AICS, validating the proposed idea without electrolytic capacitor. Moreover, due to its fast dynamic response, the low frequency ripple is not transferred to the output. Finally, an ac to dc HB-LED driver for retrofit lamps applications without electrolytic capacitor is achieved.

II. Revewing Active Intut Current Shaper (AICS)

A. Basic concepts about AISC

The concept of the AICS is very well known in the design of ac to dc Switching Mode Power Supplies (SMPS), [13-17]. This solution is based on conventional dc to dc converters with a slight modification: an additional output, obtained from the converter transformer (Fig. 1a), is connected between the diode bridge and the bulk capacitor (C_B).

This output is called "delayed output" in [11] and it was proposed into the context of two fully regulate outputs in dc to dc converters [12]. It seems similar to a conventional forward output. However, an extra inductor (L_D) is placed between one terminal of the secondary side transformer and the diode D_1 (Fig. 1a). With this extra inductor and with L working in Continuous Conduction Mode (CCM, i.e. $L >> L_D$), the Thévenin equivalent circuit of the "delayed output" becomes a voltage source (V_S, see Fig. 1b) a loss-free resistor (R_{LF}, see Fig. 1b). This "delayed output" recycles some amount of energy redirecting it to the input in order to shape line input current. By properly choosing the values of these two elements (i.e. V_S and R_L), the AISC can achieve both high efficiency and limited low-frequency harmonic content of input current.

The current in a half cycle of input voltage can be easily deduced from the AICS behavior. The input rectifier start to conduct when input voltage (i.e. $v_g(t)=V_{gp}\cdot|\sin(\omega_L t)|$) reaches ($V_S$-$V_C$). Thus, the expression of the rectified input current can be expressed as:

$$i_{gdc}(t) = \frac{V_{gp}\cdot|\sin(\omega_L t)|-V_C+V_S}{R_{LF}}, \quad (1)$$

where V_C is the voltage of intermediate bus, ω_L and V_{gp} are the angular frequency and the peak value of input voltage respectively. It should be noted that this expression is only valid for the interval $[(\pi-\phi_C)/2, (\pi+\phi_C)/2]$, being ϕ_C the conduction angle (see Fig. 1). By equaling (1) to zero, the expression of the conduction angle can be easily calculated:

$$\phi_C = 2cos^{-1}\left(\frac{V_C-V_S}{V_{gp}}\right). \quad (2)$$

Therefore, the line input current is defined by (1) into the $[(\pi-\phi_C)/2, (\pi+\phi_C)/2]$ interval and by zero outside of this interval of positive semi-cycle of the line input voltage. Also, in the same way for the negative semi-cycle of the line input voltage (see Fig. 1). Moreover, it is important to say that the higher ϕ_C the greater amount of energy recycled to the input, and therefore, the lower efficiency.

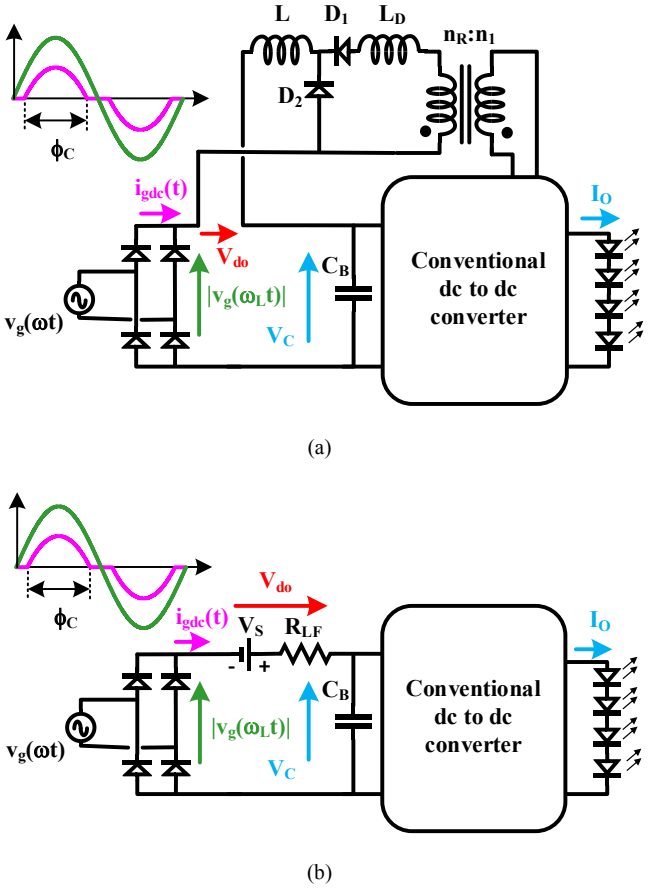

Fig. 1. a) AISC solution. b) Equivalent circuit of AISC.

From the expression of the input voltage, (1) and (2), the average input power will be:

$$P_g = \frac{1}{\pi}\int_{(\phi_C-\pi)/2}^{(\phi_C+\pi)/2}\left[i_{gdc}(t)\cdot V_{gp}\cdot|\sin(\omega_L t)|\right]dt = \\ = \frac{{V_{gp}}^2}{2\pi R_{LF}}\left(\phi_C - sin(\phi_C)\right). \quad (3)$$

The rectified input current can be rewritten as a function of the average input power, conduction angle and peak value of the input voltage by using (1), (2) and (3):

$$i_{gdc}(t) = \frac{2\pi P_g}{V_{gp}}\left(\frac{|\sin(\omega_L t)|-cos\left(\frac{\phi_C}{2}\right)}{\phi_C-sin(\phi_C)}\right). \quad (4)$$

Also, from (4), it is easy to obtain the minimum ϕ_C value which complies with international regulations for a given input voltage (i.e. the minimum ϕ_C which introduce higher efficiency). Table I shows these minimum values (i.e. ϕ_{Cmin}) which are the

same for the american and european mains supply. Some of these values have been previously calculated in [15, 17]. As you can see in Table I, the more restrictive regulation the higher value of ϕ_{Cmin}. At this point, the input current of the AICS can be represented. Figure 2 shows the normalized input current for several optimized designs that both comply international regulations at nominal input voltage and maximize efficiency. All Fig. 2 designs have been performed by following [15, 17] design procedure.

TABLE I. MINIMUN VALUE OF ϕ_C WHICH COMPLIES WITH INTERNATIONAL REGULATIONS

	ϕ_{Cmin} (°)
EN 61000-3-2 Class C regulations	140.49
EN 61000-3-2 Class D regulations	63.12
ENERGY STAR® residential applications	103.87
ENERGY STAR® for commercial applications	55.59

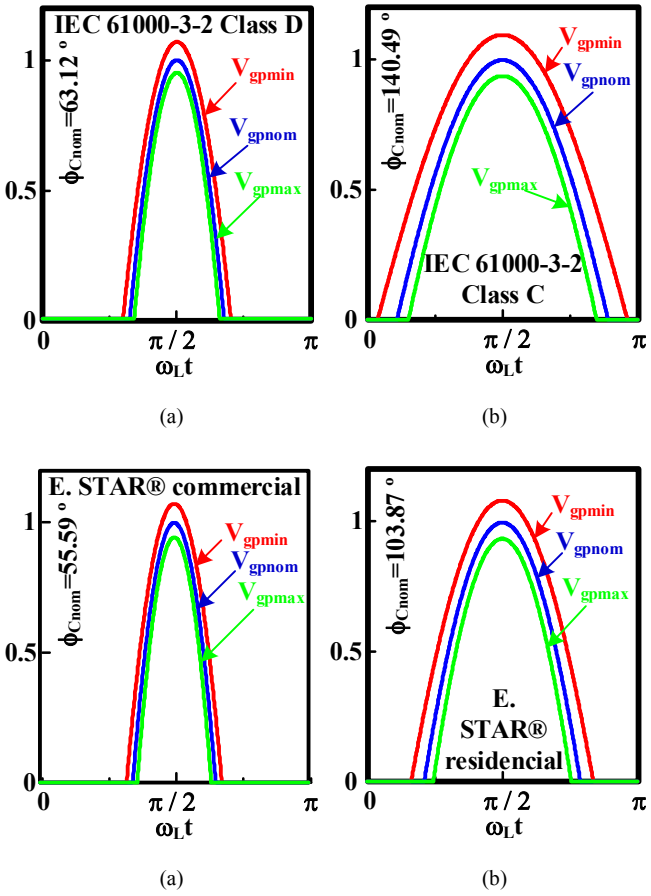

Fig. 2. Normalized input current for different optimized designs at different peak values of $v_g(t)$: a) Class D european design. b) Class C european design. c) ENERGY STAR® american desing for comercial applications. d) ENERGY STAR® american desing for residential applications.

B. Implementation of the voltage source and the LFR with the forward "delayed output"

From the analysis of the forward "delayed output" presented in [11], V_S and R_{LF} can be calculated. Figure 3 shows the equivalent circuit of the "delayed output". As you can see, it is a forward output, but with an additional inductor L_D in series with the rectifier diode D_1. Due to the action of this inductor, there is a delay between the turn-off of D_2 in comparison to traditional forward output. In fact D_2 stops conducting later because L_D must be charged until $i_L(t)$ (i.e. $i_{LD}(t)$ reaches $i_L(t)$) by the action of the voltage reflected to the secondary side of the transformer of the forward "delayed output" (see Fig.3b).

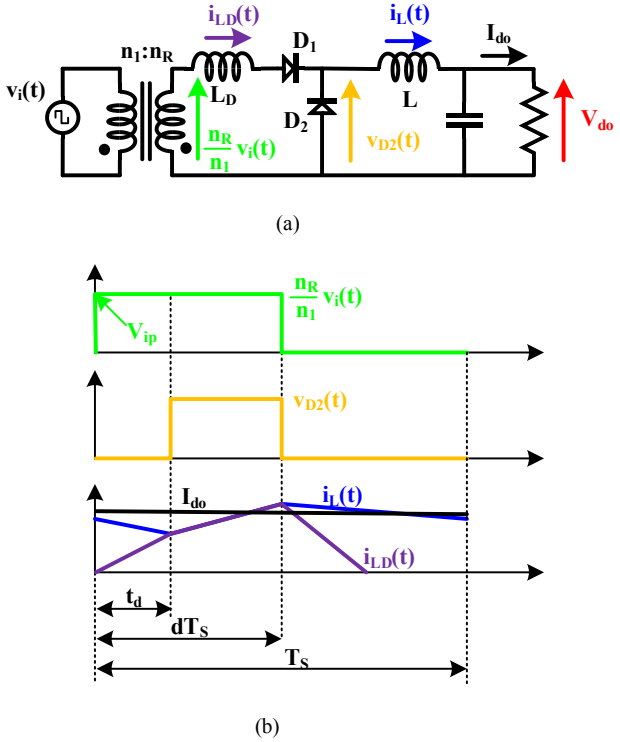

Fig. 3. a) "Delayed ouput". b) Main waveforms.

From Fig. 3b the delay time can be deduced applying Faraday´s law to the "delayed output":

$$t_d = \frac{i_L(t=t_d)}{\frac{n_R}{n_1}\cdot v_i(t)}, \quad (5)$$

where $v_i(t)n_R/n_1$ is the voltage reflected in the secondary side of the forward "delayed output", n_R/n_1 being the turns ratio of the transformer.

The effective duty cycle at the input of the output LC filter can be deduced from Fig. 3b:

$$d' = d - t_d \cdot f_s. \quad (6)$$

where d is the duty cycle and $f_S=1/T_S$ the switching frequency, T_S being the switching period.

Assuming that there is no ripple through inductor L because the forward "delayed output" operates in CCM (i.e. $L>>L_D$), the output voltage of the "delayed output" is:

$$V_{do} = \frac{n_R}{n_1}\cdot V_{ip}\cdot d - L_D \cdot f_s \cdot I_{od}, \quad (6)$$

where V_{ip} is the peak value of $v_i(t)$ and I_{od} is the output current of the "delayed output". From Fig. 1, we can deduce that the forward "delayed output" becomes a real source voltage. Therefore equation (6) can be rewritten as follows:

$$V_{do} = V_S - R_{LF} \cdot I_{od}, \quad (7)$$

where:

$$V_S = \frac{n_R}{n_1} \cdot V_{ip} \cdot d, \quad (8)$$

$$R_{LF} = L_D \cdot f_s. \quad (9)$$

It should be noted that no energy is dissipated in the R_{LF} if all components are ideal. Finally, it is important to say that L_D energy is transferred to the primary side of the transformer, in this case to the equivalent voltage source $v_i(t)$.

C. Using a flyback converter to design the AISC

Figure 4 shows the implementation of an AISC in a flyback converter (it will be equal on a member of the flyback's family of dc to dc converters, that is, SEPIC, Cuk and Zeta). First, Fig. 4a defines the basic implementation. Second, two modifications of this implementation are shown in Fig. 4b and Fig. 4c, where the transformer becomes an autotransformer. Finally, Fig. 4d shows a particularization on Fig. 4c solution. This is an easy implementation of proposed idea, ideal for low-cost solutions. This implementation only introduce two extra inductors and two extra diodes in comparison to traditional flyback topology. The price to pay is the loss of a degree of freedom in the design of the AISC, because the autotransformer disappears (i.e. $n_R=n_1$).

By using a flyback topology in order to implement the AICS, the input voltage of the dc to dc converter becomes V_C. Taking into account CCM operation, the following equation can be written:

$$V_O = \frac{n_2}{n_1} \cdot V_C \cdot \frac{d}{1-d}, \quad (10)$$

where n_2 is the number of turns of the secondary side of the transformer. Moreover equation (8) becomes:

$$V_S = \frac{n_R}{n_1} \cdot V_C \cdot d. \quad (11)$$

As (11) shows, V_S depend on V_C, the duty cycle and the turn ratio of the "delayed output". In fact a properly choice of n_R/n_1 allow us to freely set V_S. Also V_C and V_S are related by the fact that the output voltage of the AISC must be kept constant by the action of the feedback loop. A new equation must be deduced by using (2), (10) and (11):

$$V_C - \frac{n_R}{n_1} \cdot V_C \cdot \frac{V_O}{\frac{n_2}{n_1} V_C + V_O} = V_{gp} \cdot \cos\left(\frac{\phi_C}{2}\right). \quad (12)$$

From (3) and (12), the evolution of V_C as a function of the design parameters (i.e. the conduction angle for nominal conditions and full load, ϕ_{Cnom}, and the duty cycle for minimum peak value of the input voltage, d_{max}) can be calculated. V_C could be represented versus input power for different V_{gp} values. Figure 5 shows the voltage on the intermediate bus for different optimized designs following [15, 17] design procedure. (the same as Fig. 2 designs). [15,17] optimized design procedures is focused on minimizing VC value and the amount of recycled energy, keeping compliance with international regulations at nominal input voltage and full load. By an adequate choice of n_R/n_1 the voltage drop across the series connection of V_S and R_{LF} could be zero at minimum input voltage V_{gpmin} and full load (P_{gmax}). In this conditions V_C (i.e V_{Cmin}) becomes equal to V_{gpmin}.

Although V_C is minimized, it is not maintained constant for different operation conditions (i.e. P_g and V_{gp} variations),

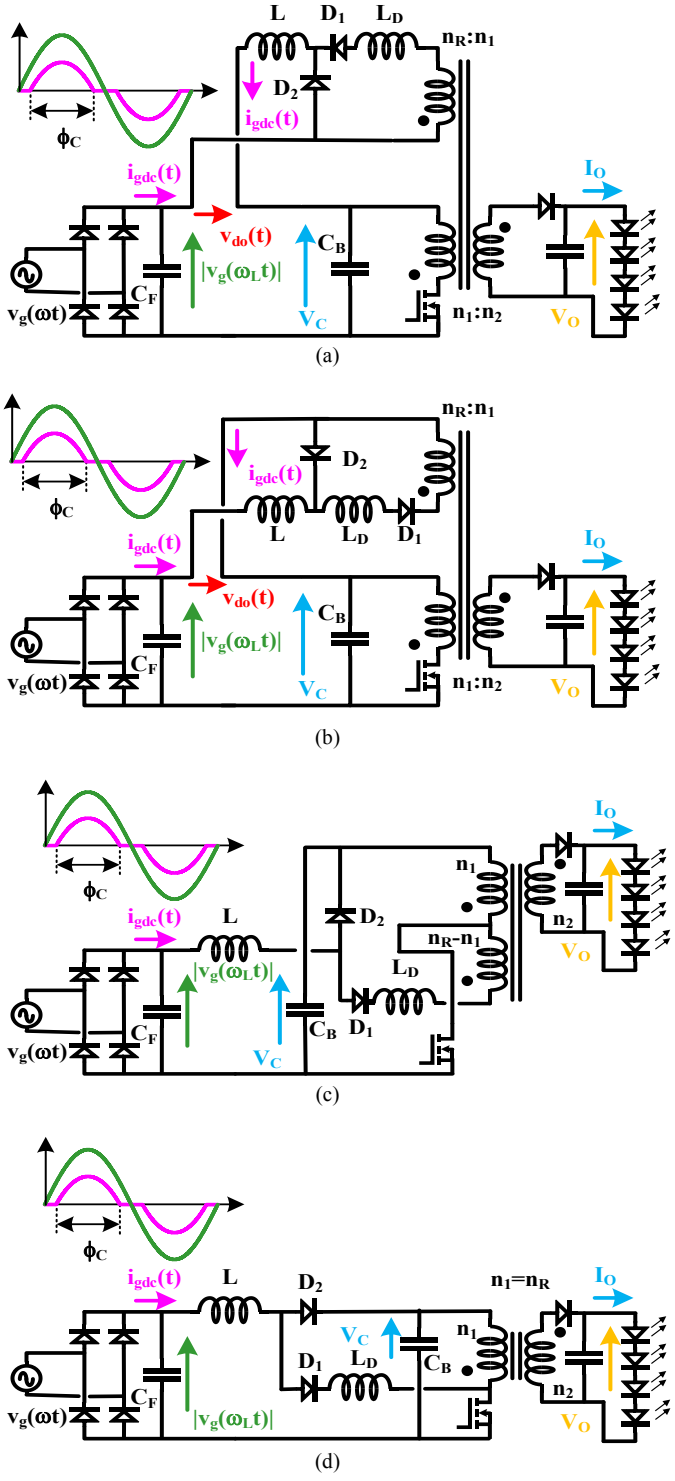

Fig. 4. Implementation of AISC based on flyback converter. a) Basic scene. b) After moving L, L_D, D_1 and D_2. c) Using an extra tap instead of "delayed output". d) Using no extra tap ($n_1=n_R$).

at least if the flyback converter is operating at constant switching frequency, as Fig. 5 shows. This is the price to pay due to the simplicity of this solution in comparison to two-stage solution,

where the voltage across the intermediate bus is controlled. Finally, it is important to say that in Fig. 4d structure, V_C limiting cannot be achieved due to the fact that n_R/n_1 is set a priori.

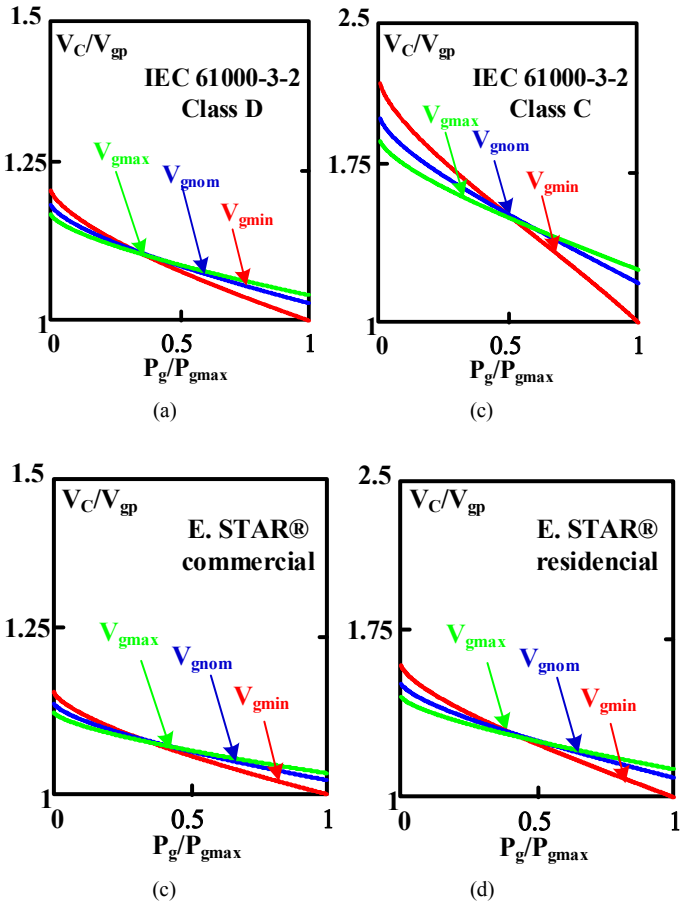

Fig. 5. Normalized voltage of the intermediate bus versus normalized power at different peak values of the input voltage for differerent optimized designs. a) Class D european design. b) Class C european design. c) ENERGY STAR® american desing for comercial applications. d) ENERGY STAR® american desing for residential applications.

III. EXPERIMENTAL RESULTS: INCREASING LOW FREQUENCY VOLTAGE RIPPLE OF AISC IN THE INTERMEDIATE BUS TO ELIMINATE ELECTROLITHYC CAPACITOR

A prototype of the proposed ac-dc HB-LED driver based on an AISC was design to widely comply with regulations (i.e. IEC 61000-3-2, Class D and ENERGY STAR® program requirements for commercial applications), built and tested. A design has been performed following [15, 17] for next specifications: ϕ_{Cnom}=70º, P_g=24 W, V_O=19 V, f_S=110 kHz, american design (i.e. $90\sqrt{2}<V_{gp}<130\sqrt{2}$ and 60 Hz), CCM operation of the "delayed output" (i.e. L=1,8 mH) and d_{max}=0.6. The circuit has been performed according to the scheme given in Fig. 6a, where R_{LF} = 43.45 (i.e. L_D=0.39 mH), $n_S=n_1$ and n_2/n_1=0.1. The prototype was controlled using a commercial IC as is shown in Fig. 6b (UC2825 by Texas Instruments). Finally, the converter output is connected to a matrix of two strings in parallel of 6 HB-LEDs each one. Table II summarize all main components.

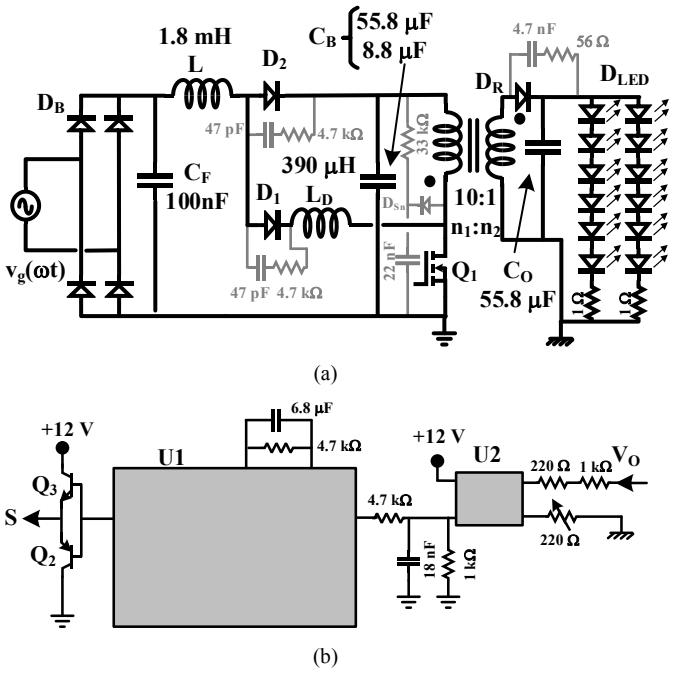

Fig. 6. Experimental prototype based on flyback converter. a) Power stage. b) Control stage.

TABLE II. COMPONENTS OF HE EXPERIMENTAL PROTOTYPE

Fig. 6 reference	Value
D_1	BYP08P140
D_2	HFADBTB
D_B	3KBP04M
D_R	8TQ100
D_{Sn}	MUR4100
D_{LED}	LXK2PW14T00 (Luxeon)
Q_1	FQPF8N80C
Q_2 and Q_3	BD140 and BD139
U_1	UC3825
U_2	MCT2

A. AISC without low frequency ripple in the intermediate bus (C_B=55.8 µF)

The prototype was tested until both the prototype temperature and the HB-LEDs temperature stabilized at the aforementioned specifications. The final operating temperature was reached after 45 min of operation. Figure 7 shows the line input current, voltage in the intermediate bus, input voltage and output voltage of the AISC. As expected, the experimental results of $i_g(t)$ match with the theoretical ones. Also, the voltage of intermediate bus is around 200 V, being the expected one. In this implementation V_C cannot be controlled, however, this is the price to pay for using an implementation as simple as the one of proposed (i.e. $n_1=n_R$).

B. AISC with low frequency ripple in the intermediate bus (CB=8.8 µF)

In this second test, the electrolytic capacitor of the intermediate bus (C_B=47 µF) has been removed and only the ceramic capacitor remains (C_B=4 x 2.2 µF). As a consequence of this, some low frequency ripple arises at the voltage of the intermediate bus (see $v_C(t)$ in Fig. 8) which increase the traditional distortion of the AICS line input current. This added

distortion is slight in comparison to traditional distortion of AICS (see $i_g(t)$ in Fig. 8). Moreover, this slightly increase of the input current distortion can be explicitly checked in comparison to the first test (Fig. 9). As you can see, compliance with IEC 61000-3-2 Class D international regulations is achieved too. Table III shows also compliance with ENERGY STAR® program requirements for commercial applications and the slight increase of THD and slight decrease of PF.

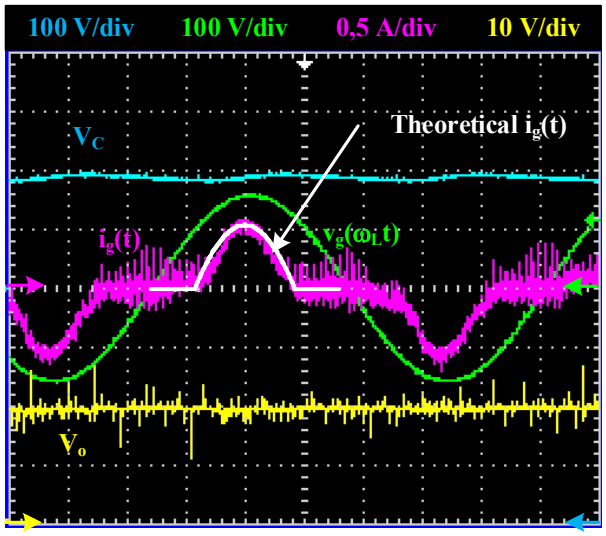

Fig. 7. Line input current ($i_g(t)$), voltage of the intermediate bus (V_C), line input voltage ($v_g(t)$) and output voltage (V_O) of the AISC without low frequency ripple in the intermediate bus.

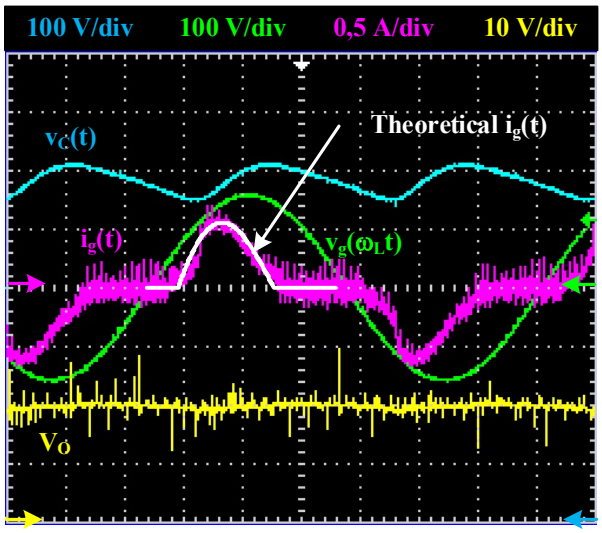

Fig. 8. Line input current ($i_g(t)$), voltage of the intermediate bus ($v_C(t)$), line input voltage ($v_g(t)$) and output voltage (V_O) of the AISC with low frequency ripple in the intermediate bus.

Now the question is how the low frequency ripple of the intermediate bus is reflected at the output of the AICS. The answer is shown in Fig. 10. As you can see, the low frequency ripple of the output voltage (V_O) and output current (I_O) is very low, because the action of the output voltage feedback loop (Fig. 6b), which have been designed to eliminate this ripple.

In order to validate the absence of flickering, [18] considerations have been followed. To limit the biological effects and detection of flicker in general illumination, the Modulation (%) should be kept within the shaded region defined by [18]. Modulation (%) must be calculated by assuming perfect ac power line conditions, being:

$$Modulation\ (\%)_C = 100 \cdot \frac{(L_{max} - L_{min})}{(L_{max} + L_{min})}, \qquad (13)$$

where L_{max} and L_{min} correspond to the maximum and minimum luminance of each harmonic of the ac component of the output current, respectively. In this test a proportionality between luminance and ac component of output current can been assumed. Results of this analysis are shown in Fig. 11. As you can see, all ac harmonic content is within the shaded region.

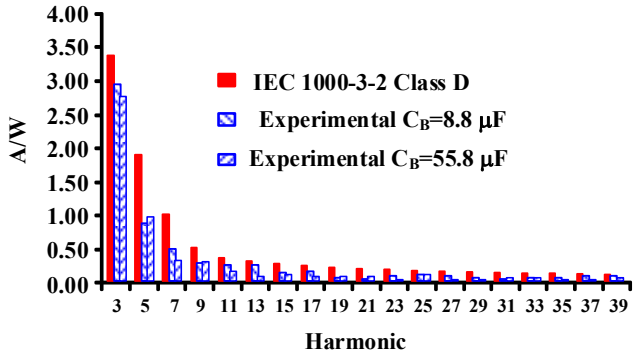

Fig. 9. Experimental harmonic content with and without electrolytic capacitor.

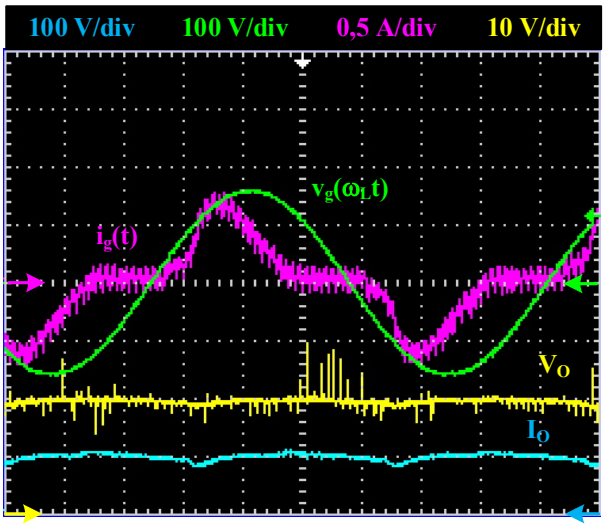

Fig. 10. Line input current ($i_g(t)$), input linevoltage ($v_g(t)$), output voltage (V_O) and output current (Io) of the AISC with low frequency ripple in the intermediate bus.

Finally, the efficiency measured in both prototypes are the same, 82 %. This efficiency is lower than other proposed topologies for replacing incandescent bulb lamps [7-10]. However, this is the price to pay for eliminating the electrolytic capacitor.

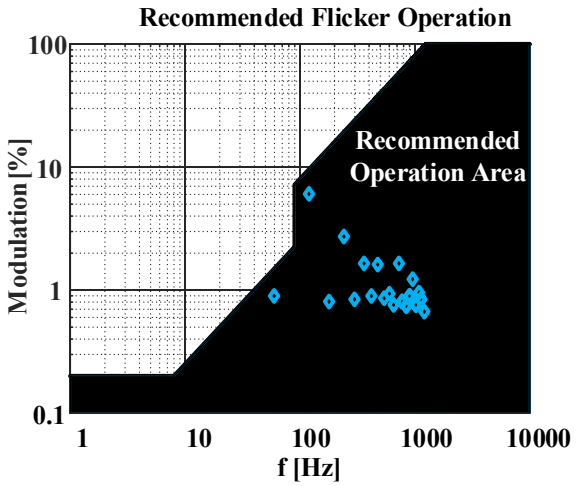

Fig. 11. Modulation (%) of the ouput current of proposed desing into recommended operation area defined in [18].

TABLE III. PF AND THD OF BOTH TEST

TEST	PF	THD(%)
AISC without low frequency ripple in the intermediate bus (CB=55.8 µF)	**0.871**	**56.2**
AISC with low frequency ripple in the intermediate bus (CB=8.8 µF)	**0.818**	**62.9**

IV. ANALYSIS OF THE AISC WITH LOW FREQUENCY VOLTAGE RIPPLE IN THE INTERMEDIATE BUS

At this point, it is obvious that a theoretical analysis of the AICS solution with low frequency ripple in the intermediate bus must be done. This analysis must be focused on the distortion of the line input current in order to validate the experimental results presented in the second test of the previous section.

If some ripple arises in the intermediate bus of AISC due to the substitution of the electrolytic capacitor by other technology, the constant voltage V_C becomes $v_C(t)$:

$$v_C(t) = V_{Cdc} - V_{Cac}\sin(2\omega_L t) = V_{Cdc}(1 - k\sin(2\omega_L t)), \quad (13)$$

where V_{Cdc} and V_{Cac} are the dc component and ac component of the voltage across the intermediate bus, and k is the value of the relative ripple of $v_C(t)$. It is important to say that only the component of twice the line frequency of $v_C(t)$ has been taking into account in the sake of simplicity.

The study will be carried out for a flyback converter operating in CCM (or a member of the flyback's family of dc to dc converters, that is, SEPIC, Cuk AND Zeta). Equation (13) and a modification of equation (10) (i.e. changing d by d(t) and V_C by $v_C(t)$), can be used in order to calculate the duty ratio:

$$d(t) = \frac{Vo}{\frac{n_2}{n_1}(V_{Cdc}(1-k\sin(2\omega_L t)))}. \quad (14)$$

Now the duty cycle varies with the line frequency due to the action of the output voltage feedback loop, which is designed to keep either the $i_O(t)$ or $v_O(t)$ constant. This output voltage feedback loop of the vAISC can be designed with very fast dynamic response in order to eliminate the low frequency ripple, which comes from the input of the flyback dc to dc converter (i.e. intermediate bus of the AICS). This characteristic of the AICS [14-17] is the key to not transfer the low frequency ripple of $v_C(t)$ to the output, and to enable that the removal of the electrolytic capacitor does not involve flickering at the output. However, this variation of the duty cycle plus the low frequency ripple of $v_C(t)$ has consequences on V_S (which becomes $v_S(t)$ in this analysis). From a modification of (11) (i.e. changing d by d(t), V_C by $v_C(t)$ and V_S by $v_S(t)$, (13) and (14), the expression of $v_S(t)$ can be deduced:

$$v_S(t) = V_o \frac{\frac{n_R}{n_1}}{\frac{n_2}{n_1}} \frac{(1-k\sin(2\omega_L t))}{(1-k\sin(2\omega_L t))+\frac{V_o}{\frac{n_2}{n_1}V_{Cdc}}}. \quad (15)$$

As (15) shows, now $v_S(t)$ is not a constant voltage source, and therefore, the line input current will be not sinusoidal during the conduction of the diodes of the rectifier bridge. Using a modification of (3) (i.e., V_C being $v_C(t)$ and V_S being $v_S(t)$), (13) and (15), the line input current will be:

$$i_{gdc}(t) = \frac{1}{R_{LF}}\cdot\left[V_{gp}|\sin(\omega_L t)| + V_o \frac{\frac{n_R}{n_1}}{\frac{n_2}{n_1}} \frac{(1-k\sin(2\omega_L t))}{(1-k\sin(2\omega_L t))+\frac{V_o}{\frac{n_2}{n_1}V_{Cdc}}} - V_{Cdc}(1-k\sin(2\omega_L t))\right]. \quad (16)$$

It should be noted that this expression is only valid for the interval where $v_g(t)$ is greater than $v_C(t)$-$v_S(t)$. This interval can be calculated by equaling to zero (16):

$$V_{gp}|\sin(\omega_L t_i)| + V_o \frac{n_S}{n} \frac{(1-k\sin(2\omega_L t_i))}{(1-k\sin(2\omega_L t_i))+\frac{V_o}{nV_{Cdc}}} - V_{Cdc}(1-k\sin(2\omega_L t_i)) = 0; \quad i = 1,2, \quad (17)$$

where the conduction angle becomes:

$$\phi_C = 2\pi\frac{t_2 - t_1}{T} \quad (18)$$

As you can deduct from (16), average input current of the AISC with ripple in the intermediate bus is non-sinusoidal during the interval $[t_1, t_2]$

Finally, the expression of R_{LF} can be deduced from the input power by using (17). In sake of simplicity R_{LF} has been considered constant in the theoretical analysis:

$$R_{LF} = \frac{1}{P_g\frac{T}{2}}\int_{t_1}^{t_2} i_{gdc}(t)V_{gp}|\sin(\omega_L t)|dt = \frac{1}{P_g\frac{T}{2}}\int_{t_1}^{t_2}\left[V_{gp}|\sin(\omega_L t)| + V_o\frac{n_S}{n}\frac{(1-k\sin(2\omega_L t))}{(1-k\sin(2\omega_L t))+\frac{V_o}{nV_{Cdc}}} - V_{Cdc}(1-k\sin(2\omega_L t))\right]\cdot V_{gp}|\sin(\omega_L t)|\,dt. \quad (19)$$

At this point, the line input current of the AICS can be theoretically calculated for a given specifications. Figure 12, shows the normalized input current for the same optimized design presented in Fig. 2, but now introducing some ripple on $v_C(t)$. From Fig. 12 waveforms analysis, we can conclude that the distortion of the line input current due to the low frequency ripple in the intermediate bus is negligible in comparison to the distortion naturally generated by the AISC operation.

Finally, with the theoretical model presented in this section the line input current of experimental results test B (i.e. k=0.2) can be calculated. As you can see in Fig. 10, the experimental results match with theoretical ones, validating the proposed model.

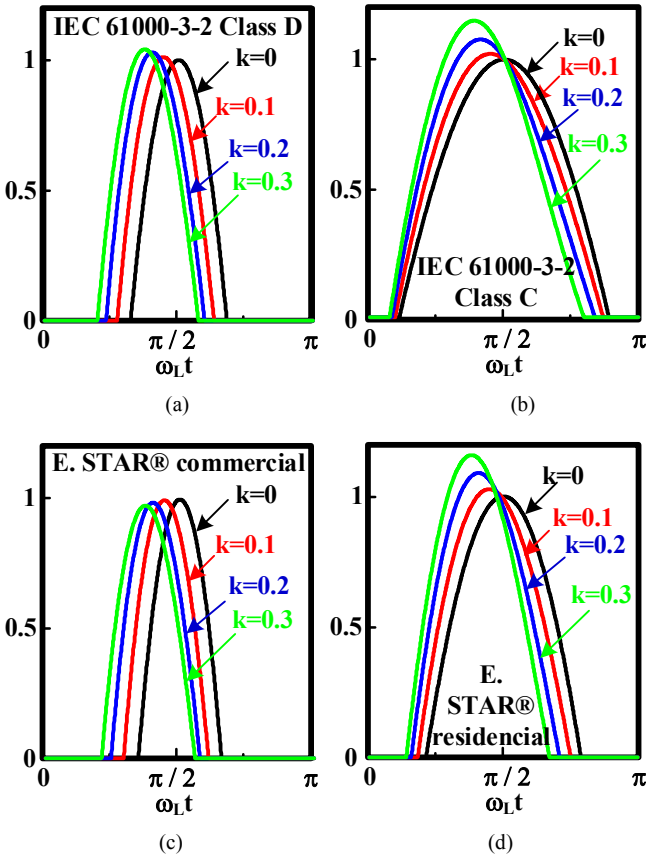

Fig. 12. Normalized input current for different optimized designs at different peak values of $v_g(t)$ and k values: a) Class D european design. b) Class C european design. c) ENERGY STAR® american desing for comercial applications. d) ENERGY STAR® american desing for residential applications.

V. CONCLUSIONS

This paper presents an ac to dc HB-LED driver with no electrolytic capacitor, based on the AICS solution. By removing the electrolytic capacitor, some low frequency ripple arises in the intermediate bus of the AICS. As a consequence of this, the distortion of the line current is increased. However, as theoretical and experimental results show, this increase in distortion is slight in comparison to the one of a standard AISC, and compliance with international regulations (i.e IEC 61000-3-2 Class D) is achieved. Moreover, no low frequency ripple is translated to the output due to the fast dynamic response of AICS, and therefore, no flickering performance is obtained in the ac to dc one-stage topology without electrolytic capacitor. However, the proposed solution presents two main drawbacks: slightly lower efficiency in comparison to other solutions and no wide input voltage range performance. This is the price to pay for a very low-cost solution without electrolytic capacitor.

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