

# Non-Isolated High-Gain Three-Port Converter for Hybrid Storage Systems

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**Abstract**—This work proposes a non-isolated power electronic topology to interface two distinct electrical energy storage units to a DC link, resulting in a Hybrid Storage System. The proposed solution, called Series-Parallel Connection, allows for interfacing these three ports in a simple, compact and reliable approach, based on the standard configuration of the H-bridge converter. The main advantage is that one of the storage units can be of much smaller voltage ratings than the other two, avoiding the use of multilevel or galvanic-isolated power stages. The resulting structure is compared against the most significant transformerless alternatives based on the H-bridge converter, stating their advantages and drawbacks. An analysis of the switching and conduction losses in the power switches of the proposed solution is carried out in order to state the design constraints at which this solution presents improved efficiency versus the alternatives. A final set of experiments in a 10 kW built prototype demonstrates the feasibility and states the benefits as well as the main limitations of the proposed scheme.

**Keywords**—Hybrid Storage Systems, Power Electronic Converters, Multiport, High Gain Converters, Supercapacitors.

## I. INTRODUCTION

Currently, Hybrid Storage Systems (HSS) attract increasing interest in power electronics [1], due their performance in key applications, such as integration of stochastic source generators in the distribution network [2]-[3], grid quality and stability upon line contingencies [4], high power transient loads in powertrains of electric and hybrid vehicles [5]-[6], industrial applications [7], and so on. Usually, these systems interface a high-dynamics low-energy system, e.g. a Supercapacitor Module (SM), to a slower, high-energy storage unit, e.g. an Electrochemical Battery (EB). If a proper control scheme is implemented, the resulting HSS presents overall enhanced performance, with the energy ratings of the main storage device and the power ratings of the auxiliary one [1], [8]-[10]. The management of the power flows is mainly done through Power Electronic Converters (PEC), in order to obtain an optimized operation of the different storage units [8]-[10]. Fig. 1 shows a representation of the power flow balance in one of such systems. In the most general case, every power flow will be bidirectional. Under regular operation, power flows from the grid to the load, or from a generator back to the grid, and the control scheme aims to guarantee a constant DC link capacitor voltage. However, upon sudden load or grid variations, the HSS must compensate these system transient parameter variations, that otherwise could affect the system performance.

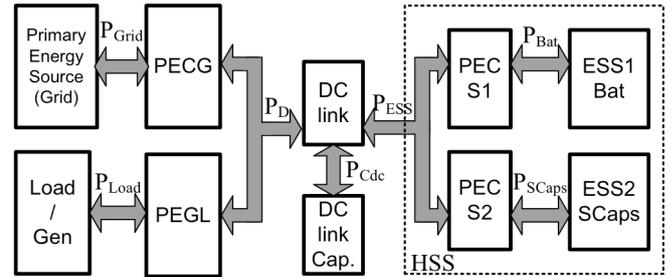


Fig. 1. Modeling approach in terms of the power flow balance in the considered Hybrid Storage System (HSS). PECG: Power Electronics Converter for Grid interface; PEGL: Power Electronics converter for Generation/Load. ESS: Energy Storage System.

The present study proposes a new configuration for the HSS three-port bidirectional converter required for a swift connection between the DC link and both energy storage subsystems. The simplest connection of these devices to a controlled DC link is the Direct Parallel Connection (DPC), depicted in Fig. 2 [11]. It is based on two bidirectional boost converters, in an H-bridge scheme. Assuming a nominal DC link voltage of around  $600V_{DC}$ , and a rated operating voltage range for the EB of  $300-400V_{DC}$  (e.g. a Li-Ion EB intended for grid supporting applications), then a bidirectional boost converter can be used for interfacing both ports. However, if a second storage device with very low rated voltage margins is connected (e.g. 50V in the case of a SM), the bidirectional boost converter cannot be directly used, as it implies the operation at duty ratios away from the optimal range (20%-80%) [12]. In addition to major effects of the parasitic elements, these duty ratio values yield to high form factors in the current and voltage waveforms in switches at the SM converter leg. Moreover, it implies a limit in the practical control margins that can be used to regulate the converter. All these issues yield to look for alternatives to interface the low voltage ratings storage unit and the DC link [18]-[20]. The most used alternatives include complex cascaded stages (multistage topologies, tapped-inductor topologies), multilevel stages, or converters with galvanic isolation [16]-[22].

This work begins by considering the non-isolated connection scheme proposed in [13] (Fig. 3.a), based on a Series Connection (SC) of the storage devices. Then, an alternate solution is proposed to overcome the drawbacks of the SC connection under very high voltage gains. The performance of the proposed Series-Parallel Connection (SPC),

has been preliminarily explored on isolated applications [23]. However, this paper is focused on applying the SPC to the non-isolated scheme, as depicted in Fig. 3.b. Therefore, the present study targets to critically assess the performance of the SPC into non-isolated applications, through an extensive theoretical analysis and validated through experimental demonstrations carried out on a 10kW rated setup.

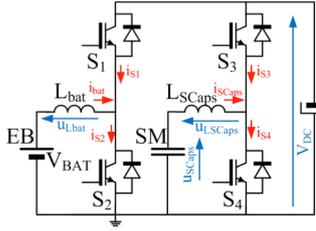


Fig. 2. Direct Parallel Connection of two energy storage devices.

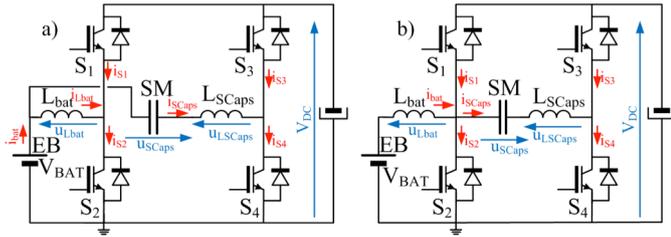


Fig. 3. Series Connection (a) and Series-Parallel Connection (b) of two energy storage devices

## II. LIMITATIONS OF THE DIRECT PARALLEL CONNECTION

As previously outlined, the DPC represented in Fig. 2 has a number of drawbacks under high voltage mismatch condition between any of the storage ports and the DC link. For example, considering the operating conditions of Table I, consisting of  $600V_{DC}$  DC link voltage,  $300V_{DC}$  EB voltage, and  $30V_{DC}$  SM voltage values, the corresponding duty ratios for the EB and SM legs are  $D_{Bat}=50\%$  and  $D_{SCaps}=5\%$ , respectively. With such a small duty ratio for the SM leg, the current waveforms at switches S3 and S4 in Fig. 2 present a significantly different average value and form factors, yielding to a high mismatch in the thermal and electrical stresses. These waveforms are shown in Fig. 4.a, for a standard H-bridge converter in DPC scheme, with the operating parameters of Table I. The main current and voltage waveforms are represented, and the extreme values of the duty ratio of the SM leg can be observed.

TABLE I: PARAMETERS OF THE SYSTEM UNDER STUDY

Symbol	Parameter	Value
$V_{DC}$	DC link Voltage	600 V
$R_{LOAD}$	DC load resistor	300 $\Omega$
$V_{BAT}$	Battery Voltage	300 V
$I_{BAT}$	Battery Current	5 A
$u_{SCaps}$	SM Voltage	30 V
$i_{SCaps}$	SM Current	10 A
$f_{sw}$	Switching Frequency	20 kHz
$D_B$	Battery Leg Duty Ratio	50%
$D_{SCaps}$ (DPC)	SM Leg Duty Ratio (DPC)	5%
$D_{SCaps}$ (SC/SPC)	SM Leg Duty Ratio (SC/SPC)	55%

Another consequence of the extreme duty ratios in the SM branch is that these values are too close to the 0%-100% limits. This critically affects the system dynamic performance. Upon a

sudden negative current demand for  $i_{SCaps}$ , the maximum control action available is from  $D_{SCaps}=5\%$  down to  $D_{SCaps}=0\%$  (S3 and S4 continuously turned off and on, respectively). Therefore  $L_{SCaps}$  will charge with a voltage equal to  $u_{SCaps}$ , yielding to an effective charging current limitation, which penalizes the charging dynamics, also introducing a non-symmetric behavior in the system performance. Fig. 4.b shows this situation for a series SM current reference steps, changing continuously from 1A to -1A. Even though this value is several orders of magnitude smaller than the expected operational range, it can be seen how at the beginning of the discharging step (i.e. current  $i_{SCaps}$  changing from -1A to 1A), the modulation stops ( $D_{SCaps}$  is clamped to 0%), as the demanded control action would drop to negative values, yielding to an unacceptable operating constraint, as well as to a non-symmetrical performance.

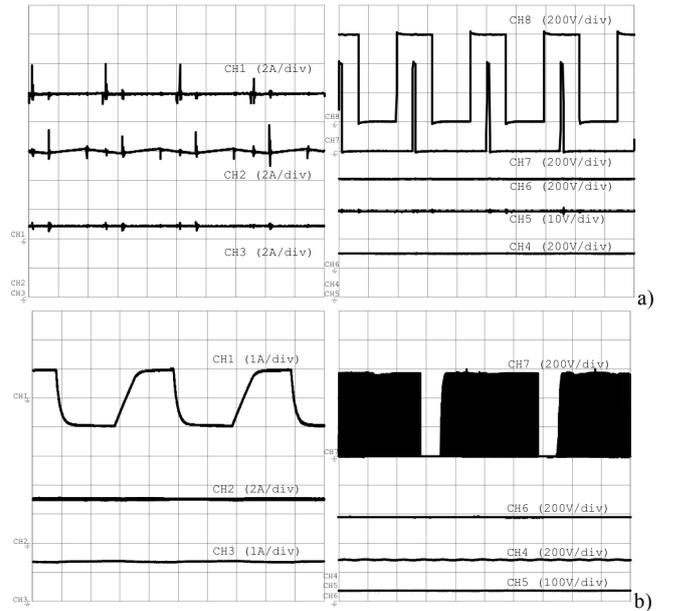


Fig. 4. Actual waveforms of the DPC scheme. a) Steady state ( $20\mu s/div$ ),  $i_{SCaps}=10A$ . b)  $i_{SCaps}$  steps from 1A to -1A ( $5 ms/div$ ). CH1:  $i_{SCaps}$ . CH2:  $i_{BAT}$ . CH3:  $I_{DC}$ . CH4:  $u_{BAT}$ . CH5:  $u_{SCaps}$ . CH6:  $V_{DC}$ . CH7:  $u_{DS2}$ . CH8:  $u_{DS1}$ .

## III. SERIES CONNECTION OF THE STORAGE SYSTEMS.

Fig. 3.a shows the SC of the storage systems [8], with the EB connected to ground, in series with the SM. Considering the mesh equation that relates switches S2 and S4, plus the battery inductor and the SM, then:

$$V_{CE2}(t) + u_{SCaps}(t) + u_{Lbat}(t) - u_{LSCaps}(t) = V_{CE4}(t) \quad (1)$$

where  $V_{CE2}(t)$  and  $V_{CE4}(t)$  are the collector to emitter voltages of switches S2 and S4, respectively,  $u_{SCaps}(t)$  is the SM voltage, and  $u_{LSCaps}(t)$  and  $u_{Lbat}(t)$  are the voltages at the inductances of the EB,  $L_{bat}$  and SM,  $L_{SCaps}$ , respectively. For the next discussion, the value of the parasitic resistance of both inductors will be neglected, which is generally accurate for good design of these reactive elements.

Given that each leg of the H-bridge operates as a bidirectional boost converter, the average values of  $V_{CE2}(t)$  and  $V_{CE4}(t)$  are a function of the duty ratios of the upper switches of the legs of the H-bridge converter,  $D_{Bat}$ , for S1 at the EB leg,

and  $D_{SCaps}$ , for S3 at the SM leg, respectively. These, in turn, are functions of DC link voltage:

$$V_{CE2} = V_{DC} \cdot D_{Bat} \quad (2)$$

$$V_{CE4} = V_{DC} \cdot D_{SCaps} \quad (3)$$

At steady state, the average inductor voltages will be null, and thus (1) turns into:

$$V_{CE2} + u_{SCaps} = V_{CE4} \quad (4)$$

where the expression  $x$  means the average value of any generic waveform as a function of time,  $x(t)$  in a switching period,  $T$ .

From (2), (3) and (4),  $D_{SCaps}$  can be calculated:

$$D_{SCaps} = D_{Bat} + \frac{u_{SCaps}}{V_{DC}} = \frac{u_{SCaps} + V_{BAT}}{V_{DC}} \quad (5)$$

Eq. (5) is interesting since the duty ratio of the SM leg is not a function of the SM and DC voltage values alone (which would yield to very small duty ratio values as in the DPC), but also a function of the battery voltage. Table I shows the difference between typical duty ratio values at the SM leg of the converter for the DPC,  $D_{SCaps}(DPC)$  and for the Series Connection,  $D_{SCaps}(SC)$ . It can be seen how it changes from 5% in the former operating condition to a 55% in the latter case.

Therefore, considering the duty ratios at the SC scheme, the current stresses balancing in the higher and lower switches of the SM leg, S3 and S4, is significantly improved. Also, an increased control action range is obtained, enabling SC configuration for a faster dynamic design, compared to the DPC scheme.

On the other hand, the most important drawback in this design is the fact that the battery current is expressed by:

$$i_{Bat} = i_{Lbat} + i_{SCaps} \quad (6)$$

Considering an independent current control scheme applied to both the storage systems (EB and SM), it yields to a forced battery inductor current evolution, which might yield to excessive voltage levels in the system due the inductive behavior, or to a limited dynamic performance if these overvoltages are prevented at control level.

By looking at Fig. 3.a, it can be argued that the SC scheme allows for certain interleaving effect in the battery current,  $i_{bat}$ . However, this effect will only be beneficial for given operating values in both the SM and battery currents. This enhanced interleaving effect will not occur for all possible conditions, particularly for SM currents much higher than battery currents.

And finally, also from (6), the EB inductor must be now designed for a peak current in the order of magnitude of the SM current, rather than of the EB current. This compromises the efficiency, the power density and/or the system cost.

#### IV. ANALYSIS OF THE SERIES-PARALLEL CONNECTION

These three main drawbacks of the SC scheme can be solved by using the proposed Series-Parallel Connection (SPC) of both storage systems, presented in Fig. 3.b. As it can be

seen, keeping the H-bridge configuration, the negative terminal of the SM is connected directly at the common point of the switching leg connected to the battery, while the other terminal is connected to the midpoint of the second leg. Again, the mesh equation that includes the voltage at the SM is considered:

$$V_{CE2}(t) + u_{SCaps}(t) - u_{LSCaps}(t) = V_{CE4}(t) \quad (7)$$

From (7), and making an analogue analysis to the one carried out for the SC scheme, finally the expression of the duty ratio for the SM leg,  $D_{SCaps}$ , can be calculated:

$$D_{SCaps} = \frac{u_{SCaps} + V_{BAT}}{V_{DC}} \quad (8)$$

This has the same expression than in the SC case. However, at SPC scheme the battery inductor is the battery current itself:

$$i_{Bat} = i_{Lbat} \quad (9)$$

In order to settle and analyze a switching scheme of the pulses at the switches in the H-bridge upon SPC scheme, the following assumptions in the operation of the converter will be considered:

- The SM voltage has only one polarity, and its negative terminal will be connected to the mid-point of the EB leg. Therefore from (8),  $D_{SCaps}$  will be greater than  $D_{Bat}$  in steady state.
- The switching frequencies of both legs are the same, and they are synchronized.
- The current ripples in the inductors and the voltage ripple in the DC link capacitor are relatively small compared to the respective average values.
- Each leg operates in complementary mode (being the control pulses for the upper switch the inverted pulses of the lower one), with an adequate but small enough dead time to avoid cross-conduction in a leg.
- The battery is being discharged towards the DC link ( $i_{bat}$  is positive).
- Initially, it is assumed that the SM is being also discharged ( $i_{SCaps} > 0$ ). However, it is also interesting to analyze what happens upon SM charging; this condition will also be considered.

Fig. 5 shows the synchronization of the pulses at both legs of the H-bridge for the SPC scheme, for a symmetrical switching strategy. Fig. 5.a corresponds to the steady state switching pattern ( $D_{SCaps}$  greater than  $D_{bat}$ ). The equivalent switching modes of the converter, considering the chronograms at Fig. 5, are analyzed ahead.

##### A. Mode I. S2 and S4 Turned On

Fig. 6.a shows both S2 and S4 turned on. The battery inductor charges through S2 ( $i_{bat} > 0$ ). Assuming also  $i_{SCaps} > 0$ , then  $L_{SCaps}$  charges through S2 and S4:

$$\begin{aligned} i_{S1}(Mode I) &= 0; & i_{S3}(Mode I) &= 0; \\ i_{S2}(Mode I) &= i_{Lbat} - i_{SCaps}; & i_{S4}(Mode I) &= i_{SCaps}; \end{aligned} \quad (10)$$

### B. Mode II. S2 and S3 Turned On

In the next switching interval, depicted in Fig 6.b, S4 turns off and S3 turns on, whereas the battery leg remains unchanged. The SM current flows towards the DC link through S3, and therefore:

$$\begin{aligned} i_{S1}(\text{Mode II}) &= 0; & i_{S3}(\text{Mode II}) &= -i_{SCaps}; \quad (11) \\ i_{S2}(\text{Mode II}) &= i_{Lbat} - i_{SCaps}; & i_{S4}(\text{Mode II}) &= 0; \end{aligned}$$

### C. Mode III. S1 and S3 Turned On

Finally, interval III keeps the SM leg as in Mode II, but now S1 is turned on as S2 turns off (Fig. 6.c). The resulting current expressions in the switches for this interval are:

$$\begin{aligned} i_{S1}(\text{Mode III}) &= -i_{Lbat} + i_{SCaps}; & i_{S3}(\text{Mode III}) &= -i_{SCaps}; \quad (12) \\ i_{S2}(\text{Mode III}) &= 0; & i_{S4}(\text{Mode III}) &= 0; \end{aligned}$$

### D. Mode IV. S1 and S4 Turned On

An additional switching mode has to be analyzed. During transients,  $D_{SCaps}$  might get smaller than  $D_{bat}$ , and therefore mode IV would take place instead of mode II (see Fig. 5.b) in the switching sequence. In this case, S1 and S4 will be turned on, whereas S2 and S3 will remain turned off (Fig. 6.d):

$$\begin{aligned} i_{S1}(\text{Mode IV}) &= -i_{Lbat} + i_{SCaps}; & i_{S3}(\text{Mode IV}) &= 0; \quad (13) \\ i_{S2}(\text{Mode IV}) &= 0; & i_{S4}(\text{Mode IV}) &= i_{SCaps}; \end{aligned}$$

## V. SPC STEADY STATE ANALYSIS

In order to assess the validity of this switching pattern, all the possible combination of operating conditions in the HSS must be taken into account. Considering that both storage systems legs are controlled in current mode, and that the DC link voltage is also controlled, the possible operating conditions, for the references of in Fig. 6 are given in Table II.

Considering (10)-(13), the current values through the battery leg switches will always be the subtraction of the current values at the battery and at the SM. Therefore, provided that the switches might carry bidirectional currents, these operating conditions can be reduced to whether these currents are added or subtracted in absolute value, yielding to consider only the cases in which SM and EB current have the same sign or opposite signs. The theoretical waveforms for these two cases are depicted in Fig 7.a (EB and SM discharging) and in Fig 7.b (EB discharging, SM charging). In both cases the claimed balancing effect in the current stresses for the SM leg switches can be seen. Therefore, analogue conclusions apply in terms of the value obtained for  $D_{SCaps}$  than in the case of the aforementioned SC scheme.

TABLE II. OPERATING CONDITIONS OF STORAGE SYSTEMS

Battery	SM	Operating Condition
Discharging $i_{Bat} < 0$	Charging $i_{SCaps} > 0$	Opposite sign in currents
Discharging $i_{Bat} < 0$	Discharging $i_{SCaps} < 0$	Same sign in currents
Charging $i_{Bat} > 0$	Charging $i_{SCaps} > 0$	Same sign in currents
Charging $i_{Bat} > 0$	Discharging $i_{SCaps} < 0$	Opposite sign in currents

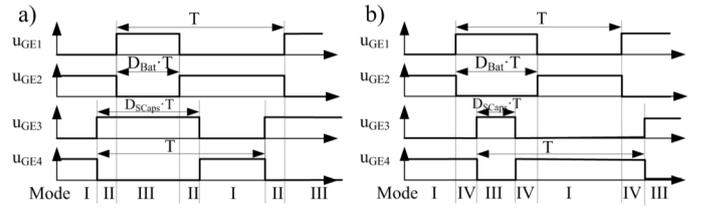


Fig. 5. Switching modes in the SPC for the pulse scheme considered. a)  $D_{SCaps}$  greater than  $D_{bat}$ . b)  $D_{SCaps}$  smaller than  $D_{bat}$  (only in transients).

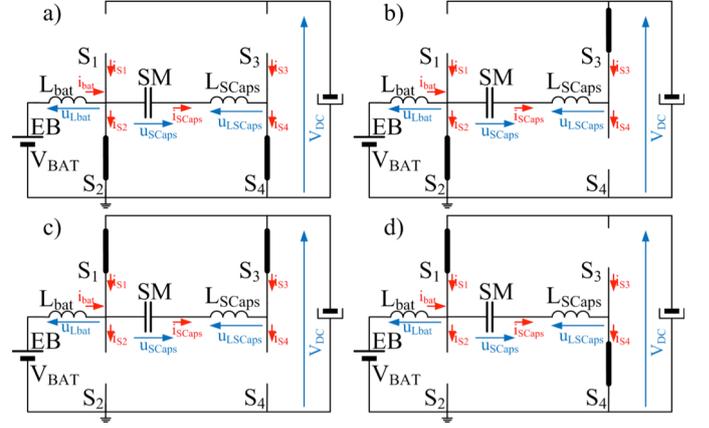


Fig. 6. Switching modes in the SPC scheme. a) Mode I, S1 off, S2 on, S3 off, S4 on. b) Mode II, S1 off, S2 on, S3 on, S4 off. c) Mode III, S1 on, S2 off, S3 on, S4 off. d) Mode IV, S1 on, S2 off, S3 off, S4 on.

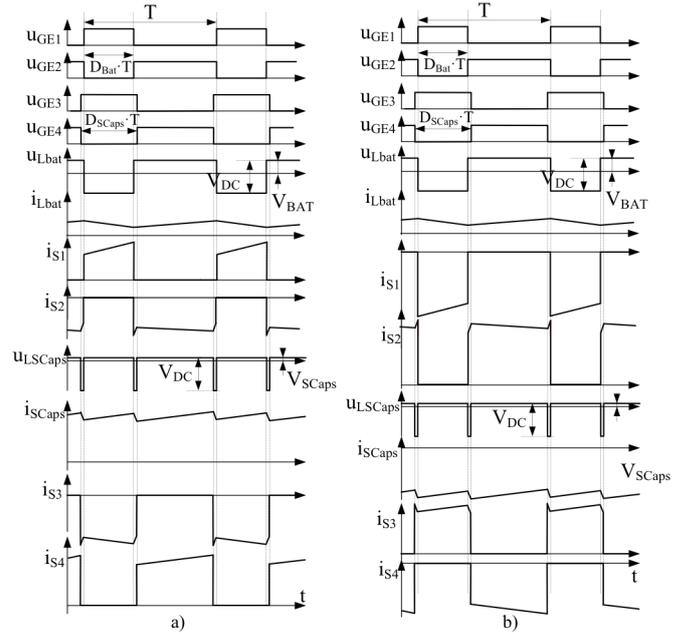


Fig. 7. Theoretical waveforms of the SPC scheme, for battery discharge mode and supercapacitor discharge (left) and charge (right) modes.

In addition, it can be seen how the current waveform through the SM inductor evolves at twice the switching frequency, thus presenting a smaller current ripples, or allowing a smaller inductance value for the same current ripple.

Fig. 8.a shows key steady state experimental waveforms in the H-bridge converter with SPC scheme, again for the rated

values of Table I. Fig. 8.b, though, shows similar results but for a SM voltage rated value of 60V.

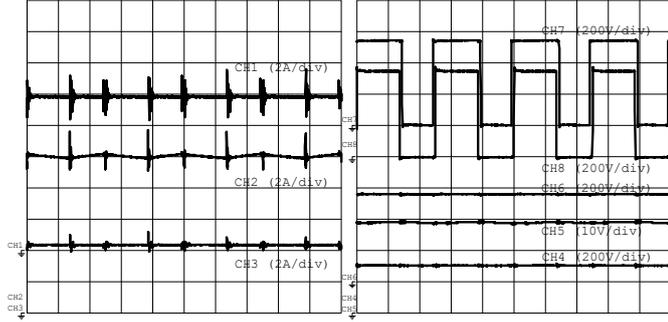


Fig. 8. Actual waveforms of the SPC scheme in steady state, a)  $u_{SCaps}$  30V, b)  $u_{SCaps}$ =60V. CH1:  $i_{SCaps}$ . CH2:  $i_{BAT}$ . CH3:  $I_{DC}$ . CH4:  $u_{BAT}$ . CH5:  $u_{SCaps}$ . CH6:  $V_{DC}$ . CH7:  $u_{DS2}$ . CH8:  $u_{DS1}$ . Time: 20 $\mu$ s/div.

## VI. LOSSES COMPARISON AND EFFECTS IN THE EFFICIENCY

From the above discussion, it is clear that the SPC can be considered as an alternative solution for a non-isolated connection of a DC link and a HSS, having one of the storage units very low voltage ratings. The proposed scheme overcomes the main drawbacks of the DPC and SC schemes, in a simple, compact and reliable converter. Still, the main concerns in the solution come from the fact that the SM current will flow also through the switches of the EB leg, therefore switching and conduction losses through these switches will be affected. In the case that the final losses at these switches results in a higher value than in the original scheme, then even though the SM leg duty ratio presents a suitable close to 50% value, the overall efficiency at the EB leg might make unfeasible the use of this solution.

In order to quantify this issue, the switching and conduction losses in every switch of the HSS converter have been calculated following a simplified theoretic approach, considering the generic equations of these losses found in the literature for inductive switching [12]. The difference between the losses on both the DPC and SPC configurations is given by:

$$\Delta P_{LOSS} = P_{LOSS}(SPC) - P_{LOSS}(DPC) \quad (14)$$

This parameter has been calculated theoretically, and the results are depicted in Fig. 9. This picture represents  $\Delta P_{LOSS}$  in a grey scale. The darker areas correspond to higher negative differences (SPC scheme presents *less* losses than the original DPC), while the clearer areas mean higher positive differences (SPC scheme implies *more* losses than DPC). For reference it must be noticed that  $\Delta P_{LOSS}$  equals to zero if  $I_{SCaps}=0$  (i.e. horizontal axis). Therefore, it can be seen how a better efficiency is obtained at the darker areas, if both SM and EB currents are large in amplitude and of the same sign (both units are being charged or both are being discharged).

In order to validate this analysis, a set of experiments has been carried out. The steady state losses and efficiencies of both the DPC and SPC configurations have been measured for a given set of conditions. These conditions are  $V_{DC}=600V$ ,  $V_{Bat}=300V$ ,  $V_{SCaps}=30V$ , at every possible combination of several battery and SM current reference values ( $I_{SCaps}=-10A$ , -

5A, 0A, +5A and +10A, for  $V_{SCaps}$  around 30V, and  $I_{Bat}=0A$ , +5A, +10A for  $V_{Bat}=300V$ ). The results are given in Table II.

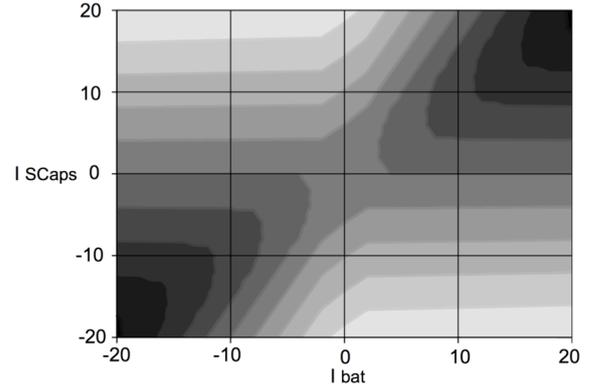


Fig. 9. Difference between the losses in DPC and SPC configurations, as a function of the SM and battery currents.

TABLE II: Experimental Losses and Efficiency Performance of SPC and DPC Configurations

Ref	Ref	Losses	Losses	$\Delta P_{LOSS}$	$\eta_{SPC}$	$\eta_{DPC}$
$I_{bat}$	$I_{SCaps}$	DPC	SPC	(W)	(%)	(%)
(A)	(A)	(W)	(W)			
0	10	142,0	248,6	106,6	-	-
0	5	82,0	147,9	65,9	-	-
0	0	20,3	15,1	-5,3	-	-
0	-5	99,8	55,3	-44,5	-	-
0	-10	206,0	250,8	44,8	-	-
5	10	240,1	224,4	-15,7	87,0%	87,4%
5	5	177,8	139,0	-38,8	89,5%	91,6%
5	0	146,0	138,3	-7,7	90,5%	91,0%
5	-5	166,0	191,8	25,9	89,1%	87,4%
5	-10	188,1	277,5	89,4	87,5%	81,9%
10	10	308,6	257,2	-51,5	90,6%	92,1%
10	5	251,8	218,7	-33,1	92,0%	93,1%
10	0	222,7	215,9	-6,9	92,6%	92,9%
10	-5	247,5	293,9	46,4	91,7%	90,3%
10	-10	286,4	363,9	77,5	90,4%	88,0%

It can be seen how the losses are lower in SPC when both the SM and Battery currents are both positive and large. On the contrary, when the signs of both currents are different, there are more losses in SPC. These results experimentally corroborate the theoretical results depicted in Fig. 9. For a more clear representation of these results, Fig. 10 plots the losses of both DPC and SPC vs. the current values, in order to compare both configurations. Again, these plots demonstrate the theoretical results of Fig. 9.

Therefore, even though at some operating points the losses will be higher with the SPC scheme than in the original DPC scheme, the full performance in terms of efficiency of the proposed topology highly depends on the application and the control scheme used.

## VII. SPC SCHEME IN HYBRID STORAGE SYSTEMS APPLICATIONS

This section deals with a specific analysis of the SPC performance for HSS applications. Particularly, it will address the effects of the operating conditions and the control scheme on the overall losses, when compared against the DPC solution. Considering the power flows stated in Fig. 1, then:

$$P_{Cdc}(t) + P_{Grid}(t) - P_{Load}(t) + P_{Bat}(t) + P_{SCaps}(t) = 0 \quad (15)$$

$$P_D(t) = P_{Grid}(t) + P_{Load}(t) \quad (16)$$

$$P_{ESS}(t) = P_{Bat}(t) + P_{SCaps}(t) \quad (17)$$

where  $P_{Cdc}$  is the power absorbed by the DC link capacitor,  $P_{Grid}$  is the power coming from the grid,  $P_{Load}$  is the power consumed by the load,  $P_{Bat}$  and  $P_{SCaps}$  are the power delivered to the DC link by both the EB and SM respectively.

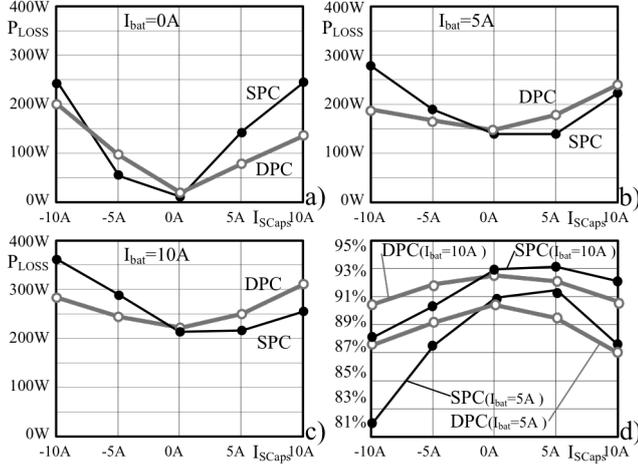


Fig. 10. Steady state losses comparison between DPC and SPC configurations, for: a)  $I_{Bat}=0A$ ; b)  $I_{Bat}=5A$ ; c)  $I_{Bat}=10A$ . d) Efficiency measurements of the DPC and SPC schemes, for  $I_{Bat}=5A$  and  $I_{Bat}=10A$ .

These power values are defined as functions of the voltage and current at each device, as follows:

$$P_{Grid}(t) = V_{DC}(t) \cdot I_{Grid}(t) \quad (18)$$

$$P_{Load}(t) = V_{DC}(t) \cdot I_{Load}(t) \quad (19)$$

$$P_{Bat}(t) = V_{Bat}(t) \cdot I_{Bat}(t) = V_{DC}(t) \cdot I_{DCBat}(t) \quad (20)$$

$$P_{SCaps}(t) = V_{SCaps}(t) \cdot I_{SCaps}(t) = V_{DC}(t) \cdot I_{DCSCaps}(t) \quad (21)$$

$$P_{Cdc}(t) = V_{DC}(t) \cdot I_{Cdc}(t) \quad (22)$$

In the system under consideration, in which the DC link voltage is regulated, the capacitor power,  $P_{Cdc}$ , and the power delivered to the battery and to the SM are null in steady state. Therefore, from (15):

$$P_{Grid}(t) = P_{Load}(t) \quad (23)$$

However, upon transient fluctuations, that can be represented by power steps in either the grid (line fluctuations) or in the load (random load/stochastic generator), the power balance in (23) is lost, yielding to DC link voltage variations unless the HSS compensates the power fluctuation.

For illustration purposes, the following situation is considered. Once the system is in steady state, a load instant power step takes place at a given moment. The grid power is held constant, though. It is assumed that the HSS control is designed to compensate for such variations, therefore aiming to

keep a constant voltage in the DC link. It is also stated that the dynamics of the battery (energy support) are kept much slower than the dynamics of the SM (power support). Such a situation is depicted in Fig. 11. Initially (interval 1 on Fig. 11), the load consumes a given power from the system in steady state, while the storage subsystem remains in idle mode. Therefore, the power (and hence the current) delivered by the battery and the SM are both null. Upon the sudden load change, e.g. load increase, the control demands an increased power value to the hybrid storage system, and initially both the battery and the SM start to deliver such power (interval 2).

The EB responds slowly, and hence the required power is initially provided by the SM. As both  $P_{bat}$  and  $P_{SCaps}$  have the same sign, and given that both devices behave as voltage sources with the same polarity, then the currents  $i_{bat}$  and  $i_{SCaps}$  also have the same sign, resulting in *smaller* current stresses in the battery leg switches during interval 2. The same would happen in the case that the load decreases. Afterwards, interval 3 shows a change in the sign of the SM power, as its voltage evolves again to the initial value (moving back to idle mode). This means that the currents in the battery and SM will have different signs, and thus the efforts in the battery leg (switches and inductor) will be added. Nevertheless this return back to idle mode might be done at a slower pace, thus implying smaller effort requirements, also minimizing the effect of the addition of currents.

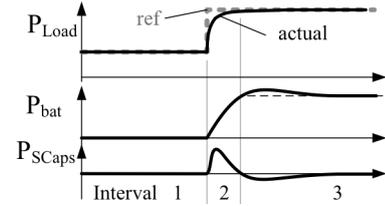


Fig. 11. Control operation intervals upon sudden load variation.

However, the most significant consequence of this connection comes from the relationship between  $D_{Bat}$  and  $D_{SCaps}$ . As stated in the assumptions for the study, from (5)  $D_{SCaps}$  is always greater than  $D_{bat}$ . But it must be noticed that (5) considers only the steady state condition; in transients, the inductor voltage at the SM might be substantially different from zero, depending on the transient current demanded, and thus  $D_{SCaps}$  can reach values below  $D_{Bat}$ . This means that the control action at the SM is not limited in such a small range as in DPC, therefore yielding to a better dynamic performance. Moreover, this behavior is now symmetric.

In order to illustrate this last assertion, Fig. 12 shows a series of current steps for the SPC connection, in the same manner that it was done in the DPC case (Fig. 4.b). The modulation is never interrupted in the SPC case, as the control action can now reach negative values naturally.

## VIII. STABILITY OF THE SPC SCHEME

The implemented current control loop for the SM current is depicted in Fig. 13.a). It is assumed that an external controller fixes the DC link voltage,  $V_{DC}$ . The signal conditioning block,  $H(s)$ , measures and filters the SM current. The resulting value is subtracted to a given current reference,  $I_{SCaps}^*$ , therefore

resulting in the current error,  $\epsilon_1$ . This error is the input of the regulator  $R(s)$ , that generates the control action that provides the input to the transfer function of the system,  $G(s)$ . From Fig. 3.b, the current through the SM is also the current through the SM inductor,  $I_{L_{SCaps}}$ . Therefore, the loop is indeed controlling this inductor current. A way to control such current in a simple manner is to consider as the output of the regulator a control action equal to the inductor voltage,  $U_{L_{SCaps}}$ . In this case, the transfer function of the system can be considered as:

$$G(s) = \frac{I_{L_{SCaps}}}{U_{L_{SCaps}}} = \frac{1}{s \cdot L_{SCaps} + R_{L_{SCaps}}} \quad (24)$$

where  $L_{SCaps}$  is the SM leg inductor, and  $R_{L_{SCaps}}$  is the parasitic resistor of the real magnetic component. This approach results in a simple first order transfer function, and therefore the tuning of the controller results very easy. Once the regulator is tuned, the duty ratio for the SM leg of the converter,  $D_{SCaps}$ , can be calculated by considering (2), (3) and (7). After linearizing:

$$D_{SCaps} = D_{Bat} + \frac{U_{SCaps} - U_{L_{SCaps}}}{V_{DC}} \quad (25)$$

Fig. 13.b) shows the block diagram of the control scheme.

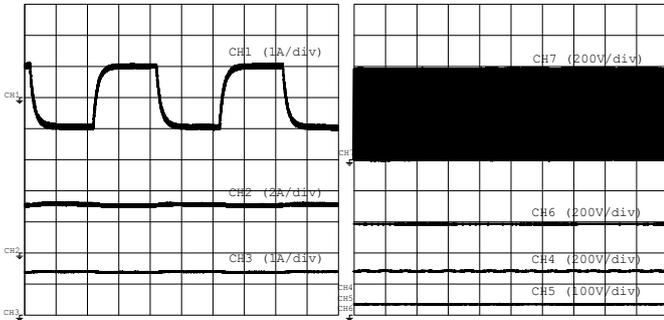


Fig. 12. Actual waveforms of the SPC scheme, for  $i_{SCaps}$  steps from 1A to -1A (5 ms/div). CH1:  $i_{SCaps}$ . CH2:  $i_{BAT}$ . CH3:  $I_{DC}$ . CH4:  $u_{BAT}$ . CH5:  $u_{SCaps}$ . CH6:  $V_{DC}$ . CH7:  $u_{DS2}$ .

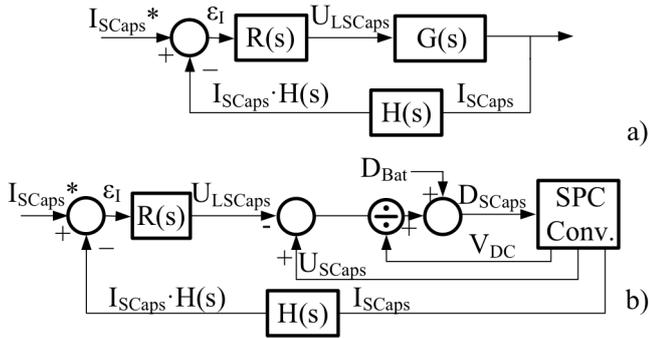


Fig. 13. a) Current control loop simplified scheme for tuning the regulator. b) Implemented control scheme, obtaining  $D_{SCaps}$  from the control action,  $U_{L_{SCaps}}$ .

Once the regulator is tuned, the stability of the control loop can be studied. The implemented filter  $H(s)$  is a second order Butterworth filter, on a Sallen-Key configuration, with a cut-off frequency of 3.5 kHz. The implemented bandwidth of the regulator  $R(s)$  is  $BW=300$  Hz. The SM inductor has an inductance value of  $L_{SCaps}=21$  mH and a series parasitic resistor of  $R_{SCaps}=0.48\Omega$ . In order to check the stability, the open loop

gain of  $G(s) \cdot R(s) \cdot H(s)$  has been plotted in Fig. 14. As it can be seen, for this design the phase margin  $PM$  is close to  $90^\circ$ , therefore the system is stable. The experimental performance of this regulator is depicted in Fig. 15, where the waveforms for a step change in the SM current from 5A to 10A are shown.

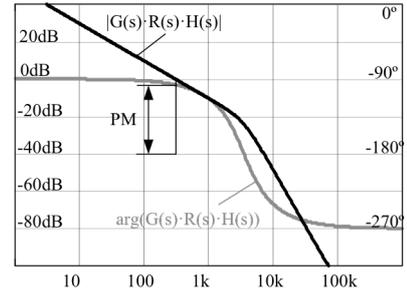


Fig. 14. Switching modes in the SPC for the pulse scheme considered. a)  $D_{SCaps}$  greater than  $D_{bat}$ . b)  $D_{SCaps}$  smaller than  $D_{bat}$  (only in transients)

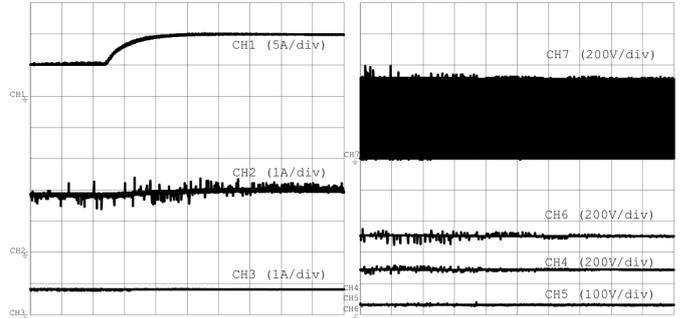


Fig. 15. Reference step at  $i_{SCaps}$  from 5A to 10A (100  $\mu$ s/div), for the regulator designed for  $BW=300$  Hz. CH1:  $i_{SCaps}$ . CH2:  $i_{BAT}$ . CH3:  $I_{DC}$ . CH4:  $u_{BAT}$ . CH5:  $u_{SCaps}$ . CH6:  $V_{DC}$ . CH7:  $u_{DS2}$ .

## IX. CONCLUSIONS AND FUTURE DEVELOPMENTS

In the present work, a detailed analysis and comparison between the standard non-isolated DPC and SC reported schemes, and the proposed SPC scheme, based on the H-bridge multiport connection, has been carried out. This comparison includes theoretical studies and simulations, as well as experimental validations carried out in a 10kW converter prototype. The main conclusions on that comparison are reported in Table III. The conclusions are valid for the particular case of a high mismatch of rated voltages between the storage devices in low to medium power applications, considering the target application of HSS.

SPC presents a better electric and thermal stresses balancing than the DPC case. Given that the SM inductor presents half the value than in the DPC case for the same target current ripple, higher power density might also be achieved. SPC also allows for extended control margin.

The efficiency results show how the performance comparison between DPC and SPC depends on the signs of the currents; therefore, the control scheme determines the overall efficiency of the system. From the above discussion, the proposed SPC scheme is considered as a feasible option for non-isolated interfacing of highly mismatched voltage rating storage systems in multiport configurations, for low to medium power applications, if the low rating storage device is controlled as to provide transient power peaks.

TABLE II: CONFIGURATION PERFORMANCE

Parameter	DPC	SPC
Efficiency	Balance depends on relative values of $I_{Bat}$ and $I_{Scaps}$	
Electrical and thermal stress balancing	High mismatch in switches current form factors	Current form factors evenly distributed
Control regulation margins	Non symmetrical, limited charge slew rate	Symmetrical, independent control
Control simplicity	Simple, independent control	independent control
Ripple through SM	Ripple at switching frequency	Ripple at twice the switching frequency
Current ratings of EB leg switches	Rated for EB peak current	Rated for algebraic sum of SM and EB currents
Size	-	SM inductor half value for the same ripple ratings.

## ACKNOWLEDGMENTS

This work has been partially supported by the Spanish Government, Innovation Development and Research Office (MEC), under research grant ENE2013-44245-R, Project "Microholo", and by the European Union through ERFD Structural Funds (FEDER). This work has been partially supported by the government of Principality of Asturias, Foundation for the Promotion in Asturias of Applied Scientific Research and Technology (FICYT), under Severo Ochoa research grant, PA-13-PF-BP13138.

## REFERENCES

- [1] Thounthong, P.; Rael, S., "The benefits of hybridization," *Industrial Electronics Magazine*, IEEE, vol.3, no.3, pp.25,37, Sept. 2009, doi: 10.1109/MIE.2009.933885
- [2] Jayasinghe, S.D.G., and D.M. Vilathgamuwa. "Flying Supercapacitors as Power Smoothing Elements in Wind Generation." *IEEE Transactions on Industrial Electronics* 60, no. 7 (July 2013): 2909–18. doi:10.1109/TIE.2012.2233693.
- [3] Wu, Hongfei, Peng Xu, Haibing Hu, Zihu Zhou, and Yan Xing. "Multiport Converters Based on Integration of Full-Bridge and Bidirectional DC-DC Topologies for Renewable Generation Systems." *IEEE Transactions on Industrial Electronics* 61, no. 2 (February 2014): 856–69. doi:10.1109/TIE.2013.2254096.
- [4] Abeywardana, D.B.W., B. Hredzak, and V.G. Agelidis. "Single-Phase Grid-Connected LiFePO Battery-Supercapacitor Hybrid Energy Storage System With Interleaved Boost Inverter." *IEEE Transactions on Power Electronics* 30, no. 10 (October 2015): 5591–5604. doi:10.1109/TPEL.2014.2372774.
- [5] Paulo G. Pereirinha, João P. Trovão, "Multiple Energy Sources Hybridization: The Future of Electric Vehicles?, New Generation of Electric Vehicles", DOI: 10.5772/53359
- [6] Lu, Shuai, K.A. Corzine, and M. Ferdowsi. "A Unique Ultracapacitor Direct Integration Scheme in Multilevel Motor Drives for Large Vehicle Propulsion." *IEEE Transactions on Vehicular Technology* 56, no. 4 (July 2007): 1506–15. doi:10.1109/TVT.2007.896970.
- [7] Abdel-baqi, O., A. Nasiri, and P. Miller. "Dynamic Performance Improvement and Peak Power Limiting Using Ultracapacitor Storage System for Hydraulic Mining Shovels." *IEEE Transactions on Industrial Electronics* 62, no. 5 (May 2015): 3173–81. doi:10.1109/TIE.2014.2386797.
- [8] Jayasinghe, S.D.G.; Vilathgamuwa, D.M.; Madawala, U.K., "A direct integration scheme for battery-supercapacitor hybrid energy storage systems with the use of grid side inverter," *Applied Power Electronics Conference and Exposition (APEC)*, 2011 Twenty-Sixth Annual IEEE, vol., no., pp.1388,1393, 6-11 March 2011. doi: 10.1109/APEC.2011.5744773
- [9] Guidi, G.; Undeland, T.M.; Hori, Y., "An Optimized Converter for Battery-Supercapacitor Interface," *Power Electronics Specialists Conference, 2007. PESC 2007.* IEEE, vol., no., pp.2976,2981, 17-21 June 2007. doi: 10.1109/PESC.2007.4342496
- [10] Barrade, P., S. Delalay, and A. Rufer. "Direct Connection of Supercapacitors to Photovoltaic Panels With On-Off Maximum Power Point Tracking." *IEEE Transactions on Sustainable Energy* 3, no. 2 (April 2012): 283–94. doi:10.1109/TSTE.2011.2174261.
- [11] H. Yoo, S. Sul, Y. Park and J. Jeong, "System Integration and Power-Flow Management for a Series Hybrid Electric Vehicle Using Supercapacitors and Batteries," *IEEE Trans. Ind. Applicat.* Vol. 44, No. 1, pp.108-114, 200
- [12] N. Mohan, T.M. Undeland, W.P. Robbins, "Power Electronics: Converters, Applications, and Design", 3rd Edition, ISBN: 978-0-471-22693-2, Ed. Wiley and Sons, November 2002, ©2003
- [13] Yamamoto, K.; Imakiire, A.; Rongyi Lin; Iimori, K., "Comparison of configurations of voltage boosters in PWM inverter with voltage boosters with regenerating circuit augmented by electric double-layer capacitor," *Electrical Machines and Systems, 2009. ICEMS 2009. International Conference on*, vol., no., pp.1,6, 15-18 Nov. 2009. doi: 10.1109/ICEMS.2009.5382975
- [14] Tucker, J.; "Understanding output voltage limitations of DC/DC buck converters", *Analog Applications Journal* 2008, TI
- [15] Song, J., & Kwasinski, A. (2009, October). Analysis of the effects of duty cycle constraints in multiple-input converters for photovoltaic applications. In *Telecommunications Energy Conference, 2009. INTELEC 2009. 31st International* (pp. 1-5). IEEE.
- [16] Dusmez, S., A. Hasanzadeh, and A. Khaligh. "Comparative Analysis of Bidirectional Three-Level DC-DC Converter for Automotive Applications." *IEEE Transactions on Industrial Electronics* 62, no. 5 (May 2015): 3305–15. doi:10.1109/TIE.2014.2336605.
- [17] Grbović, P.J., P. Delarue, P. Le Moigne, and P. Bartholomeus. "A Bidirectional Three-Level DC-DC Converter for the Ultracapacitor Applications." *IEEE Transactions on Industrial Electronics* 57, no. 10 (October 2010): 3415–30. doi:10.1109/TIE.2009.2038338.
- [18] Azongha, S., Liming Liu, and Hui Li. "Utilizing Ultra-Capacitor Energy Storage in Motor Drives with Cascaded Multilevel Inverters." In *34th Annual Conference of IEEE Industrial Electronics, 2008. IECON 2008, 2253–58, 2008.* doi:10.1109/IECON.2008.4758307.
- [19] Rufer, A., and P. Barrade. "A Supercapacitor-Based Energy-Storage System for Elevators with Soft Commutated Interface." *IEEE Transactions on Industry Applications* 38, no. 5 (September 2002): 1151–59. doi:10.1109/TIA.2002.803021.
- [20] Ding, Zhihui, Chen Yang, Zhao Zhang, Cheng Wang, and Shaojun Xie. "A Novel Soft-Switching Multiport Bidirectional DC-DC Converter for Hybrid Energy Storage System." *IEEE Transactions on Power Electronics* 29, no. 4 (April 2014): 1595–1609. doi:10.1109/TPEL.2013.2264596.
- [21] Zhou, Haihua, Tran Duong, Siew Tuck Sing, and A.M. Khambadkone. "Interleaved Bi-Directional Dual Active Bridge DC-DC Converter for Interfacing Ultracapacitor in Micro-Grid Application." In *2010 IEEE International Symposium on Industrial Electronics (ISIE)*, 2229–34, 2010. doi:10.1109/ISIE.2010.5636841.
- [22] Tao, H., A. Kotsopoulos, J.L. Duarte, and M.A.M. Hendrix. "Family of Multiport Bidirectional DC-DC Converters." *Electric Power Applications, IEE Proceedings* - 153, no. 3 (May 2006): 451–58. doi:10.1049/ip-epa:20050362.
- [23] R. Georgious, J. Garcia, A. Navarro, S. Saeed and P. Garcia, "Series-Parallel Connection of Low-Voltage sources for integration of galvanically isolated Energy Storage Systems," *2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Long Beach, CA, 2016, pp. 3508-3513. doi: 10.1109/APEC.2016.7468372